

# **DLynx**<sup>TM</sup> Series Evaluation Board Documentation

The DLynx<sup>TM</sup> series evaluation board (DLYNX\_PICO\_MICRO\_EVAL) is available in 2 formats:

- Single Footprint-supporting MDT/MVT040, UDT/UVT020, PVX003/006/012, APXW012
- Dual layout of the PicoDLynx<sup>™</sup> and the MicroDLynx<sup>™</sup> series of modules supporting PDT003/006/012 and UDT/ UVT020

Board comes with an assembled module. The specific combination of module and the board can be ordered through your sales representative. PDT modules can be provided on single footprint boards as well

# 1. Schematics

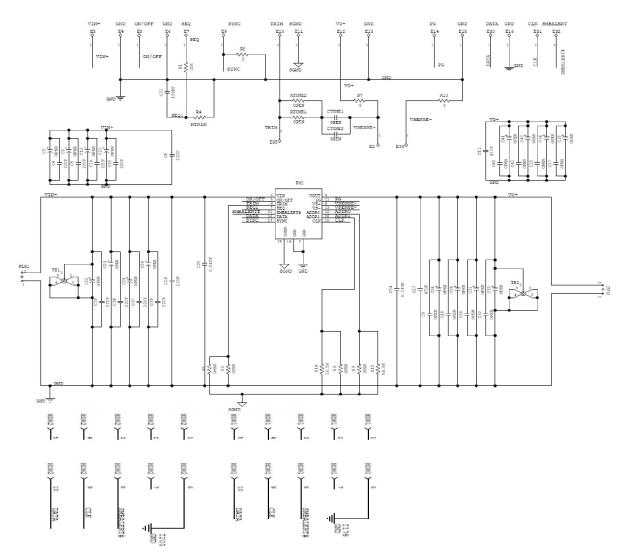


Figure 1 - Schematic of the PicoDLynx  $^{\!\top\!\!M}$  single footprint evaluation board.

Component values are for reference only; refer to the data sheet for appropriate values and pictures in this document for preinstalled components



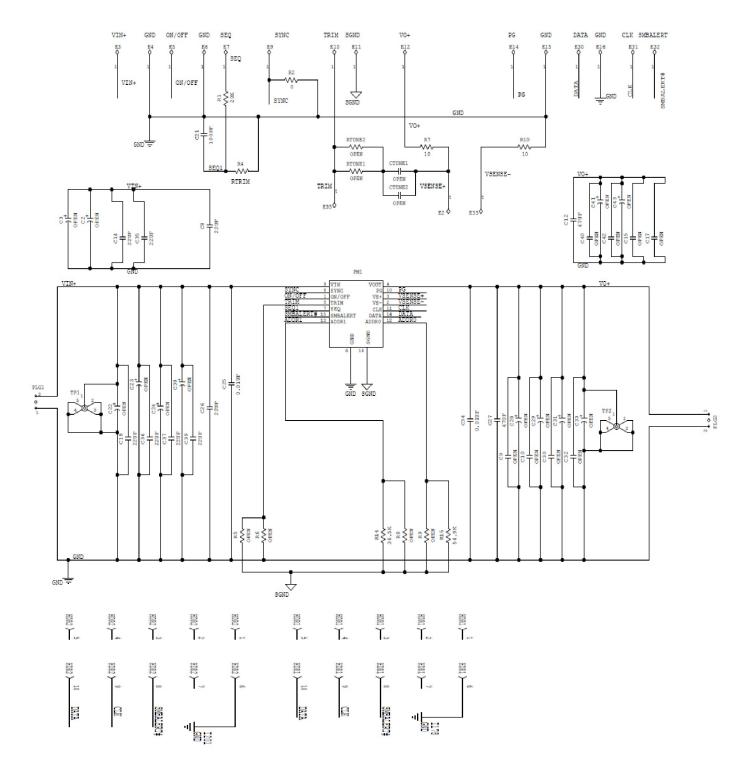


Figure 2 - Schematic of the MicroDLynx  $^{\text{TM}}$  single footprint evaluation board.

Component values are for reference only; refer to the data sheet for appropriate values and pictures in this document for preinstalled components.



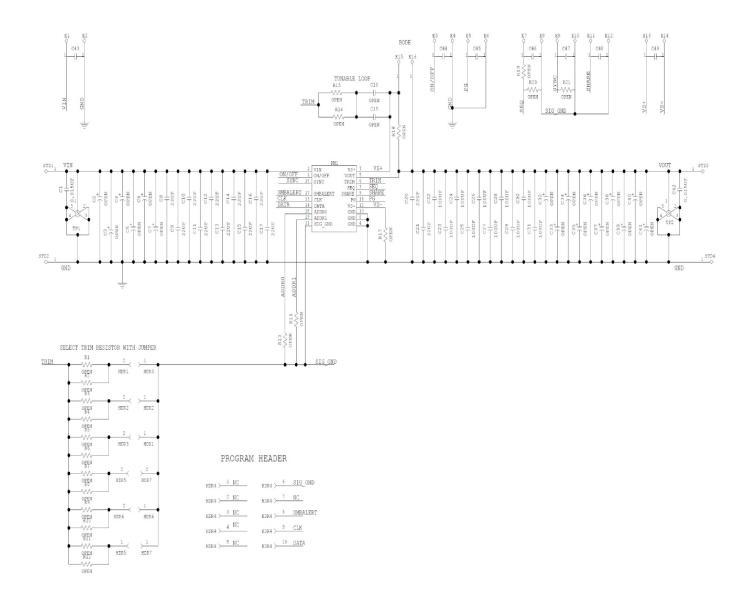


Figure 3 - Schematic of the MegaDLynx™ single footprint evaluation board.

Component values are for reference only; refer to the data sheet for appropriate values and pictures in this document for preinstalled components



Dual layouts on the same board also serve as an example for applications where dual layouts may be desirable, e.g. when the required output current is uncertain and there is an advantage in either adding a higher or lower power capability through a dual layout.

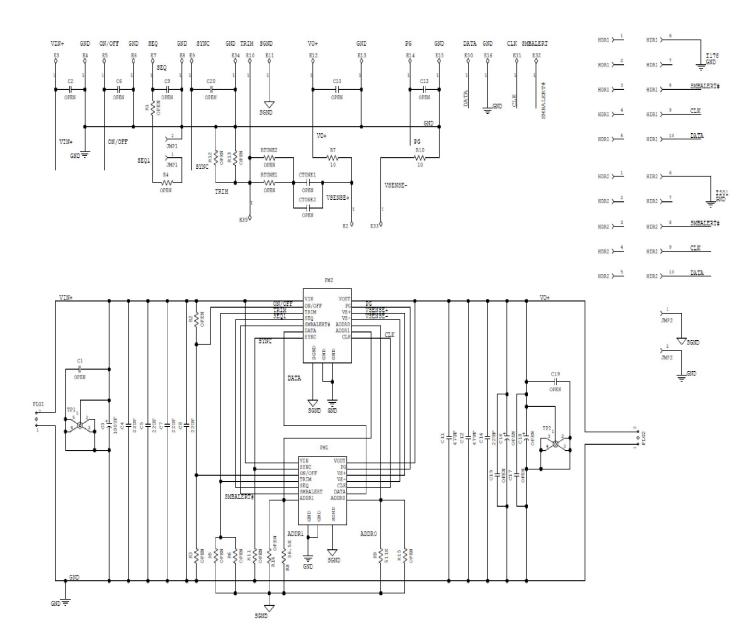


Figure 4. Schematic for the Dual Layout PicoDLynx  $^{\text{TM}}$  /MicroDLynx  $^{\text{TM}}$  Evaluation board.

Component values are for reference only; refer to the data sheet for appropriate values and pictures in this document for preinstalled components



# 2. Physical Description

An annotated photograph of the PicoDLynxTM, MicroDLynx $^{TM}$  and MegaDLynx $^{TM}$  single footprint evaluation board is shown in Figs. 5, 6 and 7 below. The arrows indicate locations of various components.

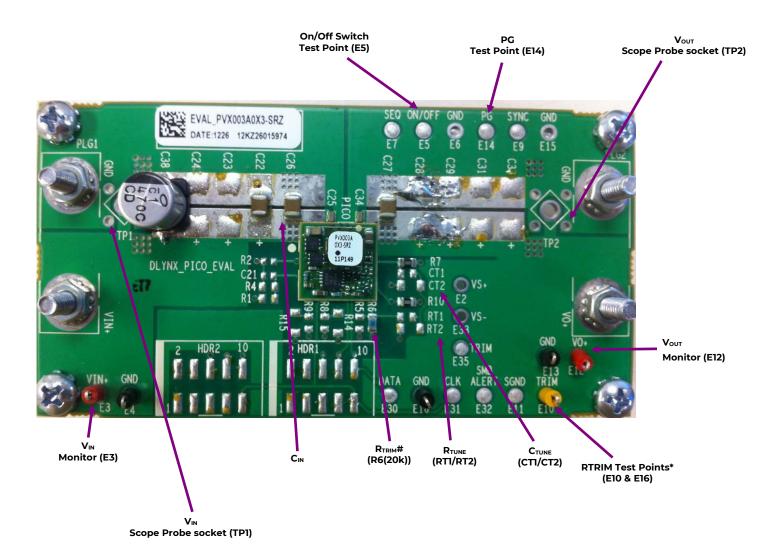


Figure 5. Power and Analog Signal Interface for the PVX003/006/012 Eval Board

Caution! Before applying power, make sure that the externally installed capacitors (input & output) have appropriate voltage and polarity ratings based on the application.

#### Notes:

# Module can be trimmed either by soldering fixed resistor(s) @ R6 or by attaching a potentiometer/resistor between test points E10 and E16.



Pre-Installed components for the MicroDLynx<sup>TM</sup> - Input filtering [ $C_{25}$  (0.047uF,16V),  $C_{22}$ (22uF,16V),  $C_{26}$ ,(22uF,16V),  $C_{38}$  (470uF,16V)], Output filtering [ $C_{34}$ (0.047uF,16V),  $C_{27}$ ,  $C_{32}$  (47µF,6.3V)],  $C_{25}$  resistors,  $C_{25}$  R<sub>10</sub> = 0 Ohms, Trim  $C_{25}$  Address R15=54.9K, R14=36.5K and some test points.

# ADDR0\* R<sub>TRIM</sub># (R9/R15) HDR1\*\* R5(20k) HDR2\*\* ADDR1\* $V_{\text{IN}}$ (R8/R14) **V**out Monitor (E3) RSYNCH Monitor (E12) R<sub>TUNE</sub> (RT1/ (R2=0)(C21) (R1 & R4) RT2) UDT020A0X3-SRZ DATE:1227 12KZ27015168 DLYNX MICRO EVAL $C_{\text{IN}}$ RTRIM Test Point\* C<sub>TUNE</sub> (CT1/CT2) V<sub>IN</sub> Scope Probe (E35) socket (TP1) $\mathbf{V}_{\mathsf{OUT}}$ On/Off Switch **Scope Probe socket** Test Point (E5) (TP2) Sync Signal Sequencing Test Test point (E9) Test Point (E14)

### 10-Pin Ribbon Cable to USB Interface Adaptor or Second Eval Board

Figure 6. Power and Analog Signal Interface for the UDT/UVT020 Eval Board

Caution! Before applying power, make sure that the externally installed capacitors (input & output) have appropriate voltage and polarity ratings based on the application.

### Notes:

# Module can be trimmed either by soldering a different fixed resistor(s) @ R5 or by attaching a potentiometer/resistor between test points E11 and E35

Point (E7)



Pre-Installed components for the MegaDLynx<sup>TM</sup> - Input filtering [ $C_{14}$ , $C_{51}$  (0.047uF,16V),  $C_{13}$ , $C_{15}$ , $C_{16}$ ,(22uF,16V),  $C_{5}$ (470uF,16V)], Output filtering [ $C_{20}$ , $C_{21}$ , $C_{52}$ , $C_{53}$ (0.047uF,16V),C22,C23,C24,C25 (6x47µF,6.3V)],  $R_{SENSE}$  resistors,  $R_{17}$  &  $R_{18}$  = 0 Ohms, Trim  $R_{1}$  = 20K, Address R13=54.9K, R14=36.5K and some test points.

10-Pin Ribbon Cable to USB Interface Adaptor or Second

# **Eval Board V**out HDR2\*\* **C**<sub>TUNE</sub> (C18/ Scope Probe socket (TP2) R<sub>TRIM</sub> R1 ADDR0\* C19) $V_{\text{OUT}}$ (20K) ADDR1\* (R13) Monitor (E13) On/Off Switch (R14) Test Point (E3) R<sub>TUNE</sub> (R15/R16) R<sub>SEQ</sub> (R19) R<sub>SYNCH</sub> (R2=0) C<sub>SEQ</sub>(C21) Monitor (E3) Cout HDR1\*\* Sequencing PG (TP1)Test Sync Signal Test Point (E7) Point (E14) Test point (E9)

Figure 7. Power and Analog Signal Interface for the MDT/MVT040 Eval Board

Caution! Before applying power, make sure that the externally installed capacitors (input & output) have appropriate voltage and polarity ratings based on the application.

**Notes:** Module can be trimmed either by soldering a different fixed resistor(s) @ R1 or by attaching a potentiometer/resistor between test points E17 and E18.

Scope Probe socket (TP1)



Pre-Installed components for the MegaDLynx<sup>TM</sup> - Input filtering [ $C_{14}$ , $C_{51}$  (0.047uF,50V),  $C_{13}$ , $C_{15}$ , $C_{16}$ ,(10uF,50V), Output filtering [ $C_{20}$ , $C_{21}$ , $C_{52}$ , $C_{52}$ , $C_{53}$ (0.047uF,50V), $C_{22}$ , $C_{23}$ , $C_{24}$ , $C_{25}$  (4x10µF,50V)],  $R_{SENSE}$  resistors,  $R_{17}$  &  $R_{18}$  = 0 Ohms, Trim  $R_1$  =20K and some test points.

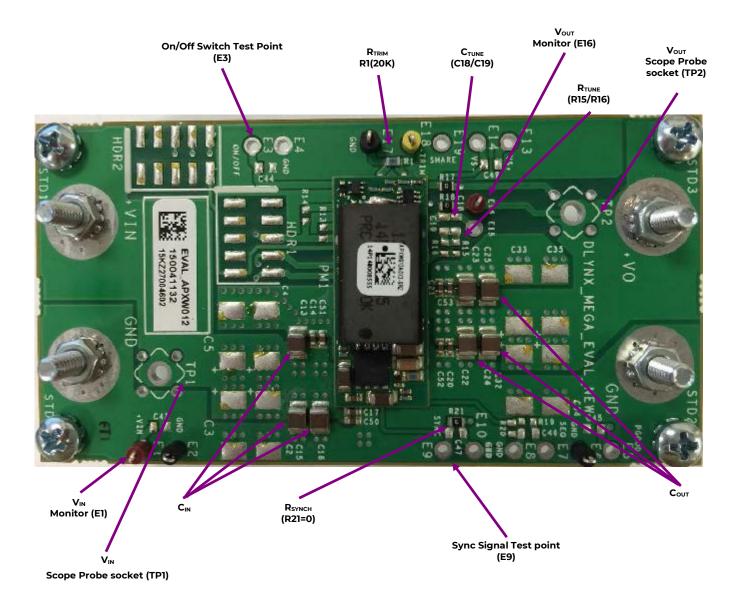


Figure 7. Power and Analog Signal Interface for the APXW012 Eval Board

Caution! Before applying power, make sure that the externally installed capacitors (input & output) have appropriate voltage and polarity ratings based on the application.

**Notes:** Module can be trimmed either by soldering a different fixed resistor(s) @ R1 or by attaching a potentiometer/resistor between test points E17 and E18. Remember to remove existing trim resistor



An annotated photograph of the Dual Layout PicoDLynx<sup>TM</sup>/MicroDLynx<sup>TM</sup> evaluation board is shown in Figs. 8, 9 and 10 below. The minimum set of external components consists of the trim resistor R5/R6, input filtering (C7, C8 =  $2 \times 22 \mu F/16V$  ceramic capacitors are recommended as a minimum and one 470 u F/16V electrolytic (C3) for bench testing. C3, C7 & C8 come pre-assembled on the board) and some modest amount of output filtering  $22 \mu F$  (minimum) ceramic (C11=22 u F/16V pre-assembled on the board). Additionally, the following components are preinstalled:

R<sub>SENSE</sub> resistors, R7 & R10 = 0 Ohms, RSYNCH resistor, R11=10K, R<sub>TRIM</sub> =20K, Address R15=54.9K, R14=36.5K

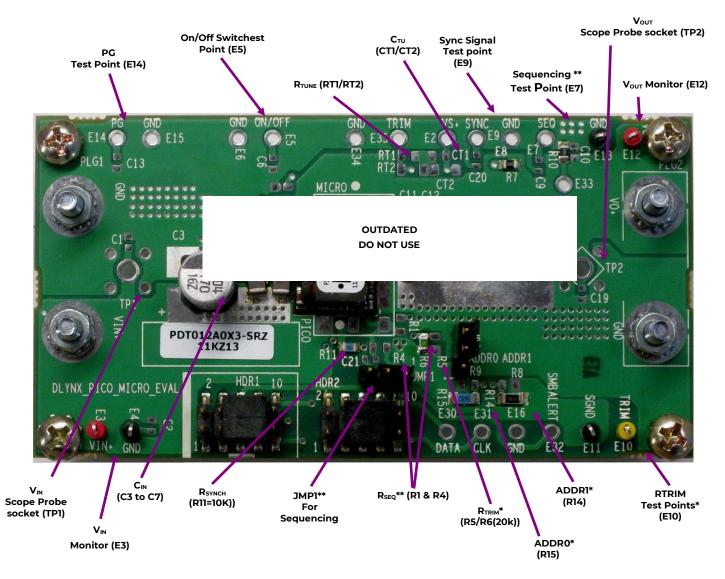


Figure 8. Power and Analog Signal Interface for the Dual Layout PDT012 Eval Board

Caution! Before applying power, make sure that the externally installed capacitors (input & output) have appropriate voltage and polarity ratings based on the application.

#### Notes:

- \* Module can be trimmed either by soldering fixed resistor(s) @ R5/R6 or by attaching a potentiometer/resistor between test points E10 and E11.
- \*\* Place Shorting Jumper (JMP1) on the left two pins (as shown) when NOT testing for sequencing (SEQ pin open). When testing for Sequencing, place JMP1 on the right two pins and select/install  $R_{SEQ}$  resistors, R1 & R4. For further details see the module's data sheet and Application Note ANO4-008 "Application Guidelines for Non-Isolated Converters: Guidelines for Sequencing of Multiple Modules".



The minimum set of external components consists of the trim resistor R5/R6, input filtering (C7, C8 =  $2 \times 22\mu F/16V$  ceramic capacitors are recommended as a minimum and one  $470\mu F/16V$  electrolytic (C3) for bench testing. C3, C7 & C8 come pre-assembled on the board) and some modest amount of output filtering  $22\mu F$  (minimum) ceramic (C11= $22\mu F/16V$  pre-assembled on the board). Additionally, the following components are preinstalled:

R<sub>SENSF</sub> resistors, R7 & R10 = 0 Ohms, RSYNCH resistor, R11=10K, R<sub>TRIM</sub> =20K, Address R15=54.9K, R14=36.5K

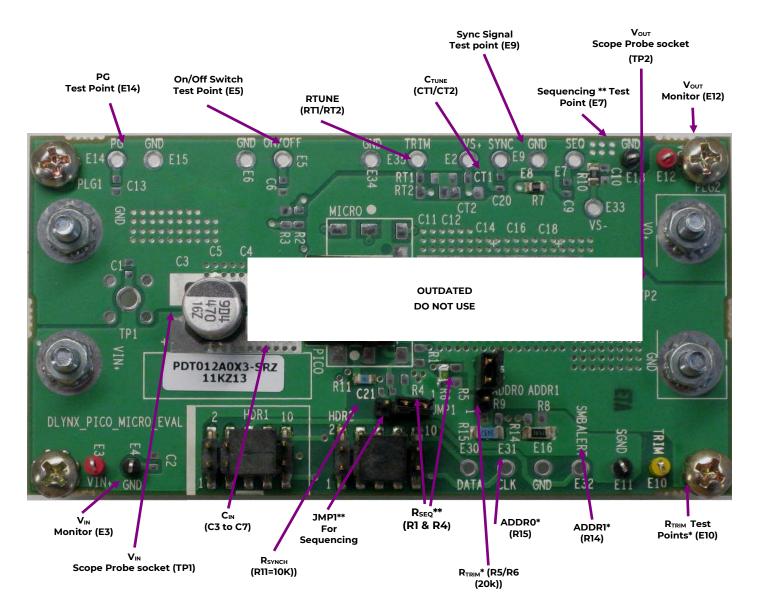


Figure 9. Power and Analog Signal Interface for the Dual Layout UDT020 Eval Board

Caution! Before applying power, make sure that the externally installed capacitors (input & output) have appropriate voltage and polarity ratings based on the application.

#### Notes:

- \* Module can be trimmed either by soldering fixed resistor(s) @ R5/R6 or by attaching a potentiometer/resistor between test points E10 and E11.
- \*\* Place Shorting Jumper (JMPI) on the left two pins (as shown) when NOT testing for sequencing (SEQ pin open). When testing for Sequencing, place JMPI on the right two pins and select/install  $R_{SEQ}$  resistors, RI & R4. For further details see the module's data sheet and Application Note AN04-008 "Application Guidelines for Non-Isolated Converters: Guidelines for Sequencing of Multiple Modules".



**Digital Interface:** The components and test points highlighted in the following figure can be used to evaluate PMBus Digital Interface functionality for the Digital DLynx<sup>TM</sup> modules.

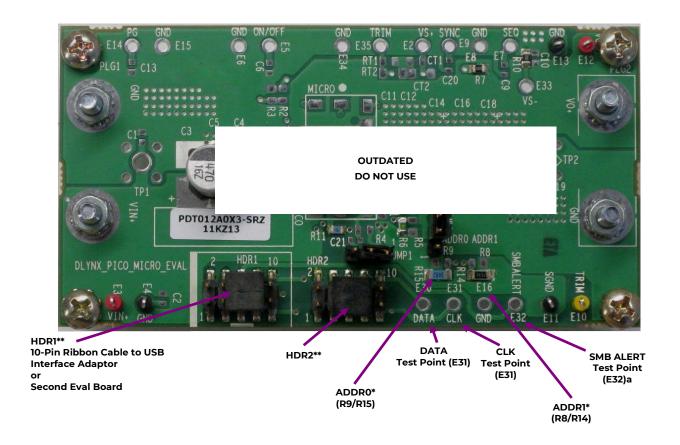


Figure 10. PMB us Digital Interface for the Dual Layout Board

### **Notes:**

\* The digital DLynx Module can be assigned a specific address by connecting resistors (R9/R15) from the ADDR0 pin to GND and resistors (R8/R14) from the AADR1 pin to GND. The evaluation board comes with preinstalled ADDR1 resistor, R14=36.5K and ADDR0 resistor, R15=54.9K as an example. These values correspond to Octal digits "3 4" equivalent to HEX number "1C" (equivalent to 28 decimal). Please refer to the data sheet for additional details.

\*\* HDR1/HDR2 allow the unit on the Eval board to interface (via 10 pin Ribbon Cable) with another unit on a different Eval Board and/or to OmniOn's "USB Interface Adapter" module in order for multiple modules to be controlled by the GUI. For further details, please refer to the OmniOn document, "Digital Power Insight™ User Manual".

Note1: The red wire on the ribbon cable should be aligned to Pin 1 (left side) of the HDR1 or HDR2 connectors.

Note2: Headers and Ribbon Cable Assembly details:

Part Description (HDR1 & HDR2): 10-Pin Dual Row Male Pin Header, SMT

e.g. FCI P/N: 95157-210 (Digi-Key P/N: 95157-210-ND) or Molex P/N: 0015910100

Part Description: IDC Ribbon Cable Assembly

e.g.: 3M P/N: M3DDA-1018J (Digi-Key P/N: M3DDA-1018J-ND) or Molex P/N: 111062-022



# Dual Layout 12A/6A/3A Analog PicoDLynx<sup>TM</sup>:

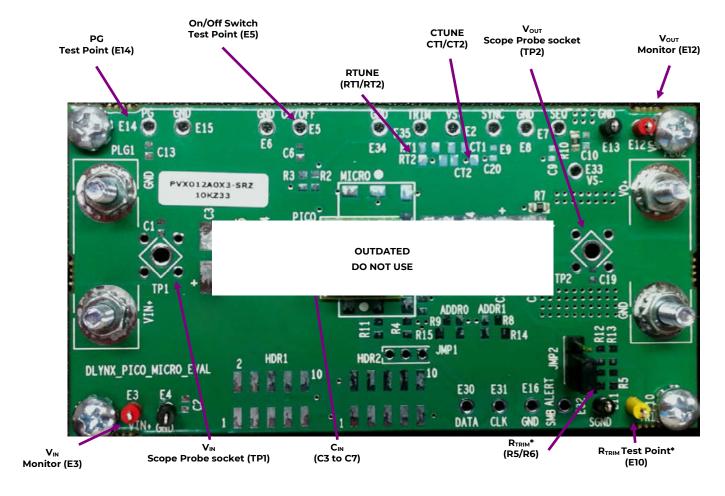


Figure 11. Analog Dual Layout 12A PicoDLynx (PVX012A0X) Interface

**Note1:** Place Shorting Jumper (JMP2) on the bottom two pins as shown (SGND and GND will be shorted) or place  $R_{TRIM}$  resistors on pads identified as R12 & R13. (Other versions of this evaluation board may not have R12 & R13 pads).

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