

## 1.1W AUDIO POWER AMPLIFIER WITH ACTIVE-LOW SHUTDOWN MODE

March 2024

### GENERAL DESCRIPTION

The IS31AP4991A has been designed for demanding audio applications such as mobile phones and permits the reduction of the number of external components.

It is capable of delivering 1.1W of continuous RMS output power into an 8Ω load @ 5V.

An externally-controlled standby mode reduces the supply current to much less than 1μA. It also includes internal thermal shutdown protection.

The unity-gain stable amplifier can be configured by external gain setting resistors.

### FEATURES

- Operating from  $V_{CC} = 2.7V \sim 5.5V$
- 1.1W output power @  $V_{CC} = 5V$ , THD+N= 1%,  $f = 1kHz$ , with 8Ω load
- Ultra-low consumption in standby mode (much less than 1μA)
- 56dB PSRR @217Hz in grounded mode
- Near-zero click-and-pop
- Ultra-low distortion (0.074%@0.5W, 1kHz)
- SOP-8 and MSOP-8 packages
- RoHS & Halogen-Free Compliance
- TSCA Compliance

### APPLICATIONS

- Mobile phones
- PDAs
- Portable electronic devices
- Notebook computer

### TYPICAL APPLICATION CIRCUIT

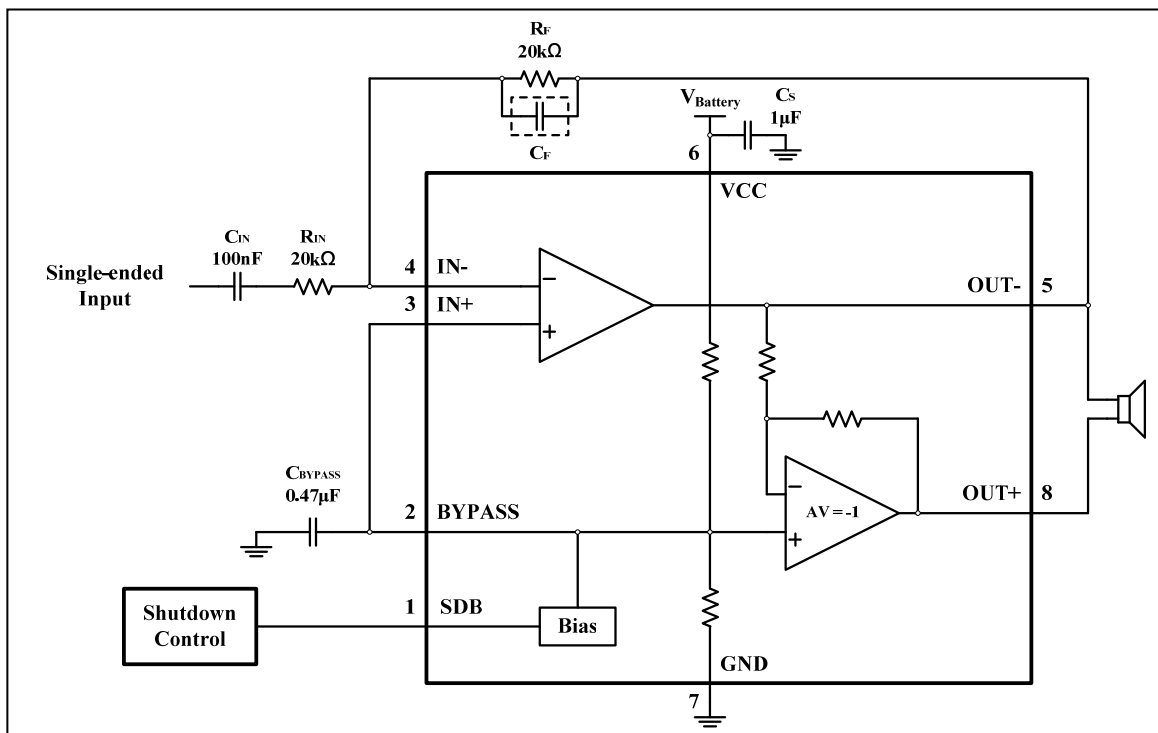


Figure 1 Typical Application Circuit (Single-ended input)

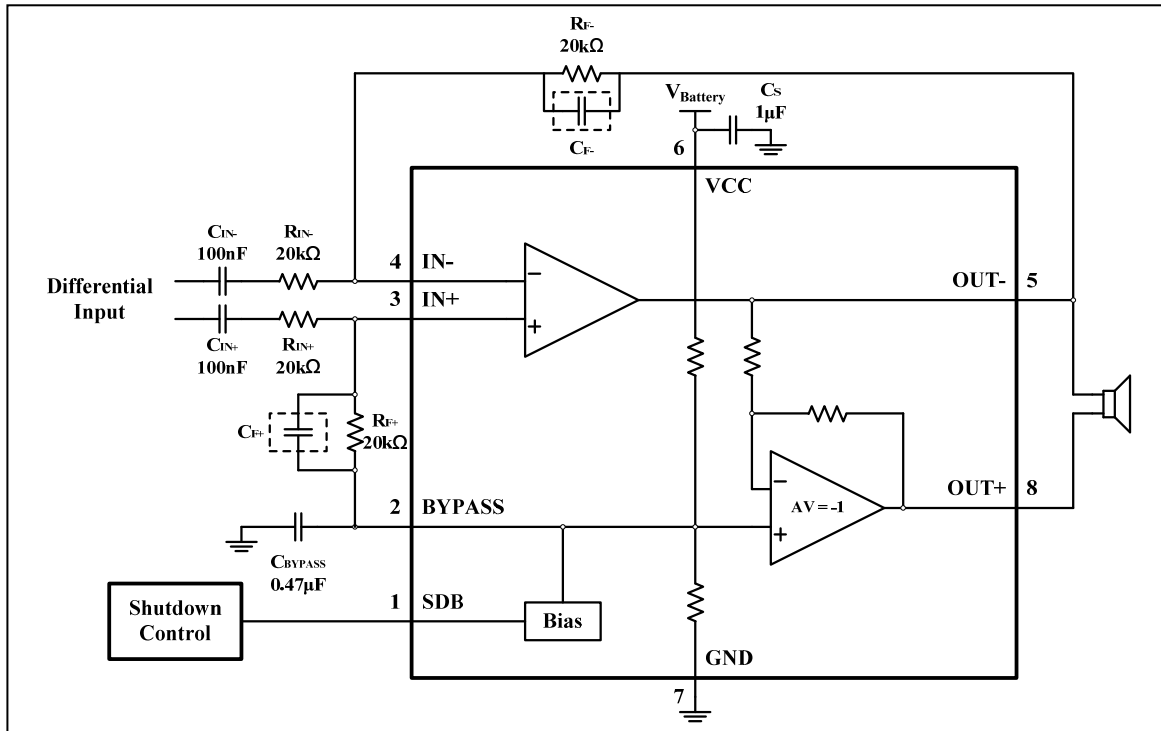
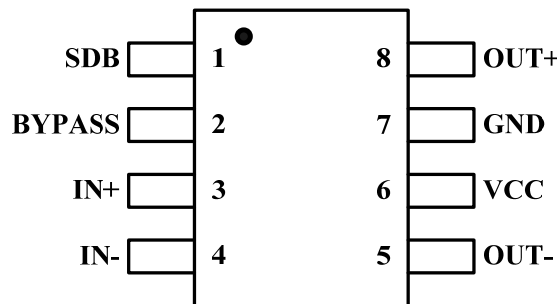


Figure 2 Typical Application Circuit (Differential input)

## PIN CONFIGURATION

Package	Pin Configuration (Top View)
SOP-8 MSOP-8	

## PIN DESCRIPTION

No.	Pin	Description
1	SDB	The device enters shutdown mode when a low level is applied on this pin.
2	BYPASS	Bypass capacitor pin which provides the common mode voltage ( $V_{CC}/2$ ).
3	IN+	Positive input of the first amplifier.
4	IN-	Negative input of the first amplifier, receives the audio input signal. Connected to the feedback resistor $R_F$ and to the input resistor $R_{IN}$ .
5	OUT-	Negative output of the IS31AP4991A. Connected to the load and to the feedback resistor $R_F$ .
6	VCC	Positive analog supply of the chip.
7	GND	Ground.
8	OUT+	Positive output of the IS31AP4991A. Connected to the load.

# IS31AP4991A



## ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Order Part No.	Package	QTY/Reel
IS31AP4991A-GRLS2-TR	SOP-8, Lead-free	2500
IS31AP4991A-SLS2-TR	MSOP-8, Lead-free	2500

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- b.) the user assume all such risks; and
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## ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Supply voltage, $V_{CC}$	-0.3V ~ +6.0V
Voltage at any input pin	-0.3V ~ $V_{CC}+0.3V$
Maximum junction temperature, $T_{JMAX}$	+150°C
Storage temperature range, $T_{STG}$	-65°C ~ +150°C
Operating temperature range, $T_A$	-40°C ~ +85°C
Maximum power dissipation, SOP-8(25°C/85°C) (Note 2) MSOP-8(25°C/85°C)	720mW/380mW 590mW/310mW

**Note 1:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:** Thermal simulation @ 25°C /85°C ambient temperature, still air convection, 2s2p boards according to JESD51. The Pd (max by package) is evaluated by  $(T_{jmax}-T_a)/\Theta_{ja}$ .

## ELECTRICAL CHARACTERISTICS

The following specifications apply for  $C_{IN} = 0.1\mu F$ ,  $R_{IN} = R_F = 20k\Omega$ ,  $C_{BYPASS} = 0.47\mu F$ , unless otherwise specified. Limits apply for  $T_A = 25^\circ C$ .  $V_{CC}=5V$  (Note 3 or specified)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$I_{CC}$	Quiescent power supply current	$V_{CC} = 0V$ , $I_o = 0A$ , no Load		3.0		mA
$I_{SDB}$	Shutdown current	$V_{SDB} = GND$ , $R_L = \infty$			1	$\mu A$
$V_{SD\_H}$	Shutdown voltage input high	$V_{CC} = 5.5V$	1.4			V
$V_{SD\_L}$	Shutdown voltage input low	$V_{CC} = 2.7V$			0.4	V
$V_{OS}$	Output offset voltage				15	mV
$P_o$	Output power (8 $\Omega$ )	THD+N = 1%; f = 1kHz		1.15		W
		THD+N = 10%; f = 1kHz		1.40		
$t_{WU}$	Wake-up time (Note 4)	$C_{BYPASS} = 0.47\mu F$		100	250	ms
THD+N	Total harmonic distortion+noise (Note 4)	$P_o = 0.5W_{rms}$ ; f = 1kHz		0.074		%
PSRR	Power supply rejection ratio (Note 4)	$V_{ripple\ p-p} = 200mV$ Input Grounded	f = 217Hz		56	dB
			f = 1kHz		68	

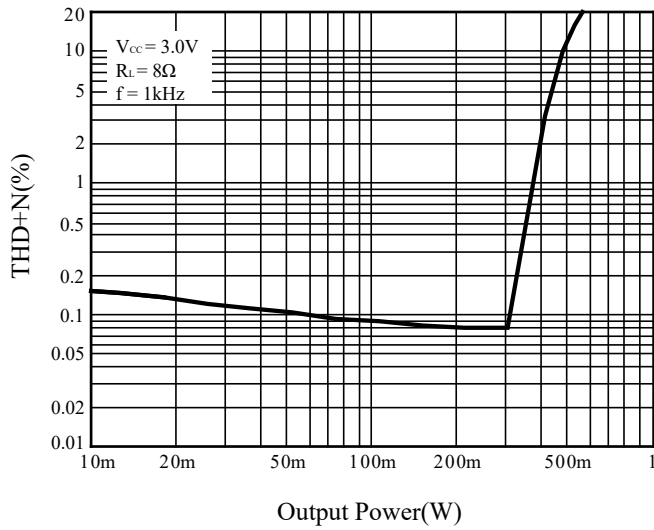
The following specifications apply for  $C_{IN} = 0.1\mu F$ ,  $R_{IN} = R_F = 20k\Omega$ ,  $C_{BYPASS} = 0.47\mu F$ , unless otherwise specified. Limits apply for  $T_A = 25^\circ C$ .  $V_{CC}=3V$  (Note 3 or specified)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$I_{CC}$	Quiescent power supply current	$V_{CC} = 0V$ , $I_o = 0A$ , no Load		2.2		mA
$I_{SDB}$	Shutdown current	$V_{SDB} = GND$ , $R_L = \infty$			1	$\mu A$
$P_o$	Output power (8 $\Omega$ )	THD+N = 1%; f = 1kHz		380		mW
		THD+N = 10%; f = 1kHz		490		
$t_{WU}$	Wake-up time (Note 4)	$C_{BYPASS} = 0.47\mu F$		90	200	ms
THD+N	Total harmonic distortion+noise (Note 4)	$P_o = 0.3W_{rms}$ ; f = 1kHz		0.076		%

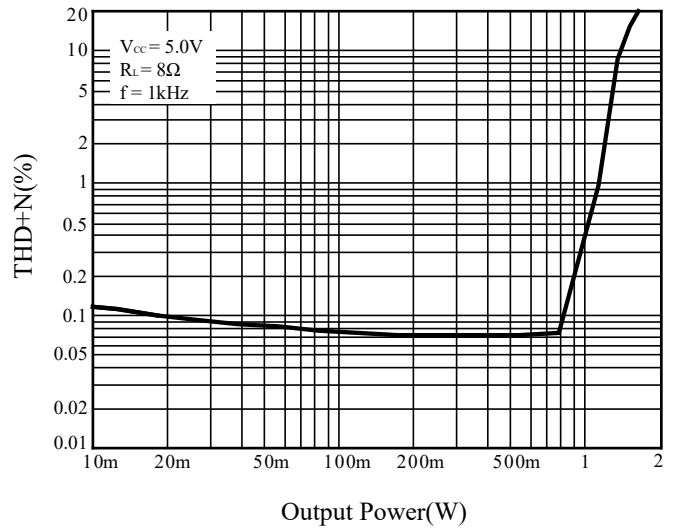
**Note 3:** Production testing of the device is performed at 25°C. Functional operation of the device and parameters specified over other temperature range, are guaranteed by design, characterization and process control.

**Note 4:** Guaranteed by design.

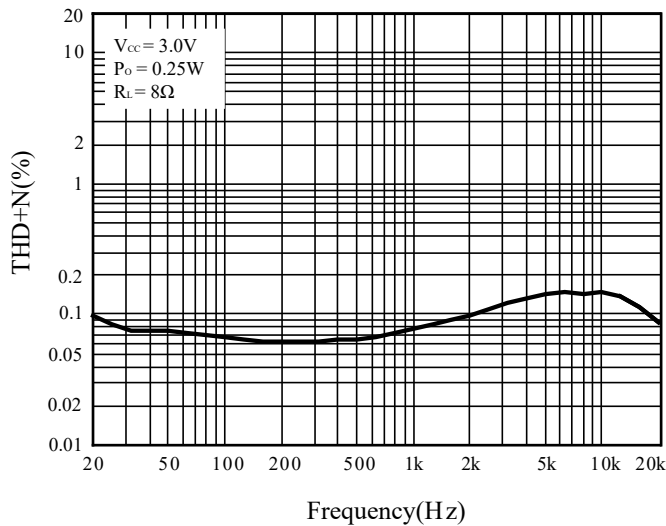
## TYPICAL PERFORMANCE CHARACTERISTIC



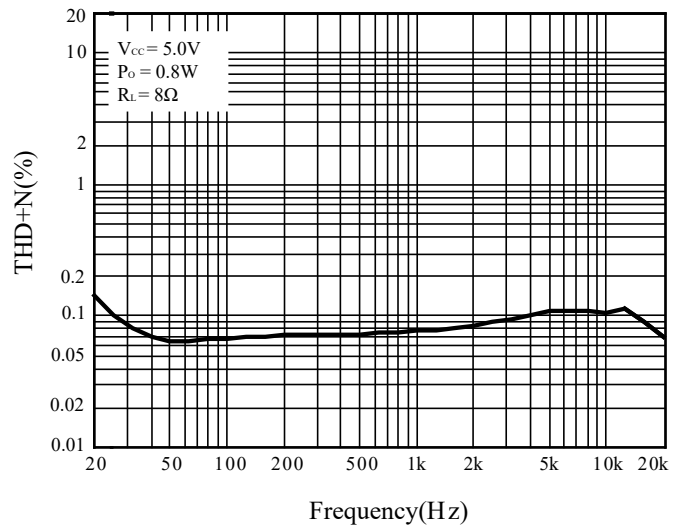
**Figure 3** THD+N vs. Output Power



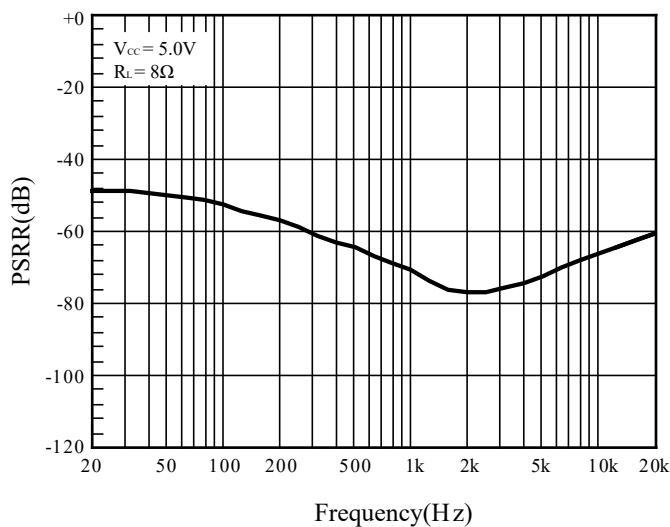
**Figure 4** THD+N vs. Output Power



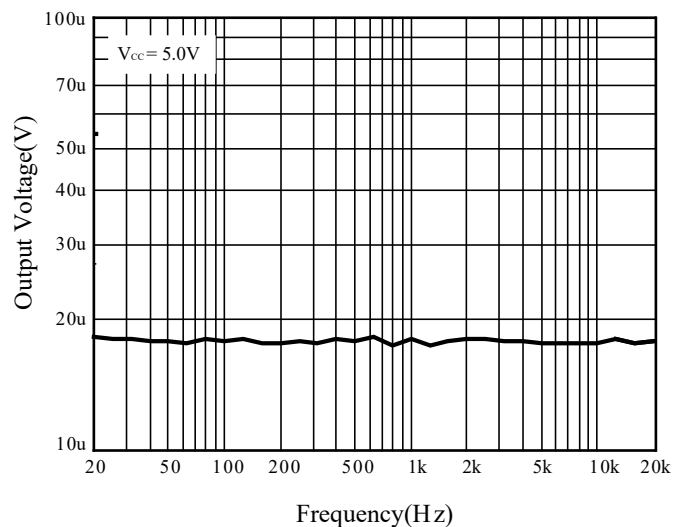
**Figure 5** THD+N vs. Frequency



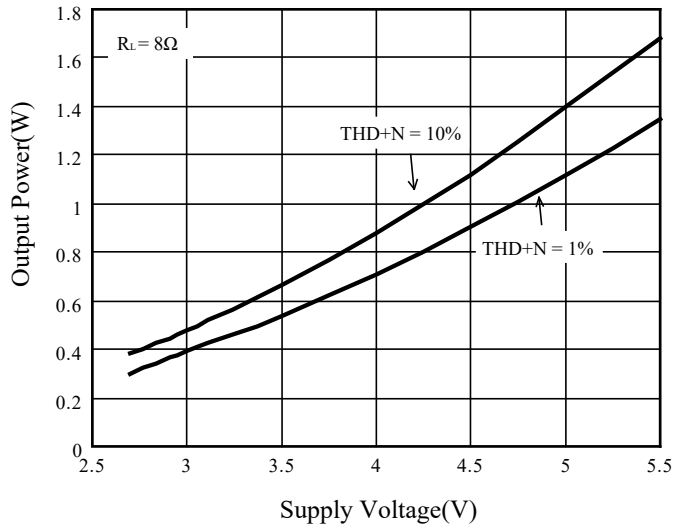
**Figure 6** THD+N vs. Frequency



**Figure 7** PSRR vs. Frequency



**Figure 8** Noise Floor



**Figure 9** Output Power vs. Power Supply

## APPLICATION INFORMATION

### BTL CONFIGURATION PRINCIPLE

The IS31AP4991A is a monolithic power amplifier with a BTL output type. BTL (bridge tied load) means that each end of the load is connected to two single-ended output amplifiers. Thus, we have:

Single-ended output 1 =  $V_{OUT+} = V_{OUT}$  (V)

Single ended output 2 =  $V_{OUT-} = -V_{OUT}$  (V)

and

$V_{OUT+} - V_{OUT-} = 2V_{OUT}$  (V)

The output power is:

$$P_{OUT} = \frac{(2V_{OUT_{RMS}})^2}{R_L}$$

For the same power supply voltage, the output power in BTL configuration is four times higher than the output power in single ended configuration.

### GAIN IN A TYPICAL APPLICATION SCHEMATIC

The typical application schematic is shown in Figure 1 on page 1.

In the flat region (no  $C_{IN}$  effect), the output voltage of the first stage is (in Volts):

$$V_{OUT-} = (-V_{IN}) \frac{R_F}{R_{IN}}$$

For the second stage:  $V_{OUT+} = -V_{OUT-}$  (V)

The differential output voltage is (in Volts):

$$V_{OUT+} - V_{OUT-} = 2V_{IN} \frac{R_F}{R_{IN}}$$

The differential gain,  $G_v$ , is given by:

$$G_v = \frac{V_{OUT+} - V_{OUT-}}{V_{IN}} = 2 \frac{R_F}{R_{IN}}$$

$V_{OUT-}$  is in phase with  $V_{IN}$  and  $V_{OUT+}$  is phased  $180^\circ$  with  $V_{IN}$ . This means that the positive terminal of the loudspeaker should be connected to  $V_{OUT+}$  and the negative to  $V_{OUT-}$ .

### LOW AND HIGH FREQUENCY RESPONSE

In the low frequency region,  $C_{IN}$  starts to have an effect.  $C_{IN}$  forms with  $R_{IN}$  a high-pass filter with a -3dB cut-off frequency.  $f_{CL}$  is in Hz.

$$f_{CL} = \frac{1}{2\pi R_{IN} C_{IN}}$$

In the high frequency region, you can limit the bandwidth by adding a capacitor ( $C_F$ ) in parallel with  $R_F$ . It forms a low-pass filter with a -3dB cut-off frequency.  $f_{CH}$  is in Hz.

$$f_{CH} = \frac{1}{2\pi R_F C_F}$$

### DECOUPLING OF THE CIRCUIT

Two capacitors are needed to correctly bypass the IS31AP4991A: a power supply bypass capacitor  $C_S$  and a bias voltage bypass capacitor  $C_{BYPASS}$ .

$C_S$  has particular influence on the THD+N in the high frequency region (above 7kHz) and an indirect influence on power supply disturbances. With a value for  $C_S$  of  $1\mu F$ , you can expect THD+N levels similar to those shown in the datasheet.

In the high frequency region, if  $C_S$  is lower than  $1\mu F$ , it increases THD+N and disturbances on the power supply rail are less filtered.

On the other hand, if  $C_S$  is higher than  $1\mu F$ , those disturbances on the power supply rail are more filtered.

$C_{BYPASS}$  has an influence on THD+N at lower frequencies, but its function is critical to the final result of PSRR (with input grounded and in the lower frequency region).

If  $C_{BYPASS}$  is lower than  $0.47\mu F$ , THD+N increases at lower frequencies and PSRR worsens.

If  $C_{BYPASS}$  is higher than  $0.47\mu F$ , the benefit on THD+N at lower frequencies is small, but the benefit to PSRR is substantial.

Note that  $C_{IN}$  has a non-negligible effect on PSRR at lower frequencies. The lower the value of  $C_{IN}$ , the higher the PSRR is.

### WAKE-UP TIME ( $t_{WU}$ )

When the standby is released to put the device on, the bypass capacitor  $C_{BYPASS}$  will not be charged immediately. As  $C_{BYPASS}$  is directly linked to the bias of the amplifier, the bias will not work properly until the  $C_{BYPASS}$  voltage is correct. The time to reach this voltage is called wake-up time or  $t_{WU}$  and specified in the electrical characteristics table with  $C_{BYPASS} = 0.47\mu F$ .

### POP PERFORMANCE

Pop performance is intimately linked with the size of the input capacitor  $C_{IN}$  and the bias voltage bypass capacitor  $C_{BYPASS}$ .

The size of  $C_{IN}$  is dependent on the lower cut-off frequency and PSRR values requested. The size of  $C_{BYPASS}$  is dependent on THD+N and PSRR values requested at lower frequencies.

Moreover,  $C_{BYPASS}$  determines the speed with which the amplifier turns on.



## CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
<b>Preheat &amp; Soak</b> Temperature min (T <sub>smin</sub> ) Temperature max (T <sub>smax</sub> ) Time (T <sub>smin</sub> to T <sub>smax</sub> ) (t <sub>s</sub> )	150°C 200°C 60-120 seconds
Average ramp-up rate (T <sub>smax</sub> to T <sub>p</sub> )	3°C/second max.
Liquidous temperature (T <sub>L</sub> ) Time at liquidous (t <sub>L</sub> )	217°C 60-150 seconds
Peak package body temperature (T <sub>p</sub> )*	Max 260°C
Time (t <sub>p</sub> )** within 5°C of the specified classification temperature (T <sub>c</sub> )	Max 30 seconds
Average ramp-down rate (T <sub>p</sub> to T <sub>smax</sub> )	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

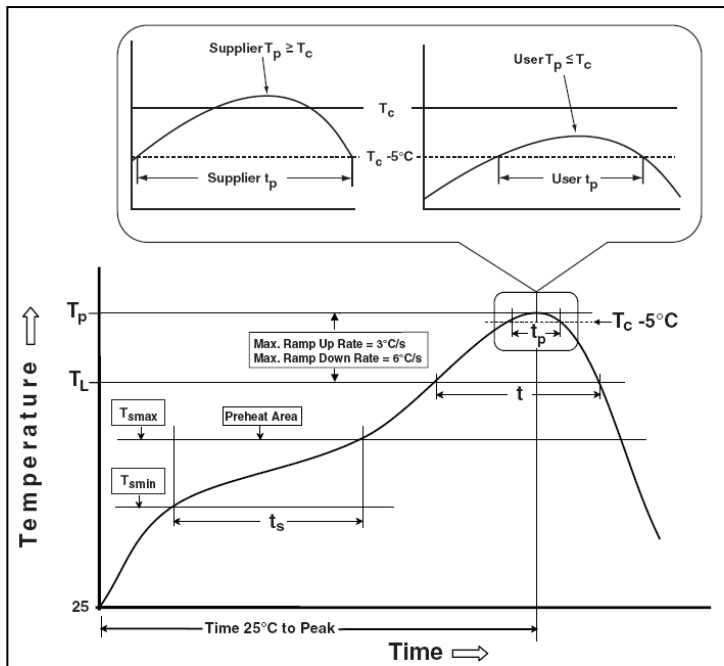
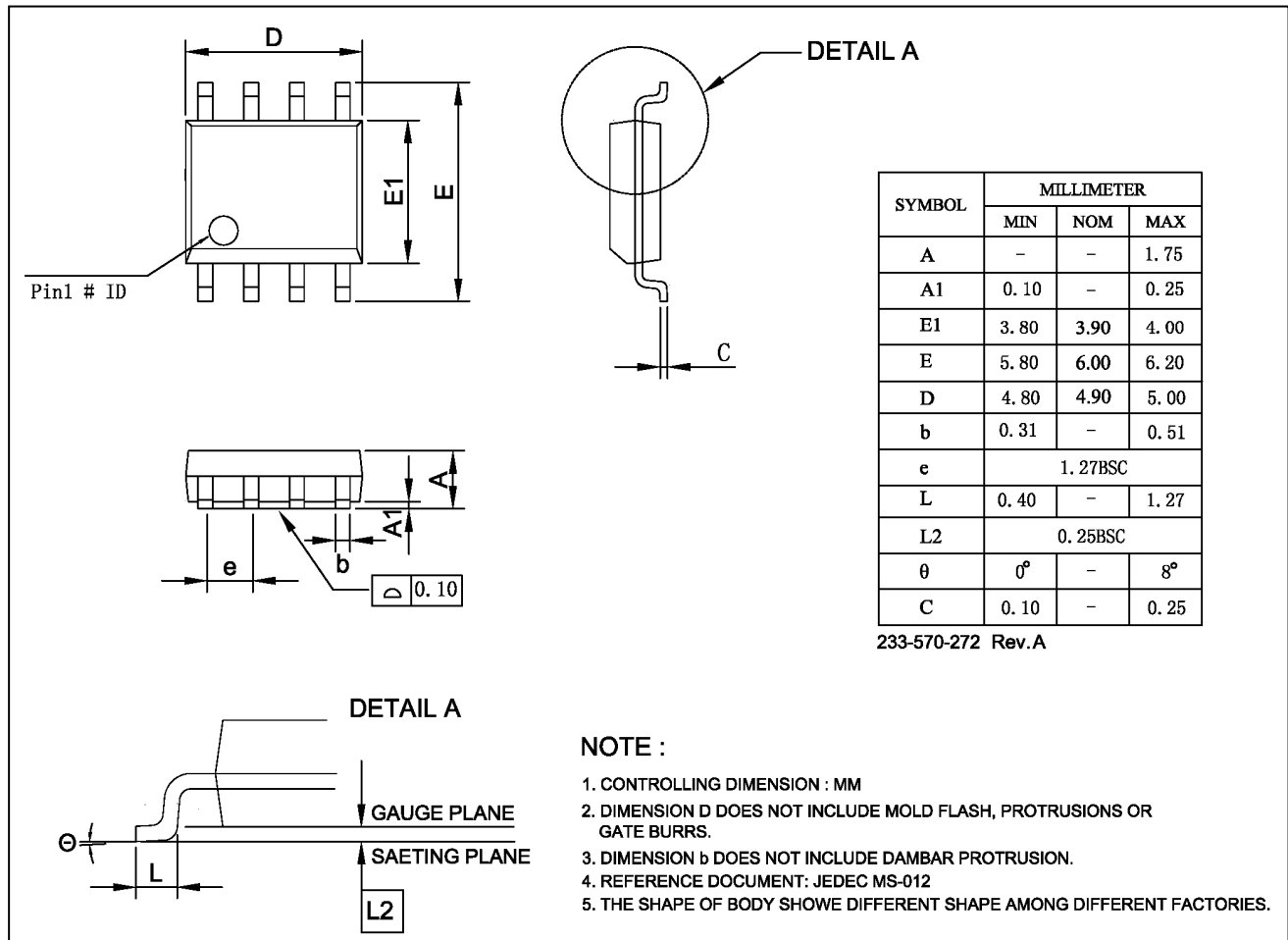


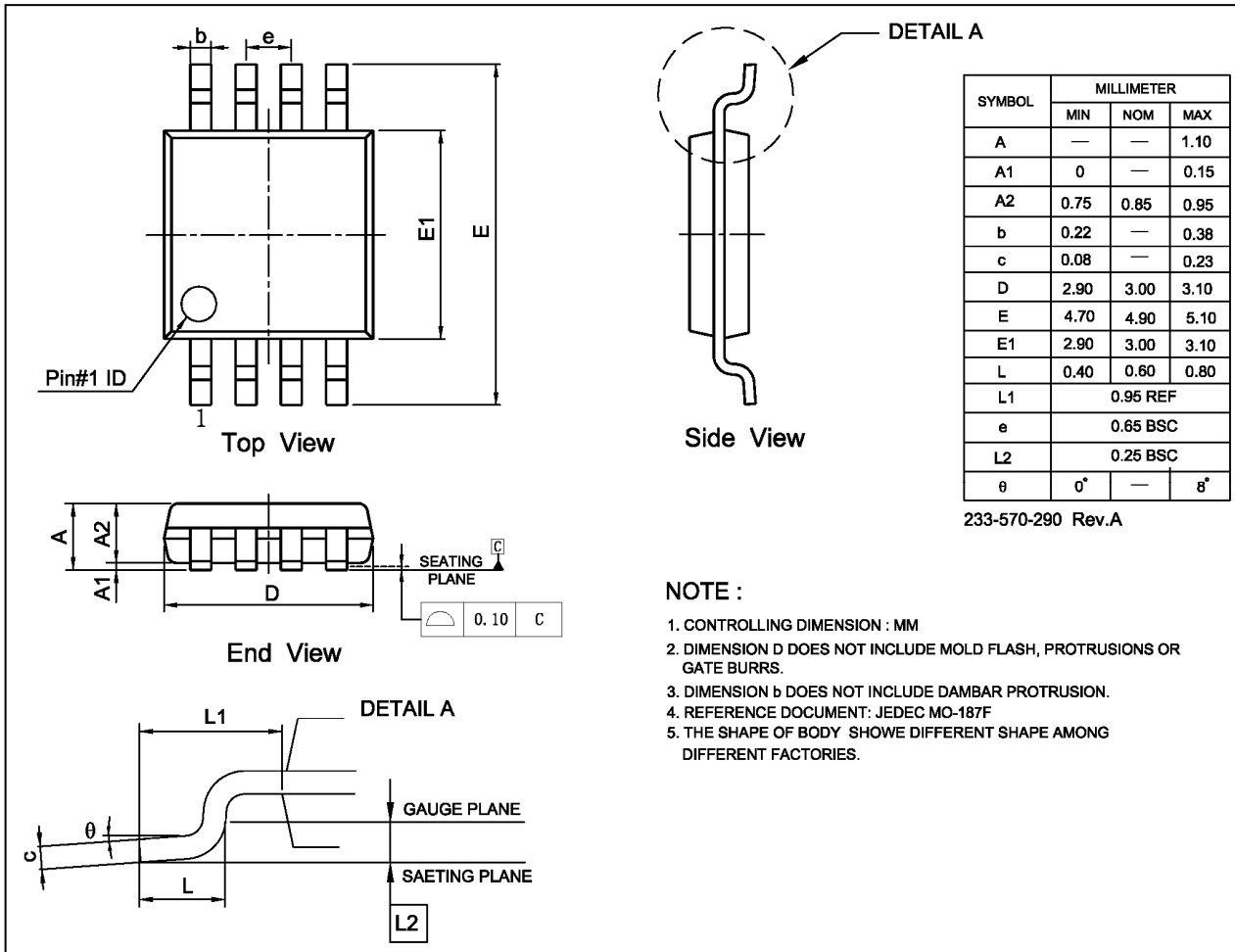
Figure 10 Classification Profile

## PACKAGE INFORMATION

### SOP-8

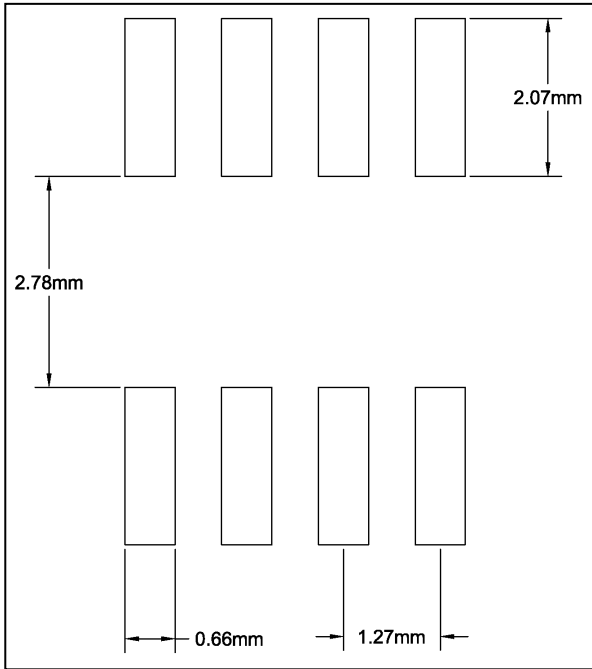


## MSOP-8

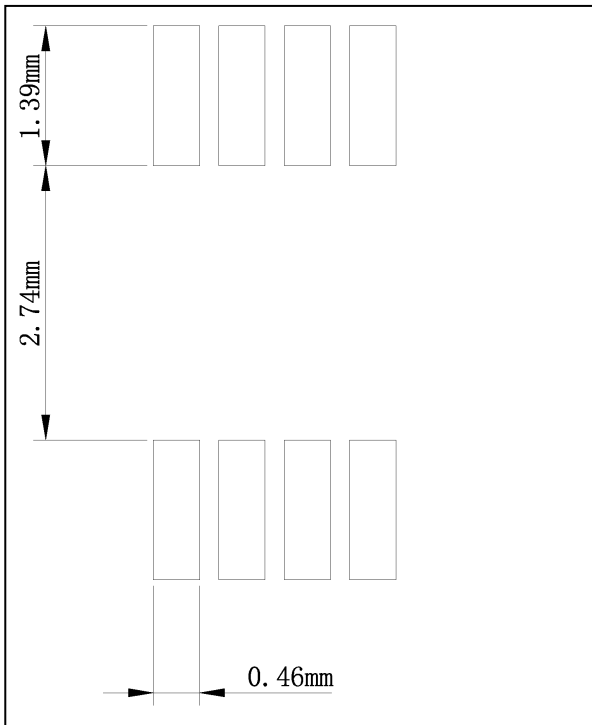


## RECOMMENDED LAND PATTERN

### SOP-8



### MSOP-8



**Note:**

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

## REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2013.03.07
B	P.5 update EC table	2013.05.14
C	P.1-2 modify typical circuit P.5 update EC table	2013.05.14
D	1. Update to new Lumissil logo 2. Update POD and add LP, RoHS	2024.03.18

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