S-UM6532

LOW CHARGE INJECTION 64-CHANNEL 6Ω HIGH-VOLTAGE ANALOG SWITCHES

Rev.1.0_00

The ABLIC S-UM6532 is a low charge injection 64-channel single-pole single-throw (SPST) high-voltage analog switch IC operated only by a single 5V for ultrasound imaging applications. The S-UM6532 has ±100V analog signal range allowing ±150V voltage overshoot.

■ Function

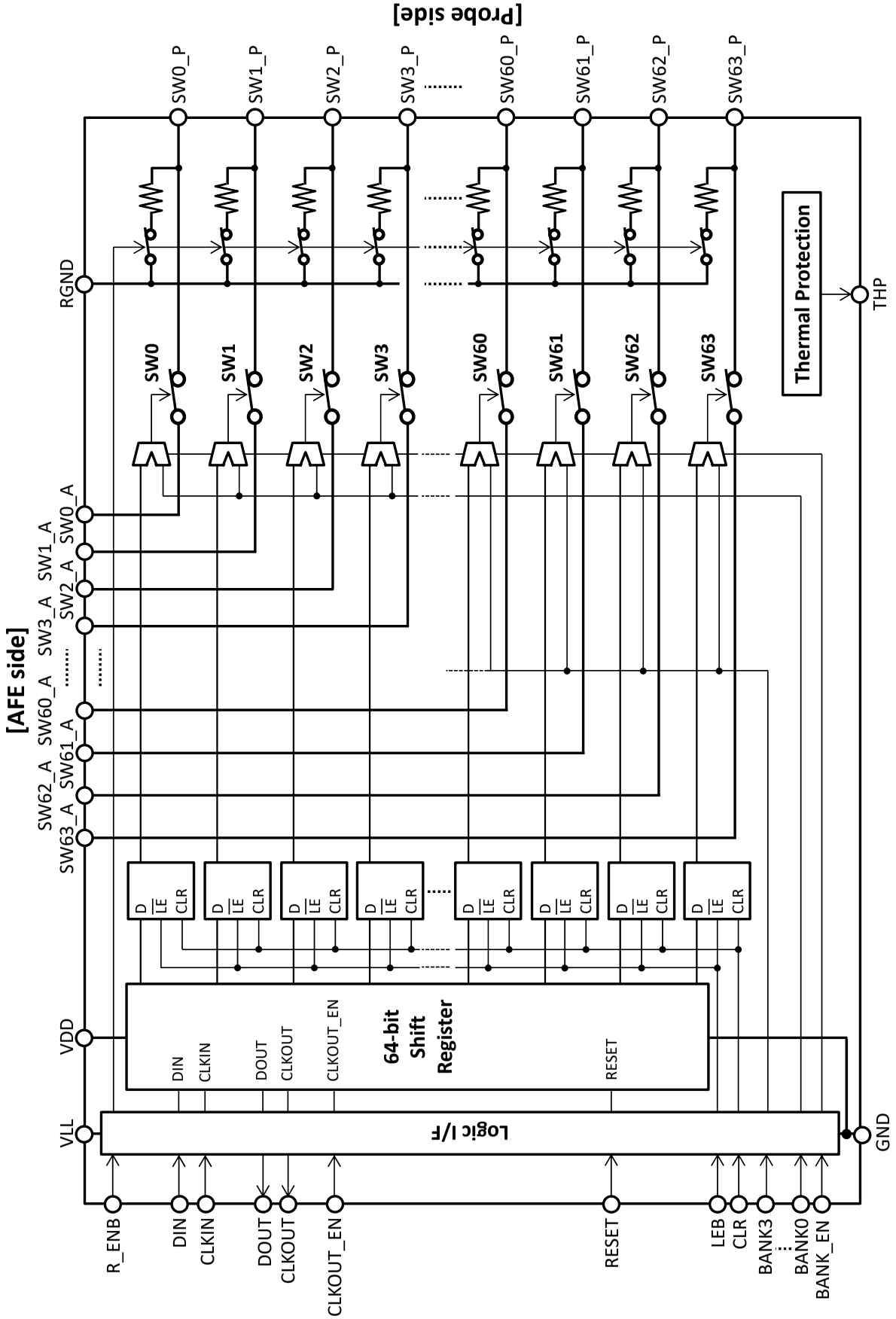
- 64-channel high-voltage SPST analog switches with user-selectable logic interface and bleed resistor

■ Features

- 0V to ±100V analog signal voltage range allowing ±150V voltage overshoot
- 10kHz to 70MHz analog signal frequency range
- 2A peak analog signal current per channel
- 6Ω switch on-resistance
- Single +5V power supply (NO HIGH-VOLTAGE POWER SUPPLY required)
- User-selectable Serial Digital Interface (64-bit shift registers) or Bank Interface (4 banks of 16-channel)
- User-selectable 40kΩ bleed resistor on probe side
- Low on/off-capacitance
- 15pC charge injection to 1000pF
- -75dB off-isolation at analog small-signal 5MHz
- -60dB switch crosstalk
- 1.8V to 5V CMOS logic interface
- Low power dissipation (static 5mW)
- Embedded thermal protection with flag indicator
- RoHS compliant 15x15mm BGA package

■ Contents

■ Block Diagram



■ Absolute Maximum Ratings

T_A=25°C unless otherwise noted.

No.	Items	Symbol	Value	Units	Condition
1	Positive logic supply voltage	V_{LL}	-0.4 to +7	V	
2	Positive supply voltage	V_{DD}	-0.4 to +7	V	
3	Logic input voltage	DIN, CLKIN, RESET, CLR, LEB, BANK0, BANK1, BANK2, BANK3, BANK_EN, CLKOUT_EN, R_ENB	-0.4 to +7	V	
4	Logic output voltage	DOUT, CLKOUT, THP	-0.4 to +7	V	
5	Analog signal range (steady state voltage)	V_{SIG}	-105 to +105	V	
6	Analog signal range (peak overshoot voltage)	V_{SIG_OS}	-150 to +150	V	Max. 500ns pulse width
7	Peak analog signal current per channel	I_{SW}	2	A	
8	Operating junction temperature	T_{Jop}	-20 to +150	°C	
9	Storage temperature	T_{STG}	-55 to +150	°C	
10	Maximum power dissipation	P_{Dmax}	4	W	

■ Operating Supply Voltages, Temperature, Logic Levels

T_A=25°C unless otherwise noted.

No.	Items	Symbol	Min	Typ	Max	Units	Condition
1	Logic supply voltage	V_{LL}	1.7	1.8 to 5	V_{DD}	V	
2	Positive supply voltage	V_{DD}	4.75	5	5.25	V	
3	Operating free-air temperature	T_A	0	-	75	°C	
4	High-level logic input voltage	V_{IH}	0.8V_{LL}	-	V_{LL}	V	
5	Low-level logic input voltage	V_{IL}	0	-	0.2V_{LL}	V	
6	High-level logic output voltage	V_{OH}	0.8V_{LL}	-	-	V	I_{SOURCE}=1mA
7	Low-level logic output voltage	V_{OL}	-	-	0.2V_{LL}	V	I_{SINK}=1mA
8	Logic input high current *1)	I_{IH}	-10	-	10	µA	DIN, CLKIN, RESET, CLR, LEB, BANK0, BANK1, BANK2, BANK3, BANK_EN, CLKOUT_EN, R_ENB
9	Logic input low current	I_{IL}	-10	-	10	µA	
10	Logic input capacitance	C_{IN}	-	2	-	pF	
11	Clock frequency	f_{CLK}	-	-	50	MHz	CLKOUT_EN=0,V_{LL}=1.8V
			-	-	80	MHz	CLKOUT_EN=0,V_{LL}=2.5V
			-	-	95	MHz	CLKOUT_EN=0,V_{LL}=3.3V
			-	-	60	MHz	CLKOUT_EN=1,V_{LL}=1.8V
			-	-	85	MHz	CLKOUT_EN=1,V_{LL}=2.5V
			-	-	130	MHz	CLKOUT_EN=1,V_{LL}=3.3V
12	Clock rise and fall times	t_R, t_F	-	-	50	ns	
13	CLKIN to DOUT delay	t_{DO}	7	10	24	ns	
14	CLKOUT to DOUT delay	t_{DO1}	1.3	-	1.9	ns	
15	CLKIN to CLKOUT delay	t_{DCKO}	7	10	24	ns	
16	DIN to CLKIN setup time	t_{SU}	1	-	-	ns	
17	DIN to CLKIN hold time	t_{HD}	2	-	-	ns	
18	LEB setup time	t_{SLEB}	5	-	-	ns	
19	LEB low-pulse width	t_{WLEB}	12	-	-	ns	
20	CLR response time	t_{DCLR}	-	-	500	ns	
21	CLR high-pulse width	t_{WCLR}	12	-	-	ns	
22	Bank interface setup time	t_{SBNK}	100	-	-	ns	
23	Bank interface hold time	t_{HBNK}	1	-	-	us	
24	BANKx minimum pulse width	t_{WBNK}	4	-	-	us	
25	RESET response time	t_{DRST}	-	-	400	ns	
26	RESET high-pulse width	t_{WRST}	12	-	-	ns	

NOTE: *1) BANK_EN, CLKOUT_EN, and R_ENB have 100µA leakage at V_{LL}=5V due to 50kΩ internal pull-down resistor.

■ Power Supply Sequencing

No power supply sequencing is required even if V_{LL} is different from V_{DD}.
Please apply the V_{DD} voltage to the V_{LL} when operating with a single 5V.

■ DC Characteristics

V_{LL}=3.3V, V_{DD}=5V, LEB=0, T_A=25°C, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Analog signal range (steady state voltage)	V_{SIG}	-100	-	+100	V	
2	Analog signal range (peak overshoot voltage)	V_{SIG_OS}	-150	-	+150	V	Max. 500ns pulse width
3	V_{LL} quiescent current	I_{LLQ}	-	0.2	-	μA	Quiescent current-1 All switches off
4	V_{DD} quiescent current	I_{DDQ}	-	4.3	-	mA	
5	V_{LL} quiescent current	I_{LLQ}	-	0.2	-	μA	Quiescent current-2 All switches on
6	V_{DD} quiescent current	I_{DDQ}	-	4.3	-	mA	
7	V_{LL} dynamic current	I_{LL}	-	2	10	μA	Dynamic current All channels switching simultaneously at f_{SW}=50kHz
8	V_{DD} dynamic current	I_{DD}	-	9	11	mA	
9	DC offset switch off	V_{OS}	-	0	-	mV	
10	Small signal switch on-resistance	R_{ONS}	-	6	8	Ω	V_{SIG}=0.1Vpp to 5Vpp @5MHz, R_S=10Ω
11	Small signal switch on-resistance matching	ΔR_{ONS}	-	2	5	%	V_{SIG}=0V, I_{SIG}=5mA
12	Large signal switch on-resistance	R_{ONL}	-	6	-	Ω	V_{SIG}=20Vpp@5MHz, R_S=10Ω
13	Bleed resistance	R_{BLD}	30	40	50	kΩ	R_ENB=0, probe side only
14	Switch output peak current	I_{SW}	-	2	-	A	100ns pulse, 0.1% duty cycle

■ Thermal Protection Characteristics

V_{LL}=3.3V, V_{DD}=5V, LEB=0, T_A=25°C, unless otherwise specified.

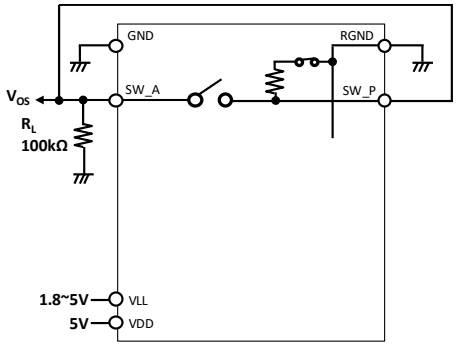
No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	THP pull-up voltage	V_{PUTHP}	-	-	5.25	V	Open drain
2	THP output current	I_{THP}	-	1.0	-	mA	-
3	THP output low voltage	V_{OLTHP}	-	-	0.5	V	THP active, V_{LL}=3.3V, I_{THP}=1mA
4	THP temperature threshold	T_{THP}	90	110	130	ºC	Thermal protection flag indicator by THP pin (open N-MOS drain, Low=THP activating)
5	THP reset hysteresis	T_{HYSTHP}	-	10	-	ºC	

■ AC Characteristics

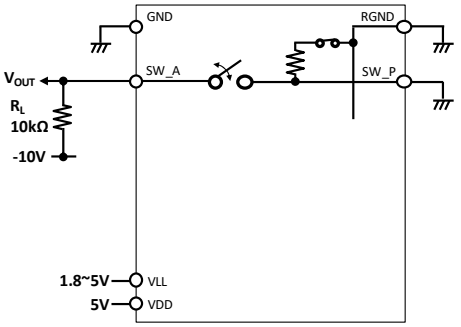
V_{LL}=3.3V, V_{DD}=5V, LEB=0, T_A=25°C, unless otherwise specified.

No.	Items		Symbol	Spec			Units	Conditions
				Min	Typ	Max		
1	Turn-on time		t_{ON}	-	2	4	µs	BANK_EN=0
			t_{ON_BNK}	-	2	4	µs	BANK_EN=1
2	Turn-off time		t_{OFF}	-	2	4	µs	BANK_EN=0
			t_{OFF_BNK}	-	2	4	µs	BANK_EN=1
3	Output switching frequency		f_{SW}	-	-	50	kHz	Duty cycle=50%
4	Small signal frequency		f_{SIG}	0.01	-	70	MHz	C_L=220pF
5	Off isolation	small signal	$V_{ISO(RX)}$	-	-75	-	dB	f_{SIG}=5MHz, R_L=50Ω
		large signal	$V_{ISO(TX)}$	-	-60	-	dB	f_{SIG}=5MHz, R_L=50Ω
6	Crosstalk		V_{CT}	-	-60	-	dB	f_{SIG}=5MHz, R_L=50Ω
7	On capacitance	small signal	$C_{ON(RX)}$	-	27	-	pF	V_{SIG}=0V, f_{SIG}=1MHz
		large signal	$C_{ON(TX)}$	-	27	-	pF	V_{SIG}=10Vpp, f_{SIG}=1MHz
8	Off capacitance SW_P to GND	small signal	$C_{OFF(SWP\_RX)}$	-	18	-	pF	V_{SIG}=0V, f_{SIG}=1MHz
9	Off capacitance SW_A to GND	small signal	$C_{OFF(SWA\_RX)}$	-	14	-	pF	V_{SIG}=0V, f_{SIG}=1MHz
		large signal	$C_{OFF(SWA\_TX)}$	-	16	-	pF	V_{SIG}=10Vpp, f_{SIG}=1MHz
10	Output spike voltage (SW_P)		$V_{SPK\_ON(SWP)}$	-	30	-	mV	50Ω load @switch on
			$V_{SPK\_OFF(SWP)}$	-	60	-	mV	50Ω load @switch off
11	Output spike voltage (SW_A)		$V_{SPK\_ON(SWA)}$	-	30	-	mV	50Ω load @switch on
			$V_{SPK\_OFF(SWA)}$	-	60	-	mV	50Ω load @switch off
12	Charge injection		QC	-	15	-	pC	

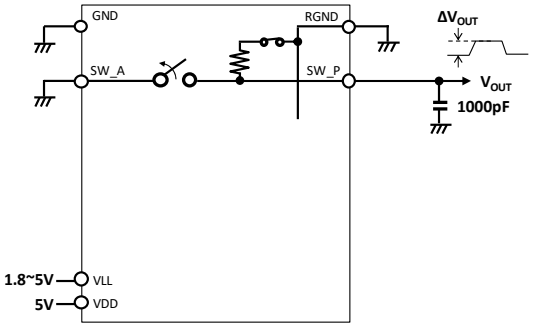
■ Test Circuits



DC Offset OFF

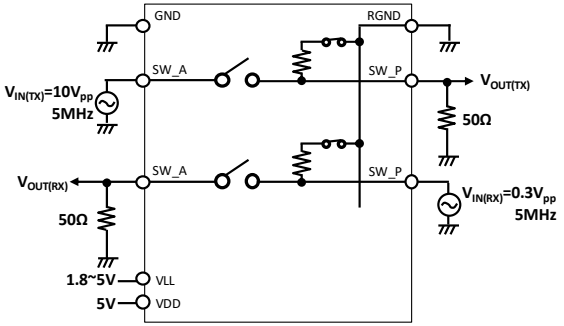


t_{ON}/t_{OFF} test circuit



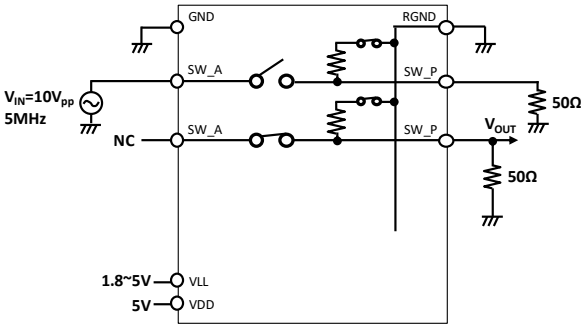
$Q=1000pF*\Delta V_{OUT}$

Charge Injection



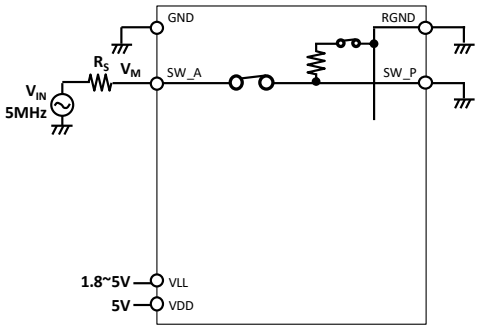
$V_{ISO}=20Log(V_{OUT}/V_{IN})$

Off isolation



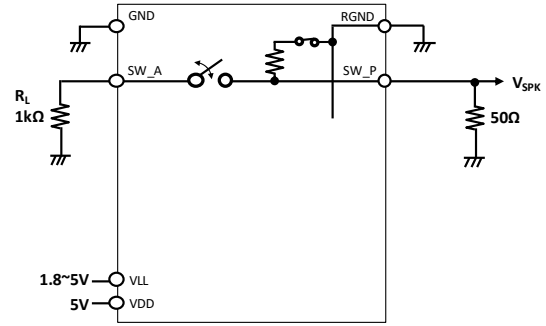
$V_{CT}=20Log(V_{OUT}/V_{IN})$

Crosstalk

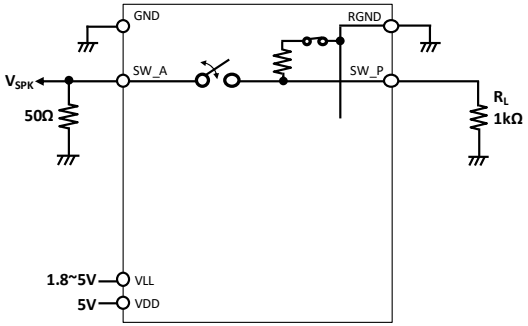


$R_{ON}=R_S*V_M/(V_{IN}-V_M)$

On resistance test circuit



Output spike voltage SW_P

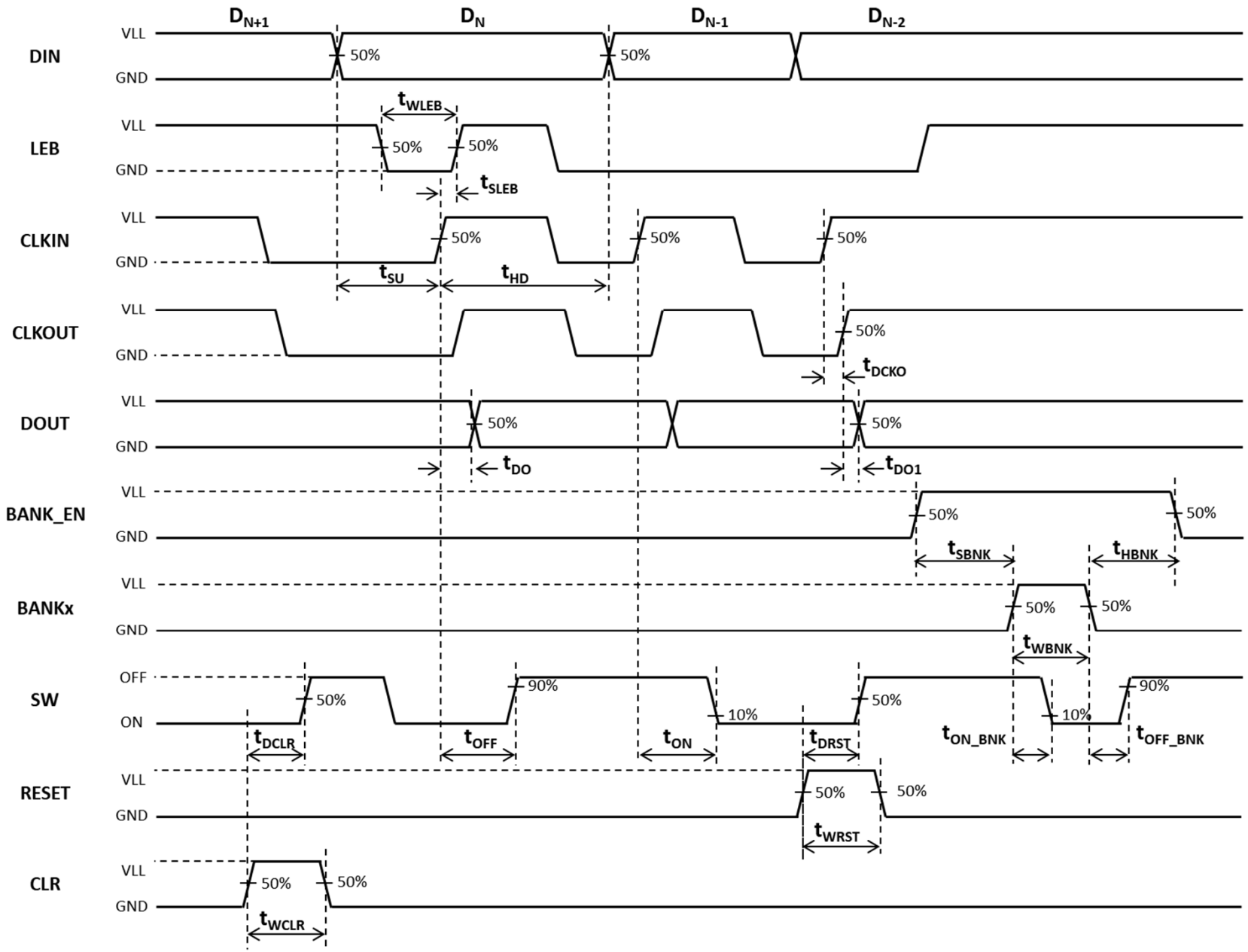


Output spike voltage SW_A

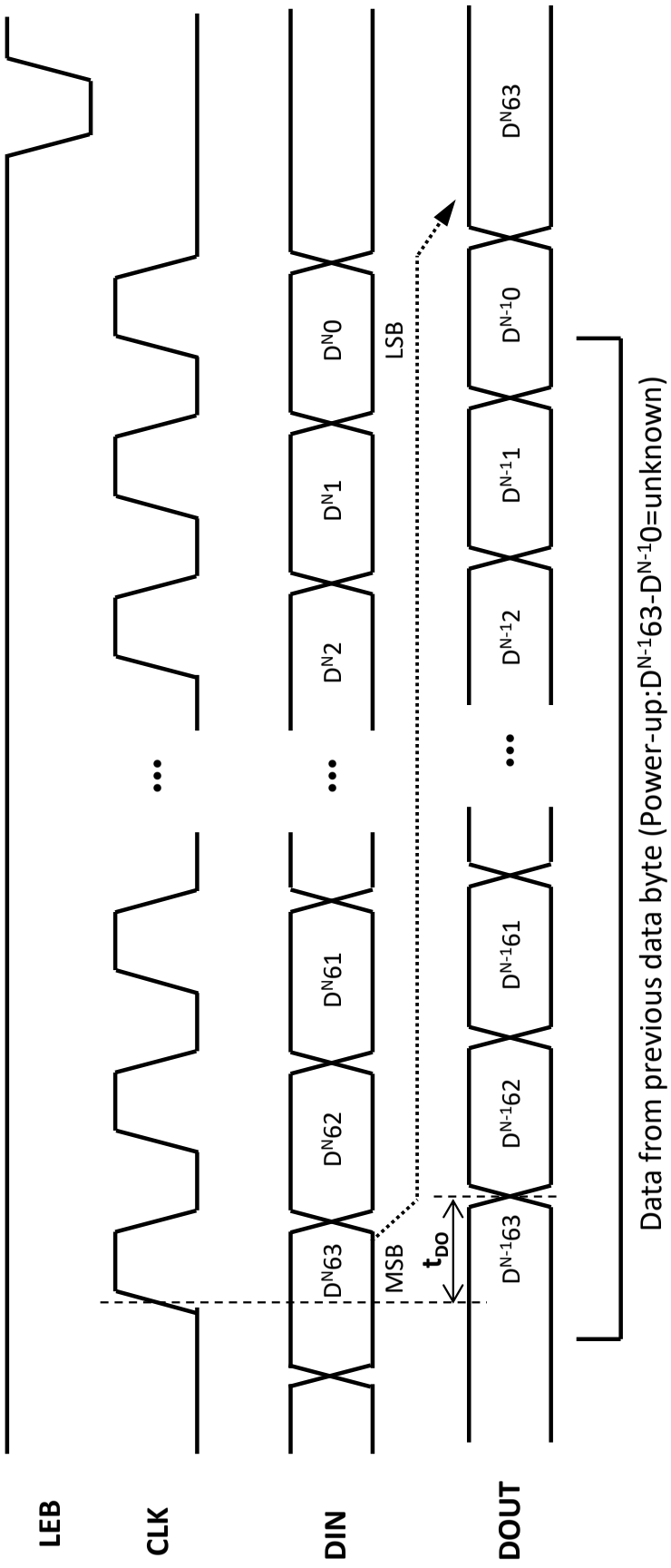
■ Truth Table

Logic Inputs																				Analog Switch State											
RESET	LEB	CLR	BANK_EN	BANK0	BANK1	BANK2	BANK3	DIN																							
								D0	...	D15	D16	...	D31	D32	...	D47	D48	...	D63	SW0	...	SW15	SW16	...	SW31	SW32	...	SW47	SW48	...	SW63
L	L	L	L	X	X	X	X	L		-	-		-	-		-	-		-	OFF		-	-		-	-		-	-		-
L	L	L	L	X	X	X	X	H		-	-		-	-		-	-		-	ON		-	-		-	-		-	-		-
L	L	L	L	X	X	X	X	-		L	-		-	-		-	-		-	-		OFF	-		-	-		-	-		-
L	L	L	L	X	X	X	X	-		H	-		-	-		-	-		-	-		ON	-		-	-		-	-		-
L	L	L	L	X	X	X	X	-		-	L		-	-		-	-		-	-		-	OFF		-	-		-	-		-
L	L	L	L	X	X	X	X	-		-	H		-	-		-	-		-	-		-	ON		-	-		-	-		-
L	L	L	L	X	X	X	X	-		-	-		L	-		-	-		-	-		-	-		OFF	-		-	-		-
L	L	L	L	X	X	X	X	-	...	-	-	...	H	-	...	-	-	...	-	-	...	-	-	...	ON	-	...	-	-	...	-
L	L	L	L	X	X	X	X	-		-	-		-	L		-	-		-	-		-	-		-	OFF		-	-		-
L	L	L	L	X	X	X	X	-		-	-		-	H		-	-		-	-		-	-		-	ON		-	-		-
L	L	L	L	X	X	X	X	-		-	-		-	-		L	-		-	-		-	-		-	-		OFF	-		-
L	L	L	L	X	X	X	X	-		-	-		-	-		H	-		-	-		-	-		-	-		ON	-		-
L	L	L	L	X	X	X	X	-		-	-		-	-		-	L		-	-		-	-		-	-		-	OFF		-
L	L	L	L	X	X	X	X	-		-	-		-	-		-	H		-	-		-	-		-	-		-	ON		-
L	L	L	L	X	X	X	X	-		-	-		-	-		-	-		L	-		-	-		-	-		-	-		OFF
L	L	L	L	X	X	X	X	-		-	-		-	-		-	-		H	-		-	-		-	-		-	-		ON
L	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Hold Previous State											
L	X	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	ALL SWs OFF											
H	H	L	L	X	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	Hold Previous State											
H	L	L	L	X	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	ALL SWs OFF											
X	X	X	H	**H**	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	**SW0~SW15 ON**			SW16~SW31 OFF			SW32~SW47 OFF			SW48~SW63 OFF		
X	X	X	H	L	**H**	L	L	X	X	X	X	X	X	X	X	X	X	X	X	SW0~SW15 OFF			**SW16~SW31 ON**			SW32~SW47 OFF			SW48~SW63 OFF		
X	X	X	H	L	L	**H**	L	X	X	X	X	X	X	X	X	X	X	X	X	SW0~SW15 OFF			SW16~SW31 OFF			**SW32~SW47 ON**			SW48~SW63 OFF		
X	X	X	H	L	L	L	**H**	X	X	X	X	X	X	X	X	X	X	X	X	SW0~SW15 OFF			SW16~SW31 OFF			SW32~SW47 OFF			**SW48~SW63 ON**		

■ Logic Timing



■ Latch Enable Interface Timing



■ Pin Description

Pin Name	I/O	Function
VLL	-	Positive voltage supply of low voltage interface (+1.8V~+5V)
VDD	-	Positive low voltage power supply (+5V)
GND	-	Drive power ground (0V)
RGND	-	Bleed resistor ground (0V)
DIN	I	Serial-Data input
DOUT	O	Serial-Data output
CLKIN	I	Serial-Clock input
CLKOUT	O	Serial-Clock output
LEB	I	Active-Low latch enable input, Hi=Hold data, Low=Latch data input
BANK0	I	Bank-Data input 0 for SW0 to SW15, Hi=ON, Low=OFF
BANK1	I	Bank-Data input 1 for SW16 to SW31, Hi=ON, Low=OFF
BANK2	I	Bank-Data input 2 for SW32 to SW47, Hi=ON, Low=OFF
BANK3	I	Bank-Data input 3 for SW48 to SW63, Hi=ON, Low=OFF
RESET	I	Shift register reset input
CLR	I	Latch clear input
CLKOUT_EN	I	Clock out enable input, Hi=Clock out, Low=Disable (Low)
R_ENB	I	Bleed resistor enable input, Hi=Disable, Low=Enable
BANK_EN	I	Bank interface enable input, Hi=Bank-Data interface, Low=Serial-Data interface
THP	O	Thermal protection output flag, open N-MOS drain (Low=THP activating)
SWx_A	I/O	Analog switch terminal n (AFE side), Suffix “x” corresponds to channel number (x=0 to 63)
SWx_P	I/O	Analog switch terminal n (Probe side), Suffix “x” corresponds to channel number (x=0 to 63)
NC	-	No connection (Not internally connected)

■ Pin Configuration (Table)

No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name
A1	DIN	B1	CLKIN	C1	VLL	D1	SW63_A	E1	NC	F1	SW61_A
A2	LEB	B2	RESET	C2	VDD	D2	NC	E2	SW62_A	F2	NC
A3	GND	B3	GND	C3	RGND	D3	SW63_P	E3	NC	F3	SW61_P
A4	SW0_A	B4	NC	C4	SW0_P	D4	NC	E4	SW62_P	F4	NC
A5	NC	B5	SW1_A	C5	NC	D5	SW1_P	E5	NC	F5	NC
A6	SW2_A	B6	NC	C6	SW2_P	D6	NC	E6	NC	F6	NC
A7	NC	B7	SW3_A	C7	NC	D7	SW3_P	E7	NC	-	-
A8	SW4_A	B8	NC	C8	SW4_P	D8	NC	E8	NC	-	-
A9	NC	B9	SW5_A	C9	NC	D9	SW5_P	E9	NC	-	-
A10	SW6_A	B10	NC	C10	SW6_P	D10	NC	E10	NC	-	-
A11	NC	B11	SW7_A	C11	NC	D11	SW7_P	E11	NC	-	-
A12	SW8_A	B12	NC	C12	SW8_P	D12	NC	E12	NC	-	-
A13	NC	B13	SW9_A	C13	NC	D13	SW9_P	E13	NC	-	-
A14	SW10_A	B14	NC	C14	SW10_P	D14	NC	E14	NC	-	-
A15	NC	B15	SW11_A	C15	NC	D15	SW11_P	E15	NC	-	-
A16	SW12_A	B16	NC	C16	SW12_P	D16	NC	E16	NC	-	-
A17	NC	B17	SW13_A	C17	NC	D17	SW13_P	E17	NC	-	-
A18	SW14_A	B18	NC	C18	SW14_P	D18	NC	E18	SW16_P	F18	NC
A19	NC	B19	SW15_A	C19	NC	D19	SW15_P	E19	NC	F19	SW18_P
A20	VLL	B20	NC	C20	RGND	D20	NC	E20	SW17_P	F20	NC
A21	GND	B21	THP	C21	GND	D21	SW16_A	E21	NC	F21	SW18_A
A22	DOUT	B22	CLKOUT	C22	VDD	D22	NC	E22	SW17_A	F22	NC

No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name
G1	NC	H1	SW59_A	J1	NC	K1	SW57_A	L1	NC	M1	SW55_A
G2	SW60_A	H2	NC	J2	SW58_A	K2	NC	L2	SW56_A	M2	NC
G3	NC	H3	SW59_P	J3	NC	K3	SW57_P	L3	NC	M3	SW55_P
G4	SW60_P	H4	NC	J4	SW58_P	K4	NC	L4	SW56_P	M4	NC
G5	NC	H5	NC	J5	NC	K5	NC	L5	NC	M5	NC
-	-	-	-	-	-	-	-	-	-	-	-
G7	GND	H7	GND	J7	GND	K7	GND	L7	GND	M7	GND
G8	GND	H8	GND	J8	GND	K8	GND	L8	GND	M8	GND
G9	GND	H9	GND	J9	GND	K9	GND	L9	GND	M9	GND
G10	GND	H10	GND	J10	GND	K10	GND	L10	GND	M10	GND
G11	GND	H11	GND	J11	GND	K11	GND	L11	GND	M11	GND
G12	GND	H12	GND	J12	GND	K12	GND	L12	GND	M12	GND
G13	GND	H13	GND	J13	GND	K13	GND	L13	GND	M13	GND
G14	GND	H14	GND	J14	GND	K14	GND	L14	GND	M14	GND
G15	GND	H15	GND	J15	GND	K15	GND	L15	GND	M15	GND
G16	GND	H16	GND	J16	GND	K16	GND	L16	GND	M16	GND
-	-	-	-	-	-	-	-	-	-	-	-
G18	NC	H18	NC	J18	NC	K18	NC	L18	NC	M18	NC
G19	NC	H19	SW20_P	J19	NC	K19	SW22_P	L19	NC	M19	SW24_P
G20	SW19_P	H20	NC	J20	SW21_P	K20	NC	L20	SW23_P	M20	NC
G21	NC	H21	SW20_A	J21	NC	K21	SW22_A	L21	NC	M21	SW24_A
G22	SW19_A	H22	NC	J22	SW21_A	K22	NC	L22	SW23_A	M22	NC

■ Pin Configuration (Table)

No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name
N1	NC	P1	SW53_A	Q1	NC	R1	SW51_A	S1	NC
N2	SW54_A	P2	NC	Q2	SW52_A	R2	NC	S2	SW50_A
N3	NC	P3	SW53_P	Q3	NC	R3	SW51_P	S3	NC
N4	SW54_P	P4	NC	Q4	SW52_P	R4	NC	S4	SW50_P
N5	NC	P5	NC	Q5	NC	R5	NC	S5	NC
-	-	-	-	-	-	-	-	-	-
N7	GND	P7	GND	Q7	GND	R7	GND	-	-
N8	GND	P8	GND	Q8	GND	R8	GND	-	-
N9	GND	P9	GND	Q9	GND	R9	GND	-	-
N10	GND	P10	GND	Q10	GND	R10	GND	-	-
N11	GND	P11	GND	Q11	GND	R11	GND	-	-
N12	GND	P12	GND	Q12	GND	R12	GND	-	-
N13	GND	P13	GND	Q13	GND	R13	GND	-	-
N14	GND	P14	GND	Q14	GND	R14	GND	-	-
N15	GND	P15	GND	Q15	GND	R15	GND	-	-
N16	GND	P16	GND	Q16	GND	R16	GND	-	-
-	-	-	-	-	-	-	-	-	-
N18	NC	P18	NC	Q18	NC	R18	NC	S18	NC
N19	NC	P19	SW26_P	Q19	NC	R19	SW28_P	S19	NC
N20	SW25_P	P20	NC	Q20	SW27_P	R20	NC	S20	SW29_P
N21	NC	P21	SW26_A	Q21	NC	R21	SW28_A	S21	NC
N22	SW25_A	P22	NC	Q22	SW27_A	R22	NC	S22	SW29_A

No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name
T1	SW49_A	U1	NC	V1	VDD	W1	BANK3	X1	BANK2
T2	NC	U2	SW48_A	V2	GND	W2	CLR	X2	CLKOUT_EN
T3	SW49_P	U3	NC	V3	R_ENB	W3	RGND	X3	GND
T4	NC	U4	SW47_P	V4	NC	W4	SW47_A	X4	NC
T5	SW48_P	U5	NC	V5	SW46_P	W5	NC	X5	SW46_A
T6	NC	U6	SW45_P	V6	NC	W6	SW45_A	X6	NC
T7	NC	U7	NC	V7	SW44_P	W7	NC	X7	SW44_A
T8	NC	U8	SW43_P	V8	NC	W8	SW43_A	X8	NC
T9	NC	U9	NC	V9	SW42_P	W9	NC	X9	SW42_A
T10	NC	U10	SW41_P	V10	NC	W10	SW41_A	X10	NC
T11	NC	U11	NC	V11	SW40_P	W11	NC	X11	SW40_A
T12	NC	U12	SW39_P	V12	NC	W12	SW39_A	X12	NC
T13	NC	U13	NC	V13	SW38_P	W13	NC	X13	SW38_A
T14	NC	U14	SW37_P	V14	NC	W14	SW37_A	X14	NC
T15	NC	U15	NC	V15	SW36_P	W15	NC	X15	SW36_A
T16	NC	U16	SW35_P	V16	NC	W16	SW35_A	X16	NC
T17	NC	U17	NC	V17	SW34_P	W17	NC	X17	SW34_A
T18	NC	U18	SW33_P	V18	NC	W18	SW33_A	X18	NC
T19	SW30_P	U19	NC	V19	SW32_P	W19	NC	X19	SW32_A
T20	NC	U20	SW31_P	V20	RGND	W20	BANK0	X20	NC
T21	SW30_A	U21	NC	V21	GND	W21	GND	X21	BANK1
T22	NC	U22	SW31_A	V22	GND	W22	VDD	X22	BANK_EN

■ Pin Configuration (MAP)

TOP VIEW

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	U	V	W	X
1	DIN	CLKIN	VLL	SW63_A	NC	SW61_A	NC	SW59_A	NC	SW57_A	NC	SW55_A	NC	SW53_A	NC	SW51_A	NC	SW49_A	NC	VDD	BANK3	BANK2
2	LEB	RESET	VDD	NC	SW62_A	NC	SW60_A	NC	SW58_A	NC	SW56_A	NC	SW54_A	NC	SW52_A	NC	SW50_A	NC	SW48_A	GND	CLR	CLKOUT_EN
3	GND	GND	RGND	SW63_P	NC	SW61_P	NC	SW59_P	NC	SW57_P	NC	SW55_P	NC	SW53_P	NC	SW51_P	NC	SW49_P	NC	R_ENB	RGND	GND
4	SW0_A	NC	SW0_P	NC	SW62_P	NC	SW60_P	NC	SW58_P	NC	SW56_P	NC	SW54_P	NC	SW52_P	NC	SW50_P	NC	SW47_P	NC	SW47_A	NC
5	NC	SW1_A	NC	SW1_P	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	SW48_P	NC	SW46_P	NC	SW46_A
6	SW2_A	NC	SW2_P	NC	NC	NC	-	-	-	-	-	-	-	-	-	-	-	NC	SW45_P	NC	SW45_A	NC
7	NC	SW3_A	NC	SW3_P	NC	-	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	-	NC	NC	SW44_P	NC	SW44_A
8	SW4_A	NC	SW4_P	NC	NC	-	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	-	NC	SW43_P	NC	SW43_A	NC
9	NC	SW5_A	NC	SW5_P	NC	-	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	-	NC	NC	SW42_P	NC	SW42_A
10	SW6_A	NC	SW6_P	NC	NC	-	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	-	NC	SW41_P	NC	SW41_A	NC
11	NC	SW7_A	NC	SW7_P	NC	-	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	-	NC	NC	SW40_P	NC	SW40_A
12	SW8_A	NC	SW8_P	NC	NC	-	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	-	NC	SW39_P	NC	SW39_A	NC
13	NC	SW9_A	NC	SW9_P	NC	-	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	-	NC	NC	SW38_P	NC	SW38_A
14	SW10_A	NC	SW10_P	NC	NC	-	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	-	NC	SW37_P	NC	SW37_A	NC
15	NC	SW11_A	NC	SW11_P	NC	-	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	-	NC	NC	SW36_P	NC	SW36_A
16	SW12_A	NC	SW12_P	NC	NC	-	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	-	NC	SW35_P	NC	SW35_A	NC
17	NC	SW13_A	NC	SW13_P	NC	-	-	-	-	-	-	-	-	-	-	-	-	NC	NC	SW34_P	NC	SW34_A
18	SW14_A	NC	SW14_P	NC	SW16_P	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	SW33_P	NC	SW33_A	NC
19	NC	SW15_A	NC	SW15_P	NC	SW18_P	NC	SW20_P	NC	SW22_P	NC	SW24_P	NC	SW26_P	NC	SW28_P	NC	SW30_P	NC	SW32_P	NC	SW32_A
20	VLL	NC	RGND	NC	SW17_P	NC	SW19_P	NC	SW21_P	NC	SW23_P	NC	SW25_P	NC	SW27_P	NC	SW29_P	NC	SW31_P	RGND	BANK0	NC
21	GND	THP	GND	SW16_A	NC	SW18_A	NC	SW20_A	NC	SW22_A	NC	SW24_A	NC	SW26_A	NC	SW28_A	NC	SW30_A	NC	GND	GND	BANK1
22	DOUT	CLKOUT	VDD	NC	SW17_A	NC	SW19_A	NC	SW21_A	NC	SW23_A	NC	SW25_A	NC	SW27_A	NC	SW29_A	NC	SW31_A	GND	VDD	BANK_EN

■ Package

Package Name	Dimension	Tray	Marking	Land	Packing
BGA-441(1515)A	RA441-A-P-S1	RA441-A-T-SD	RA441-A-M-SD	RA441-A-L-SD	RA441-A-K-SD

■ Storage, Mounting

1. Storage conditions

1. 1 The storage location should be kept at 5 to 35°C and 40 to 70% relative humidity. Keeping in a dry box is recommended. Moisture-proof property is assured for 12 months from delivery date for sealed moisture-proof packing, while it is guaranteed for 7 days from unpacked date under the condition above.

1. 2 When the storage conditions do not conform to those above or other conditions occur indicating moisture exposure, the ICs should be dried to avoid package cracks. A baking process at 125°C lasting for 24 hours results in sufficient dehumidification. The baking is not allowed more than twice, and the ICs should be mounted within 7 days after initial baking or within 10 days of total exposure after the second dehumidification.

2. Reflow soldering

The temperature rise may be different in the resin and a terminal part due to the reflow soldering.
It is necessary to check the package surface temperature (resin) before setting the temperature profile.
Figure 1 shows the resistance to soldering heat condition for package (Reflow method).
Confirm the heat resistance of the package shown below. (Based on JEDEC J-STD-020).

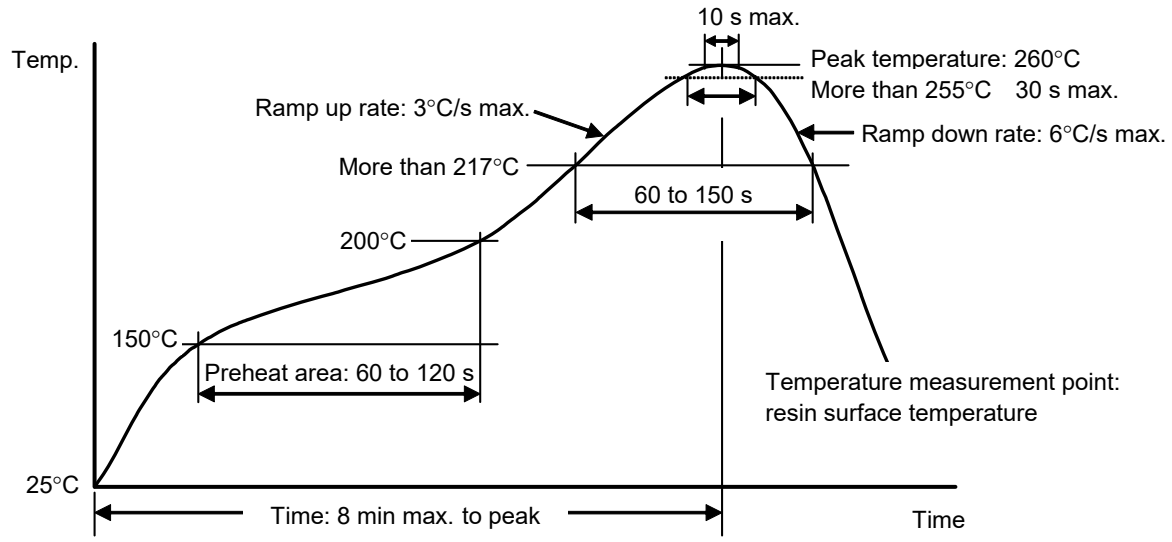


Figure 1 Resistance to Soldering Heat Condition for Package (Reflow Method)

■ Important Notice

1. ABLIC Inc. warrants performance of its hardware products (hereinafter called “products”) to the specifications applicable at the time of sale in accordance with the Product Specification. Testing and other quality control techniques are utilized to the extent ABLIC Inc. needs to meet specifications described in the Product Specification. Specific testing of all parameters of each device is not necessarily performed, except those mandated by related laws and/or regulations.

2. Should any claim be made within one month of product delivery about products’ failure to meet performance described in the Product Specification, all the products in relevant lot(s) shall be re-tested and re-delivered. Products delivered more than one month before such claim shall not be counted for such response.

3. ABLIC Inc. assumes no obligation or any way of compensation should any fault about customer products and applications using ABLIC Inc. products be found in marketplace. Only in such a case fault of ABLIC Inc. is evident and products concerned do not meet the Product Specification, compensation shall be conducted if claimed within one year of product delivery up to in the way of product replacement or payment of equivalent amount.

4. ABLIC Inc. reserves the right to make changes to the Product Specification at any time and to discontinue mass production of the relevant products without notice. Customers are advised before placing orders to confirm that the Product Specification of inquiry is the latest version and that the relevant product is currently on mass production status.

5. In no event shall ABLIC Inc. be liable for any damage that may result from an accident or any other cause during operation of the user’s units according to the Product Specification. ABLIC Inc. assumes no responsibility for any intellectual property claims or any other problems that may result from applications of information, products or circuits described in the Product Specification.

6. No license is granted by the Product Specification under any patents or other rights of any third party or ABLIC Inc.

7. The Product Specification may not be reproduced or duplicated, in any form, in whole or in part, without the expressed written permission of ABLIC Inc.

8. Resale of ABLIC Inc. products with statements different from or beyond the parameters described in the Product Specification voids all express and any implied warranties for the products, and is an unfair and deceptive business practice. ABLIC Inc. is not responsible or liable for any such statements.

9. Products (technologies) described in the Product Specification are not to be provided to any party whose purpose in their application will hinder maintenance of international peace and safety nor are they to be applied to that purpose by their direct purchasers or any third party. When exporting those products (technologies), the necessary procedures are to be taken in accordance with related laws and regulations.

■ Cautions

1. Customers are advised to follow the cautions below to protect products from damage caused by electrical static discharge (ESD).

1. 1 Material of container or any device to carry products should be free from ESD, which may be caused by vibration while transportation. It is recommended that electric-conductive container or aluminum sheet be used as an effective countermeasure.

1. 2 Those that touch products, such as work platform, machine, or measurement/test equipment, should be grounded.

1. 3 Those who deal with products should be grounded through a large series impedance around 100kΩ to 1MΩ.

1. 4 Prevent friction with other materials made with high polymer.

1. 5 Prevent vibration or friction when carrying the printed circuit board (PCB) where products are mounted. To short circuit terminals is a recommended countermeasure to keep the same electric potential on the PCB.

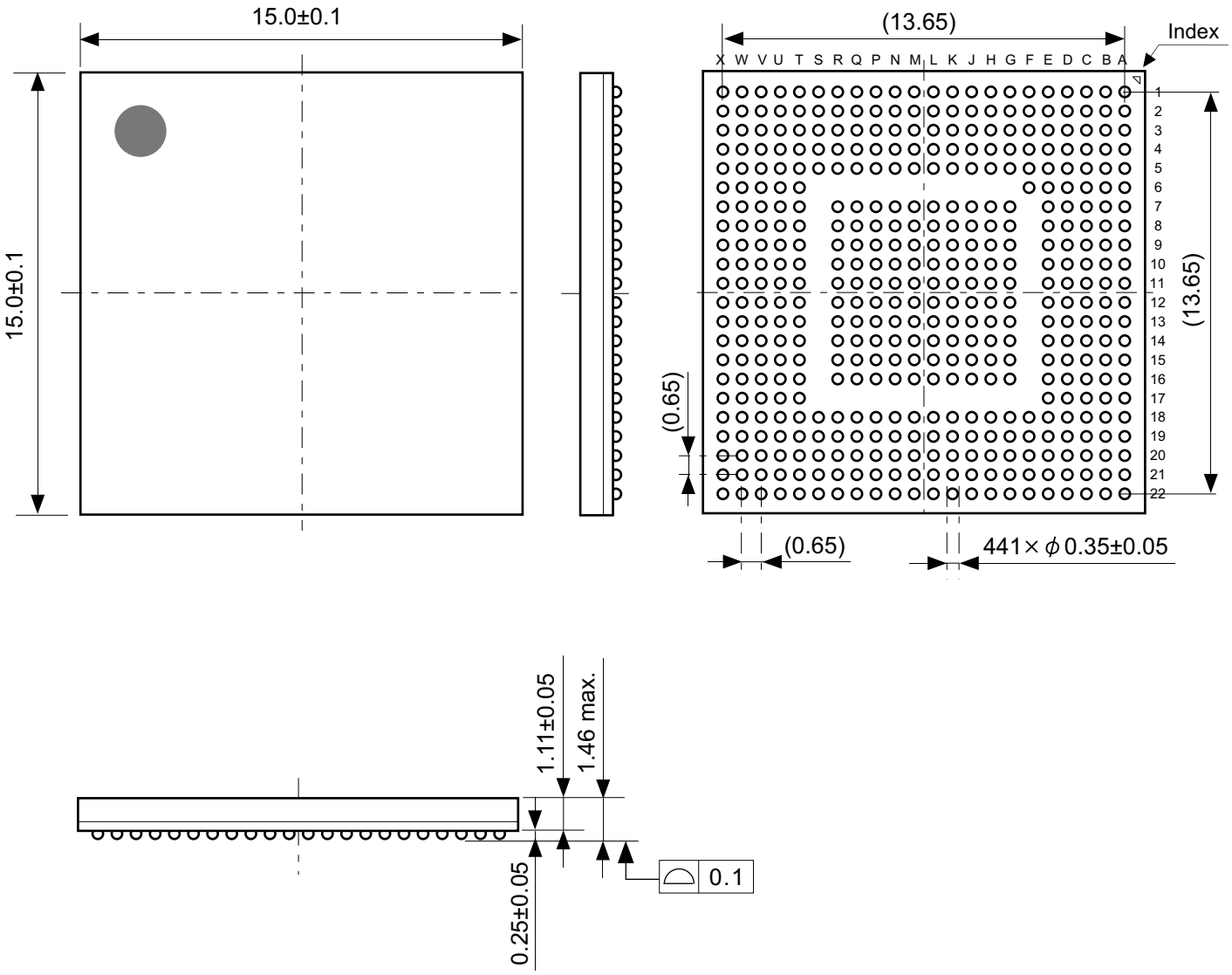
1. 6 Avoid dealing with or storing products in an extremely arid environment.

2. "Absolute maximum ratings" should never be exceeded during use regardless of any change in external conditions. Otherwise, products may be damaged or destroyed. In no event shall ABLIC Inc. be liable for any failure in products or any secondary damage resulting from use at a value exceeding the absolute maximum ratings.

3. Products may experience failures due to accident or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy or prevention of erroneous action, to avoid extensive damage in the event of a failure. (If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)

4. Products may experience failures or malfunction in poor surroundings, such as electrical leakage in products due to long-term use in high humidity, malfunctioning or permanent damage due to chemical reaction of products in corrosive environment or due to discharge by strongly charged object near products or due to excessive mechanical shock. To use products in radiation environment is not assumed. To use products near material easy to ignite may cause a fire due to its flammable package. Avoid using products in such environment or take appropriate countermeasures depending on the environment.

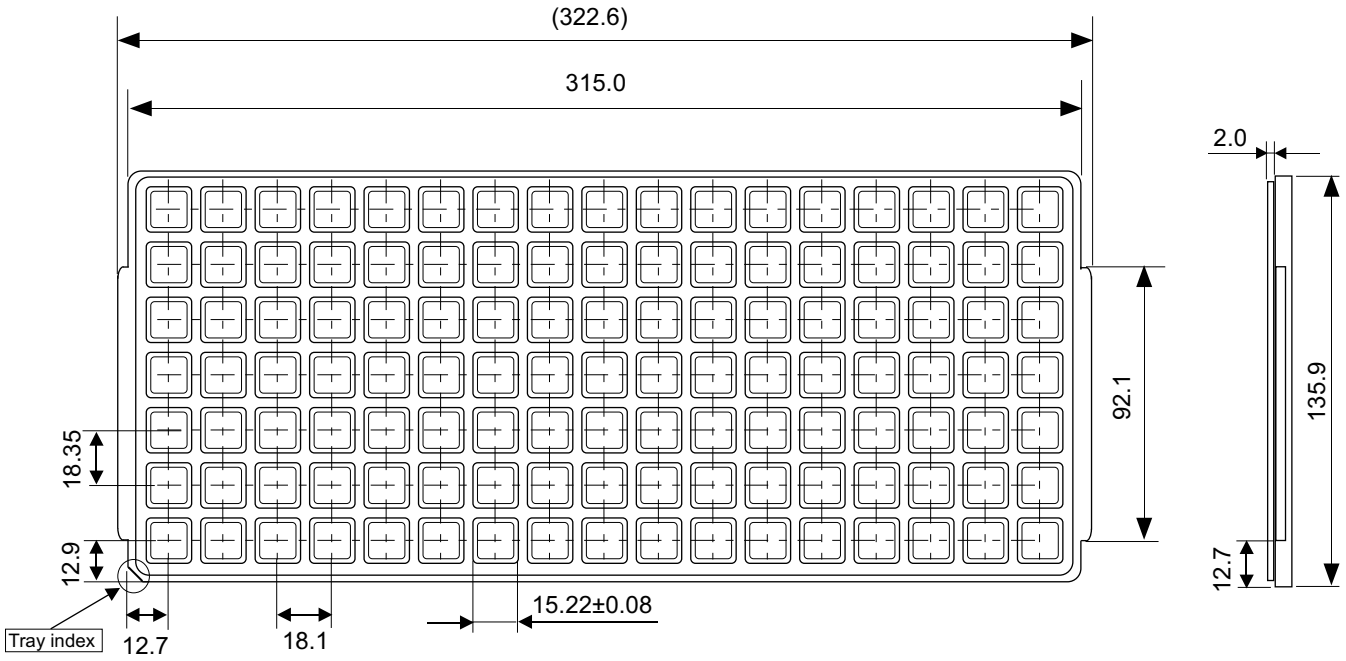
5. Products are not designed, manufactured, or warranted to be suitable for use where extremely high reliability is required (such as use in nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment). Inclusion of products in such application shall be fully at the risk of customers. ABLIC Inc. assumes no liability for applications assistance, customer product design, or performance.

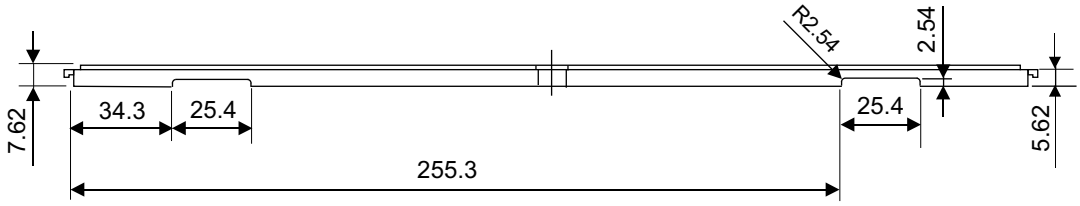


No. RA441-A-P-S1-1.0

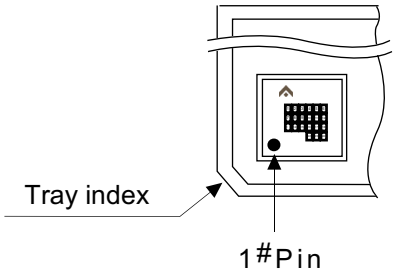
TITLE	BGA441-A-PKG Dimensions (S-UM6532)
No.	RA441-A-P-S1-1.0
ANGLE	
UNIT	mm

ABLIC Inc.



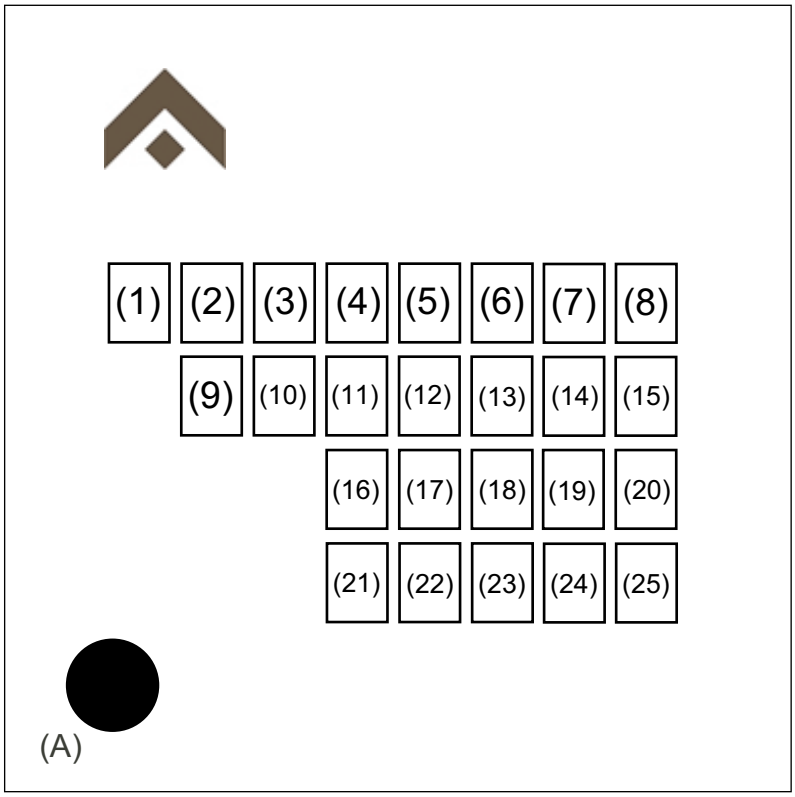


(Direction of IC in tray)



No. RA441-A-T-SD-1.0

TITLE	BGA441-A-Tray		
No.	RA441-A-T-SD-1.0		
ANGLE		QTY.	119
UNIT	mm		
ABLIC Inc.			



(1) to (10) : Product code

(11) , (12) : Quality control code

(13) : Year of assembly

(14) : Month of assembly

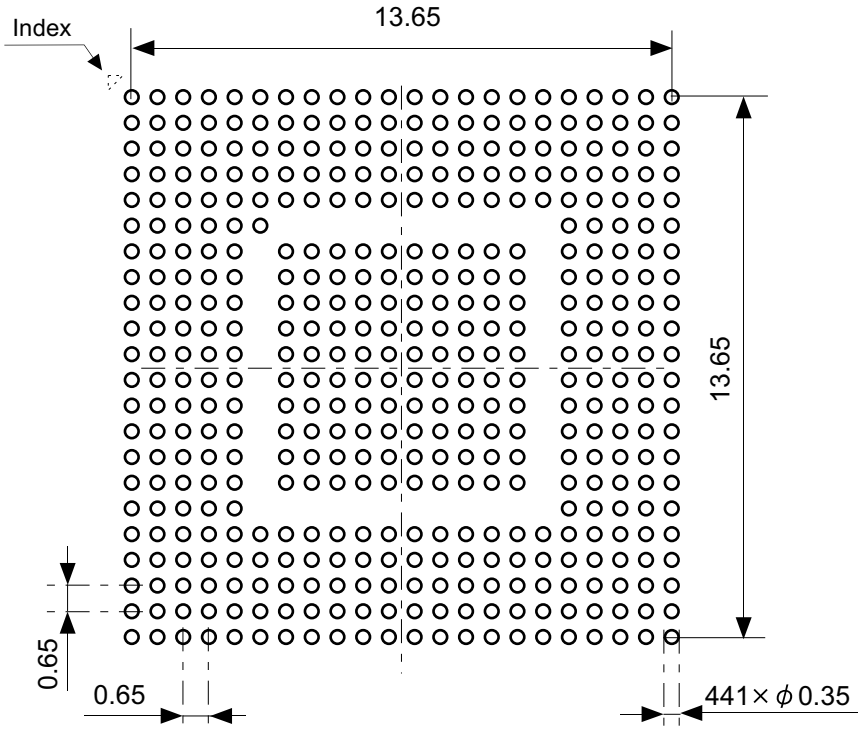
(15) : Week of assembly

(16) to (25) : Quality control code

(A) : 1-pin mark

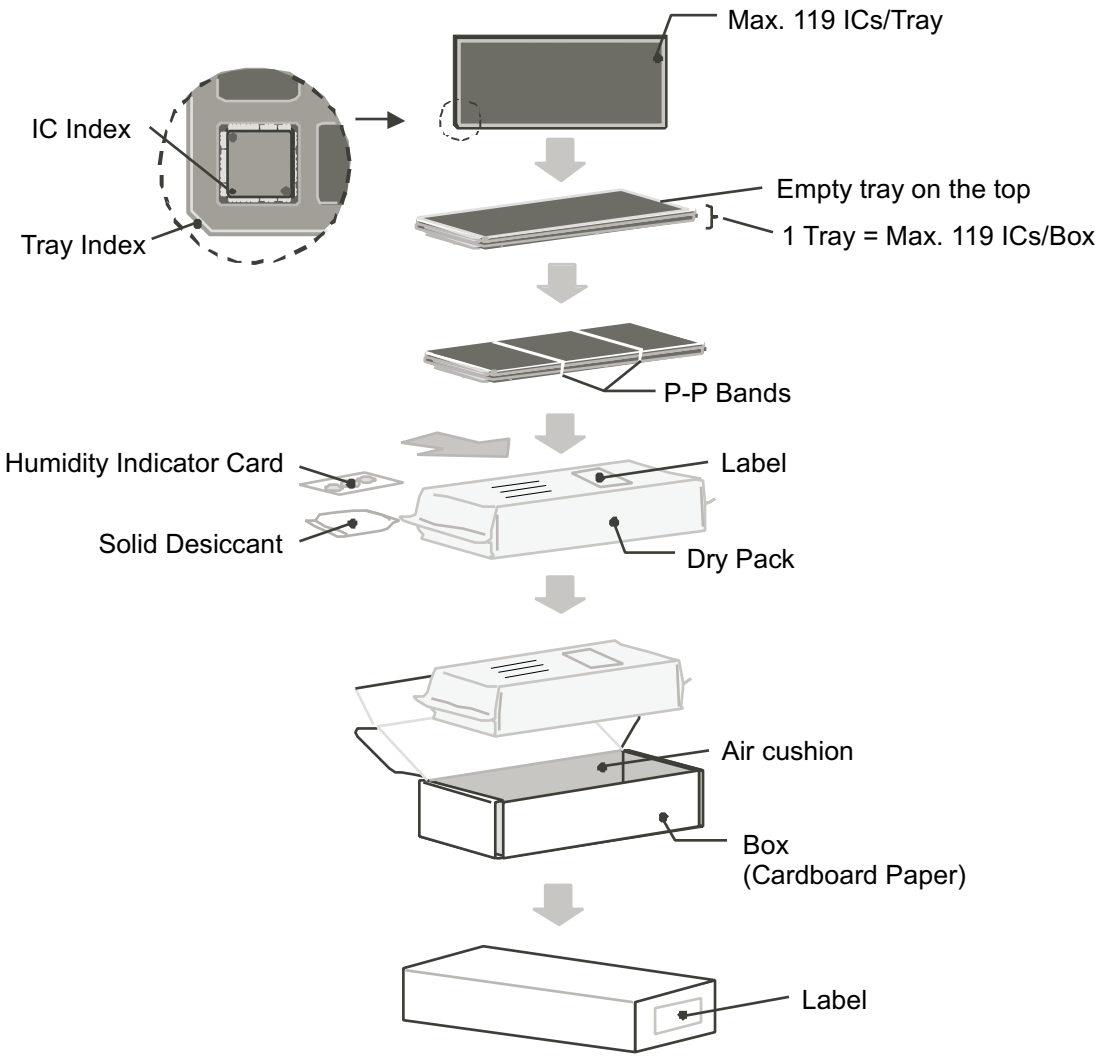
No. RA441-A-M-SD-1.0

TITLE	BGA441-A-Markings		
No.	RA441-A-M-SD-1.0		
ANGLE			
UNIT		TYPE	LASER
	ABLIC Inc.		



No. RA441-A-L-SD-1.0

TITLE	BGA441-A -Land Recommendation
No.	RA441-A-L-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	



No. RA441-A-K-SD-1.0

TITLE	BGA441-A -Packing Procedure
No.	RA441-A-K-SD-1.0
ANGLE	
UNIT	
ABLIC Inc.	

Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the reasons other than the products described herein (hereinafter "the products") or infringement of third-party intellectual property right and any other right due to the use of the information described herein.
3. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the incorrect information described herein.
4. Be careful to use the products within their ranges described herein. Pay special attention for use to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by failures and / or accidents, etc. due to the use of the products outside their specified ranges.
5. Before using the products, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products are strictly prohibited from using, providing or exporting for the purposes of the development of weapons of mass destruction or military use. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by any provision or export to the person or entity who intends to develop, manufacture, use or store nuclear, biological or chemical weapons or missiles, or use any other military purposes.
8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses by ABLIC, Inc. Do not apply the products to the above listed devices and equipments.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by unauthorized or unspecified use of the products.
9. In general, semiconductor products may fail or malfunction with some probability. The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.
   The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of ABLIC Inc. The information described herein does not convey any license under any intellectual property rights or any other rights belonging to ABLIC Inc. or a third party. Reproduction or copying of the information from this document or any part of this document described herein for the purpose of disclosing it to a third-party is strictly prohibited without the express permission of ABLIC Inc.
14. For more details on the information described herein or any other questions, please contact ABLIC Inc.'s sales representative.
15. This Disclaimers have been delivered in a text using the Japanese language, which text, despite any translations into the English language and the Chinese language, shall be controlling.

2.4-2019.07