

LOW CHARGE INJECTION 32-CHANNEL 8Ω HIGH-VOLTAGE ANALOG SWITCHES

The ABLIC S-UM6522E is a low charge injection 32-channel single-pole, single-throw (SPST) high-voltage analog switch IC operated only by a single 5V for ultrasound imaging applications.

Users can select either Serial Digital Interface (SDI) or Bank Interface.

The S-UM6522E has the same packaging and pinout as the HDL6M06522BN with improved Con/Coff and off isolation performance.

■ Functions

- 32-channel high-voltage SPST analog switches with user-selectable SDI or Bank interface

■ Features

- 0V to ±100V analog signal voltage range allowing ±150V voltage overshoot
- 10kHz to 85MHz analog signal frequency range
- 2A peak analog signal current per channel
- 8Ω switch on-resistance
- 40kΩ bleed resistor on probe side
- 32-bit shift registers
- Low on/off-capacitance
- 15pC charge injection to 1000pF
- -75dB off-isolation at analog small-signal 5MHz
- -60dB switch crosstalk
- Selectable Serial Digital Interface (32-bit shift registers) or Bank Interface (1 bank of 32-channel)
- 1.8V to 5V CMOS logic interface
- Single +5V power supply (NO HIGH-VOLTAGE POWER SUPPLY required)
- Low power dissipation (static 5mW)
- Embedded thermal protection flag indicator
- Unique pin configuration for easy PCB traces
- RoHS compliant 84-lead 10x10mm QFN

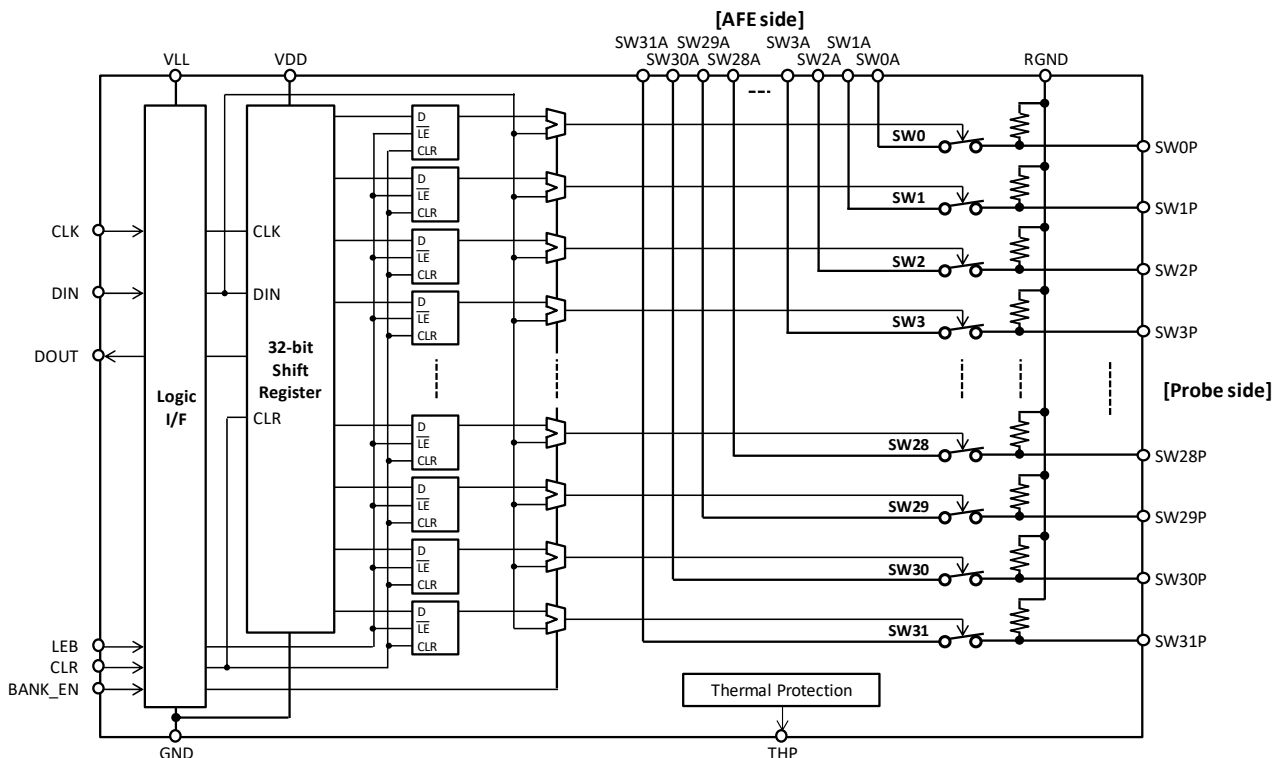


Figure 1 Block Diagram
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■ **Absolute Maximum Ratings**

T_A=25°C unless otherwise noted.

Table 1 Absolute Maximum Ratings

No.	Items	Symbol	Value	Units	Condition
1	Positive logic supply voltage	V _{LL}	-0.4 to +7	V	
2	Positive supply voltage	V _{DD}	-0.4 to +7	V	
3	Logic input voltage	DIN, LEB, CLK, CLR_BSEL, BANK_EN	-0.4 to +7	V	
4	Logic output voltage	DOUT, THP	-0.4 to +7	V	
5	Analog signal range (steady state voltage)	V _{SIG}	-105 to +105	V	
6	Analog signal range (peak overshoot voltage)	V _{SIG_OS}	-150 to +150	V	Max. 500ns pulse width
7	Peak analog signal current per channel	I _{SW}	2.5	A	
8	Operating junction temperature	T _{Jop}	-20 to +150	°C	
9	Storage temperature	T _{STG}	-55 to +150	°C	
10	Maximum power dissipation	P _{Dmax}	4	W	

Remark Stresses beyond the absolute maximum ratings may cause permanent damage to the product.

■ Operating Supply Voltages, Logic Levels, and Application Circuits

1. Operating supply voltages, temperature, and logic levels

Table 2 Operating Supply Voltages and Logic Levels

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	Logic supply voltage	V _{LL}	1.7	1.8 to 5	V _{DD}	V	
2	Positive supply voltage	V _{DD}	4.75	5	5.25	V	
3	IC substrate voltage *1	V _{SUB}	-	0	-	V	
4	Operating free-air temperature	T _A	0	-	75	°C	
5	High-level logic input voltage	V _{IH}	0.8V _{LL}	-	V _{LL}	V	
6	Low-level logic input voltage	V _{IL}	0	-	0.2V _{LL}	V	
7	High-level logic output voltage	V _{oH}	0.8V _{LL}	-	-	V	I _{SOURCE} = 1mA
8	Low-level logic output voltage	V _{oL}	-	-	0.2V _{LL}	V	I _{SINK} = 1mA
9	Logic input high current *2	I _{IH}	-10	-	10	μA	DIN, LEB, CLK, CLR_BSEL, BANK_EN
10	Logic input low current	I _{IL}	-10	-	10	μA	
11	Logic input capacitance	C _{IN}	-	2	-	pF	
12	Set up time before LEB rises	t _{SD}	25	-	-	ns	
13	Time width of LEB	t _{wLEB}	12	-	-	ns	
14	Clock delay time to data out	t _{DO}	7	10	24	ns	
15	Time width of CLR_BSEL	t _{OLR}	55	-	-	ns	
16	Clock frequency	f _{CLK}	-	-	50	MHz	V _{LL} =1.8V
			-	-	80	MHz	V _{LL} =2.5V
			-	-	95	MHz	V _{LL} =3.3V
17	Clock rise and fall times	t _R , t _F	-	-	50	ns	
18	Setup time data to clock	t _{SU}	4	-	-	ns	
19	Hold time data from clock	t _{HLD}	4	-	-	ns	
20	Bank interface setup time	t _{SD_BNK}	100	-	-	ns	
21	BANKx minimum pulse width	t _{wBANK}	4	-	-	μs	

*1. Thermal pad on the bottom of the package must be soldered to the ground.

*2. BANK_EN has 100μA leakage at V_{LL}=5V due to 50kΩ internal pull-down resistor.

2. Power supply sequencing

No power supply sequencing is required even if V_{LL} is different from V_{DD}.

Please apply the V_{DD} voltage to the V_{LL} when operating with a single 5V.

■ **Electrical Characteristics**

1. DC characteristics

Table 3 DC Characteristics

$V_{LL}=3.3V$, $V_{DD}=5V$, $LEB=0$, $BANK_EN=0/1$, $T_A=25^{\circ}C$, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Analog signal range (steady state voltage)	V_{SIG}	-100	-	+100	V	
2	Analog signal range (peak overshoot voltage)	V_{SIG_OS}	-150	-	+150	V	Max. 500ns pulse width
3	V_{LL} quiescent current	I_{LLQ}	-	0.2	-	μA	Quiescent current-1 All switches off
4	V_{DD} quiescent current	I_{DDQ}	-	1.5	-	mA	
5	V_{LL} quiescent current	I_{LLQ}	-	0.2	-	μA	Quiescent current-2 All switches on
6	V_{DD} quiescent current	I_{DDQ}	-	1.5	-	mA	
7	V_{LL} dynamic current	I_{LL}	-	2	10	μA	Dynamic current All channels switching simultaneously at $f_{sw}=50kHz$
8	V_{DD} dynamic current	I_{DD}	-	3.4	4.6	mA	
9	DC offset switch off	V_{OS}	-	0	-	mV	
10	Small signal switch on-resistance	R_{ONS}	-	8	10	Ω	$V_{SIG}=0.1V_{pp}$ to $5V_{pp}$ @5MHz, $R_S=10\Omega$
11	Small signal switch on-resistance matching	ΔR_{ONS}	-	2	5	%	$V_{SIG}=0V$, $I_{SIG}=5mA$
12	Large signal switch on-resistance	R_{ONL}	-	8	-	Ω	$V_{SIG}=20V_{pp}$ @5MHz, $R_S=10\Omega$
13	Shunt resistance	R_{BLD}	30	40	50	k Ω	On probe side
14	Switch output peak current	I_{SW}	-	2	-	A	100ns pulse, 0.1% duty cycle

2. Thermal protection

Table 4 Thermal Protection Characteristics

$V_{LL}=3.3V$, $V_{DD}=5V$, $LEB=0$, $BANK_EN=0/1$, $T_A=25^{\circ}C$, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	THP pull-up voltage	V_{PUTHP}	-	-	5.25	V	Open drain
2	THP output current	I_{THP}	-	1.0	-	mA	
3	THP output low voltage	V_{OLTHP}	-	-	0.5	V	THP active, $V_{LL}=3.3V$, $I_{THP}=1mA$
4	THP temperature threshold	T_{THP}	90	110	130	$^{\circ}C$	Thermal protection flag indicator by THP pin (open N-MOS drain, Low=THP activating)
5	THP reset hysteresis	T_{HYSTHP}	-	10	-	$^{\circ}C$	

3. AC Characteristics

Table 5 AC Characteristics

$V_{LL}=3.3V$, $V_{DD}=5V$, $LEB=0$, $BANK_EN=0/1$, $T_A=25^{\circ}C$, unless otherwise specified.

No.	Items		Symbol	Spec			Units	Conditions
				Min	Typ	Max		
1	Turn-on time		t_{ON}	-	2	4	μs	
			t_{ON_BNK}	-	2	4	μs	
2	Turn-off time		t_{OFF}	-	2	4	μs	
			t_{OFF_BNK}	-	2	4	μs	
3	Output switching frequency		f_{SW}	-	-	50	kHz	Duty cycle=50%
4	Small signal frequency		f_{SIG}	0.01	-	85	MHz	$C_L=220pF$
5	Off isolation	small signal	$V_{ISO(RX)}$	-	-75	-	dB	$f_{SIG}=5MHz$, $R_L=50\Omega$
		large signal	$V_{ISO(TX)}$	-	-67	-	dB	$f_{SIG}=5MHz$, $R_L=50\Omega$
6	Crosstalk		V_{CT}	-	-60	-	dB	$f_{SIG}=5MHz$, $R_L=50\Omega$
7	On capacitance	small signal	$C_{ON(RX)}$	-	25	-	pF	$V_{SIG}=0V$, $f_{SIG}=1MHz$
		large signal	$C_{ON(TX)}$	-	15	-	pF	$V_{SIG}=10V_{pp}$, $f_{SIG}=1MHz$
8	Off capacitance SW_P to GND	small signal	$C_{OFF(SWP_RX)}$	-	20	-	pF	$V_{SIG}=0V$, $f_{SIG}=1MHz$
9	Off capacitance SW_A to GND	small signal	$C_{OFF(SWA_RX)}$	-	18	-	pF	$V_{SIG}=0V$, $f_{SIG}=1MHz$
		large signal	$C_{OFF(SWA_TX)}$	-	10	-	pF	$V_{SIG}=10V_{pp}$, $f_{SIG}=1MHz$
10	Output spike voltage (SW_P)		$V_{SPK_ON(SWP)}$	-	50	-	mV	50Ω load @switch on
			$V_{SPK_OFF(SWP)}$	-	50	-	mV	50Ω load @switch off
11	Output spike voltage (SW_A)		$V_{SPK_ON(SWA)}$	-	50	-	mV	50Ω load @switch on
			$V_{SPK_OFF(SWA)}$	-	50	-	mV	50Ω load @switch off
12	Charge injection		QC	-	10	-	pC	

■ Test Circuits

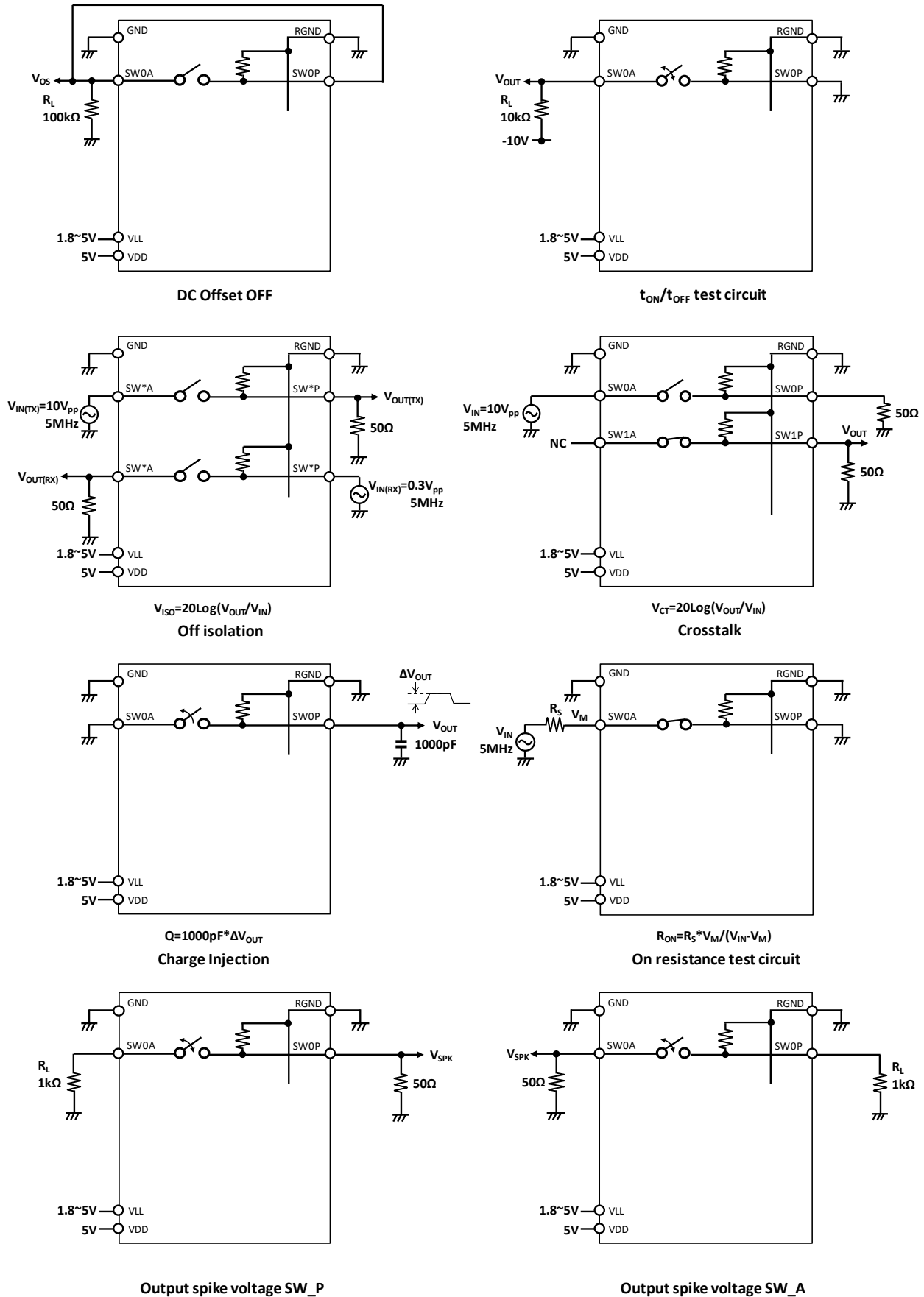


Figure 2 Test Circuits
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■ Truth Table

Table 6 Truth Table

Logic Inputs								Analog Switch State				
LEB	CLR	BANK_EN	DIN					SW0	SW1	...	SW30	SW31
			D0	D1	...	D30	D31					
L	L	L	L	-		-	-	OFF	-		-	-
L	L	L	H	-		-	-	ON	-		-	-
L	L	L	-	L		-	-	-	OFF		-	-
L	L	L	-	H		-	-	-	ON		-	-
L	L	L	-	-		-	-	-	-		-	-
L	L	L	-	-		-	-	-	-		-	-
L	L	L	-	-		-	-	-	-		-	-
L	L	L	-	-	...	-	-	-	-	...	-	-
L	L	L	-	-		-	-	-	-		-	-
L	L	L	-	-		-	-	-	-		-	-
L	L	L	-	-		-	-	-	-		-	-
L	L	L	-	-		-	-	-	-		-	-
L	L	L	-	-		L	-	-	-		OFF	-
L	L	L	-	-		H	-	-	-		ON	-
L	L	L	-	-		-	L	-	-		-	OFF
L	L	L	-	-		-	H	-	-		-	ON
H	L	L	X	X	X	X	X	Hold Previous State				
X	H	L	X	X	X	X	X	ALL SWs OFF				
X	X	H	L					ALL SWs OFF				
X	X	H	H					ALL SWs ON				

■ Logic Timing

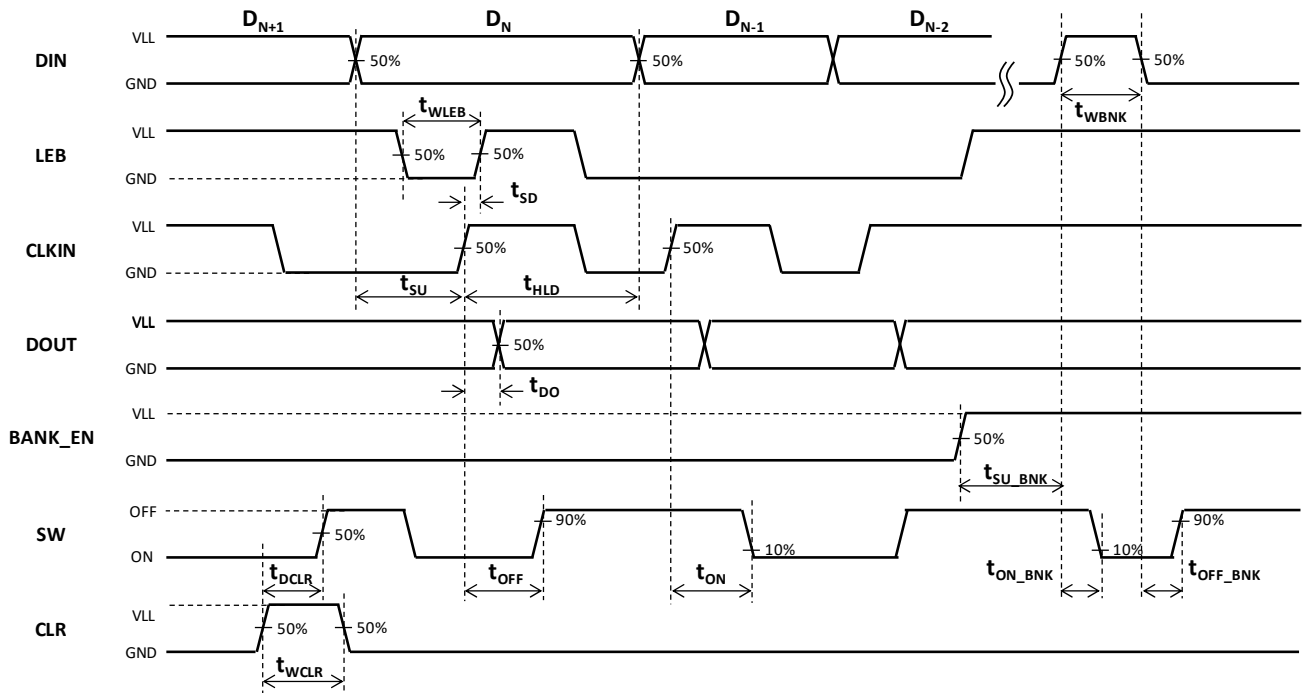


Figure 3 Logic Timing

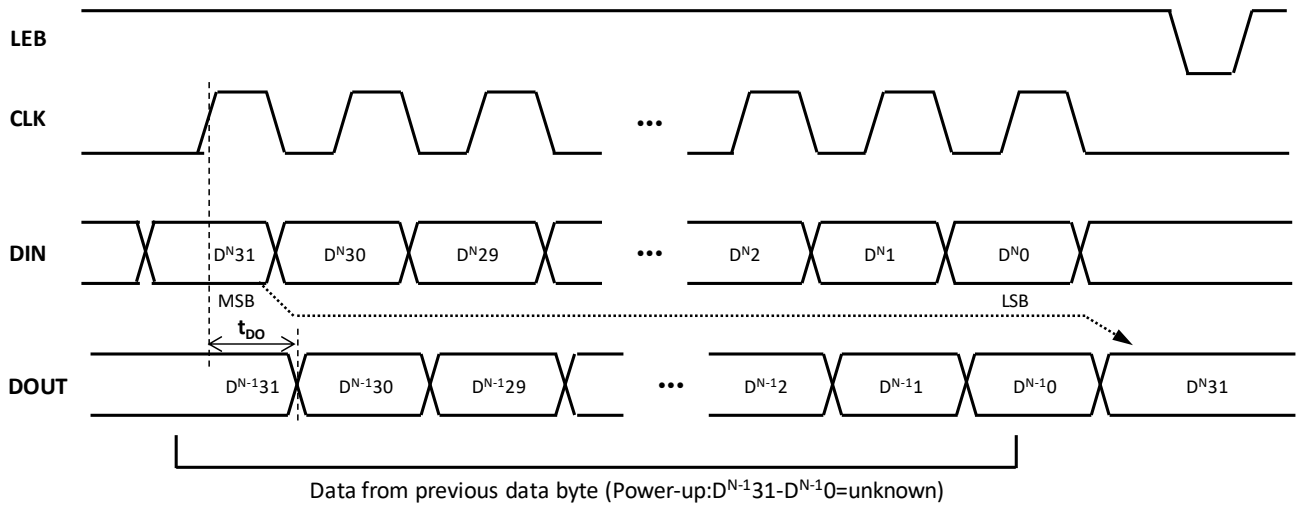


Figure 4 Latch Enable Interface Timing

■ Pin Configuration

		THP	VLL	SW15A	SW14A	SW13A	SW12A	SW11A	SW10A	SW9A	SW8A	NC	SW23A	SW22A	SW21A	SW20A	SW19A	SW18A	SW17A	SW16A	GND	BANK_EN	
		63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	
GND	64																					42	CLR
RGND	65																					41	VDD
SW15P	66																					40	SW16P
SW14P	67																					39	SW17P
SW13P	68																					38	SW18P
SW12P	69																					37	SW19P
SW11P	70																					36	SW20P
SW10P	71																					35	SW21P
SW9P	72																					34	SW22P
SW8P	73																					33	SW23P
NC	74																					32	NC
SW7P	75																					31	SW24P
SW6P	76																					30	SW25P
SW5P	77																					29	SW26P
SW4P	78																					28	SW27P
SW3P	79																					27	SW28P
SW2P	80																					26	SW29P
SW1P	81																					25	SW30P
SW0P	82																					24	SW31P
VDD	83																					23	RGND
LEB	84																					22	CLK
	○	DIN	GND	SW0A	SW1A	SW2A	SW3A	SW4A	SW5A	SW6A	SW7A	NC	SW24A	SW25A	SW26A	SW27A	SW28A	SW29A	SW30A	SW31A	VLL	DOUT	
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	

Figure 5 Pin Configuration

Table 7 Pin Configuration (1 / 2)

Pin#	Pin Name	I/O	Function
1	DIN	I	Serial-Data (BANK_EN=0) / Bank-Data (BANK_EN=1) input
2	GND	-	Drive power ground (0V)
3	SW0A	I/O	Analog switch terminal 0 (AFE side)
4	SW1A	I/O	Analog switch terminal 1 (AFE side)
5	SW2A	I/O	Analog switch terminal 2 (AFE side)
6	SW3A	I/O	Analog switch terminal 3 (AFE side)
7	SW4A	I/O	Analog switch terminal 4 (AFE side)
8	SW5A	I/O	Analog switch terminal 5 (AFE side)
9	SW6A	I/O	Analog switch terminal 6 (AFE side)
10	SW7A	I/O	Analog switch terminal 7 (AFE side)
11	NC	-	No connection (Not internally connected)
12	SW24A	I/O	Analog switch terminal 24 (AFE side)
13	SW25A	I/O	Analog switch terminal 25 (AFE side)
14	SW26A	I/O	Analog switch terminal 26 (AFE side)
15	SW27A	I/O	Analog switch terminal 27 (AFE side)
16	SW28A	I/O	Analog switch terminal 28 (AFE side)
17	SW29A	I/O	Analog switch terminal 29 (AFE side)
18	SW30A	I/O	Analog switch terminal 30 (AFE side)
19	SW31A	I/O	Analog switch terminal 31 (AFE side)
20	VLL	-	Positive voltage supply of low voltage interface (+1.8V~+5V)
21	DOUT	O	Serial-Data output
22	CLK	I	Serial-Clock input
23	RGND	-	Bleed resistor ground (0V)
24	SW31P	I/O	Analog switch terminal 31 (Probe side)
25	SW30P	I/O	Analog switch terminal 30 (Probe side)
26	SW29P	I/O	Analog switch terminal 29 (Probe side)
27	SW28P	I/O	Analog switch terminal 28 (Probe side)
28	SW27P	I/O	Analog switch terminal 27 (Probe side)
29	SW26P	I/O	Analog switch terminal 26 (Probe side)
30	SW25P	I/O	Analog switch terminal 25 (Probe side)
31	SW24P	I/O	Analog switch terminal 24 (Probe side)
32	NC	-	No connection (Not internally connected)
33	SW23P	I/O	Analog switch terminal 23 (Probe side)
34	SW22P	I/O	Analog switch terminal 22 (Probe side)
35	SW21P	I/O	Analog switch terminal 21 (Probe side)
36	SW20P	I/O	Analog switch terminal 20 (Probe side)
37	SW19P	I/O	Analog switch terminal 19 (Probe side)
38	SW18P	I/O	Analog switch terminal 18 (Probe side)
39	SW17P	I/O	Analog switch terminal 17 (Probe side)
40	SW16P	I/O	Analog switch terminal 16 (Probe side)
41	VDD	-	Positive low voltage power supply (+5V)
42	CLR	I	Shift register and latch clear input

Table 7 Pin Configuration (2 / 2)

Pin#	Pin Name	I/O	Function
43	BANK_EN	I	Logic interface control, Hi=Bank interface, Low=Serial data interface
44	GND	-	Drive power ground (0V)
45	SW16A	I/O	Analog switch terminal 16 (AFE side)
46	SW17A	I/O	Analog switch terminal 17 (AFE side)
47	SW18A	I/O	Analog switch terminal 18 (AFE side)
48	SW19A	I/O	Analog switch terminal 19 (AFE side)
49	SW20A	I/O	Analog switch terminal 20 (AFE side)
50	SW21A	I/O	Analog switch terminal 21 (AFE side)
51	SW22A	I/O	Analog switch terminal 22 (AFE side)
52	SW23A	I/O	Analog switch terminal 23 (AFE side)
53	NC	-	No connection (Not internally connected)
54	SW8A	I/O	Analog switch terminal 8 (AFE side)
55	SW9A	I/O	Analog switch terminal 9 (AFE side)
56	SW10A	I/O	Analog switch terminal 10 (AFE side)
57	SW11A	I/O	Analog switch terminal 11 (AFE side)
58	SW12A	I/O	Analog switch terminal 12 (AFE side)
59	SW13A	I/O	Analog switch terminal 13 (AFE side)
60	SW14A	I/O	Analog switch terminal 14 (AFE side)
61	SW15A	I/O	Analog switch terminal 15 (AFE side)
62	VLL	-	Positive voltage supply of low voltage interface (+1.8V~+5V)
63	THP	O	Thermal protection output flag, open N-MOS drain
64	GND	-	Drive power ground (0V)
65	RGND	-	Bleed resistor ground (0V)
66	SW15P	I/O	Analog switch terminal 15 (Probe side)
67	SW14P	I/O	Analog switch terminal 14 (Probe side)
68	SW13P	I/O	Analog switch terminal 13 (Probe side)
69	SW12P	I/O	Analog switch terminal 12 (Probe side)
70	SW11P	I/O	Analog switch terminal 11 (Probe side)
71	SW10P	I/O	Analog switch terminal 10 (Probe side)
72	SW9P	I/O	Analog switch terminal 9 (Probe side)
73	SW8P	I/O	Analog switch terminal 8 (Probe side)
74	NC	-	No connection (Not internally connected)
75	SW7P	I/O	Analog switch terminal 7 (Probe side)
76	SW6P	I/O	Analog switch terminal 6 (Probe side)
77	SW5P	I/O	Analog switch terminal 5 (Probe side)
78	SW4P	I/O	Analog switch terminal 4 (Probe side)
79	SW3P	I/O	Analog switch terminal 3 (Probe side)
80	SW2P	I/O	Analog switch terminal 2 (Probe side)
81	SW1P	I/O	Analog switch terminal 1 (Probe side)
82	SW0P	I/O	Analog switch terminal 0 (Probe side)
83	VDD	-	Positive low voltage power supply (+5V)
84	LEB	I	Active-Low latch enable input, Hi=Hold data, Low=Latch data input

■ **Package**

Table 8 Package Drawing Codes

Package Name	Dimension	Tray	Marking	Land	Packing
QFN-84(1010)B	QN084-B-P-SD	QN084-B-T-SD	QN084-B-M-SD	QN084-B-L-SD	QN084-B-K-SD

■ **Storage, Mounting**

1. Storage conditions

- 1.1 The storage location should be kept at 5 to 35°C and 40 to 70% relative humidity. Keeping in a dry box is recommended. Moisture-proof property is assured for 12 months from delivery date for sealed moisture-proof packing, while it is guaranteed for 7 days from unpacked date under the condition above.
- 1.2 When the storage conditions do not conform to those above or other conditions occur indicating moisture exposure, the ICs should be dried to avoid package cracks. A baking process at 125°C lasting for 24 hours results in sufficient dehumidification. The baking is not allowed more than twice, and the ICs should be mounted within 7 days after initial baking or within 10 days of total exposure after the second dehumidification.

2. Reflow soldering

The temperature rise may be different in the resin and a terminal part due to the reflow soldering. It is necessary to check the package surface temperature (resin) before setting the temperature profile.

Figure 6 shows the resistance to soldering heat condition for package (Reflow method).

Confirm the heat resistance of the package shown below. (Based on JEDEC J-STD-020).

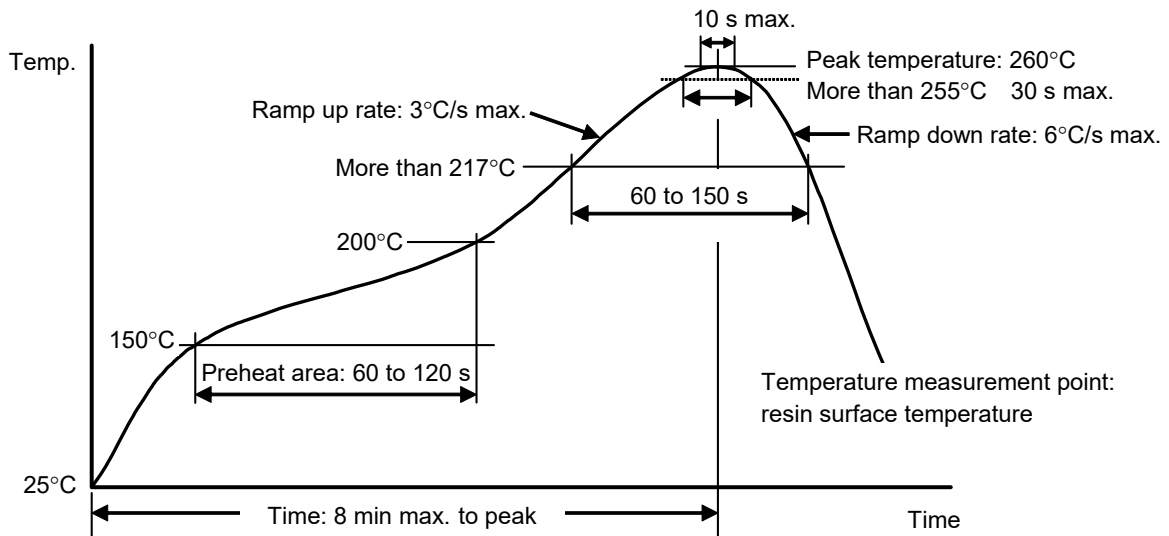


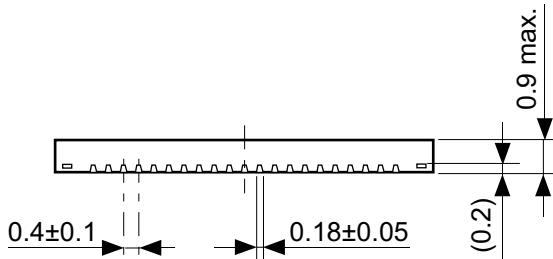
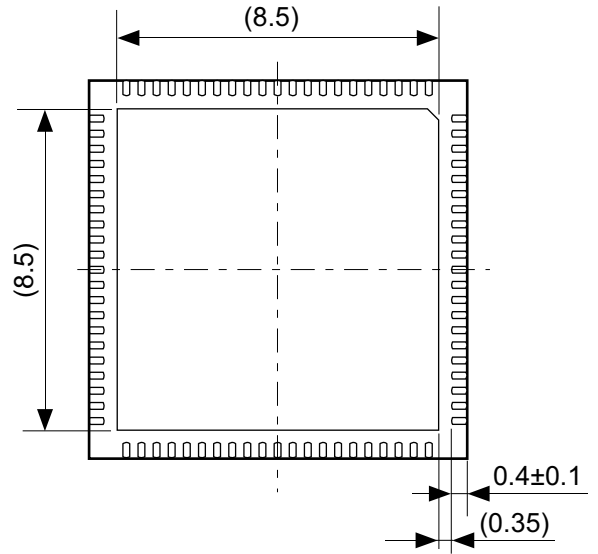
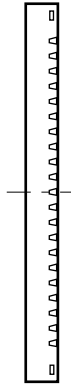
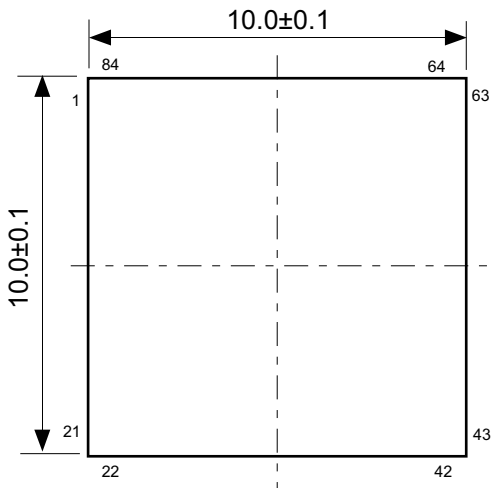
Figure 6 Resistance to Soldering Heat Condition for Package (Reflow Method)

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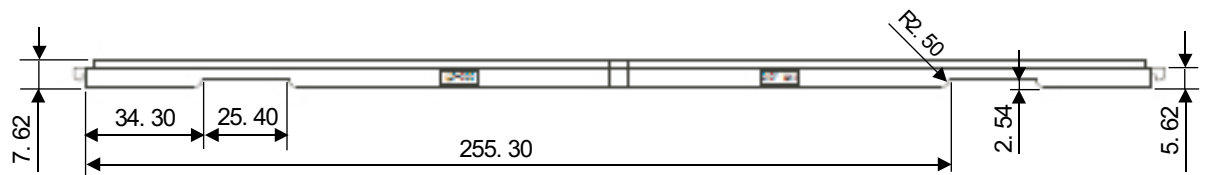
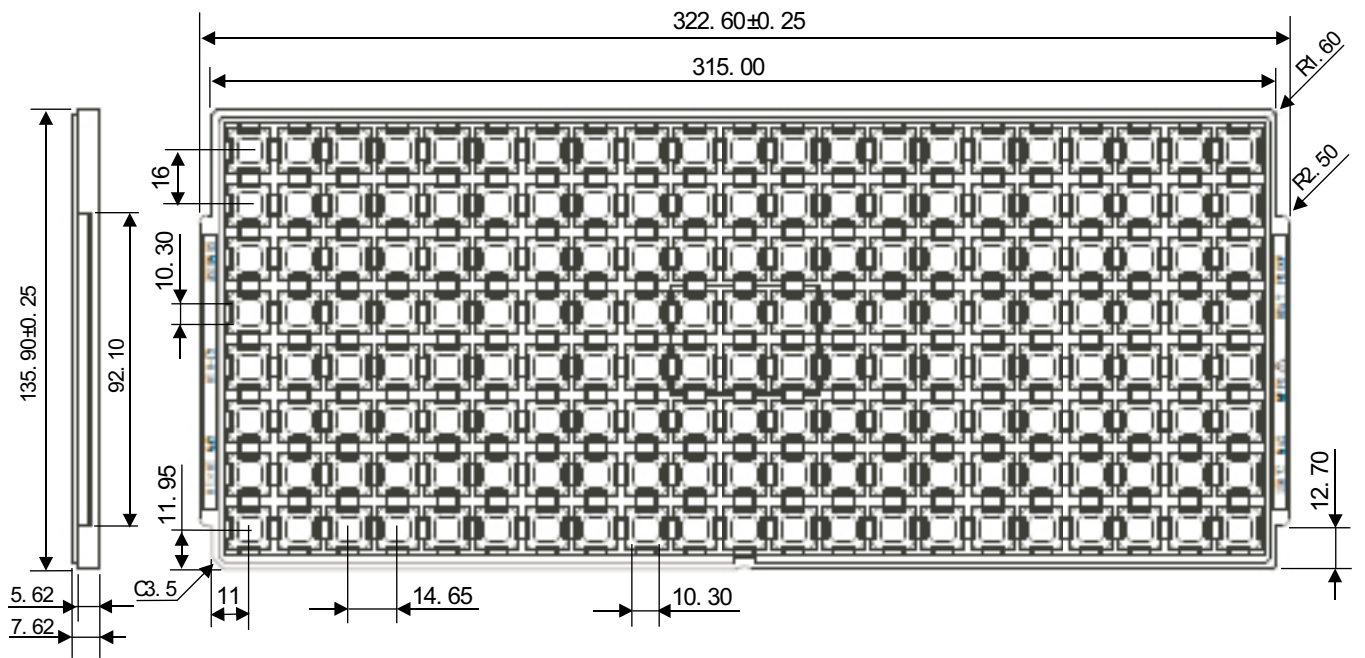
■ **Cautions**

1. Customers are advised to follow the cautions below to protect products from damage caused by electrical static discharge (ESD).
 - 1.1 Material of container or any device to carry products should be free from ESD, which may be caused by vibration while transportation. It is recommended that electric-conductive container or aluminum sheet be used as an effective countermeasure.
 - 1.2 Those that touch products, such as work platform, machine, or measurement/test equipment, should be grounded.
 - 1.3 Those who deal with products should be grounded through a large series impedance around 100kΩ to 1MΩ.
 - 1.4 Prevent friction with other materials made with high polymer.
 - 1.5 Prevent vibration or friction when carrying the printed circuit board (PCB) where products are mounted. To short circuit terminals is a recommended countermeasure to keep the same electric potential on the PCB.
 - 1.6 Avoid dealing with or storing products in an extremely arid environment.
2. "Absolute maximum ratings" should never be exceeded during use regardless of any change in external conditions. Otherwise, products may be damaged or destroyed. In no event shall ABLIC Inc. be liable for any failure in products or any secondary damage resulting from use at a value exceeding the absolute maximum ratings.
3. Products may experience failures due to accident or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy or prevention of erroneous action, to avoid extensive damage in the event of a failure. (If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)
4. Products may experience failures or malfunction in poor surroundings, such as electrical leakage in products due to long-term use in high humidity, malfunctioning or permanent damage due to chemical reaction of products in corrosive environment or due to discharge by strongly charged object near products or due to excessive mechanical shock. To use products in radiation environment is not assumed. To use products near material easy to ignite may cause a fire due to its flammable package. Avoid using products in such environment or take appropriate countermeasures depending on the environment.
5. Products are not designed, manufactured, or warranted to be suitable for use where extremely high reliability is required (such as use in nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment). Inclusion of products in such application shall be fully at the risk of customers. ABLIC Inc. assumes no liability for applications assistance, customer product design, or performance.

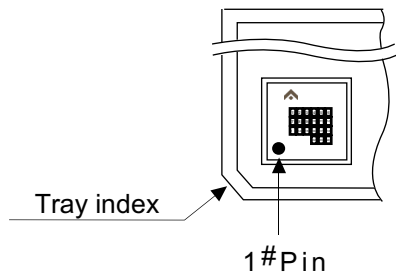


No. QN084-B-P-SD-1.0

TITLE	QFN84-B-PKG Dimensions
No.	QN084-B-P-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

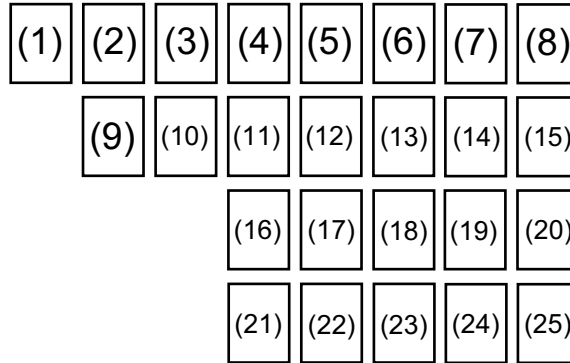


(Direction of IC in tray)



No. QFN84-B-T-SD-1.0

TITLE	QFN84-B-Tray		
No.	QN084-B-T-SD-1.0		
ANGLE		QTY.	168
UNIT	mm		
ABLIC Inc.			



(A)

(1) to (10) : Product code

(11) , (12) : Quality control code

(13) : Year of assembly

(14) : Month of assembly

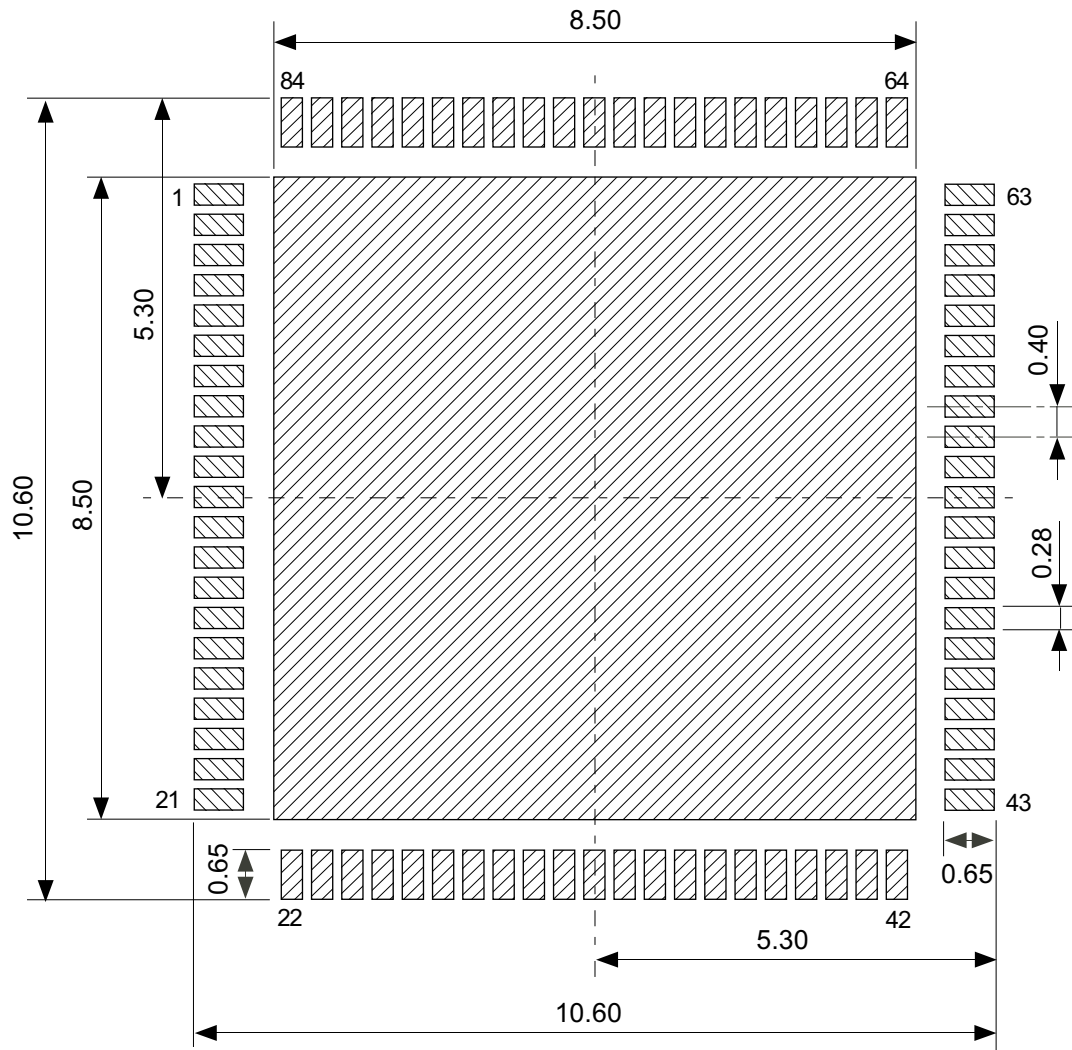
(15) : Week of assembly

(16) to (25) : Quality control code

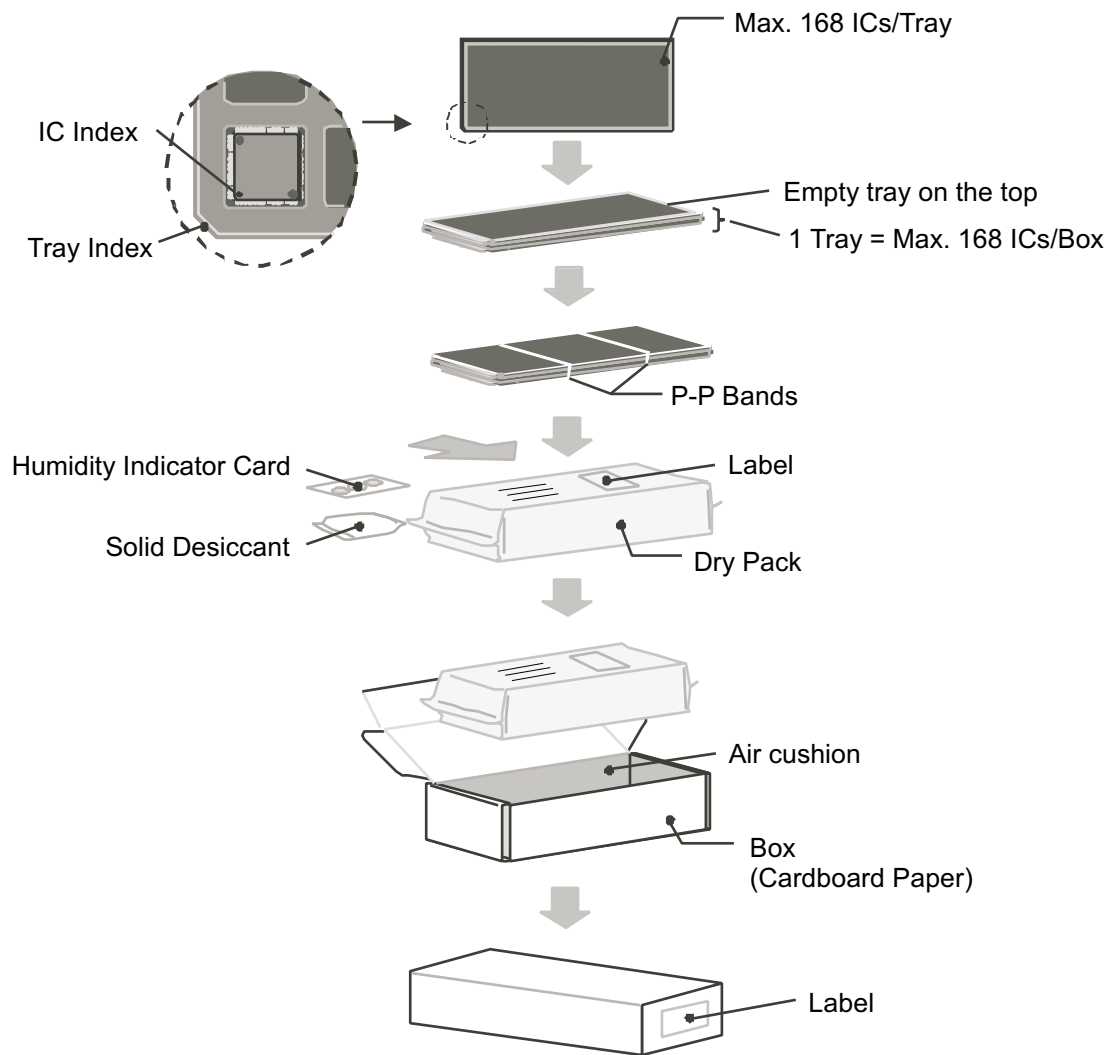
(A) : 1-pin mark

No. QFN84-B-M-SD-1.0

TITLE	QFN84-B-Markings		
No.	QN084-B-M-SD-1.0		
ANGLE			
UNIT		TYPE	LASER
ABLIC Inc.			



TITLE	QFN84-B -Land Recommendation
No.	QN084-B-L-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	



TITLE	QFN84-B -Packing Procedure
No.	QN084-B-K-SD-1.0
ANGLE	
UNIT	
ABLIC Inc.	

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1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
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The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
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2.4-2019.07

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