S-UM5587EF

16-CHANNEL PROGRAMMABLE 3-LEVEL HIGH-VOLTAGE ULTRASOUND TRANSMIT BEAMFORMER

Rev.1.0_00

S-UM5587EF is a 16-channel programmable 3-level high-voltage ultrasound transmit beam-former.
The S-UM5587EF comprises control logic, waveform memory, delay calculator, level translators, gate drive buffers with floating voltage regulators, high-voltage, high-current MOSFETs, and active T/R switches.

■ Functions

- 16-channel programmable 3-level transmit beam-former with active T/R-switch

■ Features

- 0 to ±100V output voltage
- ±1A source and sink current with 2-mode current control for the high-voltage pulses
- ±0.5A source and sink peak current for active ground clamp
- 250Ω active ground clamp without blocking diode for anti-leakage
- 20MHz output frequency at ±60V output, 80pF load
- Symmetrical positive and negative pulse waveforms for low 2nd order harmonic distortion
- 1.8V to 3.3V LVCMOS logic interface
- Waveform memory and registers with 100MHz Write /50MHz Read SPI
- 0.2µs to 41µs common delay time range from TRIG signal
- 0 to 2.55µs channel-to-channel delay time range
- 5ns channel-to-channel delay time resolution with dual-edge 100MHz LVDS/LVCMOS clock
- Minimum 10ns pulse width with 5ns time resolution with dual-edge 100MHz LVDS/LVCMOS clock
- 28Ω active T/R switch
- Noise-cut diodes at each high-voltage output
- High-voltage clamp diodes between each high-voltage output and power rails
- Automatic thermal protection with indicator
- Power-up/down reset function for free power sequencing and for fail-safe in abrupt power drop
- Latch-up free, low crosstalk between channels by SOI CMOS technology
- QFN-68(1010)B: 68-lead 10x10mm QFN package (RoHS compliant)

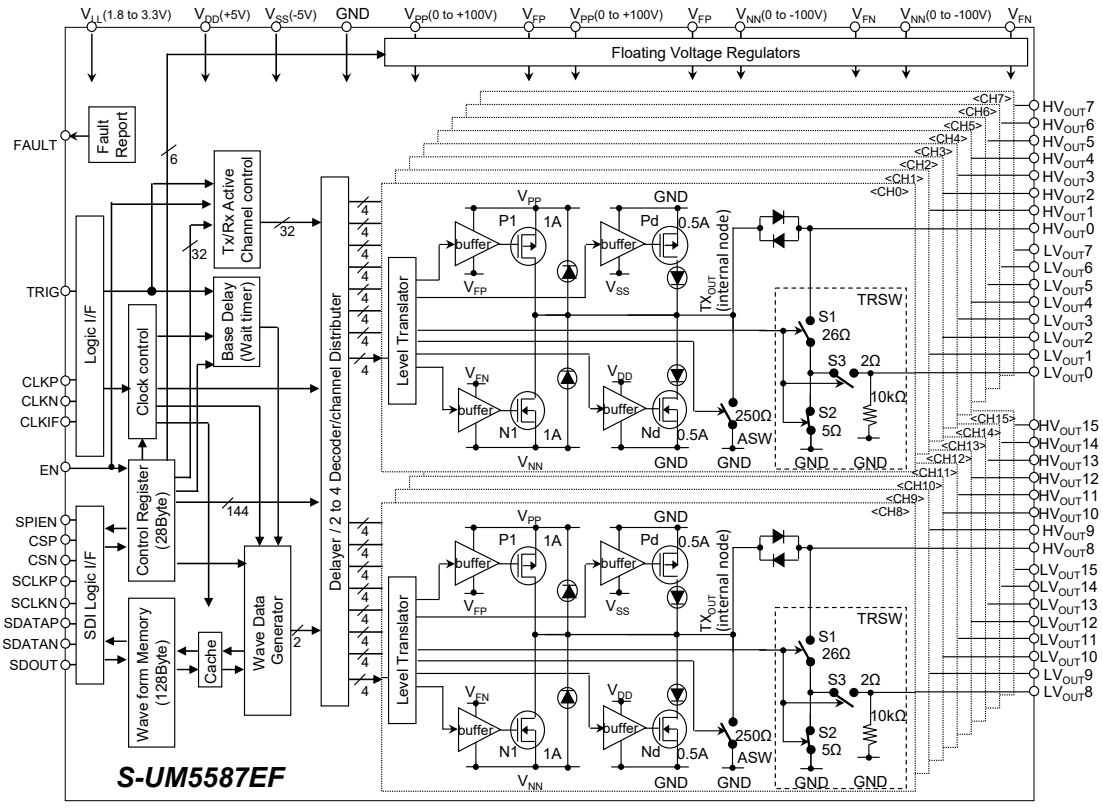

Figure 1 Block Diagram

■ Absolute Maximum Ratings

T_A = 25°C unless otherwise specified.

Table 1 Absolute Maximum Ratings

No.	Items	Symbol	Value	Units	Condition
1	Logic supply voltage	V_{LL}	-0.4 to +7	V	
2	Positive supply voltage	V_{DD}	-0.4 to +7	V	
3	Negative supply voltage	V_{SS}	-7 to +0.4	V	
4	Positive high-voltage supplies	V_{PP}	-0.5 to +105	V	
5	Negative high-voltage supplies	V_{NN}	-105 to +0.5	V	
6	High-voltage outputs (x = 0 to 15)	$HV_{OUT}x$	-105 to +105	V	
7	Low-voltage outputs (x = 0 to 15)	$LV_{OUT}x$	-1 to +1	V	
8	Logic output voltage	SDOUT, FAULT	-0.4 to +7	V	
9	Logic input voltages	EN, CLKIF, CLKP, CLKN, TRIG, SPIEN, CSP, CSN, SCLKP, SCLKN, SDATAP, SDATAN	-0.4 to +7	V	
10	Operating junction temperature	T_{Jop}	-20 to +125	°C	
11	Storage temperature	T_{STG}	-55 to +150	°C	
12	Maximum power dissipation	P_{Dmax}	4	W	

Remark Stresses beyond the absolute maximum ratings may cause permanent damage to the product.

■ Operating Supply Voltages and Logic Inputs

1. Operating supply voltage and temperature

Table 2 Operating Supply Voltage and Temperature

No.	Items	Symbol	Min.	Typ.	Max.	Units	Condition
1	Logic supply voltage	V_{LL}	1.71	1.8 to 3.3	3.6	V	
2	Positive supply voltage	V_{DD}	4.75	5	5.25	V	
3	Negative supply voltage	V_{SS}	-5.25	-5	-4.75	V	
4	Positive high-voltage supplies	V_{PP}	0	-	100	V	
5	Negative high-voltage supplies	V_{NN}	-100	-	0	V	
6	IC substrate voltage *1	V_{SUB}	-	0	-	V	
7	$V_{PP\_}$, $V_{NN\_}$ slew rate	SR_{MAX}	-	-	25	V/ms	
8	Operating free-air temperature	T_a	0	-	75	°C	

*1. The package exposed pad internally connected to the chip substrate must be soldered to the ground.

2. Logic inputs and outputs

2.1 LVDS differential logic inputs

Table 3 CLKP/CLKN, CSP/CSN, SCLKP/SCLKN, SDATAP/SDATAN

No.	Items	Symbol	Min.	Typ.	Max.	Units	Condition
1	High-level input voltage	V_{IH}	1.265	–	–	V	V_{IHCMR}(Typ) + V_{DIFF}(Min)/2
2	Low-level input voltage	V_{IL}	–	–	1.135	V	V_{IHCMR}(Typ) - V_{DIFF}(Min)/2
3	Differential input voltage range	$V_{DIFF(range)}$	0.13	0.35	0.49	±V	Same as voltage swing
4	Differential input voltage peak to peak swing	$V_{DIFF(p-p)}$	0.26	0.7	0.98	V_{pp}	Differential peak-to-peak absolute voltage swing
5	Input voltage common mode range	V_{IHCMR}	0.84	1.2	1.56	V	
6	High-level input current	I_{IH}	–	–	5.8	mA	
7	Low-level input current	I_{IL}	–	–	5.8	mA	
8	Input rise/fall time	t_r, t_f	–	–	600	ps	20% to 80% of V_{DIFF}
9	Input clock frequency (Tx)	f_{CLK}	–	–	100	MHz	CLKP/CLKN, SCLKP/SCLKN
	Input clock frequency (SPI)	f_{SCLK}	–	–	100	MHz	SCLKP/SCLKN (Write mode)
			–	–	50	MHz	SCLKP/SCLKN (Read mode)
10	Clock duty cycle	D_{CLK}	48	50	52	%	CLKP/CLKN
		D_{SCLK}	45	50	55	%	SCLKP/SCLKN
11	CS setup time	t_{SU_CS}	2.5	–	–	ns	CS to SCLK rise
12	CS hold time	t_{HLD_CS}	2.5	–	–	ns	CS to SCLK rise
13	CS width	t_{W_CS}	1043 T_{SCLK}	–	–	ns	Data write to memory
			1050 T_{SCLK}	–	–	ns	Data read from memory
			91 T_{SCLK}	–	–	ns	Data write to 9Byte register
			108 T_{SCLK}	–	–	ns	Data read from 9Byte register
			243 T_{SCLK}	–	–	ns	Data write to 28Byte register
			250 T_{SCLK}	–	–	ns	Data read from 28Byte register
			26 T_{SCLK}	–	–	ns	Data read of other register
14	SDATA setup time	t_{SU_SDATA}	2.5	–	–	ns	SDATA to SCLK rise
15	SDATA hold time	t_{HLD_SDATA}	2.5	–	–	ns	SDATA to SCLK rise

Remark: External termination Resister (100Ω) is necessary for LVDS I/F differential inputs.

2.2 CMOS logic inputs & outputs

Table 4 CLKP/CLKN, CSP/CSN, SCLKP/SCLKN, SDATAP/SDATAN [*3] EN, CLKIF, TRIG, SPIEN, SDOUT

No.	Items	Symbol	Min.	Typ.	Max.	Units	Condition
1	High-level logic input voltage	V_{IH}	$0.8V_{LL}$	–	V_{LL}	V	
2	Low-level logic input voltage	V_{IL}	0	–	$0.2V_{LL}$	V	
3	Logic input capacitance	C_{IN}	–	3	–	pF	
4	Logic input high current [*1]	I_{IH}	-10	–	10	µA	
5	Logic input low current [*2]	I_{IL}	-10	–	10	µA	
6	Input rise/fall time	t_r , t_f	–	–	2.0	ns	10% to 90% of signal
7	TRIG fall to clock rise setup time	$t_{SU\_TRFtoCKR}$	1.5	–	–	ns	LVDS clock
			1.5	–	–		CMOS clock
8	TRIG fall to clock rise hold time	$t_{HLD\_TRFtoCKR}$	1.5	–	–	ns	LVDS clock
			1.5	–	–		CMOS clock
9	TRIG width	t_{W_TRIG}	$3T_{CLK}$	–	–	ns	
10	High-level logic output voltage	V_{OH}	$0.8V_{LL}$	–	V_{LL}	V	SDOUT
11	Low-level logic output voltage	V_{OL}	0	–	$0.2V_{LL}$	V	SDOUT
12	Logic output off leak current	$I_{OFFLEAK}$	-10	–	10	µA	SDOUT Hi-Z output
13	SDOUT Propagation delay	t_{D_SDOUT}	8	12	18	ns	V_{LL} = 1.8V, 10pF load
			7	11	17	ns	V_{LL} = 2.5V, 10pF load
			6	10	16	ns	V_{LL} = 3.3V, 10pF load

*1. CLKIF has 50µA leakage at V_{LL} = 2.5V due to 50kΩ internal pull-down resistor.
*2. EN, SPIEN has 50µA leakage at V_{LL} = 2.5V due to 50kΩ internal pull-up resistor.
*3. Differential CMOS or Single-ended CMOS is also available for CLKP/N, CSP/N, SCLKP/N and SDATAP/N. In case of single-ended CMOS, N-terminals (CLKN, CSPN, SCLKN and SDATAN) need to be connected to half of V_{LL} (V_{LL}/2).

2.3 Open drain output

Table 5 FAULT

No.	Items	Symbol	Min.	Typ.	Max.	Units	Condition
1	Pull-up voltage	$V_{PUFAULT}$	–	–	V_{LL}	V	Connected to V_{LL} with R1
2	Output low voltage	$V_{OLFAULT}$	–	–	0.5	V	Active, V_{LL} = 2.5V, R1 = 2.5kΩ
3	Output current	I_{FAULT}	–	1.0	–	mA	V_{LL} = 2.5V, R1 = 2.5kΩ
4	Off leak current	$I_{OFFLEAK}$	-10	–	10	µA	Disabled (Hi-Z)

2.4 Logic inputs timing chart

2.4.1 LVDS clock inputs

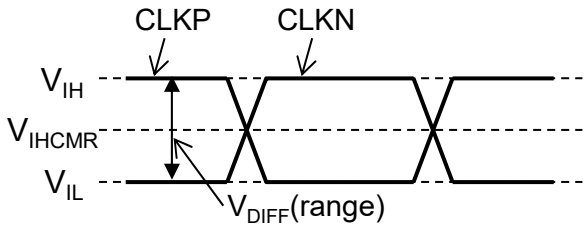

Figure 2 Differential Input Voltage Range (V_{DIFF}(range))

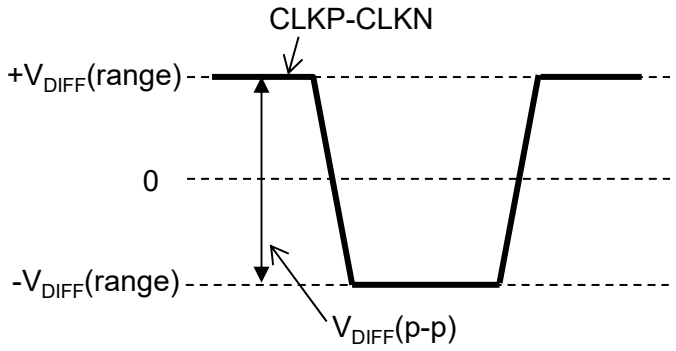

Figure 3 Differential Input Voltage Peak to Peak Swing ($V_{DIFF(p-p)}$)

2.4.2 TRIG and setup/hold time

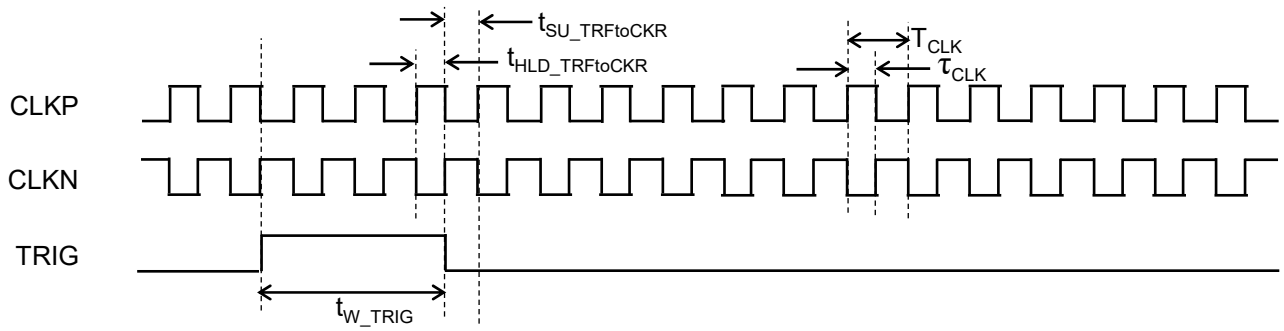

Figure 4

2.4.3 SPI inputs and setup/hold time

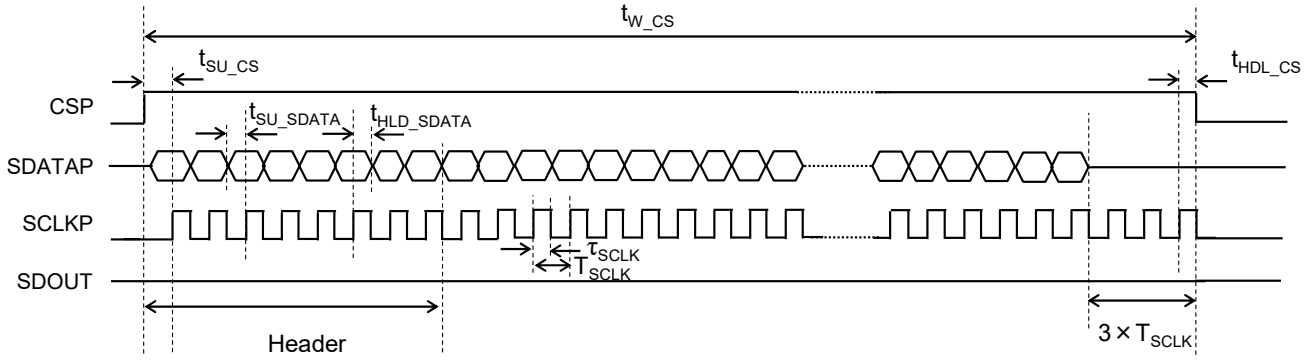

Figure 5 Write Data to Waveform Memory or Registers

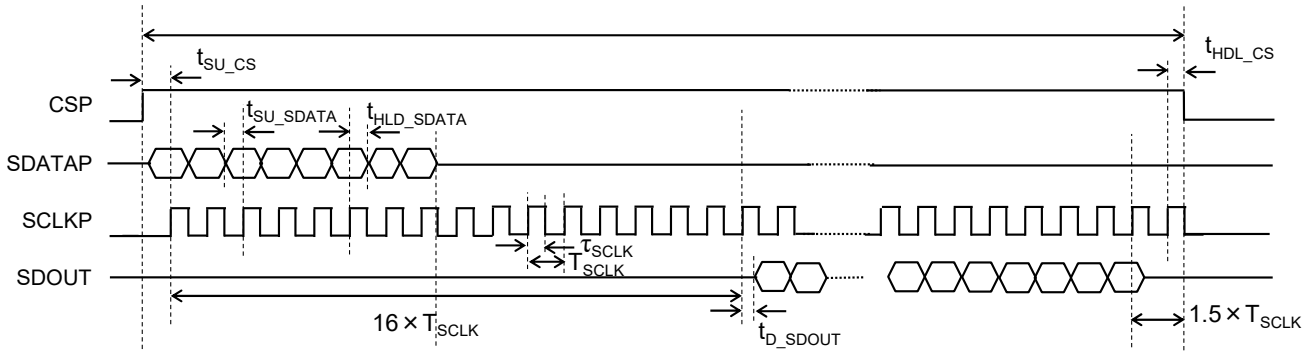

Figure 6 Read Data from Waveform Memory or Registers

2.4.4 Note on CSP rise timing

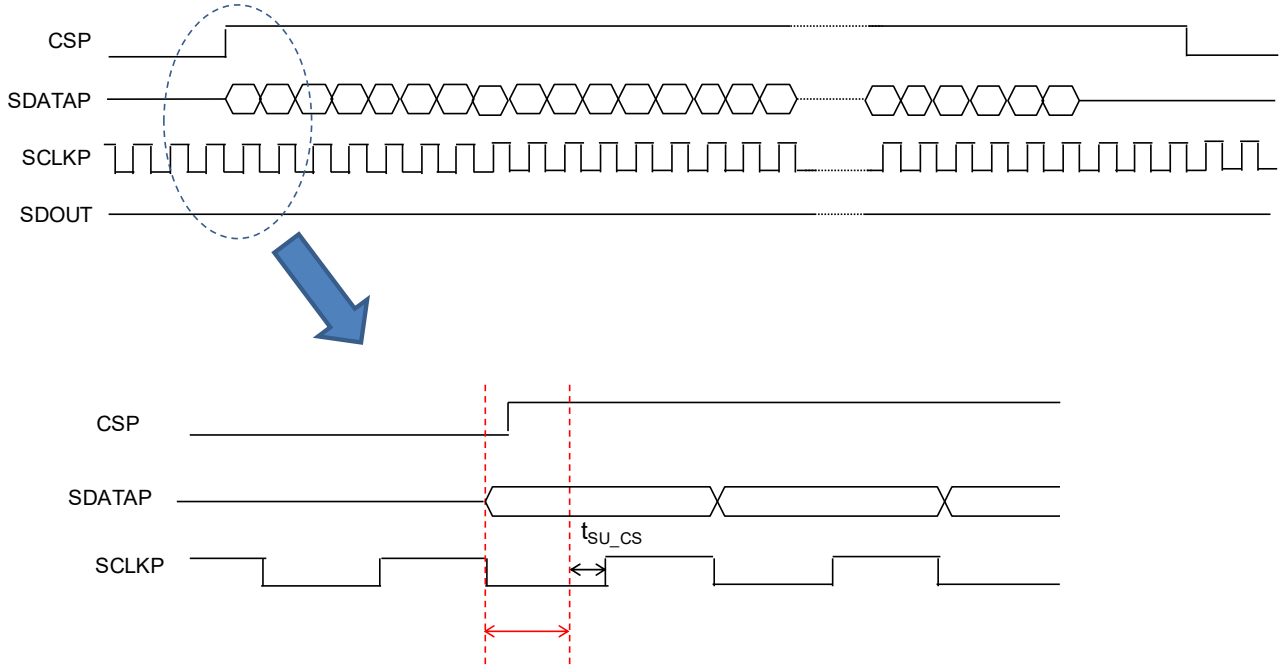

Figure 7 Note on CSP Rise Timing in Case that SCLKP Operates before CSP Rising as Following

In case that SCLKP operates before CSP rising, CSP has to rise during SCLKP is “low” except for setup time “t_{SU_CS}”.

■ Typical Application Circuit

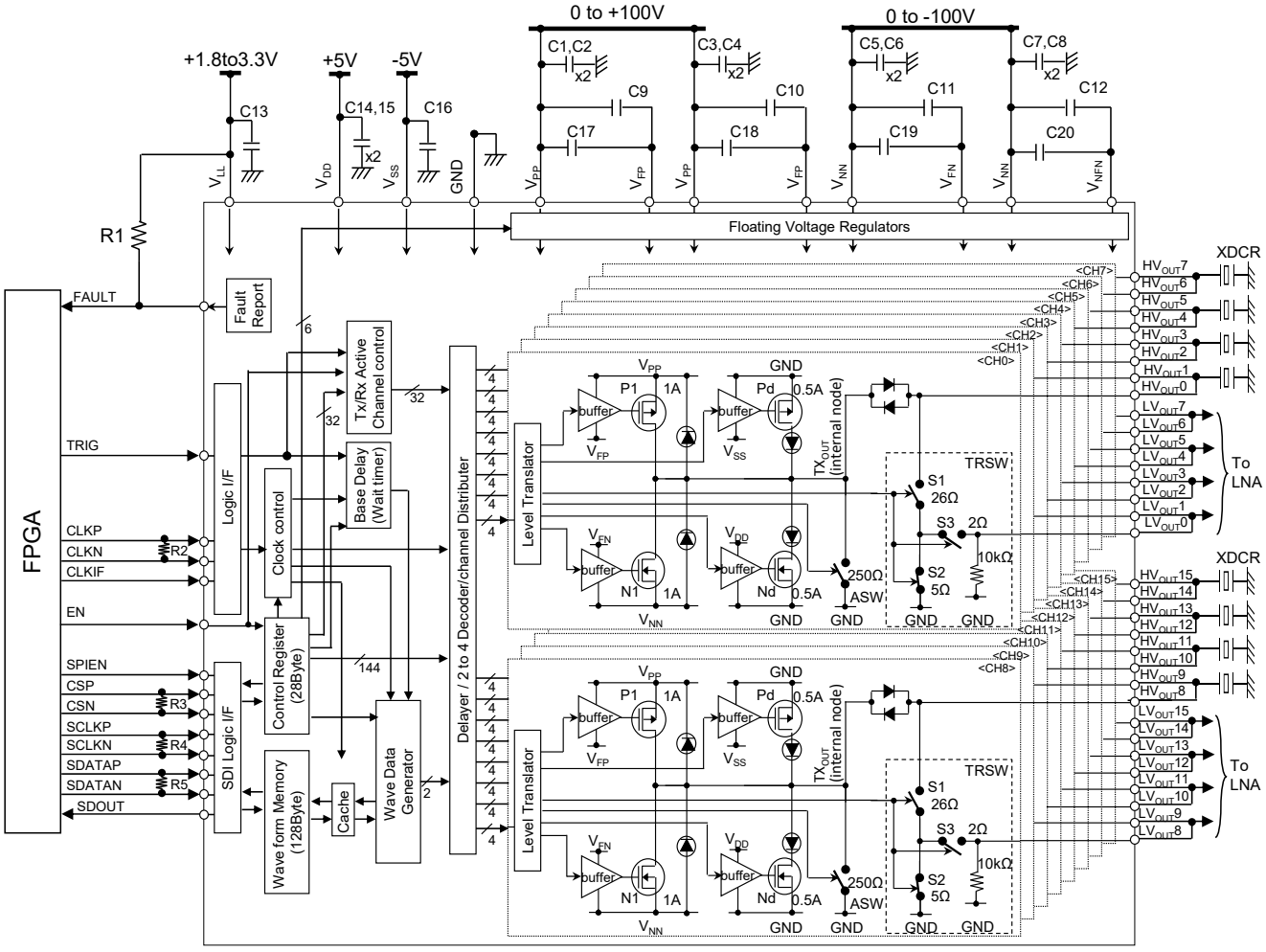

Figure 8 Typical Application Circuit

Remark C1 to C8: Ceramic capacitors of ≥200V 0.1μF to 1μF
C9 to C12: Ceramic capacitors of ≥16V 10μF
C13 to C20: Ceramic capacitors of ≥16V 0.1μF
R1: 2.5kΩ
R2 to R5: 100Ω (for LVDS)

■ Electrical Characteristics

1. Operating supply currents

Table 6 Operating Supply Currents（1/2）

V_{LL} = 2.5V, V_{DD}/V_{SS} = ±5V, T_A = 25ºC, CLKP/CLKN = 100MHz, HV_{OUT} load = 80pF//100Ω, LV_{OUT} load = 200pF//300Ω, unless otherwise specified.

No.	Items		Symbol	Spec			Units	Conditions
				Min.	Typ.	Max.		
1	V_{LL} current	SPIEN = H	I_{LLQD}	–	0.05	–	mA	Quiescent current-1 EN = 1 (Disable) Current mode 1 (CC = ’1’) V_{PP}/V_{NN} = ±100V
		SPIEN = L		–	0.10	–	mA	
2	V_{DD} current	SPIEN = H	I_{DDQD}	–	6	–	mA	
		SPIEN = L		–	14	–	mA	
3	V_{SS} current		I_{SSQD}	–	1.0	–	mA	
4	V_{PP} current		I_{PPQD}	–	0.1	–	mA	
5	V_{NN} current		I_{NNQD}	–	0.1	–	mA	
6	V_{LL} current	SPIEN = H	I_{LLQE}	–	0.10	–	mA	Quiescent current-2 EN = 0 (Enable) Current mode 1 (CC = ’1’) V_{PP}/V_{NN} = ±100V
		SPIEN = L		–	0.15	–	mA	
7	V_{DD} current	SPIEN = H, CLKIF = H (CMOS)	I_{DDQE}	–	9	–	mA	
		SPIEN = H, CLKIF = L (LVDS)		–	11	–	mA	
		SPIEN = L, CLKIF = H (CMOS)		–	16	–	mA	
		SPIEN = L, CLKIF = L (LVDS)		–	18	–	mA	
8	V_{SS} current		I_{SSQE}	–	1.0	–	mA	
9	V_{PP} current		I_{PPQE}	–	0.3	–	mA	
10	V_{NN} current		I_{NNQE}	–	0.3	–	mA	
11	V_{LL} current	SPIEN = H	I_{LLPW}	–	0.10	–	mA	PW operating current EN = 0 Current mode 1 (CC = ’1’) 16-channel active Bipolar 3-level 2-cycle f = 5MHz, PRT = 200µs V_{PP}/V_{NN} = ±60V
		SPIEN = L		–	0.15	–	mA	
12	V_{DD} current	SPIEN = H, CLKIF = H (CMOS)	I_{DDPW}	–	10	–	mA	
		SPIEN = H, CLKIF = L (LVDS)		–	13	–	mA	
		SPIEN = L, CLKIF = H (CMOS)		–	18	–	mA	
		SPIEN = L, CLKIF = L (LVDS)		–	21	–	mA	
13	V_{SS} current		I_{SSPW}	–	2	–	mA	
14	V_{PP} current		I_{PPPW}	–	8	–	mA	
15	V_{NN} current		I_{NNPW}	–	9	–	mA	

Table 6 Operating Supply Currents（2/2）

V_{LL} = 2.5V, V_{DD}/V_{SS} = ±5V, T_A = 25ºC, CLKP/CLKN = 100MHz, HV_{OUT} load = 80pF//100Ω, LV_{OUT} load = 200pF//300Ω unless otherwise specified.

No.	Items		Symbol	Spec			Units	Conditions
				Min.	Typ.	Max.		
16	V_{LL} current	SPIEN = H	I_{LLCW3}	–	0.1	–	mA	CW operating current-1 EN = 0, CKDIV[1:0] = 10 Current mode 3 (CC='1') 16-channel active Bipolar 3-level Continuous f = 5MHz V_{PP}/V_{NN} = ±5V
		SPIEN = L		–	0.15	–	mA	
17	V_{DD} current	SPIEN = H, CLKIF = H(CMOS)	I_{DDCW3}	–	181	–	mA	
		SPIEN = H, CLKIF = L(LVDS)		–	185	–	mA	
		SPIEN = L, CLKIF = H(CMOS)		–	189	–	mA	
		SPIEN = L, CLKIF = L(LVDS)		–	193	–	mA	
18	V_{SS} current		I_{SSCW3}	–	34	–	mA	
19	V_{PP} current		I_{PPCW3}	–	360	–	mA	
20	V_{NN} current		I_{PPCW3}	–	380	–	mA	
21	V_{LL} current	SPIEN = H	I_{LLCW2}	–	0.1	–	mA	CW operating current-2 EN = 0, CKDIV[1:0] = 10 Current mode 2 (CC='0') 16-channel active Bipolar 3-level Continuous f = 5MHz V_{PP}/V_{NN} = ±5V
		SPIEN = L		–	0.15	–	mA	
22	V_{DD} current	SPIEN = H, CLKIF = H(CMOS)	I_{DDCW2}	–	171	–	mA	
		SPIEN = H, CLKIF = L(LVDS)		–	175	–	mA	
		SPIEN = L, CLKIF = H(CMOS)		–	179	–	mA	
		SPIEN = L, CLKIF = L(LVDS)		–	183	–	mA	
23	V_{SS} current		I_{SSCW2}	–	26	–	mA	
24	V_{PP} current		I_{PPCW2}	–	310	–	mA	
25	V_{NN} current		I_{NNCW2}	–	330	–	mA	

2. Static characteristics

Table 7 Static Characteristics

V_{LL} = 2.5V, V_{DD}/V_{SS} = ±5V, T_A = 25ºC, VFP[2:0] = 000, VFN[2:0] = 000, DRVPADJ = 0, DRVNADJ = 0, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Condition
			Min.	Typ.	Max.		
1	$HV_{OUT}x$ output voltage range	$HV_{OUT}x$	-100	–	+100	V	
2	$HV_{OUT}x$ high-side peak current	I_{OH}	–	1.0	–	A	V_{PP}/V_{NN} = ±60V, Current mode 1 (CC = 1)
			–	0.5	–	A	V_{PP}/V_{NN} = ±60V, Current mode 0 (CC = 0)
3	$HV_{OUT}x$ high-side GND clamp peak current	I_{OHCL}	–	0.5	–	A	V_{PP}/V_{NN} = ±60V
4	$HV_{OUT}x$ low-side peak current	I_{OL}	–	1.0	–	A	V_{PP}/V_{NN} = ±60V, Current mode 1 (CC = 1)
			–	0.5	–	A	V_{PP}/V_{NN} = ±60V, Current mode 0 (CC = 0)
5	$HV_{OUT}x$ low-side GND clamp peak current	I_{OLCL}	–	0.5	–	A	V_{PP}/V_{NN} = ±60V
6	$HV_{OUT}x$ high-side on-resistance	R_{ONH}	–	18	–	Ω	I_{OH} = 100mA, Current mode 1 (CC = 1)
			–	31	–	Ω	I_{OH} = 100mA, Current mode 0 (CC = 0)
7	$HV_{OUT}x$ high-side GND clamp on-resistance	R_{ONHCL}	–	34	–	Ω	I_{OHCL} = 100mA
8	$HV_{OUT}x$ low-side on-resistance	R_{ONL}	–	17	–	Ω	I_{OL} = 100mA, Current mode 1 (CC = 1)
			–	30	–	Ω	I_{OL} = 100mA, Current mode 0 (CC = 0)
9	$HV_{OUT}x$ low-side GND clamp on-resistance	R_{ONLCL}	–	33	–	Ω	I_{OLCL} = 100mA
10	$HV_{OUT}x$ off-capacitance	C_{HVOFF}	–	17	–	pF	$TX_{OUT}x$ = GND, TRSW = off

3. Dynamic characteristics

Table 8 Dynamic Characteristics

V_{LL} = 2.5V, V_{DD}/V_{SS} = ±5V, T_A = 25ºC, CLKP/CLKN = 100MHz, VFP[2:0] = VFN[2:0] = '000', HV_{OUT} load = 80pF//100Ω, LV_{OUT} load = 200pF//300Ω, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Condition
			Min.	Typ.	Max.		
1	Output frequency	f_{OUT}	–	20	–	MHz	
2	Output rise propagation delay	t_{dr}	–	40	–	ns	
3	Output fall propagation delay	t_{df}	–	40	–	ns	
4	Output rise propagation delay clamp	t_{drCL}	–	40	–	ns	
5	Output fall propagation delay clamp	t_{dfCL}	–	40	–	ns	
6	Propagation delay matching	Δt_d	–	±1	±3	ns	
7	Output rise time	t_r	–	13	–	ns	CC = 1
			–	21	–	ns	CC = 0
		t_{rCL}	–	9	–	ns	
8	Output fall time	t_f	–	13	–	ns	CC = 1
			–	21	–	ns	CC = 0
		t_{fCL}	–	9	–	ns	
9	2nd harmonic distortion	HD2	–	-40	–	dBc	Bipolar, 2-cyc, f_{OUT} = 5MHz
10	Pulse cancellation	HDPC	–	-40	–	dBc	
		HDPC2	–	-40	–	dBc	
11	RMS output jitter	t_J	–	10	–	ps	Bipolar CW, f_{OUT} = 5MHz, V_{PP}/V_{NN} = ±5V
12	Crosstalk between channels	X_{TLK}	–	-70	–	dB	f_{OUT} = 5MHz, $10V_{p-p}$, HV_{OUT} load = 50Ω

4. Integrated Peripheral Circuits Characteristics

4. 1 T/R Switch characteristics

Table 9 T/R Switch Characteristics

V_{LL} = 2.5V, V_{DD}/V_{SS} = ±5V, V_{PP}/V_{NN} = ±60V, T_A = 25ºC, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Condition
			Min.	Typ.	Max.		
1	$LV_{OUT}x$ output voltage range	$LV_{OUT}x$	-0.85	–	+0.85	V	
2	TRSW on-resistance	R_{ONTR}	–	28	–	Ω	$HV_{OUT}x$ = 100mV, $LV_{OUT}x$ = 0V
3	TRSW on-capacitance	C_{ONTR}	–	7	–	pF	$LV_{OUT}x$ = 0V
4	TRSW off-resistance on HVOUTx	$R_{OFFTRHV}$	1	–	–	MΩ	
5	TRSW off-resistance on LVOUTx	$R_{OFFTRLV}$	8	10	12	kΩ	
6	Spike voltage on $HV_{OUT}x$ and $LV_{OUT}x$	V_{TRN}	–	–	110	mV_{PP}	80pF//100Ω load on $HV_{OUT}x$ 200pF//300Ω load on $LV_{OUT}x$
7	TRSW turn-on time	t_{dTRON}	–	300	–	ns	Logic input-to-ready for Rx signal See Fig.15
8	TRSW turn-off time	t_{dTROFF}	–	50	100	ns	See Fig.15

4. 2 Analog Switch

Table 10 Analog Switch Characteristics

V_{LL} = 2.5V, V_{DD}/V_{SS} = ±5V, T_A = 25ºC, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Condition
			Min.	Typ.	Max.		
1	ASW on-resistance	R_{ONASW}	–	250	–	Ω	

4. 3 HV Blocking Diode

Table 11 HV Blocking Diode Characteristics

V_{LL} = 2.5V, V_{DD}/V_{SS} = ±5V, T_A = 25ºC, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Condition
			Min.	Typ.	Max.		
1	Forward voltage	V_{FHVD}	–	1.0	–	V	I_F = 100mA
			–	1.2	–	V	I_F = 200mA
2	Reverse voltage	V_{RHVD}	200	–	–	V	I_R = 1μA

4. 4 LV Noise-cut Diode

Table 12 LV Noise-cut Diode Characteristics

V_{LL} = 2.5V, V_{DD}/V_{SS} = ±5V, T_A = 25ºC, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Condition
			Min.	Typ.	Max.		
1	Forward voltage	V_{FLVD}	–	1.1	–	V	I_F = 100mA
			–	1.25	–	V	I_F = 200mA

4. 5 Thermal Protection

Table 13 Thermal Protection Characteristics

V_{LL} = 2.5V, V_{DD}/V_{SS} = ±5V, T_A = 25ºC, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Condition
			Min.	Typ.	Max.		
1	THP temperature threshold	T_{THP}	90	110	120	ºC	THPCTL[1:0] = 00
			120	130	140		THPCTL[1:0] = 01
			140	150	160		THPCTL[1:0] = 10
			120	130	140		THPCTL[1:0] = 11 (THP is disabled.)
2	THP reset hysteresis	T_{HYSTHP}	5	10	20	ºC	

■ Operation Mode

Table 14 Operation Mode

Section	EN	CSP	SPIEN*1	TRIG	Tx-PT(x)*2	SPI LVDS Receiver	Memory Write	Memory Read	Register Write	Register Read	Tx	Rx	Operation Mode
A	1	0	0	×	×	Bias on	–	–	–	–	–	–	IC disabled
			1			Bias off							
B	1	1	0	×	×	Bias on	✓	✓	–	✓	–	–	IC disabled, W/R of Memory and Read of Register
			1			Bias off	–	–	–	–			
C	0	1	0	×	×	Bias on	✓	✓	✓	✓	–	✓*3	Rx, W/R of Memory or Register, Reset of Tx Operation
			1			Bias off	–	–	–	–			
D	0	0	0	1	×	Bias on	–	–	–	–	–	✓*3	Rx & Reset of Tx Operation
			1			Bias off							
E	0	0	0	0	Generated	Bias on	–	–	–	–	✓*3	–	Tx
			1			Bias off							
F	0	0	0	0	none	Bias on	–	–	–	–	–	✓*3	Rx
			1			Bias off							

***1.** SPIEN Signal is used to reduce the bias current of SPI LVDS Receiver when SPI is not used. (Power on/off time of LVDS receiver is <300ns/<100ns.)
***2.** Tx-PT(x) : Tx pattern signal of ch(x)
***3.** Individual register parameter on Tx/Rx active channel (TXACT[x] and RXACT[x]) is necessary to be set “1”.

Remark ✓: Available
–: Not available
×: Don't care

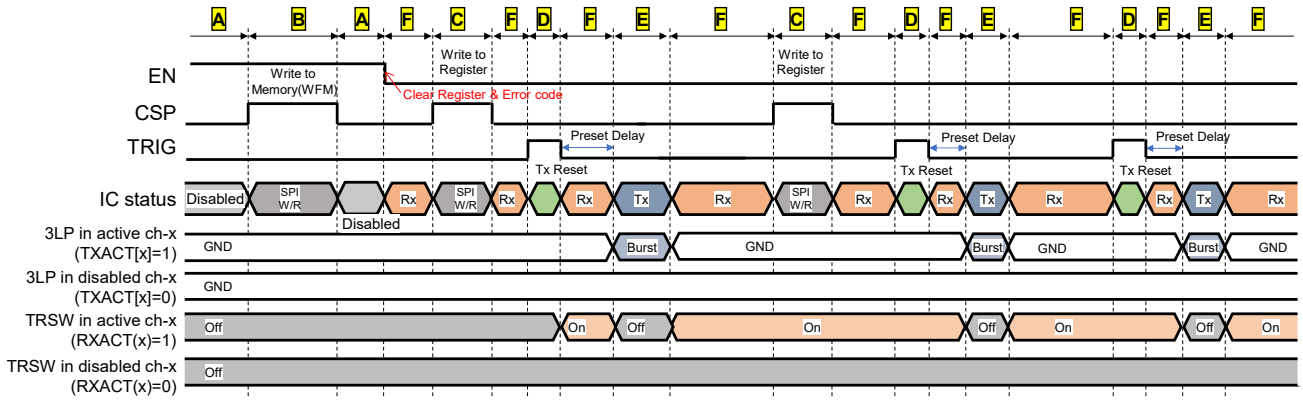

Figure 9 An Example of Operating Sequence

■ SPI Header Configuration

Table 15 SPI Operation

SDATA Control Header (First 1Byte of SDATA)								SPI operation
D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	
0	0	0	0	0000 (Reserved)				Write to the first 9Byte (R#0 to R#8) Control Registers and CRC[7:0]
0	1	0	0					Write to all 28Byte Control Registers and CRC[7:0]
1	0	0	0					N/A
1	1	0	0					Write to Memory and CRC[7:0]
0	0	0	1					Read from the first 9Byte (R#0 to R#8) Control Registers and CRC[7:0]
0	1	0	1					Read from all 28Byte Control Registers and CRC[7:0]
1	0	0	1					N/A
1	1	0	1					Read from Memory and CRC[7:0] through SDOUT pin
×	×	1	0					Read from ERROR[7:0] through SDOUT pin
×	×	1	1					Read from DSUM[7:0] through SDOUT pin

< 8bit CRC Conditions>
CRC initial value = 00000000
CRC Polynomial equation is $X^8+X^5+X^4+1$

Remark ×: Don't care

■ Access to Memory or Registers with SPI

1. SPI write to memory or registers operation

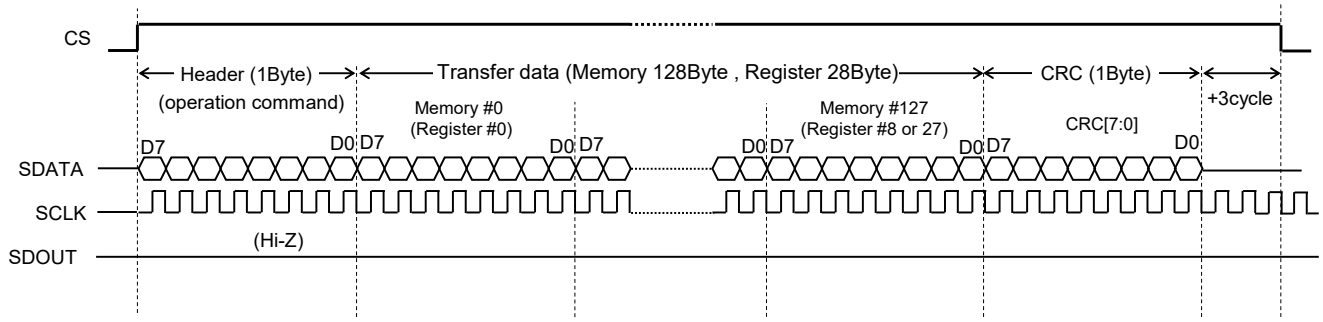

Figure 10 Sequence of Writing to Memory or Registers with SPI

Remark < CRC Conditions>
CRC initial value = 00000000
CRC Polynomial equation is $X^8+X^5+X^4+1$

In SPI "WRITE" operation, internal logic circuit also calculates the CRC ,and writes it to internal Register DSUM[7:0]. If CRC[7:0] matches DSUM[7:0], ERROR[0] = 0. If unmatched, ERROR[0] = 1 and FAULT pin reports, unless fault report is released.

.

2. Read back form memory or registers operation

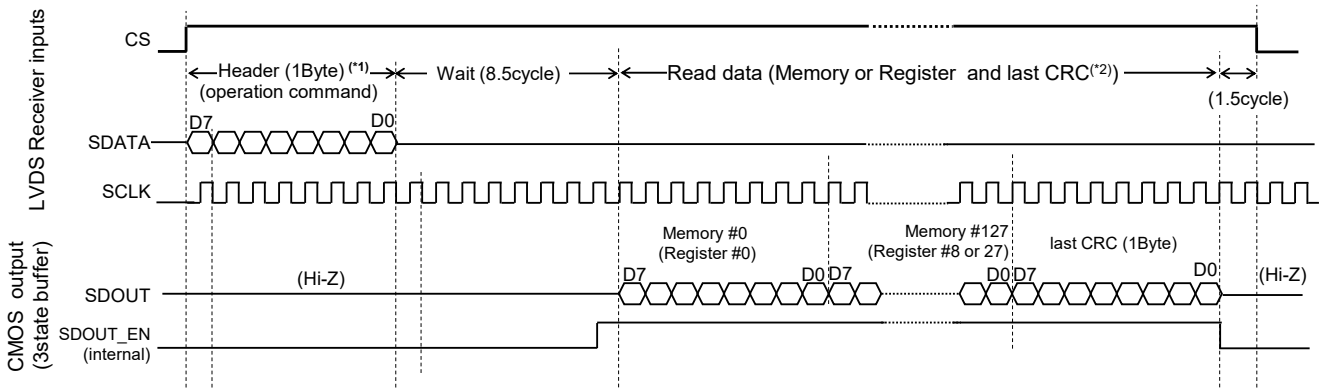

Figure 11 Sequence of Reading from Memory or Registers with SPI

***1.** In case of "READ" operation, SDATA inputs except for Header are ignored (CRC error detection is disabled).
***2.** Last CRC is the received CRC data from FPGA in previous "WRITE" operation to Memory or Register.

■ 3LP+TRSW Operation Example

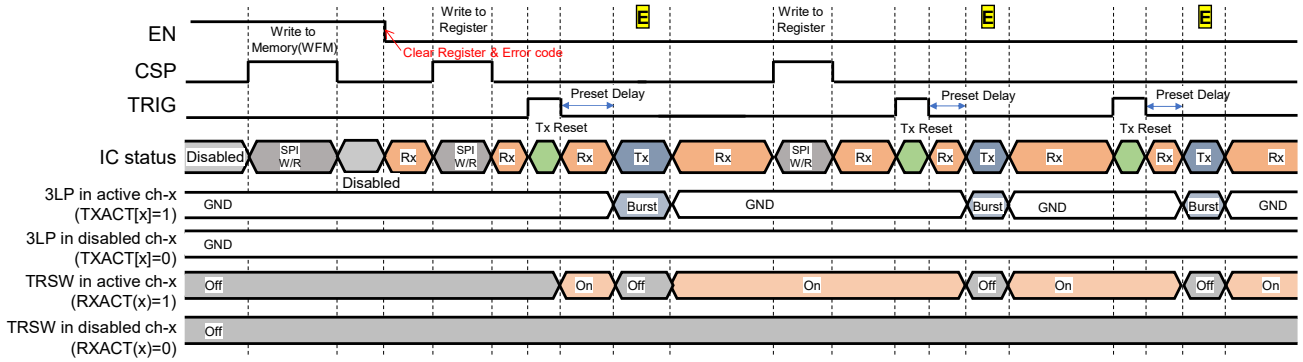

Figure 12 An Example of IC State Timing Diagram and 3LP Operation

E Tx starts from TRIG fall edge with preset delay time.
TRSW turns on except for Tx Burst period or IC-disabled.

Generating Tx WF Pattern
CODE_[1:0] = output state (±HV, GND) see **Truth Table**
Pulse width = 5ns×(W_[5:0]+2) (decimal, 10ns to 325ns)
START [6:0] = starting address
STOP [6:0] = stopping address
Repeat count(s) = 1, 1×REPEAT[7:0], 1×REPEAT[7:0], CW
CW mode ends with CS = 1 or TRIG = 1.

Generating Tx Delay (16ch)
CHx delay time from TRIG fall edge = BASE-DELAY + CHx-DELAY
BASE-DELAY(common) = 160ns×(BASEDL[7:0]) + 200ns
(decimal, 0.2µs to 41µs)
CHx-DELAY(/ch) = 5ns×(CHxDL[8:0])
(x = 0 to 15, decimal, 0 to 2.55µs)
Delay time resolution = 5ns

WFM

START[6:0]
STOP[6:0]

M#	Item	D7	D6	D5	D4	D3	D2	D1	D0
0	Pulse #0	CODE0 [1]	CODE0 [0]	W0 [5]	W0 [4]	W0 [3]	W0 [2]	W0 [1]	W0 [0]
1	Pulse #1	CODE1 [1]	CODE1 [0]	W1 [5]	W1 [4]	W1 [3]	W1 [2]	W1 [1]	W1 [0]
2	Pulse #2	CODE2 [1]	CODE2 [0]	W2 [5]	W2 [4]	W2 [3]	W2 [2]	W2 [1]	W2 [0]
.	.	.	.	.	.	.	.	.	.
127	Pulse #127	CODE127 [1]	CODE127 [0]	W127 [5]	W127 [4]	W127 [3]	W127 [2]	W127 [1]	W127 [0]

Register

R#	D7	D6	D5	D4	D3	D2	D1	D0
0	reserved	START[6]	START[5]	START[4]	START[3]	START[2]	START[1]	START[0]
1	reserved	STOP[6]	STOP[5]	STOP[4]	STOP[3]	STOP[2]	STOP[1]	STOP[0]
2	INV	MUL-RPT	reserved	CC	CKDIV[1]	CKDIV[0]	THPCTL[1]	THPCTL[0]
3	REPEAT[7]	REPEAT[6]	REPEAT[5]	REPEAT[4]	REPEAT[3]	REPEAT[2]	REPEAT[1]	REPEAT[0]
4	DRVPADJ	VFP[2]	VFP[1]	VFP[0]	DRVNADJ	VFN[2]	VFN[1]	VFN[0]
5	TXACT[15]	TXACT[14]	TXACT[13]	TXACT[12]	TXACT[11]	TXACT[10]	TXACT[9]	TXACT[8]
6	TXACT[7]	TXACT[6]	TXACT[5]	TXACT[4]	TXACT[3]	TXACT[2]	TXACT[1]	TXACT[0]
7	RXACT[15]	RXACT[14]	RXACT[13]	RXACT[12]	RXACT[11]	RXACT[10]	RXACT[9]	RXACT[8]
8	RXACT[7]	RXACT[6]	RXACT[5]	RXACT[4]	RXACT[3]	RXACT[2]	RXACT[1]	RXACT[0]
9	BASEDL[7]	BASEDL[6]	BASEDL[5]	BASEDL[4]	BASEDL[3]	BASEDL[2]	BASEDL[1]	BASEDL[0]
10	CH0DL[8]	CH0DL[7]	CH0DL[6]	CH0DL[5]	CH0DL[4]	CH0DL[3]	CH0DL[2]	CH0DL[1]
11	CH0DL[0]	CH1DL[8]	CH1DL[7]	CH1DL[6]	CH1DL[5]	CH1DL[4]	CH1DL[3]	CH1-DL[2]
:	:	:	:	:	:	:	:	:	:
26	CH14DL[6]	CH14DL[5]	CH14DL[4]	CH14DL[3]	CH14DL[2]	CH14DL[1]	CH14DL[0]	CH15DL[8]
27	CH15DL[7]	CH15DL[6]	CH15DL[5]	CH15DL[4]	CH15DL[3]	CH15DL[2]	CH15DL[1]	CH15DL[0]

■ Truth Table

Table 16 Truth Table

	IC status		External signal			Internal Tx-PT(x)	Control Register		WFM CODE[1:0]		Control Register	CHx TLP MOSFET/ASW/TRSW status						CHx Output state	
	mode	SPI	EN	CS	TRIG		CHx_TX	CHx_RX	[1]	[0]	INV	P1	N1	Pd	Nd	250Ω ASW	TRSW	$TXOUT_x$	$LVOUT_x$
A	IC disabled	no op.	1	0	×	none	×	×	×	×	×	OFF	OFF	**ON**	**ON**	**ON**	OFF	GND	10kΩ
B		Mem. W	1	1	×	none	×	×	×	×	×	OFF	OFF	**ON**	**ON**	**ON**	OFF	GND	10kΩ
C	Rx & Tx Reset by SPI W/R	Memory W/R or Register W/R	0	1	×	none	0	0	×	×	×	OFF	OFF	**ON**	**ON**	**ON**	OFF	GND	10kΩ
			0	1	×	none	0	1	×	×	×	OFF	OFF	**ON**	**ON**	**ON**	**ON**	GND	$HVOUT_x$
			0	1	×	none	1	0	×	×	×	OFF	OFF	**ON**	**ON**	**ON**	OFF	GND	10kΩ
			0	1	×	none	1	1	×	×	×	OFF	OFF	**ON**	**ON**	**ON**	**ON**	GND	$HVOUT_x$
D	Rx & Tx Reset By TRIG	no op.	0	0	1	none	0	0	×	×	×	OFF	OFF	**ON**	**ON**	**ON**	OFF	GND	10kΩ
			0	0	1	none	0	1	×	×	×	OFF	OFF	**ON**	**ON**	**ON**	**ON**	GND	$HVOUT_x$
			0	0	1	none	1	0	×	×	×	OFF	OFF	**ON**	**ON**	**ON**	OFF	GND	10kΩ
			0	0	1	none	1	1	×	×	×	OFF	OFF	**ON**	**ON**	**ON**	**ON**	GND	$HVOUT_x$
E	Tx	no op.	0	0	0	Gen.	1	×	0	0	×	OFF	OFF	**ON**	**ON**	**ON**	OFF	GND	10kΩ
			0	0	0	Gen.	1	×	0	1	0	**ON**	OFF	OFF	OFF	OFF	OFF	+HV	10kΩ
			0	0	0	Gen.	1	×	0	1	1	OFF	**ON**	OFF	OFF	OFF	OFF	-HV	10kΩ
			0	0	0	Gen.	1	×	1	0	0	OFF	**ON**	OFF	OFF	OFF	OFF	-HV	10kΩ
			0	0	0	Gen.	1	×	1	0	1	**ON**	OFF	OFF	OFF	OFF	OFF	+HV	10kΩ
			0	0	0	Gen.	1	×	1	1	×	N/A						N/A	
F	Rx	no op.	0	0	0	none	×	0	×	×	×	OFF	OFF	**ON**	**ON**	**ON**	OFF	GND	10kΩ
			0	0	0	none	×	1	×	×	×	OFF	OFF	**ON**	**ON**	**ON**	**ON**	GND	$HVOUT_x$

Remark ×: Don't care

Table 17

Current mode	CC	DRVP ADJ	DRVN ADJ	IOUT[A]	
				P1	N1
0	0	0	0	0.5	0.5
		0	1	0.5	0.6
		1	0	0.6	0.5
		1	1	0.6	0.6
1	1	0	0	1	1
		0	1	1	1.05
		1	0	1.05	1
		1	1	1.05	1.05

Table 18

VFPCTL			VPP-VFP [V]
[2]	[1]	[0]	
0	0	0	5
0	0	1	5.15
0	1	0	5.3
0	1	1	5.45
1	0	0	5
1	0	1	4.85
1	1	0	4.7
1	1	1	4.55

Table 19

VFNCTL			VFN-VNN [V]
[2]	[1]	[0]	
0	0	0	5
0	0	1	5.15
0	1	0	5.3
0	1	1	5.45
1	0	0	5
1	0	1	4.85
1	1	0	4.7
1	1	1	4.55

Table 20

THPCTL		THP Threshold [degC]	Tx reset function	FAULT Indication
[1]	[0]			
0	0	110	ON	ON
0	1	130	ON	ON
1	0	150	ON	ON
1	1	130	OFF	ON

■ Timing Chart

Control Registers
START[6:0] = n
STOP[6:0] = n+1

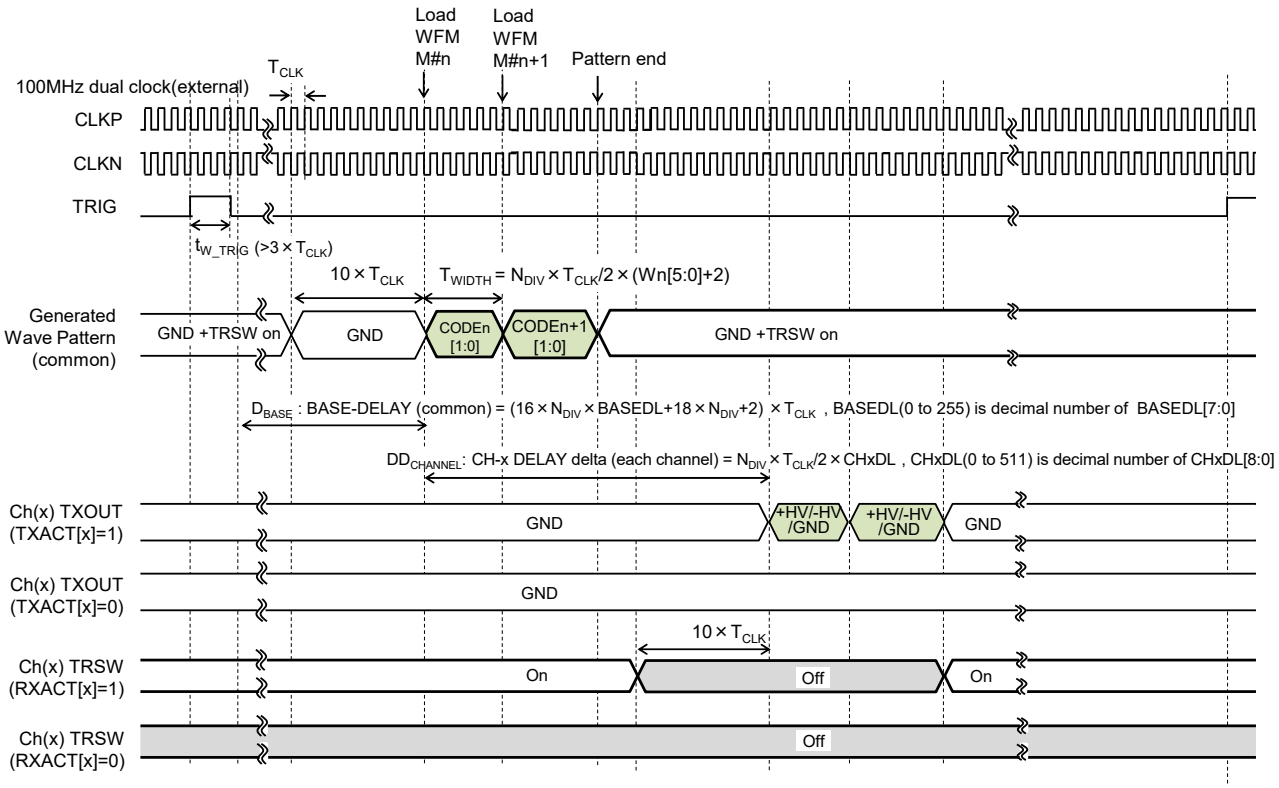

Figure 13 An Example of 3LP State Timing Diagram with Register TXACT[x] & RXACT[x] (x = 0 to 15)

■ Tx Burst Timing Chart

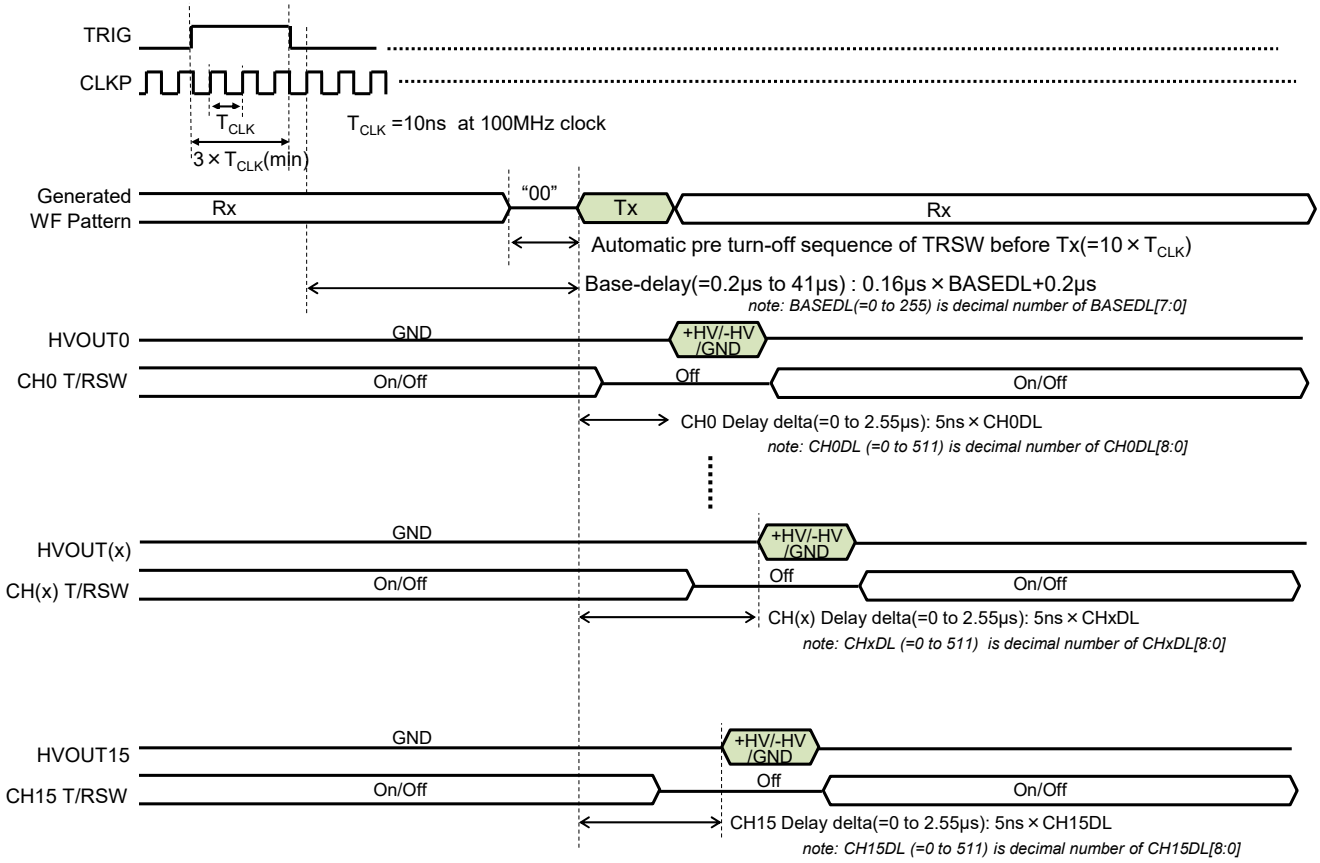

Figure 14 An Example of 3LP State Timing Diagram with Register BASEDL[7:0] & CHxDL[8:0] (x = 0 to 15)

■ Tx Propagation Delay and Rise/Fall Time Definition

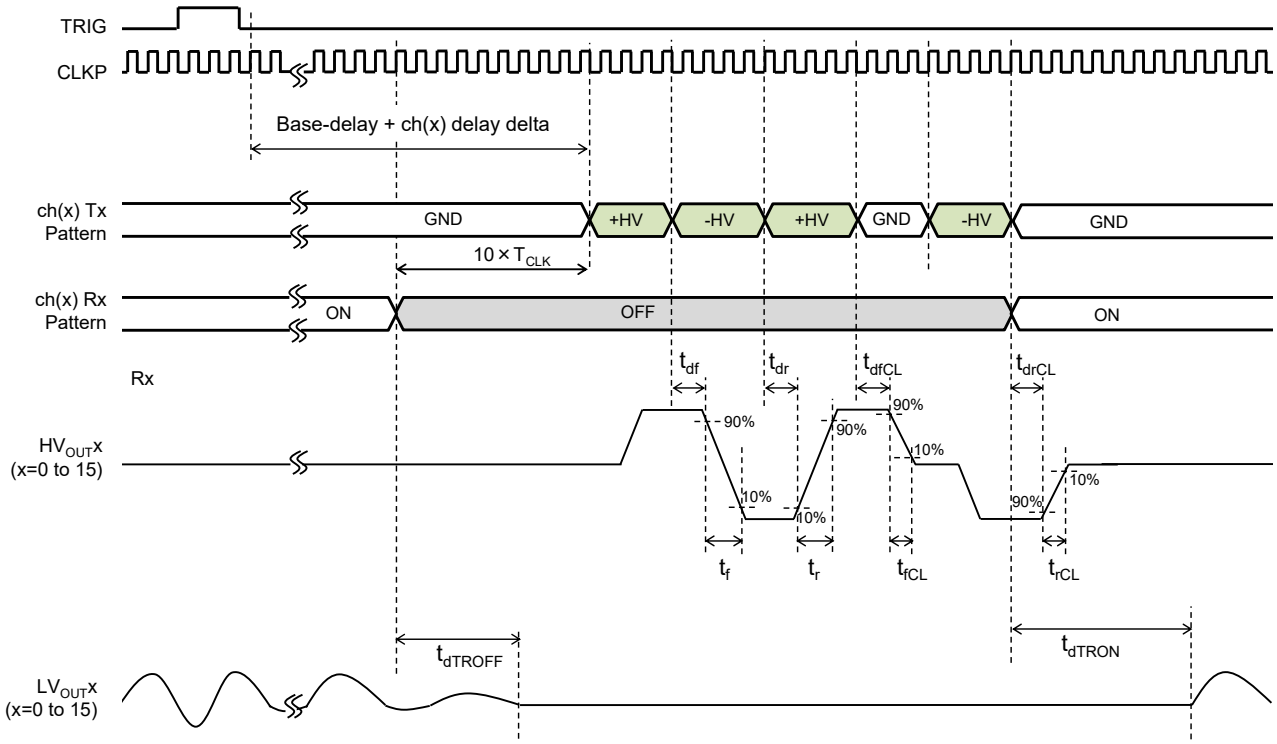

Figure 15 Tx Propagation Delay and Rise/fall Time

■ Tx Pulse Width and Delay Control Table

Table 21 Tx Pulse Width and Delay Control Table

No.	Items		Symbol	Spec			Units	Note
				Min.	Typ.	Max.		
1	Tx pulse width	N_{DIV} = 1	T_{WIDTH}	10	–	325	ns	T_{WIDTH} [ns] = N_{DIV} ×T_{CLK}/2 × (WIDTHx + 2) WIDTHx(= 0 to 63) is decimal number of WIDTHx[5:0] in memory #x, x = 0 to 127
		N_{DIV} = 2		20	–	650		
		N_{DIV} = 4		40	–	1300		
2	Tx pulse width resolution	N_{DIV} = 1	ΔT_{WIDTH}	–	5	–	ns	ΔT_{WIDTH} = N_{DIV}×T_{CLK}/2
		N_{DIV} = 2		–	10	–		
		N_{DIV} = 4		–	20	–		
3	Base delay Range	N_{DIV} = 1	D_{COM}	0.2	–	41	µs	D_{COM}=(16×N_{DIV}×BASEDL+18×N_{DIV}+2)×T_{CLK} BASEDL(= 0 to 255) is decimal number of BASEDL[7:0]
		N_{DIV} = 2		0.38	–	81.98		
		N_{DIV} = 4		0.74	–	163.94		
4	Base delay resolution	N_{DIV} = 1	ΔD_{COM}	–	0.16	–	µs	ΔD_{COM} = 16×N_{DIV}×T_{CLK}
		N_{DIV} = 2		–	0.32	–		
		N_{DIV} = 4		–	0.64	–		
5	CHx delay delta range (x = 0 to 15)	N_{DIV} = 1	$DD_{CHANNEL}$	0	–	2555	ns	$DD_{CHANNEL}$ = N_{DIV}×T_{CLK}/2×CHxDL CHxDL(= 0 to 511) is decimal number of CHxDL[8:0] x = 0 to 15
		N_{DIV} = 2		0	–	5110		
		N_{DIV} = 4		0	–	10220		
6	CHx delay delta resolution (x = 0 to 15)	N_{DIV} = 1	$\Delta DD_{CHANNEL}$	–	5	–	ns	$\Delta DD_{CHANNEL}$ = N_{DIV}×T_{CLK}/2
		N_{DIV} = 2		–	10	–		
		N_{DIV} = 4		–	20	–		

Remark N_{DIV}(= 1,2,4) is internal clock dividing factor with Register CKDIV[1:0].
CKDIV[1:0] = 00 : N_{DIV} = 1
CKDIV[1:0] = 01 : N_{DIV} = 2
CKDIV[1:0] = 10,11 : N_{DIV} = 4

■ Memory Map

Table 22 Memory Map

Memory #	D7	D6	D5	D4	D3	D2	D1	D0
0	CODE0[1:0]		WIDTH0[5:0]					
1	CODE1[1:0]		WIDTH1[5:0]					
2	CODE2[1:0]		WIDTH2[5:0]					
3	CODE3[1:0]		WIDTH3[5:0]					
⋮	⋮		⋮					
124	CODE124[1:0]		WIDTH124[5:0]					
125	CODE125[1:0]		WIDTH125[5:0]					
126	CODE126[1:0]		WIDTH126[5:0]					
127	CODE127[1:0]		WIDTH127[5:0]					

Remark 1. In Memory Map, each 1-byte code consists of upper 2-bit CODEx[1:0] and lower 6-bit WIDTHx[5:0].Suffix “x” corresponds to 1-byte Memory number (x = 0 to 127).

2. CODEx[1:0] stands for an output state of Tx burst as shown in “**Truth Table**”.

3. WIDTHx[5:0] expresses the pulse width (T_{WIDTH}) which is calculated as follows.

T_{WIDTH} [ns] = $N_{DIV} \times T_{CLK}/2 \times (WIDTHx + 2)$

4. Where, T_{CLK} is the CLKP/CLKN clock period, WIDTHx(= 0 to 63) is decimal number of WIDTHx[5:0] and N_{DIV}(= 1,2,4) is internal clock dividing factor with Register CKDIV[1:0].

5. In case of 100MHz CLK,

CKDIV[1:0] = 00 : N_{DIV} = 1, T_{WIDTH} [ns] is 10ns to 325ns (5ns step).
CKDIV[1:0] = 01 : N_{DIV} = 2, T_{WIDTH} [ns] is 20ns to 650ns (10ns step).
CKDIV[1:0] = 10,11 : N_{DIV} = 4, T_{WIDTH} [ns] is 40ns to 1300ns (20ns step).

■ Register Parameter Function

Table 23 Register Parameter Function

Items	Register	type	function
WFM Read Address(start)	START[6:0]	common	Starting address of the Waveform Memory for generating the Tx waveform pattern
WFM Read Address(stop)	STOP[6:0]	common	Stop address of the Waveform Memory for generating the Tx waveform pattern
TX Waveform control	INV	common	Inversion control of generating Tx waveform pattern
Wave generation Repeat control(1)	MUL-RPT	common	Multiplying factor selection for REPEAT[7:0] (1: 1×REPEAT[7:0] , 0: 16×REPEAT[7:0])
Tx driver current control	CC	common	P1/N1 Tx driver current control (0 = 0.5A, 1 = 1A)
Tx clock dividing	CKDIV[1:0]	common	Internal clock dividing factor "N_{DIV}" selection (00:N_{DIV} = 1, 01:N_{DIV} = 2, 10 or 11 :N_{DIV} = 4)
P1 Driver adjustment	DRVPADJ	common	0: none, 1: Add 0.1A to P1 driver current
N1 Driver adjustment	DRVNADJ	common	0: none, 1: Add 0.1A to N1 driver current
Built-in power supply control for P1	VFP[2:0]	common	VFP[2] = 0: VPP1-VFP1 (= 5 to 5.45) : 5+0.15×VFP, VFP is decimal number of VFP[1:0] VFP[2] = 1: VPP1-VFP1(= 4.55 to 5) : 5-0.15×VFP, VFP is decimal number of VFP[1:0]
Built-in power supply control for N1	VFN[2:0]	common	VFN[2] = 0: VFN1-VNN1 (= 5 to 5.45) : 5+0.15×VFN, VFN is decimal number of VFN[1:0] VFN[2] = 1: VFN1-VNN1(= 4.55 to 5) : 5-0.15×VFN, VFN is decimal number of VFN[1:0]
THP detection control	THPCTL [1:0]	common	THP detection control (00: 110°C, 01: 130°C, 10: 150°C, 11: Disabled)
Wave generation Repeat control(2)	REPEAT [7:0]	common	Repeat counts control of Tx waveform pattern generation
Active channel control for Tx	TXACT [15:0]	/channel	Active channel control in Tx, TXACT[x] corresponds to ch(x) in Tx
Active channel control for Rx	RXACT [15:0]	/channel	Active channel control of T/R-SW, RXACT[x] corresponds to TRSW of ch(x)
TX delay control (1)	BASEDL [7:0]	common	Tx offset delay (common to all channel) : (16×N_{DIV}×BASEDL+14×N_{DIV}+2)×T_{CLK} BASEDL(= 0 to 255) is decimal number of BASEDL[7:0], T_{CLK} is external clock period.
TX delay control (2)	CHxDL[8:0]	/channel	Tx delay for each channel x (x = 0 to 15) : CHxDL×N_{DIV} ×T_{CLK}/2 CHxDL(= 0 to 511) is decimal number of CHxDL[8:0] , T_{CLK} is external clock period.

REPEAT[7:0] (Repeat counts control of Tx waveform pattern generation)
REPEAT[7:0] = 00000000 : repeat count = 1
REPEAT[7:0] = 00000001 to 11111110 : repeat count = 1(or 16)×REPEAT[7:0]
REPEAT[7:0] = 11111111 : continuous

■ Tx Control Register MAP

Table 24 Tx Control Register MAP

R#	D7	D6	D5	D4	D3	D2	D1	D0
0	reserved	START[6]	START[5]	START[4]	START[3]	START[2]	START[1]	START[0]
1	reserved	STOP[6]	STOP[5]	STOP[4]	STOP[3]	STOP[2]	STOP[1]	STOP[0]
2	INV	MUL-RPT	reserved	CC	CKDIV[1]	CKDIV[0]	THPCTL[1]	THPCTL[0]
3	REPEAT[7]	REPEAT[6]	REPEAT[5]	REPEAT[4]	REPEAT[3]	REPEAT[2]	REPEAT[1]	REPEAT[0]
4	DRVPADJ	VFP[2]	VFP[1]	VFP[0]	DRVNADJ	VFN[2]	VFN[1]	VFN[0]
5	TXACT[15]	TXACT[14]	TXACT[13]	TXACT[12]	TXACT[11]	TXACT[10]	TXACT[9]	TXACT[8]
6	TXACT[7]	TXACT[6]	TXACT[5]	TXACT[4]	TXACT[3]	TXACT[2]	TXACT[1]	TXACT[0]
7	RXACT[15]	RXACT[14]	RXACT[13]	RXACT[12]	RXACT[11]	RXACT[10]	RXACT[9]	RXACT[8]
8	RXACT[7]	RXACT[6]	RXACT[5]	RXACT[4]	RXACT[3]	RXACT[2]	RXACT[1]	RXACT[0]
9	BASEDL[7]	BASEDL[6]	BASEDL[5]	BASEDL[4]	BASEDL[3]	BASEDL[2]	BASEDL[1]	BASEDL[0]
10	CH0DL[8]	CH0DL[7]	CH0DL[6]	CH0DL[5]	CH0DL[4]	CH0DL[3]	CH0DL[2]	CH0DL[1]
11	CH0DL[0]	CH1DL[8]	CH1DL[7]	CH1DL[6]	CH1DL[5]	CH1DL[4]	CH1DL[3]	CH1-DL[2]
12	CH1DL[1]	CH1DL[0]	CH2DL[8]	CH2DL[7]	CH2DL[6]	CH2DL[5]	CH2DL[4]	CH2DL[3]
13	CH2DL[2]	CH2DL[1]	CH2DL[0]	CH3DL[8]	CH3DL[7]	CH3DL[6]	CH3DL[5]	CH3DL[4]
14	CH3DL[3]	CH3DL[2]	CH3DL[1]	CH3DL[0]	CH4DL[8]	CH4DL[7]	CH4DL[6]	CH4DL[5]
15	CH4DL[4]	CH4DL[3]	CH4DL[2]	CH4DL[1]	CH4DL[0]	CH5DL[8]	CH5DL[7]	CH5DL[6]
16	CH5DL[5]	CH5DL[4]	CH5DL[3]	CH5DL[2]	CH5DL[1]	CH5DL[0]	CH6DL[8]	CH6DL[7]
17	CH6DL[6]	CH6DL[5]	CH6DL[4]	CH6DL[3]	CH6DL[2]	CH6DL[1]	CH6DL[0]	CH7DL[8]
18	CH7DL[7]	CH7DL[6]	CH7DL[5]	CH7DL[4]	CH7DL[3]	CH7DL[2]	CH7DL[1]	CH7DL[0]
19	CH8DL[8]	CH8DL[7]	CH8DL[6]	CH8DL[5]	CH8DL[4]	CH8DL[3]	CH8DL[2]	CH8DL[1]
20	CH8DL[0]	CH9DL[8]	CH9DL[7]	CH9DL[6]	CH9DL[5]	CH9DL[4]	CH9DL[3]	CH9-DL[2]
21	CH9DL[1]	CH9DL[0]	CH10DL[8]	CH10DL[7]	CH10DL[6]	CH10DL[5]	CH10DL[4]	CH10DL[3]
22	CH10DL[2]	CH10DL[1]	CH10DL[0]	CH11DL[8]	CH11DL[7]	CH11DL[6]	CH11DL[5]	CH11DL[4]
23	CH11DL[3]	CH11DL[2]	CH11DL[1]	CH11DL[0]	CH12DL[8]	CH12DL[7]	CH12DL[6]	CH12DL[5]
24	CH12DL[4]	CH12DL[3]	CH12DL[2]	CH12DL[1]	CH12DL[0]	CH13DL[8]	CH13DL[7]	CH13DL[6]
25	CH13DL[5]	CH13DL[4]	CH13DL[3]	CH13DL[2]	CH13DL[1]	CH13DL[0]	CH14DL[8]	CH14DL[7]
26	CH14DL[6]	CH14DL[5]	CH14DL[4]	CH14DL[3]	CH14DL[2]	CH14DL[1]	CH14DL[0]	CH15DL[8]
27	CH15DL[7]	CH15DL[6]	CH15DL[5]	CH15DL[4]	CH15DL[3]	CH15DL[2]	CH15DL[1]	CH15DL[0]

■ CRC and Error Register

Table 25 CRC, Calculated CRC and ERROR Register MAP

Register	D7	D6	D5	D4	D3	D2	D1	D0
CRC	CRC[7:0]							
Calculated CRC	DSUM[7:0]							
Error	ERROR[7:0]							

Table 26 CRC, Calculated CRC and ERROR Register Function

CRC[7:0]	Transferred CRC data in SDATA CRC initial value = 00000000 CRC Polynomial equation is $X^8+X^5+X^4+1$
DSUM[7:0]	Calculated CRC values with transferred SDATA signal
ERROR[7:0]	When Error has occurred, ERROR register corresponding to error type is set to be “1”. ERROR[7:3] : Not used. ERROR[2]: threshold over of the junction temperature set in advance. ERROR[1]: start and stop address for Tx waveform pattern generation are same. ERROR[0]: SPI transfer error (CRC un-match) has occurred.

Remark Error[7:0] are cleared when IC is powered on or “EN” becomes from “high” to “low” (fall edge).

■ Pin Configuration

Table 27 Pin Configuration (1/2)

Pin#	Pin Name	Function
1	VFN	Built-in power supply for channel 0 to channel 7 N-MOS (N1) gate drive
2	LVOUT1	Low voltage output of channel 1
3	LVOUT0	Low voltage output of channel 0
4	GND	Logic power ground (0V)
5	GND	Logic power ground (0V)
6	EN	Control of chip enable, H = disable, L = enable (50kΩ internal pull-up)
7	FAULT	Fault output flag, open N-MOS drain
8	VDD	Positive low voltage power supply (+5V)
9	CLKP	Positive LVDS clock input (up to 100MHz)
10	CLKN	Negative LVDS clock Input (up to 100MHz)
11	GND	Logic power ground (0V)
12	TRIG	Tx Trigger signal
13	VLL	Positive low voltage power supply (+1.8 to 3.3V)
14	CLKIF	I/F selection of CLKP/CLKN, H: CMOS, L: LVDS (50kΩ internal pull-down)
15	LVOUT15	Low voltage output of channel 15
16	LVOUT14	Low voltage output of channel 14
17	VFN	Built-in power supply for ch8 to ch15 N-MOS (N1) gate drive
18	HVOUT15	High voltage output of channel 15
19	HVOUT14	High voltage output of channel 14
20	VPP	ch8 to ch15 positive high voltage power supply (0 to +100V)
21	HVOUT13	High voltage output of channel 13
22	HVOUT12	High voltage output of channel 12
23	VNN	channel 8 to channel 15 Negative high voltage power supply (0 to -100V)
24	LVOUT13	Low voltage output of channel 13
25	LVOUT12	Low voltage output of channel 12
26	HGND	channel 8 to channel 15 Drive power ground (0V)
27	LVOUT11	Low voltage output of channel 11
28	LVOUT10	Low voltage output of channel 10
29	VNN	channel 8 to channel 15 Negative high voltage power supply (0 to -100V)
30	HVOUT11	High voltage output of channel 11
31	HVOUT10	High voltage output of channel 10
32	VPP	channel 8 to channel 15 positive high voltage power supply (0 to +100V)
33	HVOUT9	High voltage output of channel 9
34	HVOUT8	High voltage output of channel 8
35	VFP	Built-in power supply for channel 0 to channel 7 P-MOS (P1) gate drive
36	LVOUT9	Low voltage output of channel 9
37	LVOUT8	Low voltage output of channel 8
38	SDOUT	SPI serial output data
39	SPIEN	Control of SPI Receiver Enable, H = disable, L = enable (50kΩ internal pull-up)
40	SDATAP	SPI positive serial input data (LVDS/CMOS)
41	SDATAN	SPI negative serial input data (LVDS/CMOS)
42	VDD	Positive low voltage power supply (+5V)
43	GND	Logic power ground (0V)
44	VSS	Negative low voltage power supply (-5V)
45	SCLKP	SPI Positive LVDS/CMOS clock input (up to 100MHz)
46	SCLKN	SPI negative LVDS/CMOS clock Input (up to 100MHz)
47	CSP	SPI positive chip select signal (LVDS/CMOS)
48	CSN	SPI negative chip select signal (LVDS/CMOS)
49	LVOUT7	Low voltage output of channel 7
50	LVOUT6	Low voltage output of channel 6
51	VFP	Built-in power supply for channel 0 to channel 7 P-MOS (P1) gate drive

Table 27 Pin Configuration (2/2)

Pin#	Pin Name	Function
52	HVOUT7	High voltage output of channel 7
53	HVOUT6	High voltage output of channel 6
54	VPP	channel 0 to channel 7 positive high voltage power supply (0 to +100V)
55	HVOUT5	High voltage output of channel 5
56	HVOUT4	High voltage output of channel 4
57	VNN	channel 0 to channel 7 Negative high voltage power supply (0 to -100V)
58	LVOUT5	Low voltage output of channel 5
59	LVOUT4	Low voltage output of channel 4
60	HGND	channel 0 to channel 7 Drive power ground (0V)
61	LVOUT3	Low voltage output of channel 3
62	LVOUT2	Low voltage output of channel 2
63	VNN	channel 0 to channel 7 Negative high voltage power supply (0 to -100V)
64	HVOUT3	High voltage output of channel 3
65	HVOUT2	High voltage output of channel 2
66	VPP	channel 0 to channel 7 positive high voltage power supply (0 to +100V)
67	HVOUT1	High voltage output of channel 1
68	HVOUT0	High voltage output of channel 0

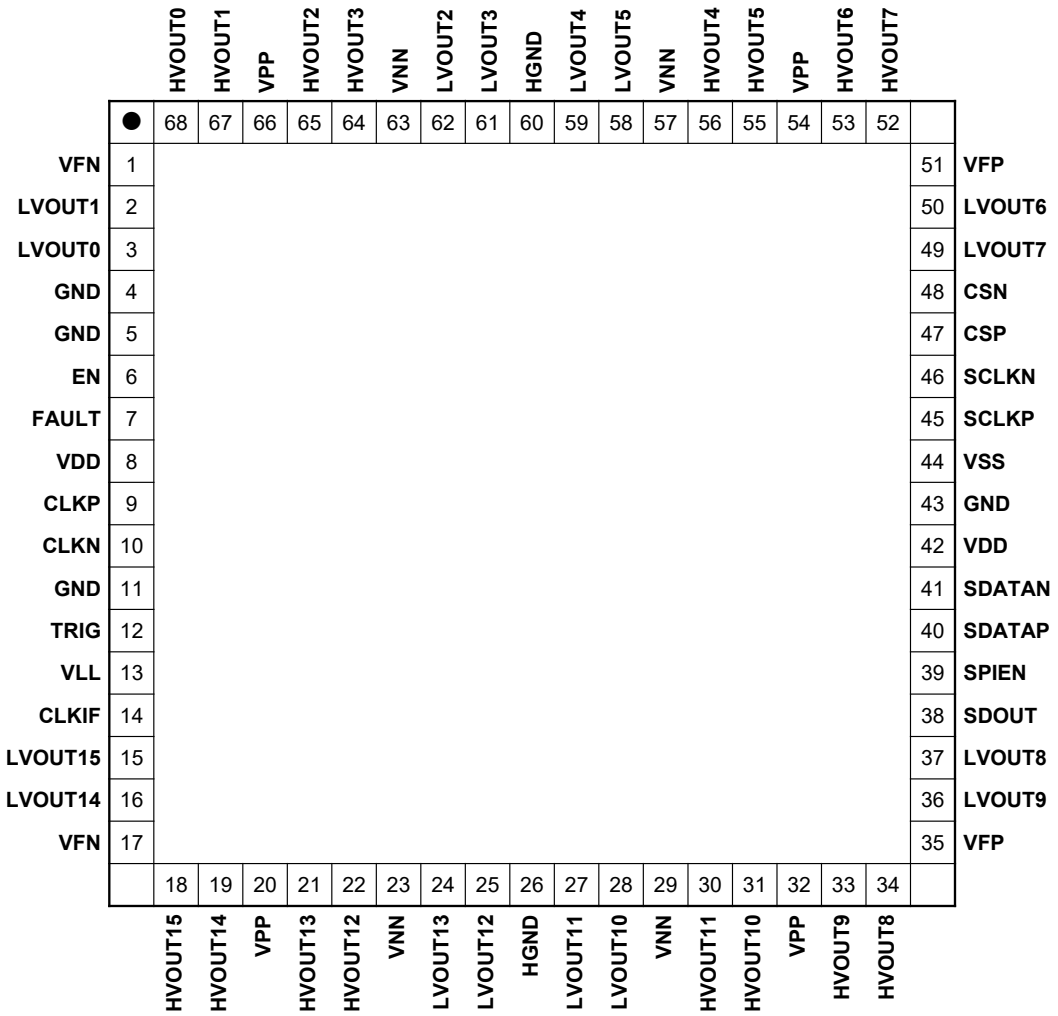

Figure 16 Pin Configuration

■ Package

Table28 Package Drawing Codes

Package Name	Dimension	Tray	Marking	Land	Packing
QFN-68(1010)B	QN068-B-P	QN068-B-T	QN068-B-M	QN068-B-L	QN068-B-K

■ Storage, Mounting

1. Storage Conditions

1.1 The storage location should be kept at 5 to 35 °C and 40 to 70% relative humidity. Keeping in a dry box is recommended. Moisture-proof property is assured for 12 months from delivery date for sealed moisture-proof packing, while it is guaranteed for 7 days from unpacked date under the condition above.

1.2 When the storage conditions do not conform to those above or other conditions occur indicating moisture exposure, the ICs should be dried to avoid package cracks. A baking process at 125 °C lasting for 24 hours results in sufficient dehumidification. The baking is not allowed more than twice, and the ICs should be mounted within 7 days after initial baking or within 10 days of total exposure after the second dehumidification.

2. Reflow soldering

The temperature rise may be different in the resin and a terminal part due to the reflow soldering.
It is necessary to check the package surface temperature (resin) before setting the temperature profile.
Figure 17 shows the resistance to soldering heat condition for package (Reflow method).
Confirm the heat resistance of the package shown below. (Based on JEDEC J-STD-020).

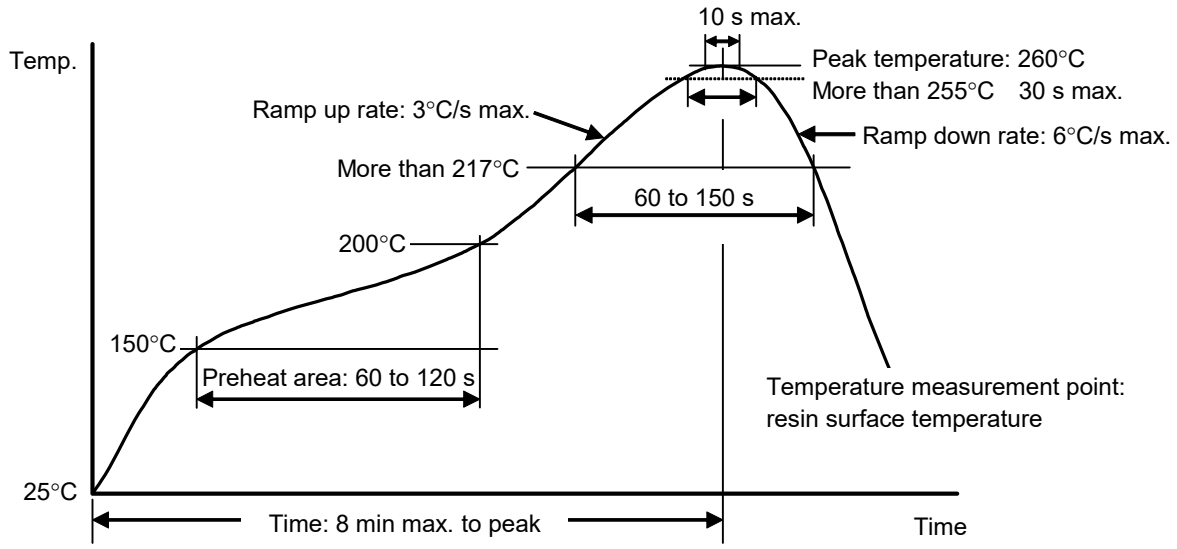

Figure 17 Resistance to Soldering Heat Condition for Package (Reflow Method)

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1.1 Material of container or any device to carry products should be free from ESD, which may be caused by vibration while transportation. It is recommended that electric-conductive container or aluminum sheet be used as an effective countermeasure.

1.2 Those what touch products such as work platform, machine, measurement/test equipment should be grounded.

1.3 Those who deal with products should be grounded through a large series impedance around 100kΩ to 1MΩ.

1.4 Prevent friction with other materials made with high polymer.

1.5 Prevent vibration or friction when carrying the printed circuit board (PCB) where products are mounted. To short circuit terminals is a recommended countermeasure to keep the same electric potential on the PCB.

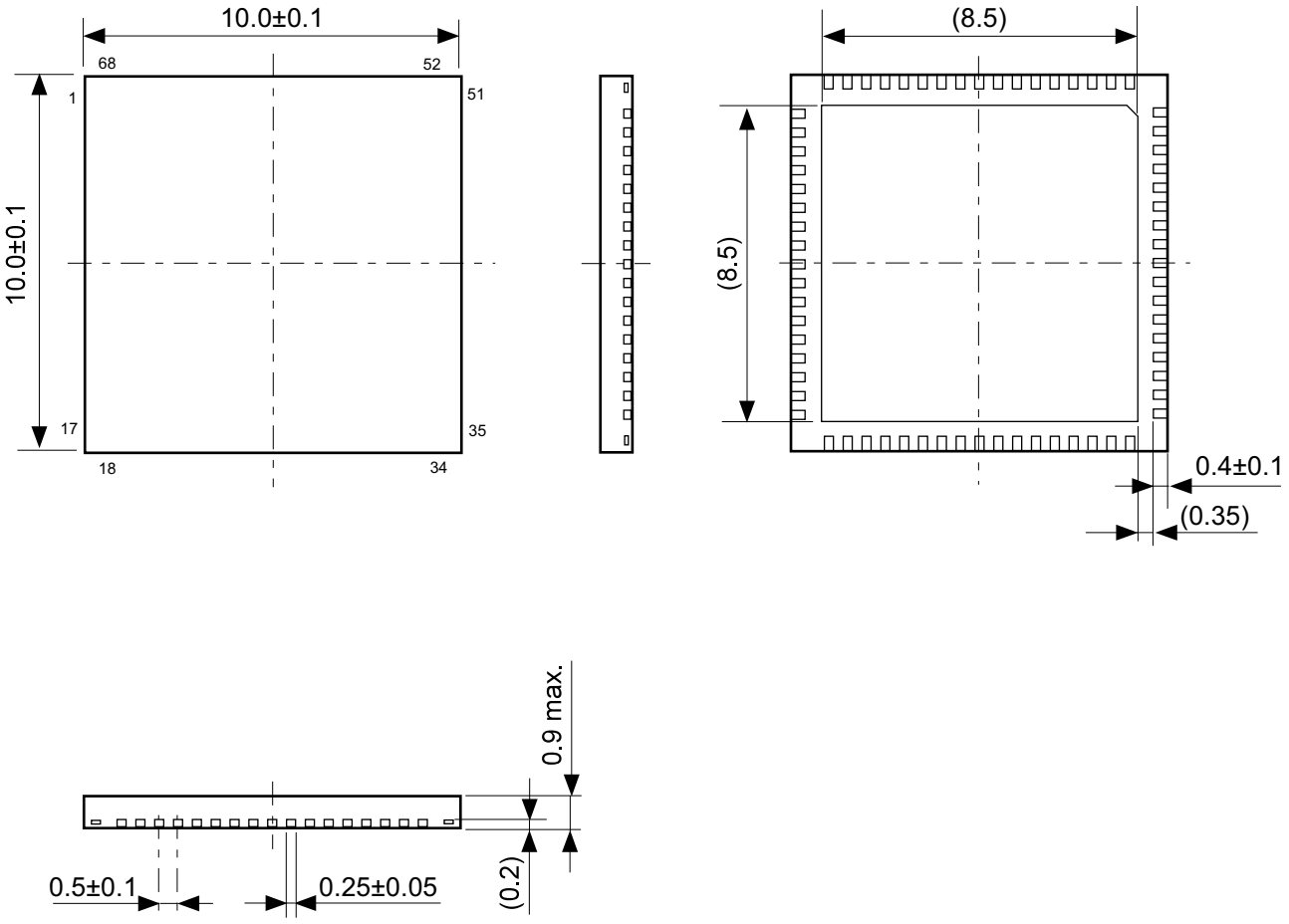
1.6 Avoid dealing with or storing products in an extremely arid environment.

2. “Absolute maximum ratings” should never be exceeded during use regardless of any change in external conditions. Otherwise, products may be damaged or destroyed. In no event shall ABLIC Inc. be liable for any failure in products or any secondary damage resulting from use at a value exceeding the absolute maximum ratings.

3. Products may experience failures due to accident or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy or prevention of erroneous action, to avoid extensive damage in the event of a failure. (If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)

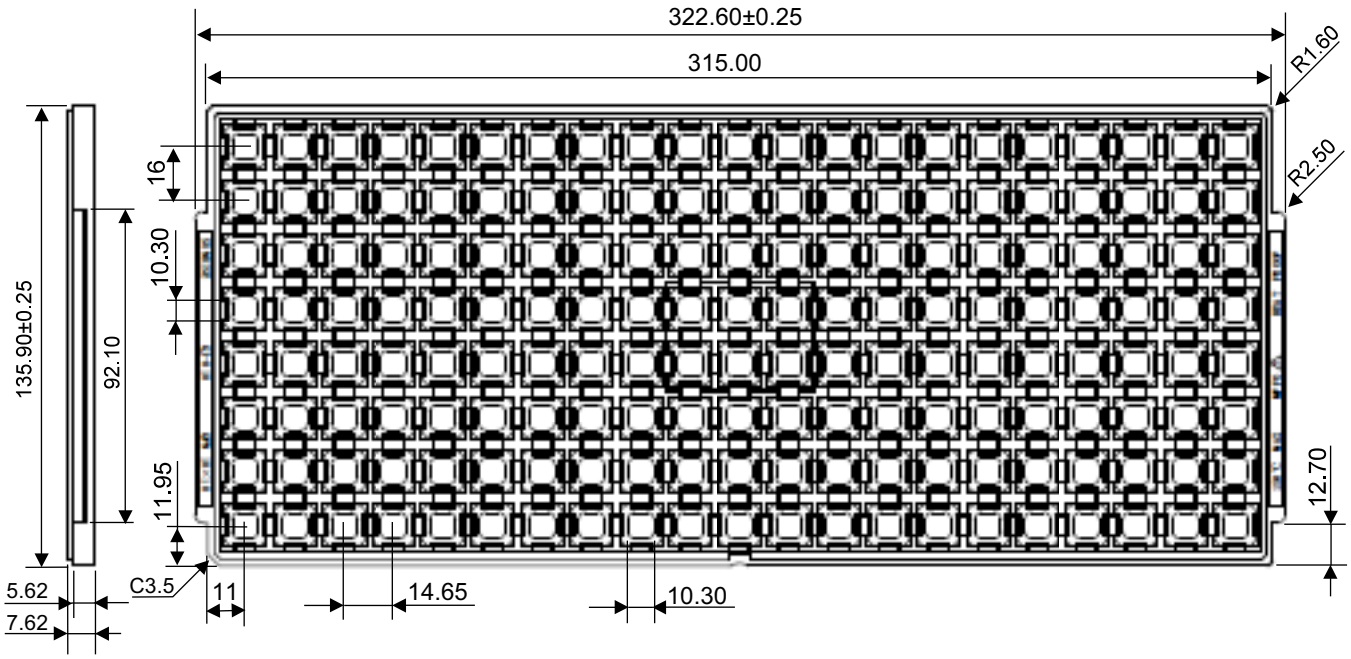
4. Products may experience failures or malfunction in poor surroundings, such as electrical leakage in products due to long-term use in high humidity, malfunctioning or permanent damage due to chemical reaction of products in corrosive environment or due to discharge by strongly charged object near products or due to excessive mechanical shock. To use products in radiation environment is not assumed. To use products near material easy to ignite may cause a fire due to its flammable package. Avoid using products in such environment or take appropriate countermeasures depending on the environment.

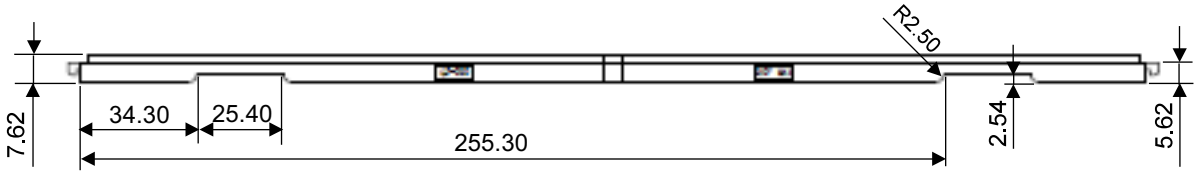
5. Products are not designed, manufactured, or warranted to be suitable for use where extremely high reliability is required (such as use in nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment). Inclusion of products in such application shall be fully at the risk of customers. ABLIC Inc. assumes no liability for applications assistance, customer product design, or performance.



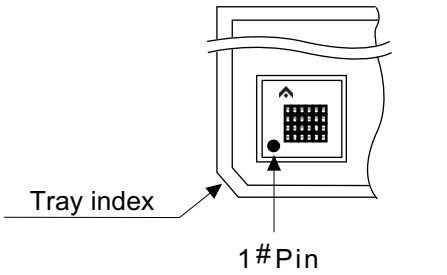
No. QN068-B-P-SD-1.0

TITLE	QFN68-B-PKG Dimensions
No.	QN068-B-P-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	



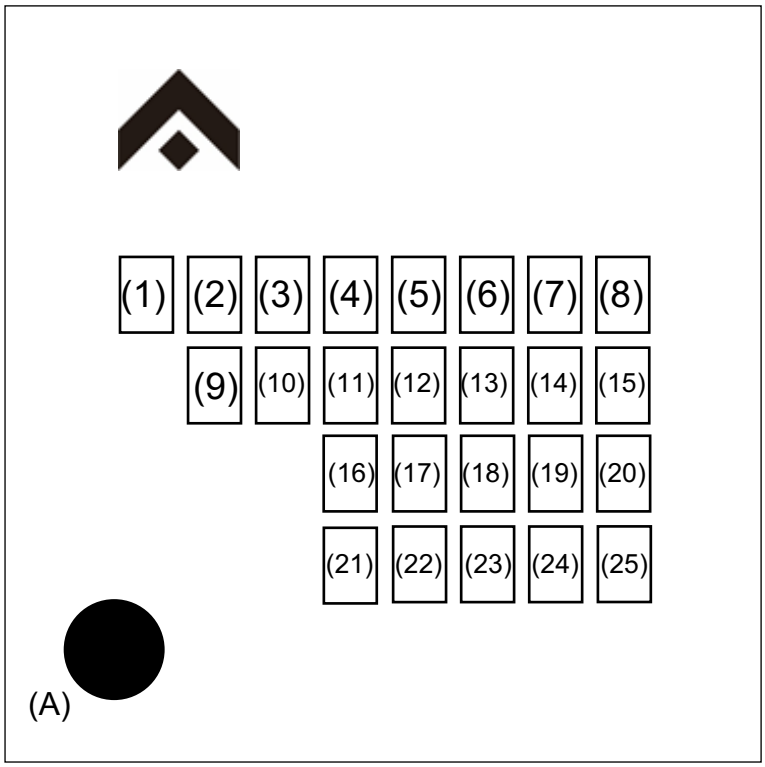


(Direction of IC in tray)



No. QN068-B-T-SD-1.0

TITLE	QFN68-B-Tray		
No.	QN068-B-T-SD-1.0		
ANGLE		QTY.	168
UNIT	mm		
ABLIC Inc.			



(1) to (10) : Product code

(11) , (12) : Quality control code

(13) : Year of assembly

(14) : Month of assembly

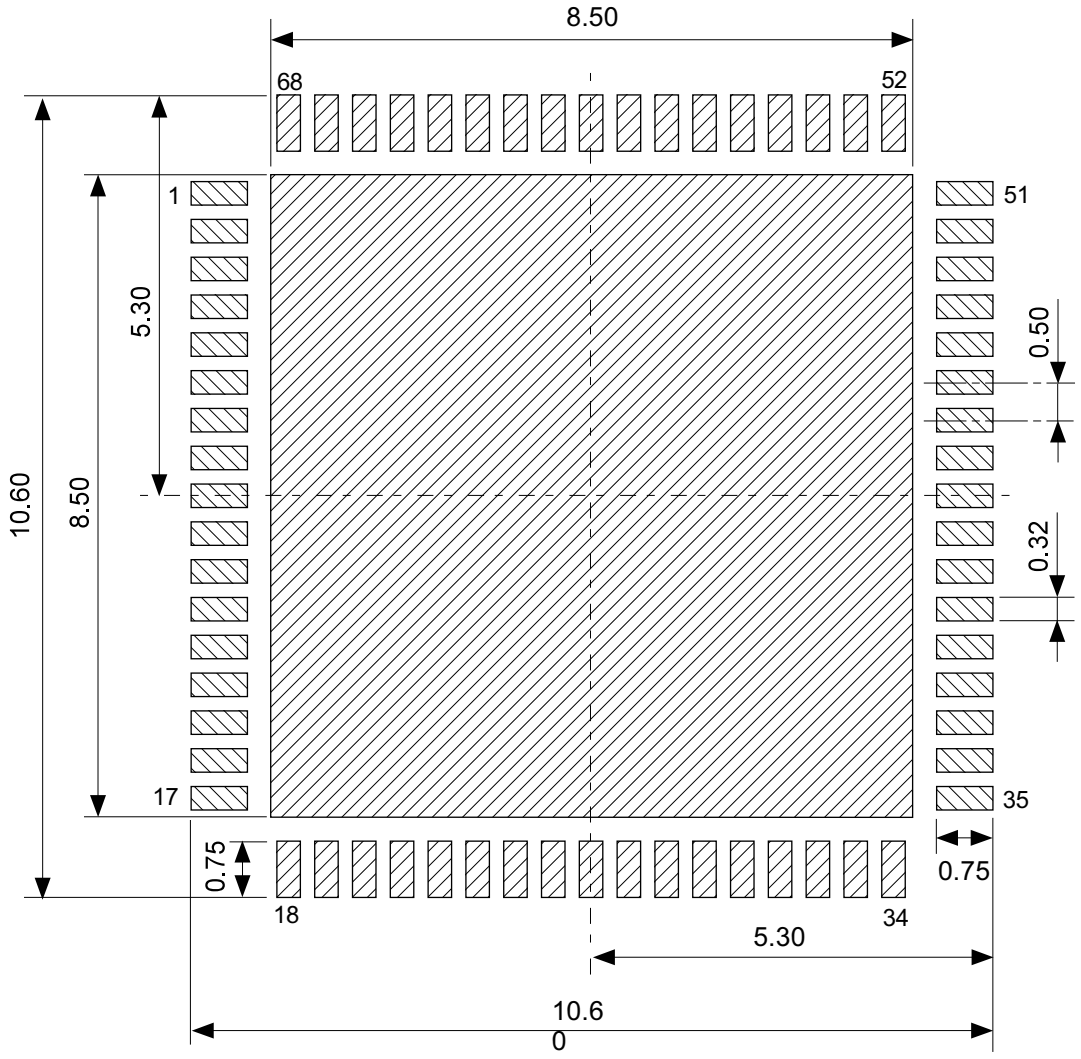
(15) : Week of assembly

(16) to (25) : Quality control code

(A) : 1-pin mark

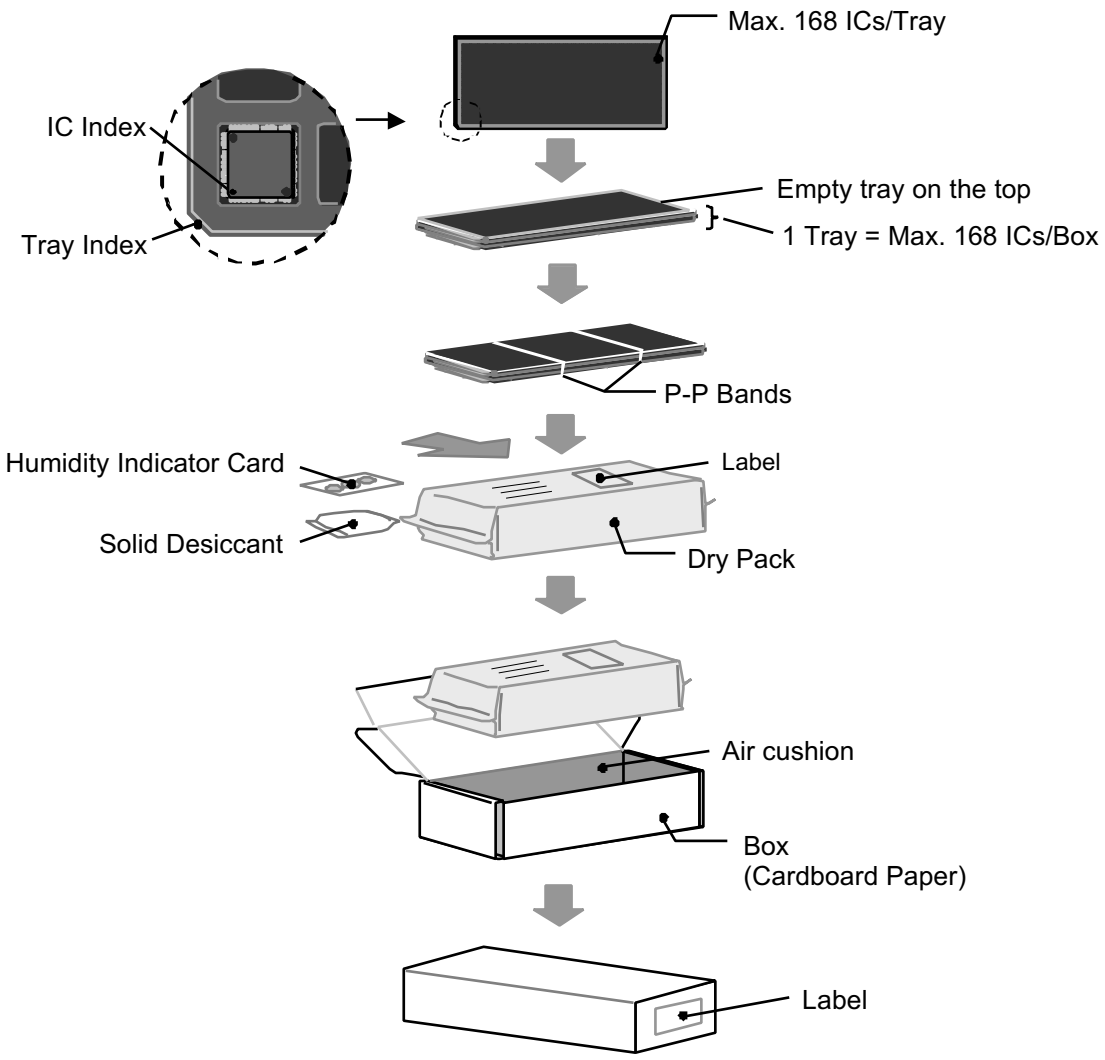
No. QN068-B-M-S1-1.0

TITLE	QFN68-B-Markings		
No.	QN068-B-M-S1-1.0		
ANGLE			
UNIT		TYPE	LASER
ABLIC Inc.			



No. QN068-B-L-SD-1.0

TITLE	QFN68-B -Land Recommendation
No.	QN068-B-L-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	



TITLE	QFN68-B -Packing Procedure
No.	QN068-B-K-SD-2.0
ANGLE	
UNIT	
ABLIC Inc.	

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