S-191AxxxxA Series

AUTOMOTIVE, 125°C OPERATION, 6 V, WINDOW VOLTAGE DETECTOR WITH FAST DETECTION RESPONSE AND MANUAL RESET FUNCTION

This IC, developed using CMOS technology, is a high-accuracy window voltage detector that detects undervoltage and overvoltage. The detection voltage and release voltage are fixed internally with an accuracy of ±1.5%.
Apart from the power supply pin, the detection voltage input pin (SENSE pin) is also prepared, so the output is stable even if the SENSE pin voltage (V_{SENSE}) falls to 0 V.
The release signal can be delayed by setting a capacitor externally, and the release delay time accuracy is ±15% (C_D = 3.3 nF). This IC also has a manual reset function. The manual reset function changes the comparator input voltage of the internal circuit, and the detector is forcibly put into the detection status. This enables a diagnosis of anomalies in the detector, such as erroneous release.
The output form is Nch open-drain output.

ABLIC Inc. offers FIT rate calculated based on actual customer usage conditions in order to support customer functional safety design.
For more information regarding our FIT rate calculation, contact our sales representatives.

Caution **This product can be used in vehicle equipment and in-vehicle equipment. Before using the product for these purposes, it is imperative to contact our sales representatives.**

■ Features

- Detection voltage: Undervoltage detection voltage 0.6 V to 4.9 V (0.05 V step); Overvoltage detection voltage 0.7 V to 5.5 V (0.05 V step)
- Detection voltage accuracy: Undervoltage detection voltage ±1.5%; Overvoltage detection voltage ±1.5%
- Hysteresis width selectable from "Available" / "Unavailable": "Available": 3.0%, 5.0%, 10.0%; "Unavailable": 0%
- Detection response time: 10.0 µs typ.
- Manual reset function: MR pin input logic: Active "L"
- Release delay time accuracy: ±15% (C_D = 3.3 nF)
- Output form: Nch open-drain output
- Current consumption: 1.5 µA typ.
- Operation voltage range: 2.5 V to 6.0 V
- Operation temperature range: Ta = –40°C to +125°C
- Lead-free (Sn 100%), halogen-free
- AEC-Q100 qualified*1

***1.** Contact our sales representatives for details.

■ Applications

- Overvoltage detection of power supply for automotive electric component
- Voltage monitoring of automotive ECUs, ADAS and other systems that require failure detection
- For automotive use (engine, transmission, suspension, ABS, related-devices for EV / HEV / PHEV, etc.)

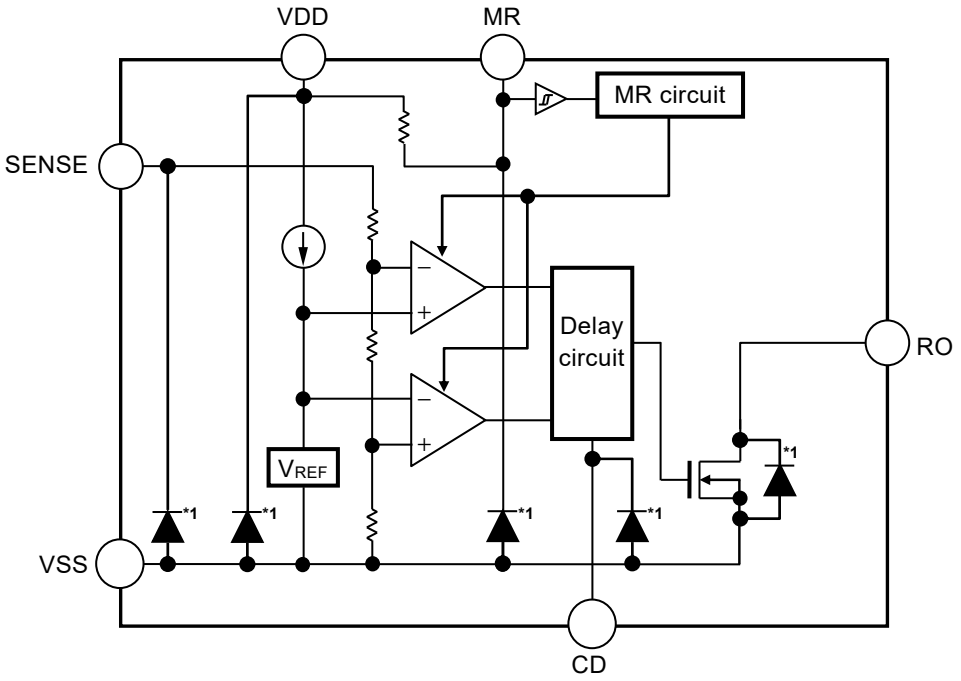
■ Packages

- SOT-23-6
- HSNT-8(1616)B

■ Block Diagrams

1. SOT-23-6

1. 1 Hysteresis width "Unavailable"

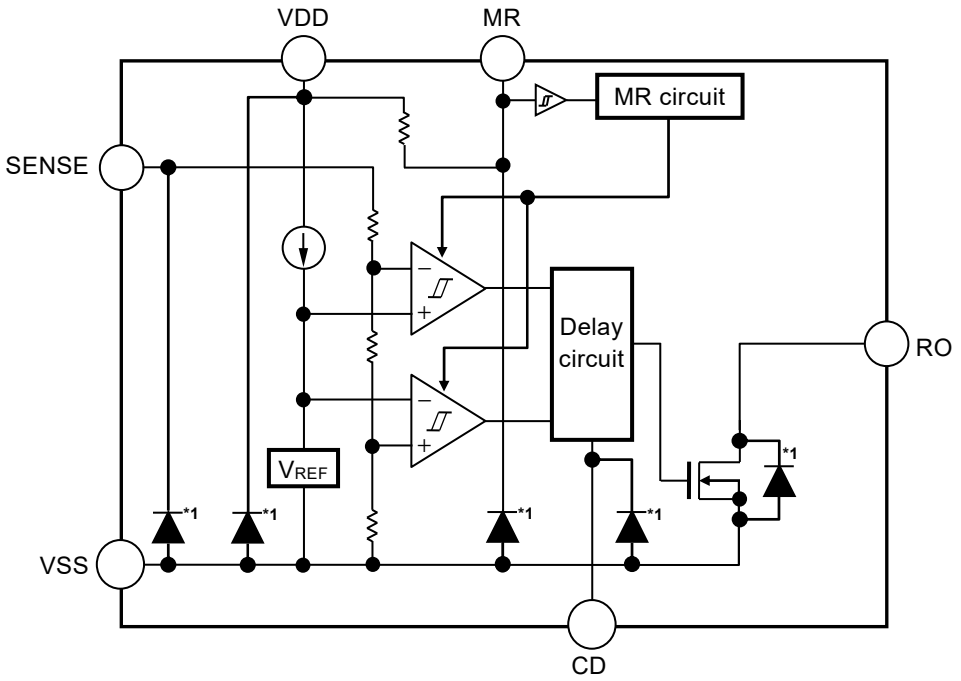


***1.** Parasitic diode

Figure 1

Product Name	Hysteresis Width (V_{UVHYS}, V_{OVHYS})	MR Pin Input Logic	RO Pin Output Form	RO Pin Output Logic
S-191A0xxxA	0%	Active "L"	Nch open-drain output	Active "L"
S-191A1xxxA	0%	Active "L"	Nch open-drain output	Active "L"
S-191A2xxxA	0%	Active "L"	Nch open-drain output	Active "L"
S-191A3xxxA	0%	Active "L"	Nch open-drain output	Active "L"
S-191A4xxxA	0%	Active "L"	Nch open-drain output	Active "L"

1. 2 Hysteresis width "Available"



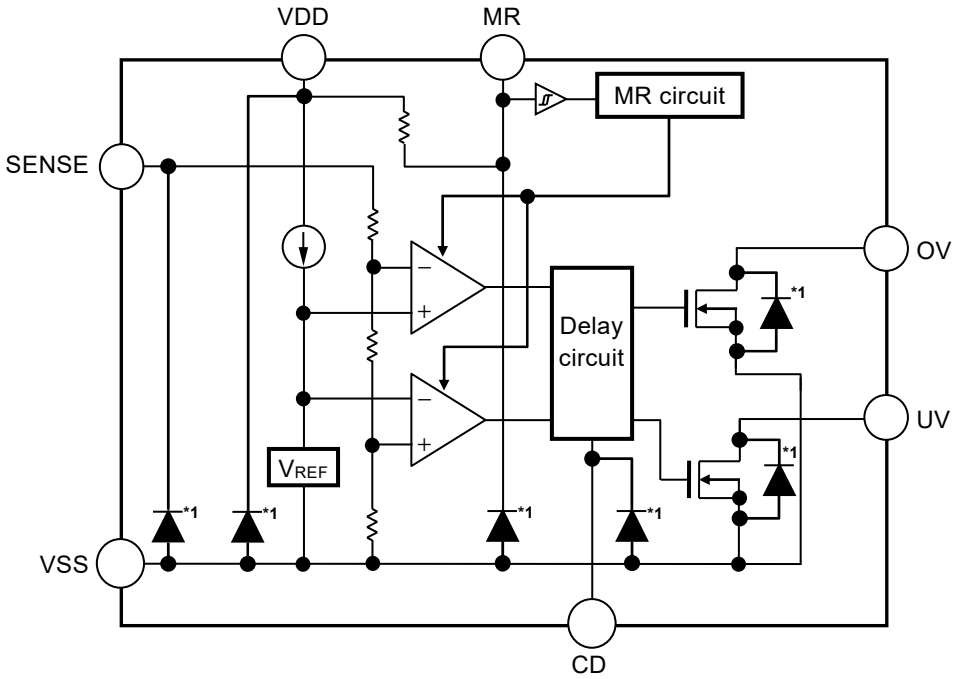
***1.** Parasitic diode

Figure 2

Product Name	Hysteresis Width (V_{UVHYS}, V_{OVHYS})	MR Pin Input Logic	RO Pin Output Form	RO Pin Output Logic
S-191AAxxxA	3.0%	Active "L"	Nch open-drain output	Active "L"
S-191ABxxxA	3.0%	Active "L"	Nch open-drain output	Active "L"
S-191ACxxxA	3.0%	Active "L"	Nch open-drain output	Active "L"
S-191ADxxxA	3.0%	Active "L"	Nch open-drain output	Active "L"
S-191AExxxA	3.0%	Active "L"	Nch open-drain output	Active "L"
S-191AGxxxA	5.0%	Active "L"	Nch open-drain output	Active "L"
S-191AHxxxA	5.0%	Active "L"	Nch open-drain output	Active "L"
S-191AJxxxA	5.0%	Active "L"	Nch open-drain output	Active "L"
S-191AKxxxA	5.0%	Active "L"	Nch open-drain output	Active "L"
S-191ALxxxA	5.0%	Active "L"	Nch open-drain output	Active "L"
S-191ANxxxA	10.0%	Active "L"	Nch open-drain output	Active "L"
S-191APxxxA	10.0%	Active "L"	Nch open-drain output	Active "L"
S-191AQxxxA	10.0%	Active "L"	Nch open-drain output	Active "L"
S-191ARxxxA	10.0%	Active "L"	Nch open-drain output	Active "L"
S-191ASxxxA	10.0%	Active "L"	Nch open-drain output	Active "L"

2. HSNT-8(1616)B

2. 1 Hysteresis width "Unavailable"

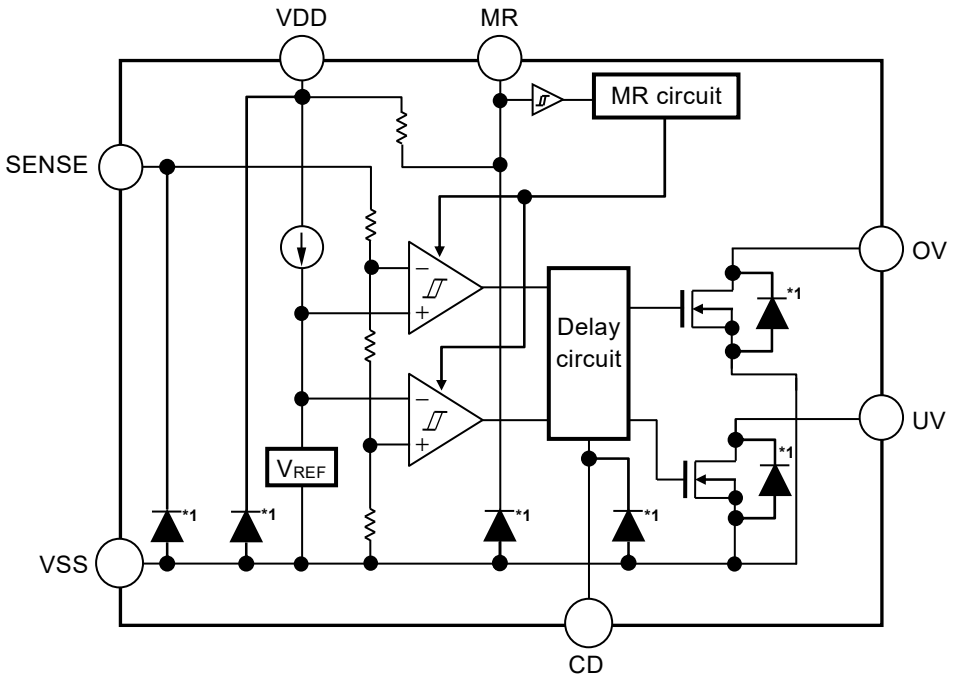


***1.** Parasitic diode

Figure 3

Product Name	Hysteresis Width (V_{UVHYS}, V_{OVHYS})	MR Pin Input Logic	UV, OV Pin Output Form	UV, OV Pin Output Logic
S-191A0xxxA	0%	Active "L"	Nch open-drain output	Active "L"
S-191A1xxxA	0%	Active "L"	Nch open-drain output	Active "L"
S-191A2xxxA	0%	Active "L"	Nch open-drain output	Active "L"
S-191A3xxxA	0%	Active "L"	Nch open-drain output	Active "L"
S-191A4xxxA	0%	Active "L"	Nch open-drain output	Active "L"

2. 2 Hysteresis width "Available"



***1.** Parasitic diode

Figure 4

Product Name	Hysteresis Width (V_{UVHYS}, V_{OVHYS})	MR Pin Input Logic	UV, OV Pin Output Form	UV, OV Pin Output Logic
S-191AAxxxA	3.0%	Active "L"	Nch open-drain output	Active "L"
S-191ABxxxA	3.0%	Active "L"	Nch open-drain output	Active "L"
S-191ACxxxA	3.0%	Active "L"	Nch open-drain output	Active "L"
S-191ADxxxA	3.0%	Active "L"	Nch open-drain output	Active "L"
S-191AExxxA	3.0%	Active "L"	Nch open-drain output	Active "L"
S-191AGxxxA	5.0%	Active "L"	Nch open-drain output	Active "L"
S-191AHxxxA	5.0%	Active "L"	Nch open-drain output	Active "L"
S-191AJxxxA	5.0%	Active "L"	Nch open-drain output	Active "L"
S-191AKxxxA	5.0%	Active "L"	Nch open-drain output	Active "L"
S-191ALxxxA	5.0%	Active "L"	Nch open-drain output	Active "L"
S-191ANxxxA	10.0%	Active "L"	Nch open-drain output	Active "L"
S-191APxxxA	10.0%	Active "L"	Nch open-drain output	Active "L"
S-191AQxxxA	10.0%	Active "L"	Nch open-drain output	Active "L"
S-191ARxxxA	10.0%	Active "L"	Nch open-drain output	Active "L"
S-191ASxxxA	10.0%	Active "L"	Nch open-drain output	Active "L"

■ AEC-Q100 Qualified

This IC supports AEC-Q100 for operation temperature grade 1.
Contact our sales representatives for details of AEC-Q100 reliability specification.

■ Product Name Structure

1. Product name

S-191A xx xx A - xxxx U 7

Environmental code
U: Lead-free (Sn 100%), halogen-free

Package abbreviation and IC packing specifications*1
M6T1: SOT-23-6, Tape
A8T7: HSNT-8(1616)B, Tape

Operation temperature
A: Ta = −40°C to +125°C

Overvoltage detection voltage*2, *3, *4
07 to 55
(e.g., when the overvoltage detection voltage is 0.7 V,
it is expressed as 07.
when the overvoltage detection voltage is 4.9 V,
it is expressed as 49.)

Hysteresis width*3, undervoltage detection voltage*3, *4
06 to 49, A6 to E9, G6 to L9, N6 to S9
(e.g., when the hysteresis width (V_{UVHYS}, V_{OVHYS}) is 0%,
the undervoltage detection voltage is 0.6 V,
it is expressed as 06.
when the hysteresis width (V_{UVHYS}, V_{OVHYS}) is 3%,
the undervoltage detection voltage is 1.4 V,
it is expressed as B4.
when the hysteresis width (V_{UVHYS}, V_{OVHYS}) is 5%,
the undervoltage detection voltage is 4.9 V,
it is expressed as L9.
when the hysteresis width (V_{UVHYS}, V_{OVHYS}) is 10%,
the undervoltage detection voltage is 2.5 V,
it is expressed as Q5.)

***1.** Refer to the tape drawing.
***2.** Set the overvoltage detection voltage higher than the undervoltage detection voltage.
***3.** For details on hysteresis width and undervoltage detection voltage, refer to **Table 1** and "**2. Function list of product types**". When determining the overvoltage detection voltage, undervoltage detection voltage and hysteresis width, refer to "**3. Relationship between overvoltage detection voltage, undervoltage detection voltage and hysteresis width**" in "**■ Usage Precautions**".
***4.** If you request the product which has 0.05 V step, contact our sales representatives.

Table 1 Relationship Between Hysteresis Width, Undervoltage Detection Voltage and Product Name

Hysteresis Width (V_{UVHYS}, V_{OVHYS})	Undervoltage Detection Voltage (V_{UVDET})	Product Name*1
0%	0.60 V to 0.95 V	S-191A0xxxA
0%	1.00 V to 1.95 V	S-191A1xxxA
0%	2.00 V to 2.95 V	S-191A2xxxA
0%	3.00 V to 3.95 V	S-191A3xxxA
0%	4.00 V to 4.90 V	S-191A4xxxA
3.0%	0.60 V to 0.95 V	S-191AAxxxA
3.0%	1.00 V to 1.95 V	S-191ABxxxA
3.0%	2.00 V to 2.95 V	S-191ACxxxA
3.0%	3.00 V to 3.95 V	S-191ADxxxA
3.0%	4.00 V to 4.90 V	S-191AExxxA
5.0%	0.60 V to 0.95 V	S-191AGxxxA
5.0%	1.00 V to 1.95 V	S-191AHxxxA
5.0%	2.00 V to 2.95 V	S-191AJxxxA
5.0%	3.00 V to 3.95 V	S-191AKxxxA
5.0%	4.00 V to 4.90 V	S-191ALxxxA
10.0%	0.60 V to 0.95 V	S-191ANxxxA
10.0%	1.00 V to 1.95 V	S-191APxxxA
10.0%	2.00 V to 2.95 V	S-191AQxxxA
10.0%	3.00 V to 3.95 V	S-191ARxxxA
10.0%	4.00 V to 4.90 V	S-191ASxxxA

***1.** The first digit symbol after S-191A indicates the integer digits of hysteresis width and undervoltage detection voltage. The second digit symbol after S-191A indicates the decimal place of the undervoltage detection voltage.

Example: If the hysteresis width is 0% and the undervoltage detection voltage is 0.6 V, it is described as S-191A06.
If the hysteresis width is 3% and the undervoltage detection voltage is 1.4 V, it is described as S-191AB4.
If the hysteresis width is 5% and the undervoltage detection voltage is 4.9 V, it is described as S-191AL9.
If the hysteresis width is 10% and the undervoltage detection voltage is 2.5 V, it is described as S-191AQ5.

Remark If you request the product which has 0.05 V step, contact our sales representatives.

2. Function list of product types

Table 2

Product Name	Hysteresis Width (V_{UVHYS}, V_{OVHYS})	MR Pin Input Logic	RO / UV, OV Pin Output Form	RO / UV, OV Pin Output Logic
S-191A0xxxA	0%	Active "L"	Nch open-drain output	Active "L"
S-191A1xxxA	0%	Active "L"	Nch open-drain output	Active "L"
S-191A2xxxA	0%	Active "L"	Nch open-drain output	Active "L"
S-191A3xxxA	0%	Active "L"	Nch open-drain output	Active "L"
S-191A4xxxA	0%	Active "L"	Nch open-drain output	Active "L"
S-191AAxxxA	3.0%	Active "L"	Nch open-drain output	Active "L"
S-191ABxxxA	3.0%	Active "L"	Nch open-drain output	Active "L"
S-191ACxxxA	3.0%	Active "L"	Nch open-drain output	Active "L"
S-191ADxxxA	3.0%	Active "L"	Nch open-drain output	Active "L"
S-191AExxxA	3.0%	Active "L"	Nch open-drain output	Active "L"
S-191AGxxxA	5.0%	Active "L"	Nch open-drain output	Active "L"
S-191AHxxxA	5.0%	Active "L"	Nch open-drain output	Active "L"
S-191AJxxxA	5.0%	Active "L"	Nch open-drain output	Active "L"
S-191AKxxxA	5.0%	Active "L"	Nch open-drain output	Active "L"
S-191ALxxxA	5.0%	Active "L"	Nch open-drain output	Active "L"
S-191ANxxxA	10.0%	Active "L"	Nch open-drain output	Active "L"
S-191APxxxA	10.0%	Active "L"	Nch open-drain output	Active "L"
S-191AQxxxA	10.0%	Active "L"	Nch open-drain output	Active "L"
S-191ARxxxA	10.0%	Active "L"	Nch open-drain output	Active "L"
S-191ASxxxA	10.0%	Active "L"	Nch open-drain output	Active "L"

3. Packages

Table 3 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
SOT-23-6	MP006-A-P-SD	MP006-A-C-SD	MP006-A-R-SD	–
HSNT-8(1616)B	PY008-B-P-SD	PY008-B-C-SD	PY008-B-R-SD	PY008-B-L-SD

■ Pin Configurations

1. SOT-23-6

Top view

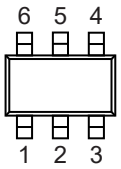


Figure 5

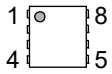
Table 4

Pin No.	Symbol	Description
1	SENSE	Detection voltage input pin
2	VDD	Voltage input pin
3	MR	Manual reset pin
4	RO	Voltage detection output pin
5	VSS	GND pin
6	CD*1	Connection pin for release delay time adjustment capacitor

***1.** Connect a capacitor between the CD pin and the VSS pin. The release delay time can be adjusted according to the capacitance.

2. HSNT-8(1616)B

Top view



Bottom view

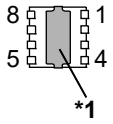


Figure 6

Table 5

Pin No.	Symbol	Description
1	MR	Manual reset pin
2	VDD	Voltage input pin
3	NC*2	No connection
4	SENSE	Detection voltage input pin
5	CD*3	Connection pin for release delay time adjustment capacitor
6	VSS	GND pin
7	UV	Undervoltage detection output pin
8	OV	Overvoltage detection output pin

***1.** Connect the heat sink of backside at shadowed area to the board, and set electric potential GND.
However, do not use it as the function of electrode.

***2.** The NC pin is electrically open.
The NC pin can be connected to the VDD pin or the VSS pin.

***3.** Connect a capacitor between the CD pin and the VSS pin. The release delay time can be adjusted according to the capacitance.

■ Absolute Maximum Ratings

Table 6

(Ta = –40°C to +125°C unless otherwise specified)

Item		Symbol	Absolute Maximum Rating	Unit
Power supply voltage		V_{DD}	V_{SS} – 0.3 to V_{SS} + 7.0	V
SENSE pin voltage		V_{SENSE}	V_{SS} – 0.3 to V_{SS} + 7.0	V
CD pin input voltage		V_{CD}	V_{SS} – 0.3 to V_{DD} + 0.3 ≤ V_{SS} + 7.0	V
MR pin input voltage		V_{MR}	V_{SS} – 0.3 to V_{DD} + 0.3 ≤ V_{SS} + 7.0	V
Output voltage	SOT-23-6	V_{RO}	V_{SS} – 0.3 to V_{SS} + 7.0	V
	HSNT-8(1616)B	V_{UV}	V_{SS} – 0.3 to V_{SS} + 7.0	V
		V_{OV}	V_{SS} – 0.3 to V_{SS} + 7.0	V
Output current	SOT-23-6	I_{RO}	25	mA
	HSNT-8(1616)B	I_{UV}	25	mA
		I_{OV}	25	mA
Junction temperature		T_j	–40 to +150	°C
Operation ambient temperature		T_{opr}	–40 to +125	°C
Storage temperature		T_{stg}	–40 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 7

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	SOT-23-6	Board A	–	159	–	°C/W
			Board B	–	124	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W
		HSNT-8(1616)B	Board A	–	214	–	°C/W
			Board B	–	172	–	°C/W
			Board C	–	52	–	°C/W
			Board D	–	55	–	°C/W
			Board E	–	43	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

1. SOT-23-6

Table 8

(Ta = –40°C to +125°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Undervoltage detection voltage*1	V_{UVDET}	V_{DD} = 5.0 V, 0.6 V ≤ $V_{UVDET(S)}$ ≤ 4.9 V	$V_{UVDET(S)}$ × 0.985	$V_{UVDET(S)}$	$V_{UVDET(S)}$ × 1.015	V	1
Overvoltage detection voltage*2	V_{OVDET}	V_{DD} = 5.0 V, 0.7 V ≤ $V_{OVDET(S)}$ ≤ 5.5 V	$V_{OVDET(S)}$ × 0.985	$V_{OVDET(S)}$	$V_{OVDET(S)}$ × 1.015	V	1
Undervoltage hysteresis width*3	V_{UVHYS}	S-191A06xx to S-191A49xx (V_{UVHYS} = 0%)	–	V_{UVDET} × 0.00	–	V	1
		S-191AA6xx to S-191AE9xx (V_{UVHYS} = 3.0%)	V_{UVDET} × 0.02	V_{UVDET} × 0.03	V_{UVDET} × 0.04	V	1
		S-191AG6xx to S-191AL9xx (V_{UVHYS} = 5.0%)	V_{UVDET} × 0.04	V_{UVDET} × 0.05	V_{UVDET} × 0.06	V	1
		S-191AN6xx to S-191AS9xx (V_{UVHYS} = 10.0%)	V_{UVDET} × 0.09	V_{UVDET} × 0.10	V_{UVDET} × 0.11	V	1
Overvoltage hysteresis width*3	V_{OVHYS}	S-191A06xx to S-191A49xx (V_{OVHYS} = 0%)	–	V_{OVDET} × 0.00	–	V	1
		S-191AA6xx to S-191AE9xx (V_{OVHYS} = 3.0%)	V_{OVDET} × 0.02	V_{OVDET} × 0.03	V_{OVDET} × 0.04	V	1
		S-191AG6xx to S-191AL9xx (V_{OVHYS} = 5.0%)	V_{OVDET} × 0.04	V_{OVDET} × 0.05	V_{OVDET} × 0.06	V	1
		S-191AN6xx to S-191AS9xx (V_{OVHYS} = 10.0%)	V_{OVDET} × 0.09	V_{OVDET} × 0.10	V_{OVDET} × 0.11	V	1
Current consumption	I_{SS1}	V_{DD} = 5.0 V, V_{SENSE} = ($V_{UVREL(S)}$ + $V_{OVREL(S)}$) / 2	–	1.5	2.6	μA	5
Operation voltage	V_{DD}	–	2.5	–	6.0	V	1
Output current	I_{OUT}	RO pin Nch driver, V_{DD} = 2.5 V, V_{DS}*4 = 0.5 V, V_{SENSE} = $V_{UVDET(S)}$ – 0.5 V	2.50	–	–	mA	2
Leakage current	I_{LEAK}	RO pin Nch driver, V_{DD} = 6.0 V, V_{RO} = 6.0 V, V_{SENSE} = ($V_{UVREL(S)}$ + $V_{OVREL(S)}$) / 2	–	–	0.20	μA	2
Detection response time*5	t_{RESET}	–	–	10.0	40.0	μs	3
Release delay time*6	t_{DELAY}	C_D = 3.3 nF	8.5	10.0	11.5	ms	3
SENSE pin resistance	R_{SENSE}	–	3.3	–	42.5	MΩ	5
MR pin input voltage "H"	V_{MRH}	–	2.0	–	–	V	4
MR pin input voltage "L"	V_{MRL}	–	–	–	0.6	V	4
MR pin resistance	R_{MR}	–	0.91	2.20	5.71	MΩ	4
CD pin discharge ON resistance	R_{CDD}	V_{DD} = 2.5 V, V_{CD} = 0.7 V	0.15	–	0.90	kΩ	–

***1.** V_{UVDET}: Actual undervoltage detection voltage value, $V_{UVDET(S)}$: Set undervoltage detection voltage value

***2.** V_{OVDET}: Actual overvoltage detection voltage value, $V_{OVDET(S)}$: Set overvoltage detection voltage value

***3.** V_{UVREL}: Actual undervoltage release voltage value, $V_{UVREL(S)}$: Set undervoltage release voltage value
V_{OVREL}: Actual overvoltage release voltage value, $V_{OVREL(S)}$: Set overvoltage release voltage value
V_{UVREL} and V_{OVREL} are as follows.
Hysteresis width "Unavailable": $V_{UVREL} = V_{UVDET}$, $V_{OVREL} = V_{OVDET}$
Hysteresis width "Available": $V_{UVREL} = V_{UVDET} + V_{UVHYS}$, $V_{OVREL} = V_{OVDET} – V_{OVHYS}$

***4.** V_{DS}: Drain-to-source voltage of the output transistor

***5.** The time period from when the pulse voltage of $V_{UVDET(S)}$ + 0.5 V → $V_{UVDET(S)}$ – 0.5 V or $V_{OVDET(S)}$ – 0.5 V → $V_{OVDET(S)}$ + 0.5 V is applied to the SENSE pin after V_{SENSE} reaches the release voltage once, until V_{UV} or V_{OV} reaches 50% of V_{DD}. It is the time period for V_{UV} or V_{OV} to reach 50% of V_{DD} after applying a pulse voltage of ($V_{UVREL(S)}$ + $V_{OVREL(S)}$) / 2 → $V_{UVREL(S)}$ – 0.5 V or ($V_{UVREL(S)}$ + $V_{OVREL(S)}$) / 2 → $V_{OVDET(S)}$ + 0.5 V to the SENSE pin, in case of $V_{OVDET(S)} – V_{UVDET(S)}$ ≤ 0.5 V.

***6.** The time period from when the pulse voltage of $V_{UVREL(S)}$ – 0.5 V → $V_{UVREL(S)}$ × 1.03 V or $V_{OVREL(S)}$ + 0.5 V → $V_{OVREL(S)}$ × 0.97 V is applied to the SENSE pin to when V_{UV} or V_{OV} reaches 50% of V_{DD}.

2. HSNT-8(1616)B

Table 9

(Ta = –40°C to +125°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Undervoltage detection voltage*1	V_{UVDET}	V_{DD} = 5.0 V, 0.6 V ≤ $V_{UVDET(S)}$ ≤ 4.9 V	$V_{UVDET(S)}$ × 0.985	$V_{UVDET(S)}$	$V_{UVDET(S)}$ × 1.015	V	6
Overvoltage detection voltage*2	V_{OVDET}	V_{DD} = 5.0 V, 0.7 V ≤ $V_{OVDET(S)}$ ≤ 5.5 V	$V_{OVDET(S)}$ × 0.985	$V_{OVDET(S)}$	$V_{OVDET(S)}$ × 1.015	V	6
Undervoltage hysteresis width*3	V_{UVHYS}	S-191A06xx to S-191A49xx (V_{UVHYS} = 0%)	–	V_{UVDET} × 0.00	–	V	6
		S-191AA6xx to S-191AE9xx (V_{UVHYS} = 3.0%)	V_{UVDET} × 0.02	V_{UVDET} × 0.03	V_{UVDET} × 0.04	V	6
		S-191AG6xx to S-191AL9xx (V_{UVHYS} = 5.0%)	V_{UVDET} × 0.04	V_{UVDET} × 0.05	V_{UVDET} × 0.06	V	6
		S-191AN6xx to S-191AS9xx (V_{UVHYS} = 10.0%)	V_{UVDET} × 0.09	V_{UVDET} × 0.10	V_{UVDET} × 0.11	V	6
Overvoltage hysteresis width*3	V_{OVHYS}	S-191A06xx to S-191A49xx (V_{OVHYS} = 0%)	–	V_{OVDET} × 0.00	–	V	6
		S-191AA6xx to S-191AE9xx (V_{OVHYS} = 3.0%)	V_{OVDET} × 0.02	V_{OVDET} × 0.03	V_{OVDET} × 0.04	V	6
		S-191AG6xx to S-191AL9xx (V_{OVHYS} = 5.0%)	V_{OVDET} × 0.04	V_{OVDET} × 0.05	V_{OVDET} × 0.06	V	6
		S-191AN6xx to S-191AS9xx (V_{OVHYS} = 10.0%)	V_{OVDET} × 0.09	V_{OVDET} × 0.10	V_{OVDET} × 0.11	V	6
Current consumption	I_{SS1}	V_{DD} = 5.0 V, V_{SENSE} = ($V_{UVREL(S)}$ + $V_{OVREL(S)}$) / 2	–	1.5	2.6	μA	10
Operation voltage	V_{DD}	–	2.5	–	6.0	V	6
Output current	I_{OUT}	UV pin Nch driver, V_{DD} = 2.5 V, V_{DS}*4 = 0.5 V, V_{SENSE} = $V_{UVDET(S)}$ – 0.5 V	2.50	–	–	mA	7
		OV pin Nch driver, V_{DD} = 2.5 V, V_{DS}*4 = 0.5 V, V_{SENSE} = $V_{OVDET(S)}$ + 0.5 V	2.50	–	–	mA	7
Leakage current	I_{LEAK}	UV pin Nch driver, V_{DD} = 6.0 V, V_{UV} = 6.0 V, V_{SENSE} = 6.0 V	–	–	0.10	μA	7
		OV pin Nch driver, V_{DD} = 6.0 V, V_{OV} = 6.0 V, V_{SENSE} = 0 V	–	–	0.10	μA	7
Detection response time*5	t_{RESET}	–	–	10.0	40.0	μs	8
Release delay time*6	t_{DELAY}	C_D = 3.3 nF	8.5	10.0	11.5	ms	8
SENSE pin resistance	R_{SENSE}	–	3.3	–	42.5	MΩ	10
MR pin input voltage "H"	V_{MRH}	–	2.0	–	–	V	9
MR pin input voltage "L"	V_{MRL}	–	–	–	0.6	V	9
MR pin resistance	R_{MR}	–	0.91	2.20	5.71	MΩ	9
CD pin discharge ON resistance	R_{CDD}	V_{DD} = 2.5 V, V_{CD} = 0.7 V	0.15	–	0.90	kΩ	–

***1.** V_{UVDET}: Actual undervoltage detection voltage value, $V_{UVDET(S)}$: Set undervoltage detection voltage value

***2.** V_{OVDET}: Actual overvoltage detection voltage value, $V_{OVDET(S)}$: Set overvoltage detection voltage value

***3.** V_{UVREL}: Actual undervoltage release voltage value, $V_{UVREL(S)}$: Set undervoltage release voltage value
V_{OVREL}: Actual overvoltage release voltage value, $V_{OVREL(S)}$: Set overvoltage release voltage value
V_{UVREL} and V_{OVREL} are as follows.
Hysteresis width "Unavailable": $V_{UVREL} = V_{UVDET}$, $V_{OVREL} = V_{OVDET}$
Hysteresis width "Available": $V_{UVREL} = V_{UVDET} + V_{UVHYS}$, $V_{OVREL} = V_{OVDET} – V_{OVHYS}$

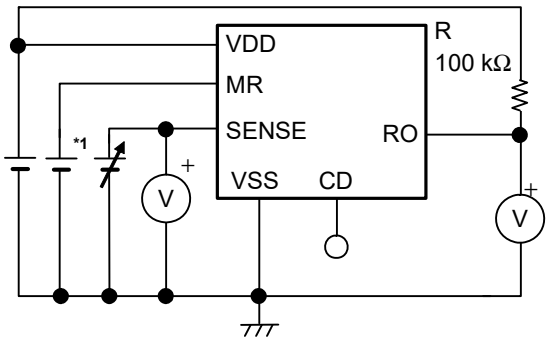
***4.** V_{DS}: Drain-to-source voltage of the output transistor

***5.** The time period from when the pulse voltage of $V_{UVDET(S)}$ + 0.5 → $V_{UVDET(S)}$ – 0.5 V or $V_{OVDET(S)}$ – 0.5 V → $V_{OVDET(S)}$ + 0.5 V is applied to the SENSE pin after V_{SENSE} reaches the release voltage once, until V_{UV} or V_{OV} reaches 50% of V_{DD}.

***6.** The time period from when the pulse voltage of $V_{UVREL(S)}$ – 0.5 V → $V_{UVREL(S)}$ × 1.03 V or $V_{OVREL(S)}$ + 0.5 V → $V_{OVREL(S)}$ × 0.97 V is applied to the SENSE pin to when V_{UV} or V_{OV} reaches 50% of V_{DD}.

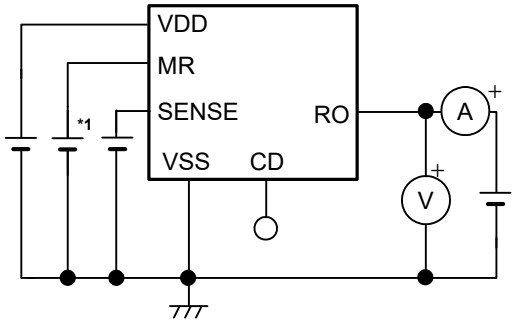
■ Test Circuits

1. SOT-23-6



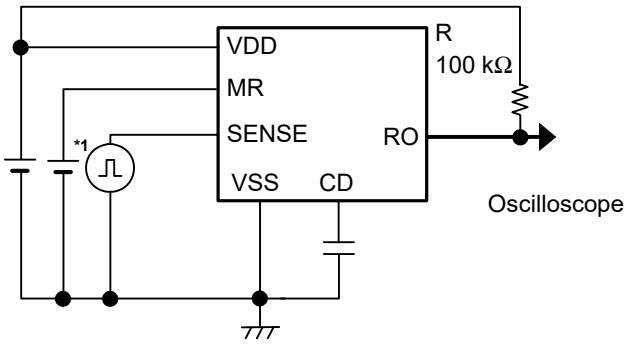
***1** Set to V_{DD}

Figure 7 Test Circuit 1



***1** Set to V_{DD}

Figure 8 Test Circuit 2



***1** Set to V_{DD}

Figure 9 Test Circuit 3

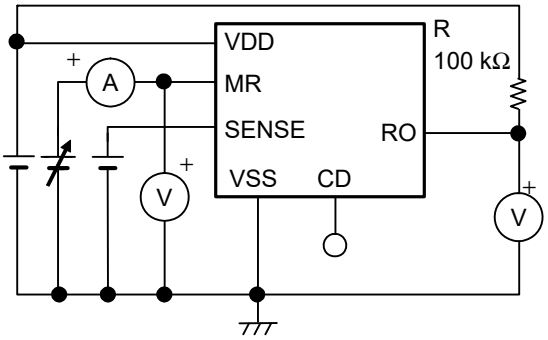
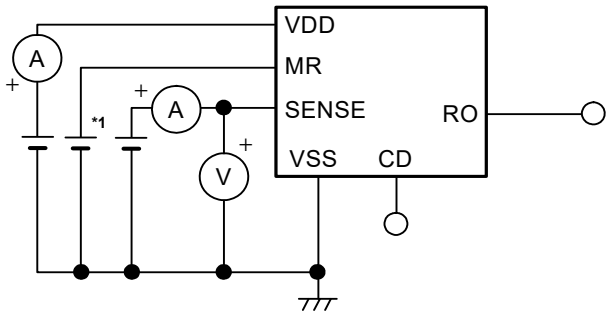


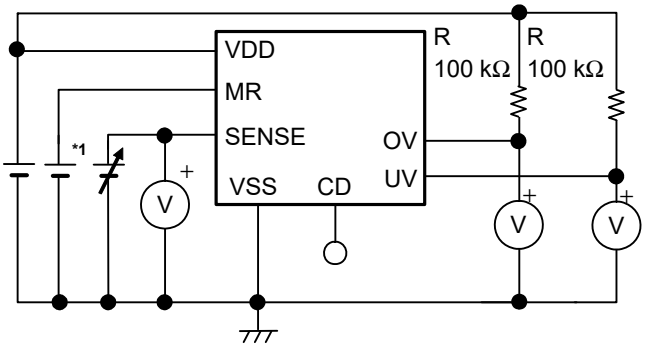
Figure 10 Test Circuit 4



***1** Set to V_{DD}

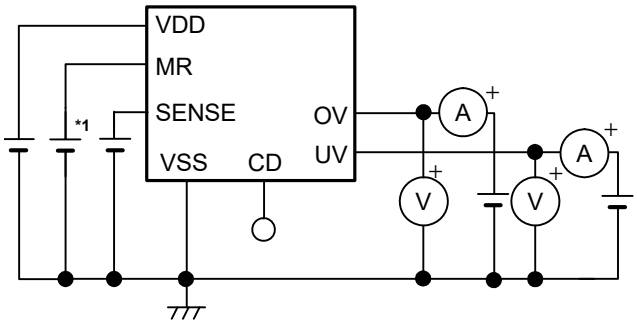
Figure 11 Test Circuit 5

2. HSNT-8(1616)B



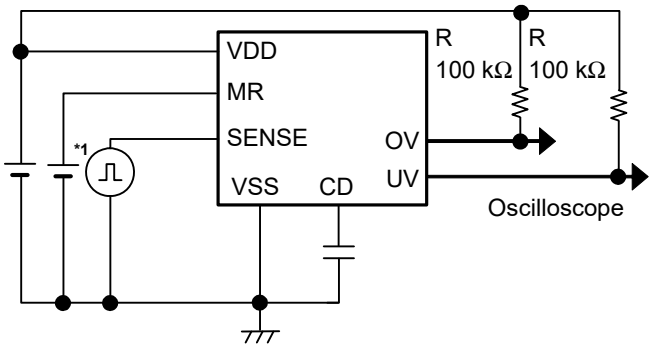
***1** Set to V_{DD}

Figure 12 Test Circuit 6



***1** Set to V_{DD}

Figure 13 Test Circuit 7



***1** Set to V_{DD}

Figure 14 Test Circuit 8

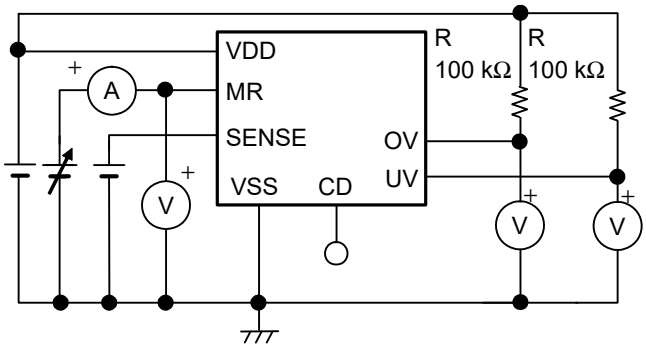
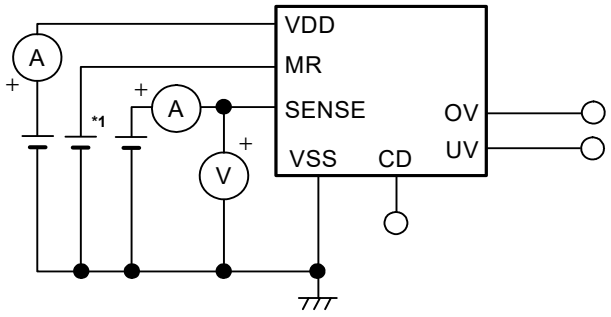


Figure 15 Test Circuit 9

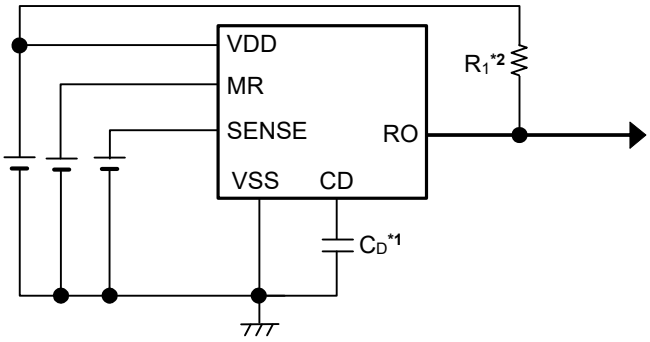


***1** Set to V_{DD}

Figure 16 Test Circuit 10

■ Standard Circuit

1. SOT-23-6

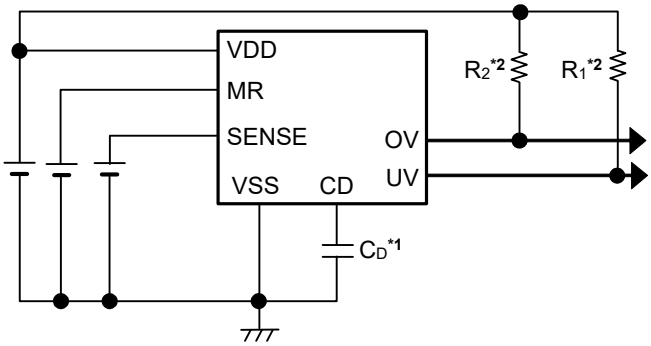


***1.** C_D is a release delay time adjustment capacitor. The C_D should be connected directly to the CD pin and the VSS pin.

***2.** R_1 is the external pull-up resistors for the output pin.

Figure 17

2. HSNT-8(1616)B



***1.** C_D is a release delay time adjustment capacitor. The C_D should be connected directly to the CD pin and the VSS pin.

***2.** R_1, R_2 are the external pull-up resistors for the output pin.

Figure 18

Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation including the temperature characteristics with an actual application to set the constants.

■ Condition of Application

Release delay time adjustment capacitor (C_D): A ceramic capacitor with capacitance of 0.33 nF or more is recommended.

■ Selection of Release Delay Time Adjustment Capacitor (C_D)

In this IC, the release delay time adjustment capacitor (C_D) is necessary between the CD pin and the VSS pin to adjust the release delay time (t_{DELAY}) of the detector. Refer to "**3. Delay circuit**" in "**■ Operation**" for details.

Caution Perform thorough evaluation including the temperature characteristics with an actual application to select C_D.

■ Explanation of Terms

1. Detection voltage (V_{UVDET}, V_{OVDET})

The detection voltage is a SENSE pin voltage at which the output voltage in **Figure 23** or **Figure 24** turns to "L". The detection voltage varies slightly among products of the same specification. The variation of detection voltage between the specified minimum and the maximum is called the detection voltage range (Refer to "**Figure 19 Overvoltage Detection Voltage**", "**Figure 21 Undervoltage Detection Voltage**").

Table 10

Detection Operation	Detection Voltage	Output Voltage	Detection Voltage Range
Undervoltage detection	V_{UVDET}	V_{RO} / V_{UV} = "H" → "L"	V_{UVDET} min. to V_{UVDET} max.
Overvoltage detection	V_{OVDET}	V_{RO} / V_{OV} = "H" → "L"	V_{OVDET} min. to V_{OVDET} max.

Example: In V_{UVDET} = 4.0 V product, the detection voltage is at any point in the range of 3.940 V ≤ V_{UVDET} ≤ 4.060 V.
This means that some V_{UVDET} = 4.0 V product has V_{UVDET} = 3.940 V and some has V_{UVDET} = 4.060 V.

2. Release voltage (V_{UVREL}, V_{OVREL})

The release voltage is a SENSE pin voltage at which the output voltage in **Figure 23** or **Figure 24** turns to "H". The release voltage varies slightly among products of the same specification. The variation of release voltage between the specified minimum and the maximum is called the release voltage range (Refer to "**Figure 20 Overvoltage Release Voltage**", "**Figure 22 Undervoltage Release Voltage**").
The release voltage becomes the value differs from the detection voltage within the range shown below.

- S-191AA6xx to S-191AE9xx: 2% to 4% (3% typ.)
- S-191AG6xx to S-191AL9xx: 4% to 6% (5% typ.)
- S-191AN6xx to S-191AS9xx: 9% to 11% (10% typ.)

Table 11

Detection Operation	Release Voltage	Output Voltage	Release Voltage Range
Undervoltage detection	V_{UVREL}	V_{RO} / V_{UV} = "L" → "H"	V_{UVREL} min. to V_{UVREL} max.
Overvoltage detection	V_{OVREL}	V_{RO} / V_{OV} = "L" → "H"	V_{OVREL} min. to V_{OVREL} max.

Example: For S-191AS0xx, V_{UVDET} = 4.0 V product, the release voltage is at any point in the range of 4.29 V ≤ V_{UVREL} ≤ 4.51 V despite V_{UVREL} = 4.40 V typ.
This means that S-191AS0xx, V_{UVDET} = 4.0 V product has V_{UVREL} = 4.29 V and some has V_{UVREL} = 4.51 V.

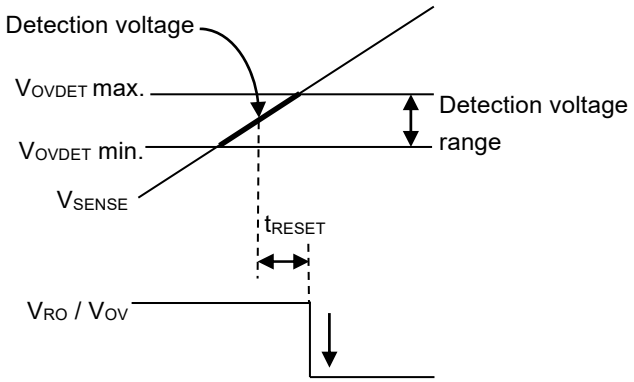


Figure 19 Overvoltage Detection Voltage

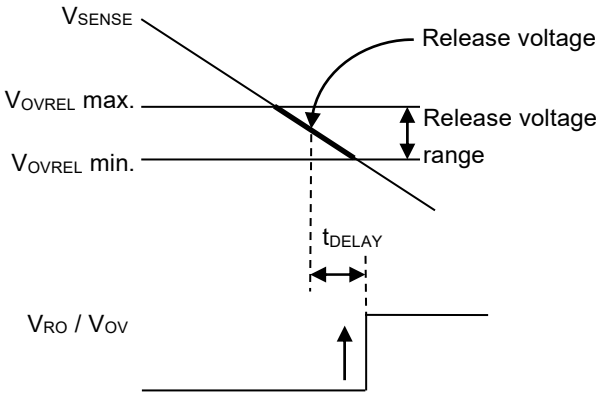


Figure 20 Overvoltage Release Voltage

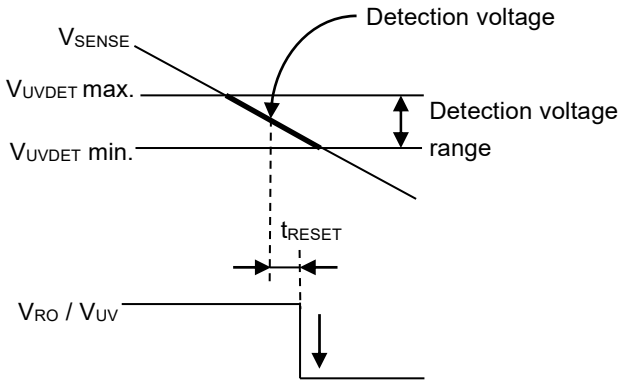


Figure 21 Undervoltage Detection Voltage

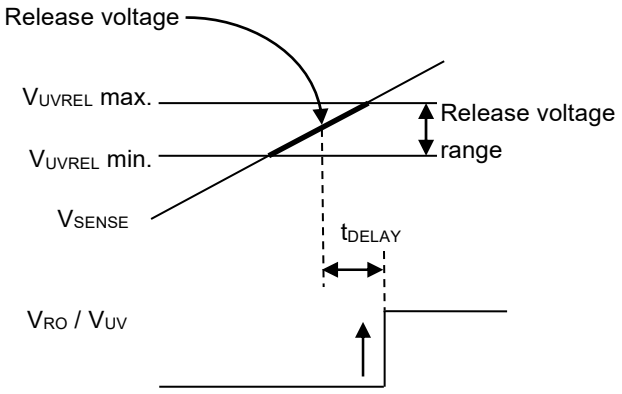


Figure 22 Undervoltage Release Voltage

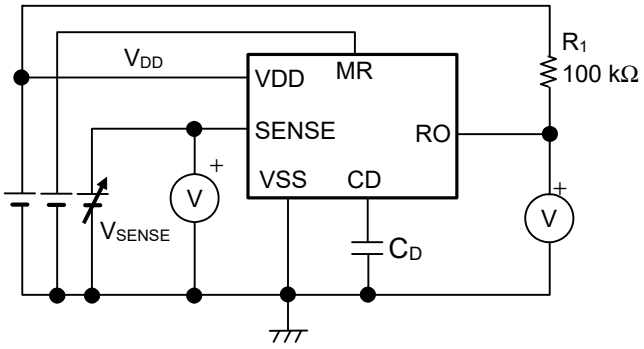


Figure 23 Test Circuit of Detection Voltage and Release Voltage for SOT-23-6

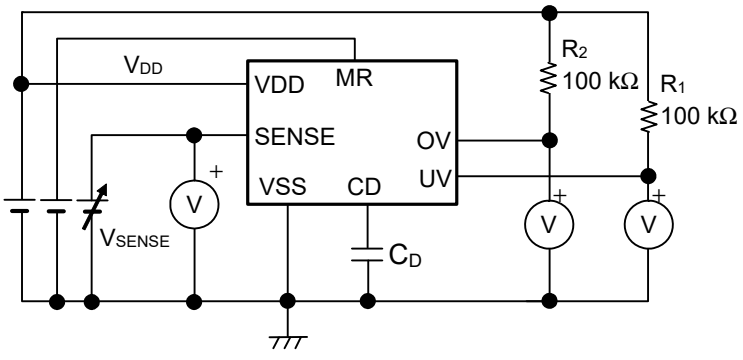


Figure 24 Test Circuit of Detection Voltage and Release Voltage for HSNT-8(1616)B

3. Hysteresis width (V_{UVHYS}, V_{OVHYS})

The hysteresis width is the voltage difference between the detection voltage and the release voltage. Setting the hysteresis width between the detection voltage and the release voltage, prevents malfunction caused by noise on the input voltage.

- Undervoltage hysteresis width (V_{UVHYS}): $V_{UVREL} - V_{UVDET}$
- Overvoltage hysteresis width (V_{OVHYS}): $V_{OVDET} - V_{OVREL}$

4. Feed-through current

The feed-through current is a current that flows instantaneously to the VDD pin at the time of detection and release of a voltage detector.

■ Operation

1. Basic operation

Figure 25, Figure 27, Figure 29, and **Figure 31** show that RO pin or UV and OV pins being pulled up by resistors (R_1, R_2) is an example of basic detector block operation.

1. 1 SOT-23-6

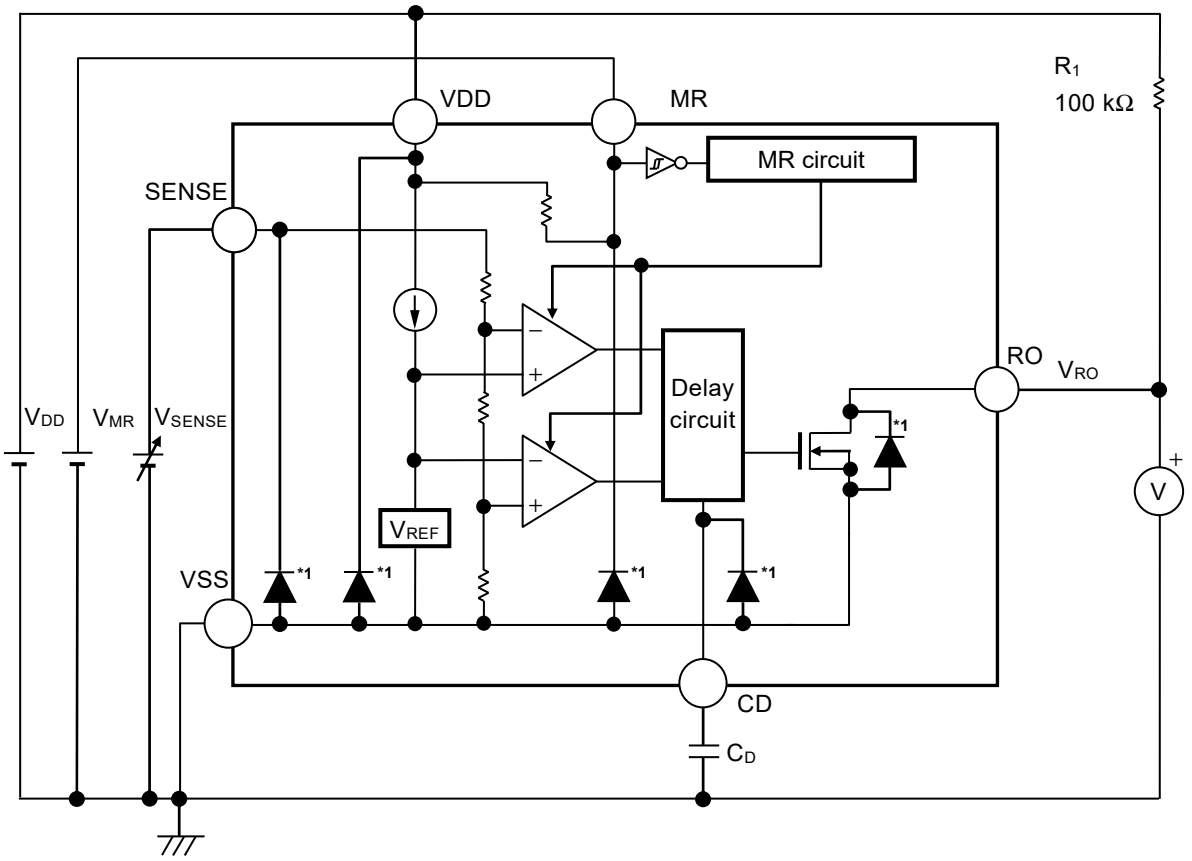
1. 1. 1 Hysteresis width "Unavailable"

(1) Undervoltage detection status to release status (undervoltage release status)
When the SENSE pin voltage (V_{SENSE}) exceeds the undervoltage release voltage (V_{UVREL} = V_{UVDET}), the RO pin voltage output becomes "H" after release delay time (t_{DELAY}).

(2) Release status to overvoltage detection status
V_{SENSE} rises, and when it exceeds the overvoltage detection voltage (V_{OVDET}), the RO pin output becomes "L" after detection response time (t_{RESET}).

(3) Overvoltage detection status to release status (overvoltage release status)
V_{SENSE} drops, and when it goes below the overvoltage release voltage (V_{OVREL} = V_{OVDET}), the RO pin output changes to "H" after t_{DELAY}.

(4) Release status to undervoltage detection status
V_{SENSE} drops, and when it goes below the undervoltage detection voltage (V_{UVDET}), the RO pin output becomes "L" after t_{RESET} and changes to undervoltage detection status.



***1.** Parasitic diode

Figure 25 Operation

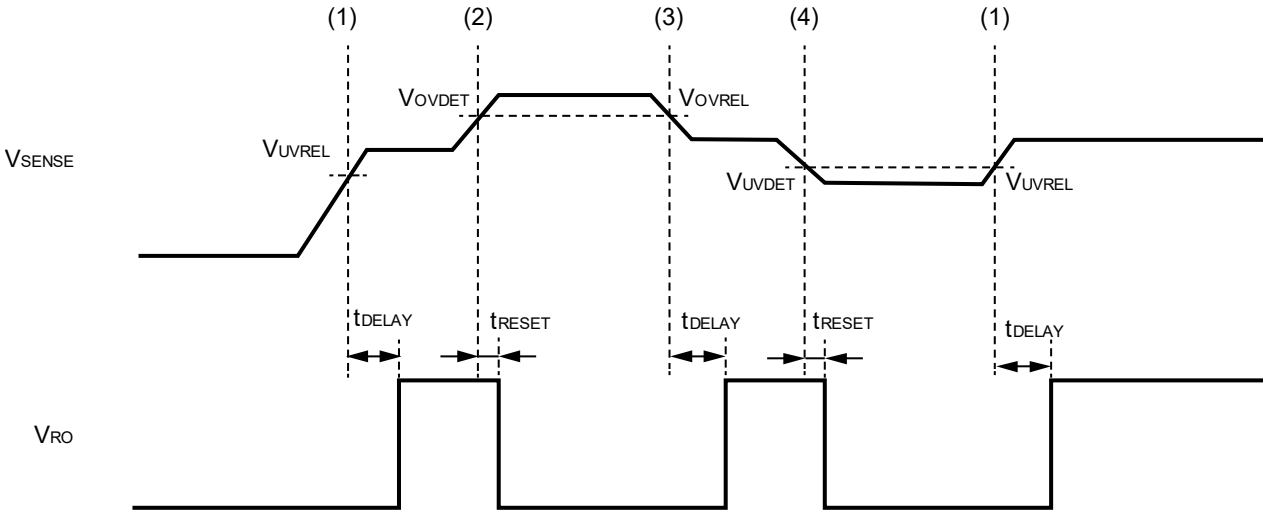


Figure 26 Timing Chart

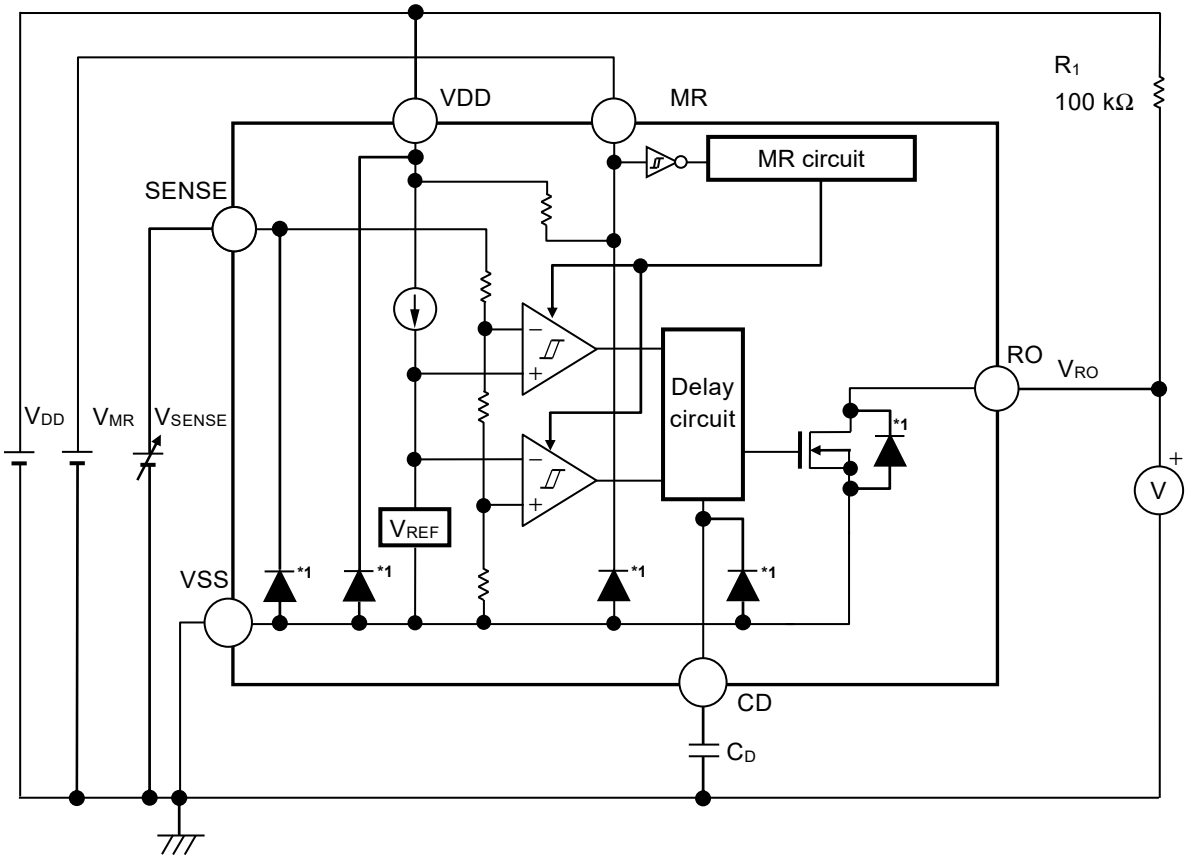
1. 1. 2 Hysteresis width "Available"

(1) Undervoltage detection status to release status (undervoltage release status)
When the SENSE pin voltage (V_{SENSE}) exceeds the undervoltage release voltage (V_{UVREL} = V_{UVDET} + V_{UVHYS}), the RO pin voltage output becomes "H" after release delay time (t_{DELAY}).

(2) Release status to overvoltage detection status
V_{SENSE} rises, and when it exceeds the overvoltage detection voltage (V_{OVDET}), the RO pin output becomes "L" after detection response time (t_{RESET}).

(3) Overvoltage detection status to release status (overvoltage release status)
V_{SENSE} drops, and when it goes below the overvoltage release voltage (V_{OVREL} = V_{OVDET} – V_{OVHYS}), the RO pin output changes to "H" after t_{DELAY}.

(4) Release status to undervoltage detection status
V_{SENSE} drops, and when it goes below the undervoltage detection voltage (V_{UVDET}), the RO pin output becomes "L" after t_{RESET} and changes to undervoltage detection status.



***1.** Parasitic diode

Figure 27 Operation

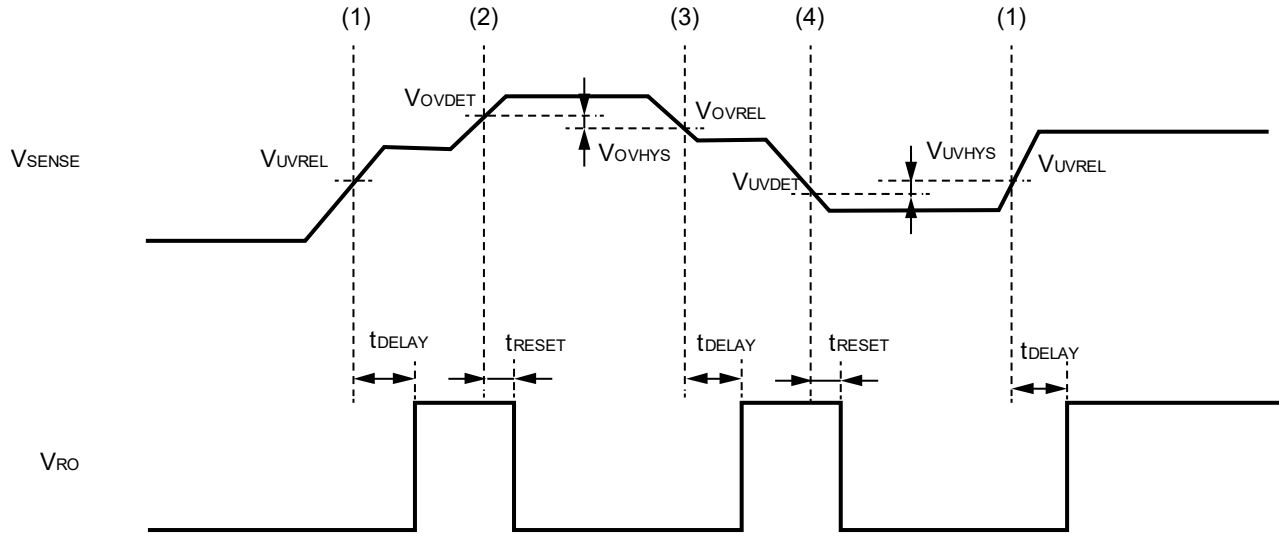


Figure 28 Timing Chart

1. 2 HSNT-8(1616)B

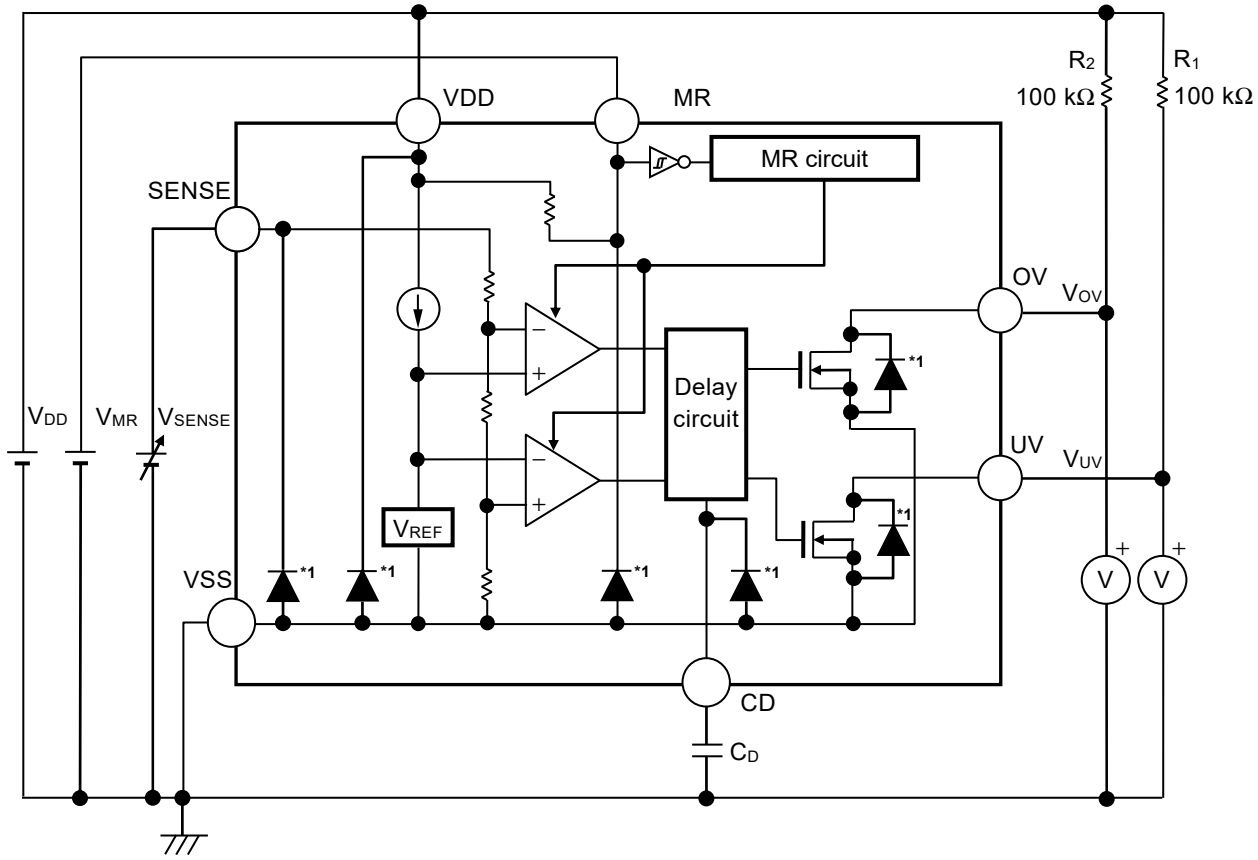
1. 2. 1 Hysteresis width "Unavailable"

(1) Undervoltage detection status to release status (undervoltage release status)
When the SENSE pin voltage (V_{SENSE}) exceeds the undervoltage release voltage (V_{UVREL} = V_{UVDET}), the UV pin voltage output becomes "H" after release delay time (t_{DELAY}). At this time, the OV pin output stays at "H".

(2) Release status to overvoltage detection status
V_{SENSE} rises, and when it exceeds the overvoltage detection voltage (V_{OVDET}), the OV pin output becomes "L" after detection response time (t_{RESET}). At this time, the UV pin stays at "H".

(3) Overvoltage detection status to release status (overvoltage release status)
V_{SENSE} drops, and when it goes below the overvoltage release voltage (V_{OVREL} = V_{OVDET}), the OV pin output changes to "H" after t_{DELAY}. At this time, the UV pin output stays at "H".

(4) Release status to undervoltage detection status
V_{SENSE} drops, and when it goes below the undervoltage detection voltage (V_{UVDET}), the UV pin output becomes "L" after t_{RESET} and changes to undervoltage detection status. At this time, the OV pin output stays at "H".



***1.** Parasitic diode

Figure 29 Operation

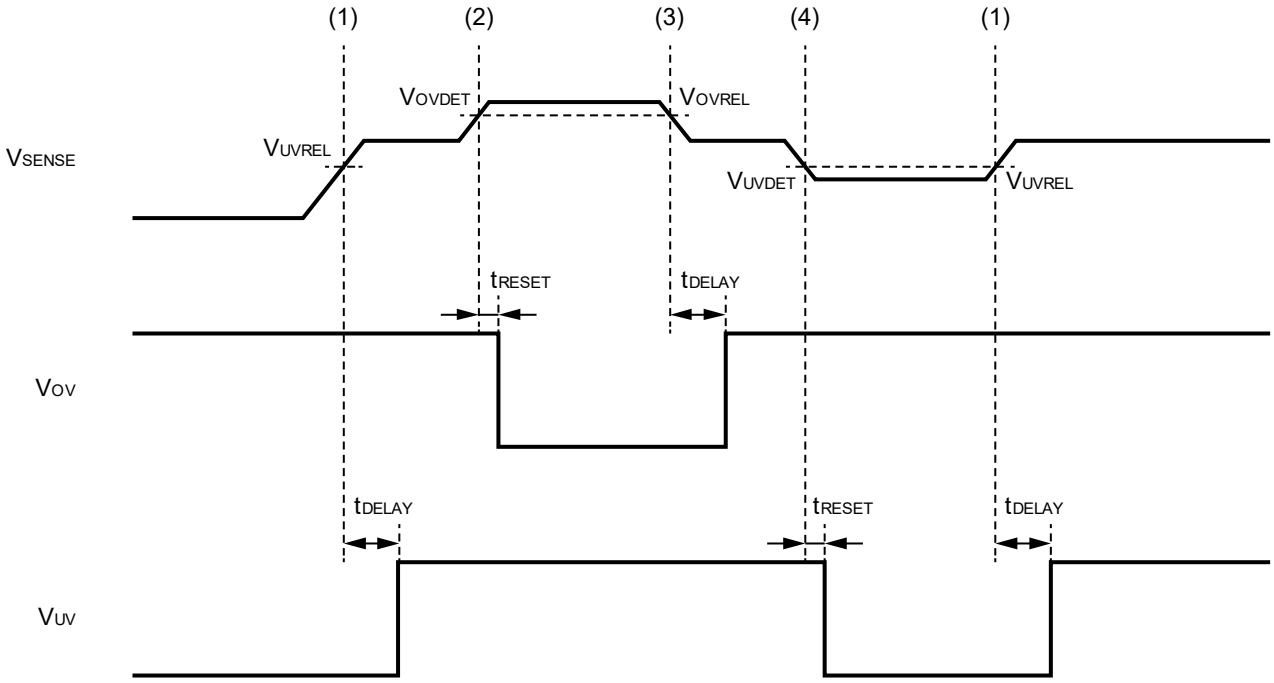


Figure 30 Timing Chart

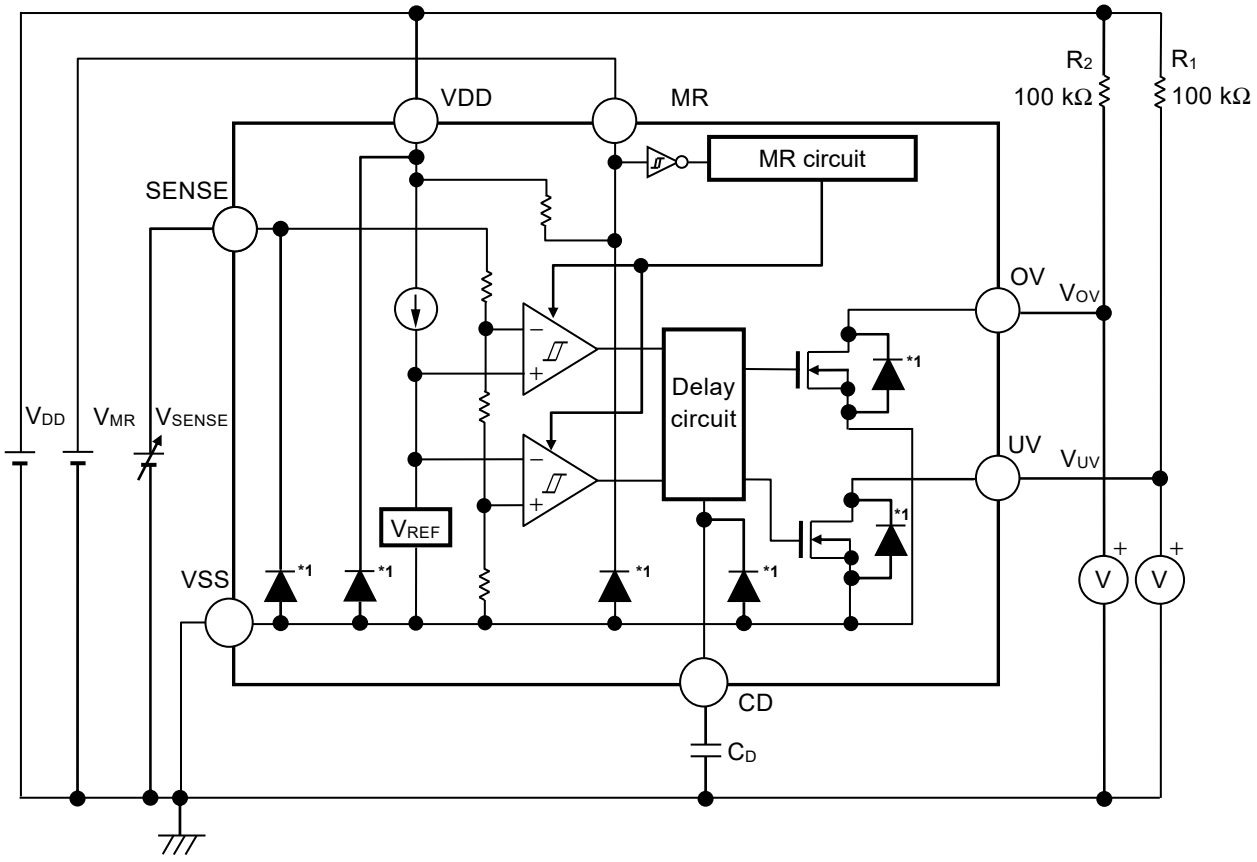
1. 2. 2 Hysteresis width "Available"

(1) Undervoltage detection status to release status (undervoltage release status)
When the SENSE pin voltage (V_{SENSE}) exceeds the undervoltage release voltage (V_{UVREL} = V_{UVDET} + V_{UVHYS}), the UV pin voltage output becomes "H" after release delay time (t_{DELAY}). At this time, the OV pin output stays at "H".

(2) Release status to overvoltage detection status
V_{SENSE} rises, and when it exceeds the overvoltage detection voltage (V_{OVDET}), the OV pin output becomes "L" after detection response time (t_{RESET}). At this time, the UV pin stays at "H".

(3) Overvoltage detection status to release status (overvoltage release status)
V_{SENSE} drops, and when it goes below the overvoltage release voltage (V_{OVREL} = V_{OVDET} – V_{OVHYS}), the OV pin output changes to "H" after t_{DELAY}. At this time, the UV pin output stays at "H".

(4) Release status to undervoltage detection status
V_{SENSE} drops, and when it goes below the undervoltage detection voltage (V_{UVDET}), the UV pin output becomes "L" after t_{RESET} and changes to undervoltage detection status. At this time, the OV pin output stays at "H".



***1.** Parasitic diode

Figure 31 Operation

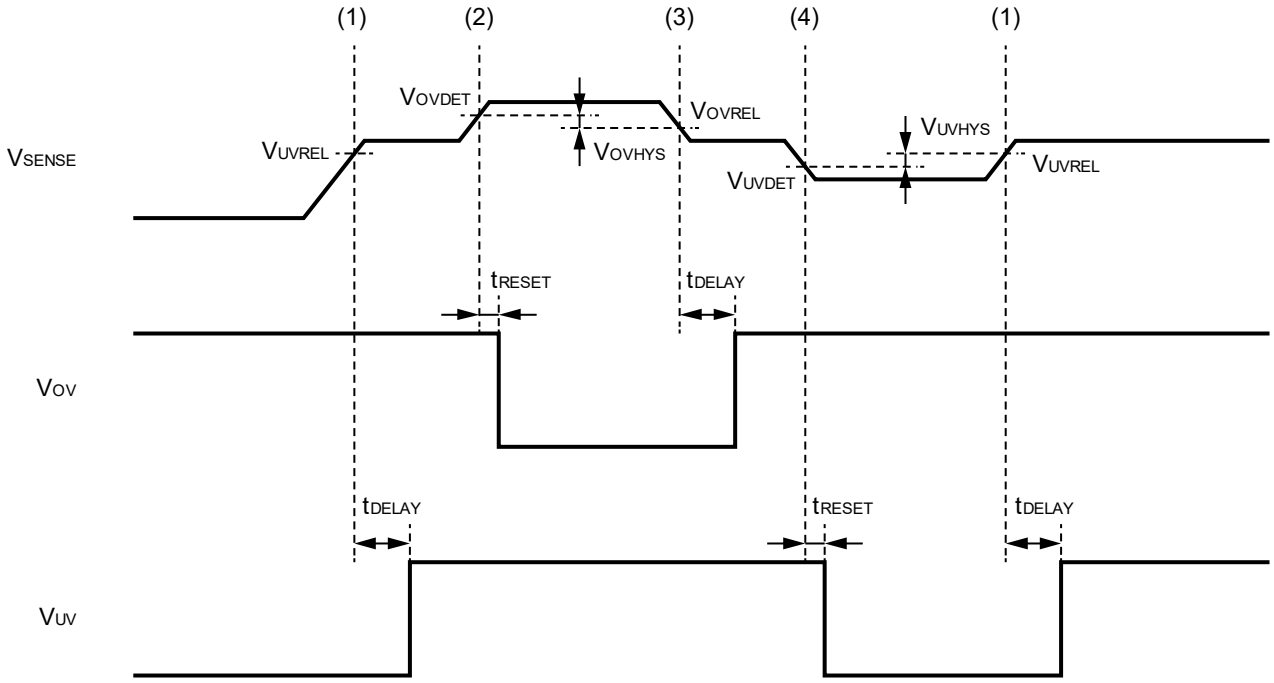


Figure 32 Timing Chart

2. SENSE pin

The SENSE pin is the input pin for the detection voltage. The power supply VDD pin and SENSE pin, for voltage detection, are divided. Therefore, as long as a voltage is supplied to the VDD pin, the reset signal will be held even if the input voltage to the SENSE pin drops below the minimum operation voltage.

2. 1 Error when detection voltage is set externally

The undervoltage detection voltage and the overvoltage detection voltage can be set externally by connecting a node that was resistance-divided by the resistor (R_A) and the resistor (R_B) to the SENSE pin as shown in **Figure 33** and **Figure 34**.

For conventional products without the SENSE pin, external resistor cannot be too large since the resistance-divided node must be connected to the VDD pin. This is because a feed-through current will flow through the VDD pin when it goes from detection to release, and if external resistor is large, problems such as oscillation or larger error in the hysteresis width may occur.

In this IC, R_A and R_B in **Figure 33** and **Figure 34** are easily made larger since the resistance-divided node can be connected to the SENSE pin through which no feed-through current flows. However, be careful of error in the current flowing through the internal resistance (R_{SENSE}) that will occur.

Although R_{SENSE}*1 in this IC is large to make the error small, R_A and R_B should be selected such that the error is within the allowable limits.

***1.** 3.3 MΩ min.

2. 2 Selection of R_A and R_B

In **Figure 33** and **Figure 34**, the relation between the external setting undervoltage detection voltage (V_{DUX}) or the overvoltage detection voltage (V_{DOX}) and the actual detection voltage (V_{UVDET}, V_{OVDET}) is ideally calculated by the equation below.

$$V_{DUX} = V_{UVDET} \times \left(1 + \frac{R_A}{R_B}\right) \cdots\cdots(1)$$

$$V_{DOX} = V_{OVDET} \times \left(1 + \frac{R_A}{R_B}\right) \cdots\cdots(1)$$

However, in reality there is an error in the current flowing through R_{SENSE}.
When considering this error, the relation between V_{DUX}, V_{DOX}, V_{UVDET} and V_{OVDET} is calculated as follows.

$$\begin{aligned} V_{DUX} &= V_{UVDET} \times \left(1 + \frac{R_A}{R_B \parallel R_{SENSE}}\right) \\ &= V_{UVDET} \times \left(1 + \frac{R_A}{\frac{R_B \times R_{SENSE}}{R_B + R_{SENSE}}}\right) \\ &= V_{UVDET} \times \left(1 + \frac{R_A}{R_B}\right) + \frac{R_A}{R_{SENSE}} \times V_{UVET} \cdots\cdots(2) \end{aligned}$$

$$V_{DOX} = V_{OVDET} \times \left(1 + \frac{R_A}{R_B}\right) + \frac{R_A}{R_{SENSE}} \times V_{OVET} \cdots\cdots(2)$$

By using equations (1) and (2), the error is calculated as $V_{UVDET} \times \frac{R_A}{R_{SENSE}}$, $V_{OVDET} \times \frac{R_A}{R_{SENSE}}$.
The error rate is calculated as follows by dividing the error by the right-hand side of equation (1).

$$\frac{R_A \times R_B}{R_{SENSE} \times (R_A + R_B)} \times 100\ [\%] = \frac{R_A \parallel R_B}{R_{SENSE}} \times 100\ [\%] \cdots(3)$$

As seen in equation (3), the smaller the resistance values of R_A and R_B compared to R_{SENSE}, the smaller the error rate becomes.

Also, the relation between the external setting undervoltage hysteresis width (V_{HUX}) or the overvoltage hysteresis width (V_{HOX}) and the hysteresis width (V_{UVHYS}, V_{OVHYS}) is calculated by equation below. Error due to R_{SENSE} also occurs to the relation in a similar way to the detection voltage.

$$V_{HUX} = V_{UVHYS} \times \left(1 + \frac{R_A}{R_B}\right) \cdots\cdots(4)$$

$$V_{HOX} = V_{OVHYS} \times \left(1 + \frac{R_A}{R_B}\right) \cdots\cdots(4)$$

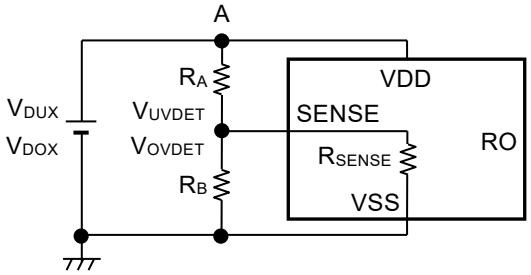


Figure 33 Detection Voltage External Setting Circuit of SOT-23-6

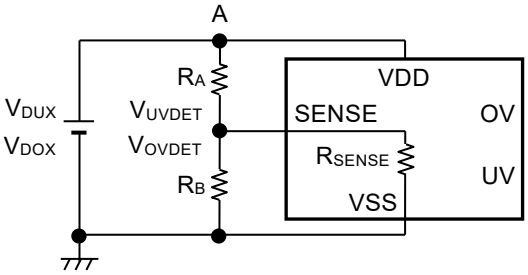


Figure 34 Detection Voltage External Setting Circuit of HSNT-8(1616)B

Caution If R_A and R_B are large, the SENSE pin input impedance becomes higher and may cause a malfunction due to noise. In this case, connect a capacitor between the SENSE pin and the VSS pin.

3. Delay circuit

The delay circuit comes with a function for adjusting the release delay time (t_{DELAY}) from when the SENSE pin voltage (V_{SENSE}) enters the state in **Table 12** and until the output pin inverts.

Table 12

Release operation	Status	Output Pin
Undervoltage release	Undervoltage release voltage (V_{UVREL} = V_{UVDET} + V_{UVHYS}) or more	RO pin / UV pin
Overvoltage release	Overvoltage release voltage (V_{OVREL} = V_{OVDET} – V_{OVHYS}) or lower	RO pin / OV pin

t_{DELAY} is determined by the delay coefficient, the release delay time adjustment capacitor (C_D) and the release delay time when the CD pin is open (t_{DELAY0}). They are calculated by the equations below.

t_{DELAY} [ms] = Delay coefficient × C_D [nF] + t_{DELAY0} [ms]

Table 13

Operation Temperature	Delay Coefficient		
	Min.	Typ.	Max.
Ta = +125°C	2.64	2.90	3.24
Ta = +25°C	2.67	3.00	3.18
Ta = –40°C	2.72	3.00	3.34

Table 14

Operation Temperature	Release Delay Time when CD Pin is Open (t_{DELAY0})		
	Min.	Typ.	Max.
Ta = +125°C	0.05	0.09	0.24
Ta = +25°C	0.05	0.10	0.22
Ta = –40°C	0.06	0.11	0.27

The release delay time ($t_{DELAYMR}$) during operation of the manual reset function is determined by the delay coefficient, the release delay time adjustment capacitor (C_D), and the release delay time ($t_{DELAYMR0}$) when the CD pin is open during operation of the manual reset function. They are calculated by the equation below.

$t_{DELAYMR}$ [ms] = Delay coefficient × C_D [nF] + $t_{DELAYMR0}$ [ms]

Table 15

Operation Temperature	Release Delay Time ($t_{DELAYMR0}$) When the CD Pin is Open During Operation of the Manual Reset Function		
	Min.	Typ.	Max.
Ta = +125°C	0.04	0.19	0.41
Ta = +25°C	0.05	0.26	0.62
Ta = –40°C	0.06	0.35	0.70

Caution 1. Mounted board layout should be made in such a way that no current flows into or flows from the CD pin since the impedance of the CD pin is high, otherwise correct delay time cannot be provided.

2. There is no limit for the capacitance of C_D as long as the leakage current of the capacitor can be ignored against the built-in constant current value (approximately 160 nA). The leakage current may cause error in delay time. When the leakage current is larger than the built-in constant current, no detect or release takes place.

3. The above equations will not guarantee successful operation. Determine the capacitance of C_D through thorough evaluation including temperature characteristics in the actual usage conditions.

**4. When the CD pin is open, a double pulse may appear at release.
To avoid the double pulse, attach 0.33 nF or more capacitor to the CD pin.**

4. Manual reset function

This IC has a manual reset function that can forcibly switch to the detection status.
This IC can activate the manual reset function by applying "L" to the MR pin from the outside.
The manual reset function changes the input voltage of the comparator when an external input signal is received from the MR pin. The manual reset function changes the comparator input voltage of the internal circuit, and the detector is forcibly put into the detection status.
Use of the manual reset function when SENSE pin voltage is held within the release voltage range makes it possible to monitor output pin logic signal to confirm that the comparator circuit, delay circuit and output transistor are operating normally.

4. 1 MR pin

The MR pin input voltage (V_{MR}) forces the output pin voltage to "L".
If the manual reset function is disabled, set the MR pin input voltage (V_{MR}) to "H" or to open.
When the MR pin is open (floating status), the MR pin resistor (R_{MR}) causes the MR pin to be internally pulled up to the VDD pin raising it to V_{DD} level. Also, take care when 0.6 V to V_{DD} min. − 0.3 V voltage is applied to the MR pin as this increases current consumption.

The structure of the MR pin is shown in **Figure 35**.
Note that when the MR pin is set to "L" level, current relative to MR pin resistance (R_{MR} = 2.2 MΩ typ.) in **Table 8** and **Table 9** in "■ **Electrical Characteristics**" and VDD pin voltage (V_{DD}) will flow to the MR pin.

Table 16

MR Pin	Internal Circuit	Output Pin Logic	Current Consumption
"H" or open: OFF	Normal operation	Depends on specific status*1	I_{SS1}
"L": ON	Forced detection	"L"	$I_{SS1} + V_{DD} / R_{MR}$

***1.** For details, refer to "**4. 2 Manual reset operation**".

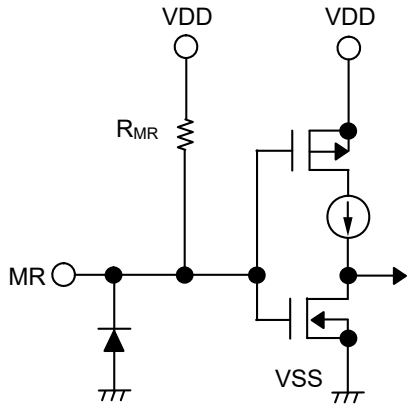


Figure 35

4. 2 Manual reset operation

Figure 36 shows a timing chart for the manual reset function. SOT-23-6 generates output via the RO pin, while the HSNT-8(1616)B generates output via the OV and UV pins.

When the SENSE pin voltage (V_{SENSE}) is $V_{UVREL} \leq V_{SENSE} \leq V_{OVREL}$, operation of the manual reset function is shown below.

(1) When a voltage lower than MR pin input voltage "L" (V_{MRL}) is applied to the MR pin, the output from the RO pin / OV pin, UV pin become "L" and the detector switches from release status to detection status after the detection response time ($t_{RESETMR}$) = 50.0 μs max. during operation of the manual reset function has elapsed. Apply a voltage of V_{MRL} or less for at least 50.0 μs.
(2) When a voltage higher than MR pin input voltage "H" (V_{MRH}) is applied to the MR pin, the output from the RO pin / OV pin, UV pin become "H" and the detector switches from detection status to release status after the release delay time ($t_{DELAYMR}$) during operation of the manual reset function has elapsed. Be sure to maintain V_{MRH} during $t_{DELAYMR}$. Refer to "**3. Delay circuit**" in "■ **Operation**" for details on $t_{DELAYMR}$.

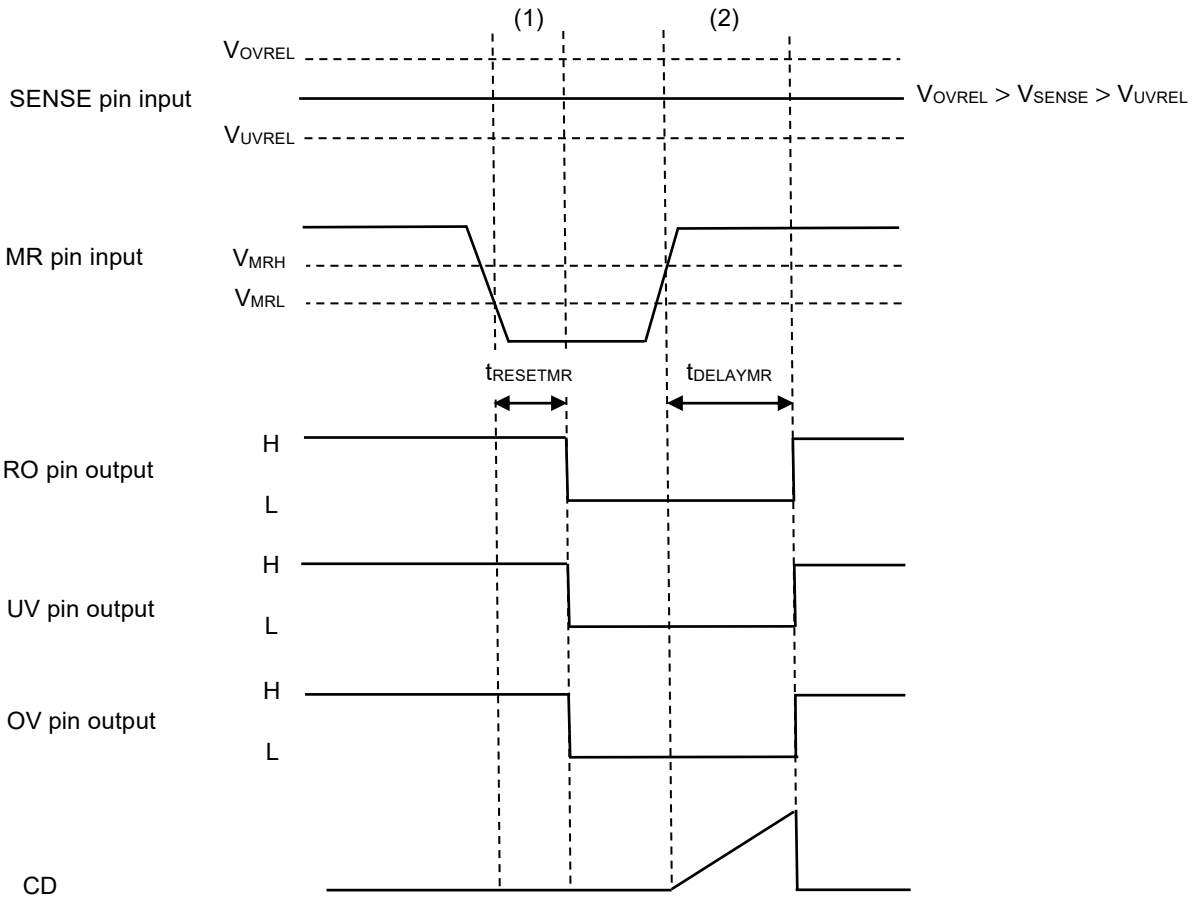


Figure 36

4. 3 When connecting a resistor (R_A) between the supply voltage (V_{DD}) and the VDD / SENSE pins

When the VDD and SENSE pins of the IC are shorted and the MR pin input voltage (V_{MR}) is at an intermediate potential ($V_{MRL} < V_{MR} < V_{MRH}$), the current consumption increases by 35.7 μA max. This current flows through R_A and causes a voltage drop.
When this voltage drop causes the VDD pin voltage (V_{IN}) to fall below the undervoltage detection voltage (V_{UVDET}), the detector switches to the detection status, and may not be able to switch to the release status unless the supply voltage (V_{DD}) is increased.
When $V_{IN} > V_{MR}$, current also flows through the MR pin input resistor (R_{MR}). For example, when V_{IN} = 6 V, V_{MR} = 1 V, and R_{MR} = 0.91 MΩ min., a current of 5.5 μA flows from the VDD pin to the MR pin. Therefore, set R_A to satisfy the following equation.

$R_A \leq (V_{DD} - (V_{UVDET})) / (35.7\ \mu A + \text{MR pin current})$

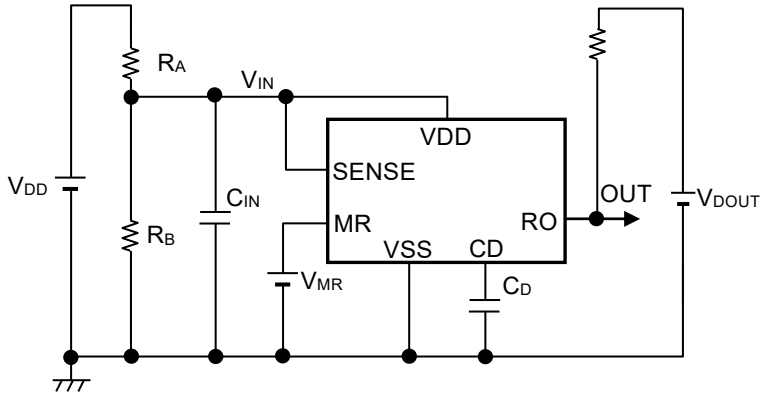


Figure 37 For SOT-23-6

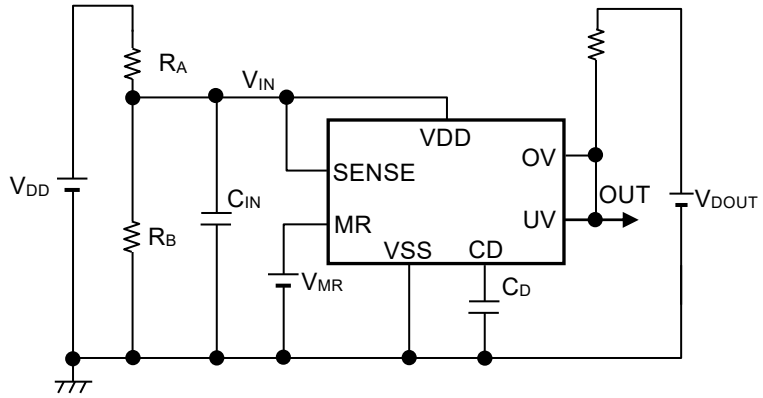


Figure 38 For HSNT-8(1616)B

■ Usage Precautions

1. Feed-through current at the time of detection and release

In this IC, a feed-through current flows instantaneously at the time of detection and release. Therefore, if the input impedance is increased, oscillation may occur due to the voltage drop caused by the feed-through current.
When this IC is used in the configuration shown in **Figure 39** and **Figure 40**, the input impedance is recommended to be 1 kΩ or less.
Perform a sufficient evaluation including the temperature characteristics under the actual operating conditions.

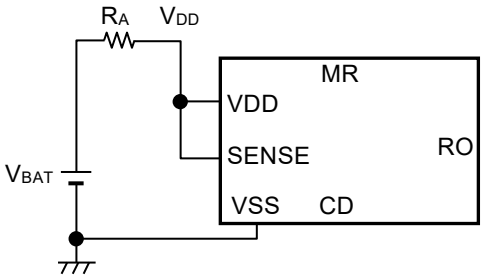


Figure 39 For SOT-23-6

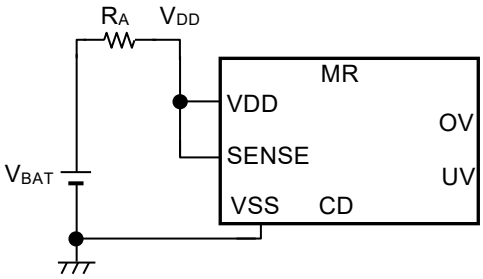


Figure 40 For HSNT-8(1616)B

2. Power on sequence

Turn on the power in one of the following two procedures.

(1) Order of VDD pin and SENSE pin (Refer to **Figure 41**)
(2) VDD pin and SENSE pin at the same time

When $V_{OVDET} \geq V_{SENSE} \geq V_{UVREL}$ applies, both the overvoltage output voltage (V_{OV}) and the undervoltage output voltage (V_{UV}) become "H", and the detector enters release status.

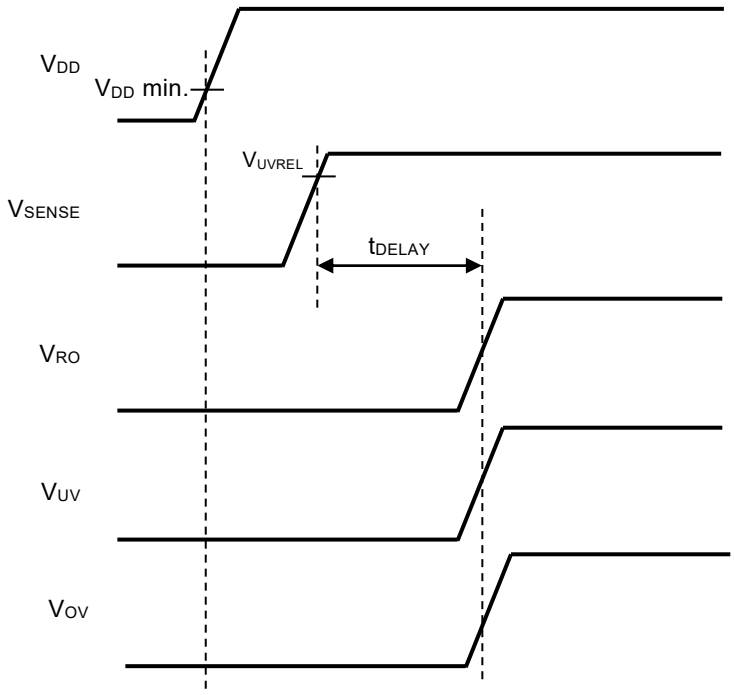


Figure 41

Caution When the SENSE pin is turned on before the VDD pin, a release may mistakenly occur even if V_{SENSE} is less than V_{UVREL}.

3. Relationship between overvoltage detection voltage, undervoltage detection voltage and hysteresis width

The nominal voltage range ($V_{NOMINAL}$) monitored by customers is defined as shown in **Figure 42.**
To ensure an appropriate $V_{NOMINAL}$ value, set the overvoltage detection voltage and undervoltage detection voltage considering the detection voltage variation, hysteresis width, and released voltage variation.
The relationship among $V_{NOMINAL}$, maximum value of undervoltage release voltage (V_{UVREL} max.) and the minimum value of the overvoltage release voltage (V_{OVREL} min.) must satisfy equation (1).

$$V_{NOMINAL} = V_{OVREL}\ \text{min.} - V_{UVREL}\ \text{max.} > 0 \cdots\cdots\cdots\cdots (1)$$

Figure 42 $V_{NOMINAL} > 0$

The equations below show the relationship among V_{UVREL} max., V_{OVREL} min., the set undervoltage detection voltage ($V_{UVDET(S)}$), the set overvoltage detection voltage ($V_{OVDET(S)}$), the undervoltage hysteresis width (V_{UVHYS}), and the overvoltage hysteresis width (V_{OVHYS}).

$$V_{UVREL}\ \text{max.} = V_{UVDET}\ \text{max.} \times (1 + V_{UVHYS}\ \text{max.}) = V_{UVDET(S)} \times 1.015 \times (1 + V_{UVHYS} + 0.01) \cdots\cdots\cdots\cdots (2)$$
$$V_{OVREL}\ \text{min.} = V_{OVDET}\ \text{min.} \times (1 - V_{OVHYS}\ \text{max.}) = V_{OVDET(S)} \times 0.985 \times (1 - V_{OVHYS} - 0.01) \cdots\cdots\cdots\cdots (3)$$

Based on equations (2) and (3), the following equation must be satisfied regarding $V_{NOMINAL}$, $V_{OVDET(S)}$ and $V_{UVDET(S)}$.

$$V_{NOMINAL} = V_{OVDET(S)} \times 0.985 \times (1 - V_{OVHYS} - 0.01) - V_{UVDET(S)} \times 1.015 \times (1 + V_{UVHYS} + 0.01) > 0 \cdots\cdots\cdots\cdots (4)$$

For example, calculating if it is possible to set $V_{UVDET(S)}$ = 3.0 V, $V_{OVDET(S)}$ = 3.6 V, and V_{OVHYS} = V_{UVHYS} = 5% typ. (accuracy ±1%), the following equation is generated.

$$V_{NOMINAL} = 3.6\ \text{V} \times 0.985 \times (1 - 0.06) - 3.0\ \text{V} \times 1.015 \times (1 + 0.06) = 0.106\ \text{V}$$

Since $V_{NOMINAL}$ is greater than 0, it can be determined that it is possible to set.

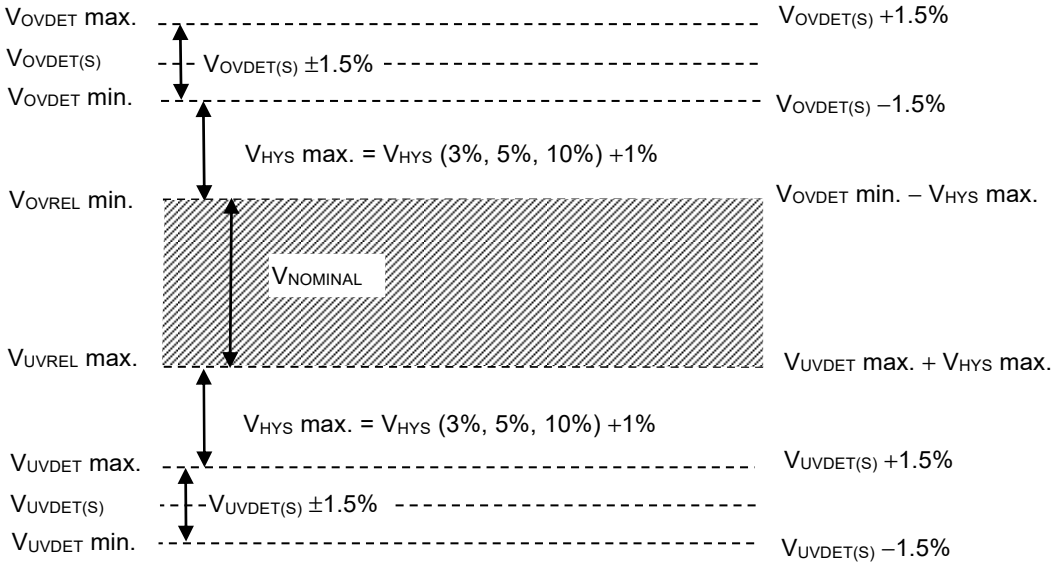


Figure 43

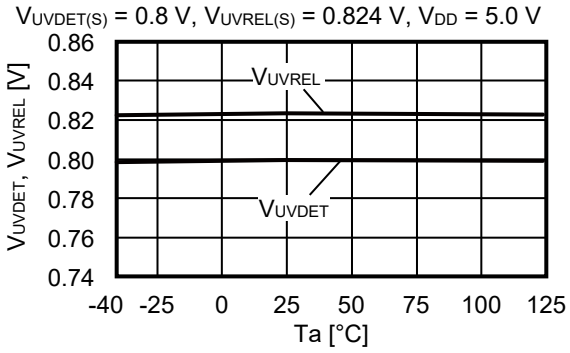
■ Precautions

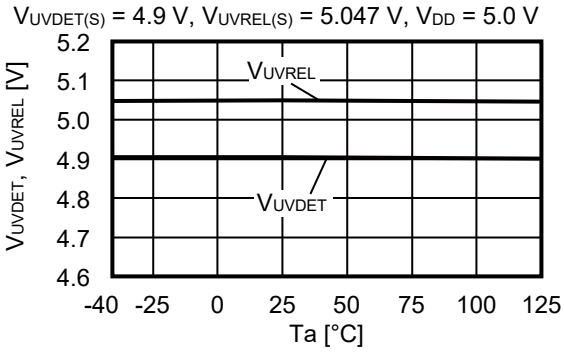
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- Because the SENSE pin has a high impedance, malfunctions may occur due to noise.
  Be careful of wiring adjoining SENSE pin wiring in actual applications.
- When using the manual reset function, be sure to hold MR pin input voltage "L" (V_{MRL}) for 50.0 μs or longer. Be careful if the V_{MRL} is held for less than 50.0 μs, because the internal logic may not be established and a malfunction could occur.
- When designing for mass production using an application circuit described herein, the product deviation and temperature characteristics should be taken into consideration. ABLIC Inc. shall not bear any responsibility for patent infringements related to products using the circuits described herein.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ Characteristics (Typical Data)

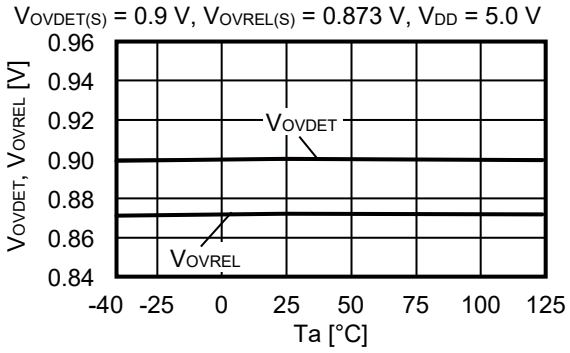
1. Detection voltage (V_{UVDET}, V_{OVDET}), Release voltage (V_{UVREL}, V_{OVREL}) vs. Temperature (Ta)

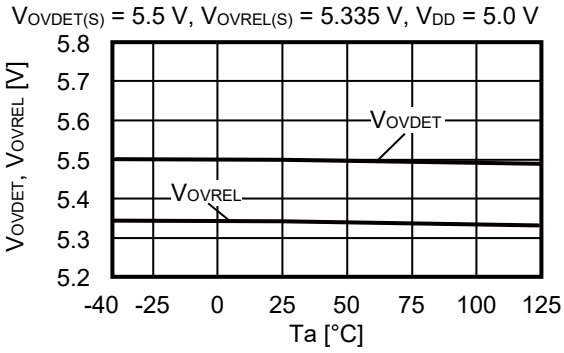
1. 1 Undervoltage detection





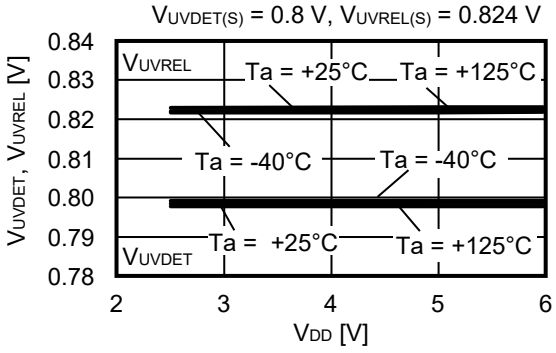
1. 2 Overvoltage detection

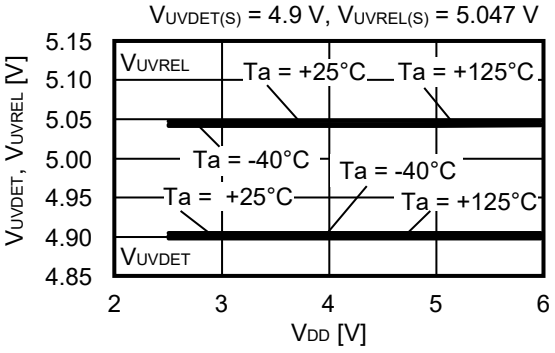




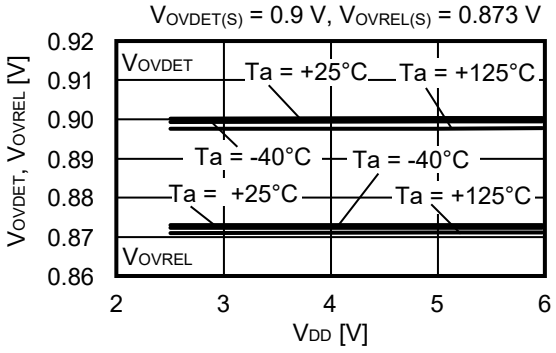
2. Detection voltage (V_{UVDET}, V_{OVDET}), Release voltage (V_{UVREL}, V_{OVREL}) vs. Power supply voltage (V_{DD})

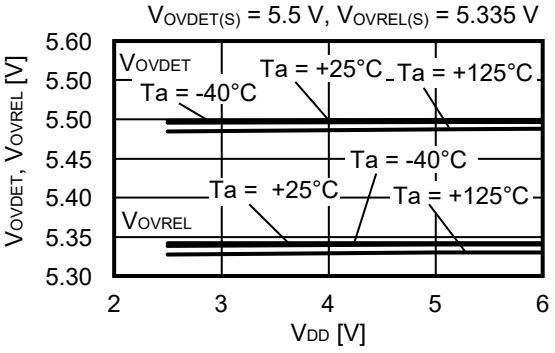
2. 1 Undervoltage detection





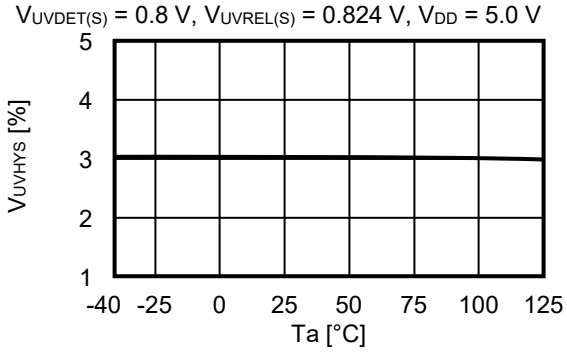
2. 2 Overvoltage detection

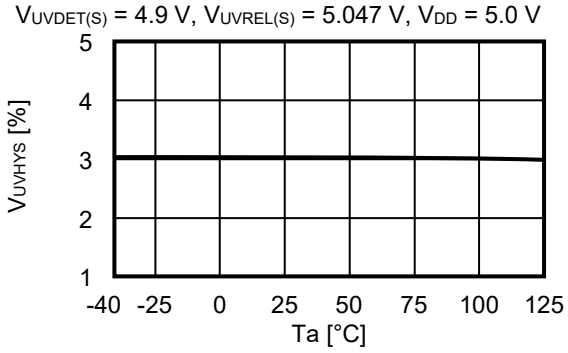




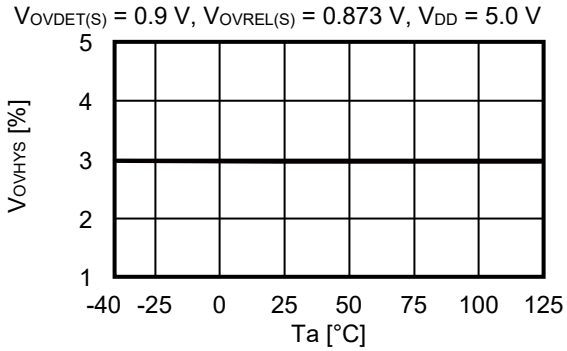
3. Hysteresis width (V_{UVHYS}, V_{OVHYS}) vs. Temperature (Ta)

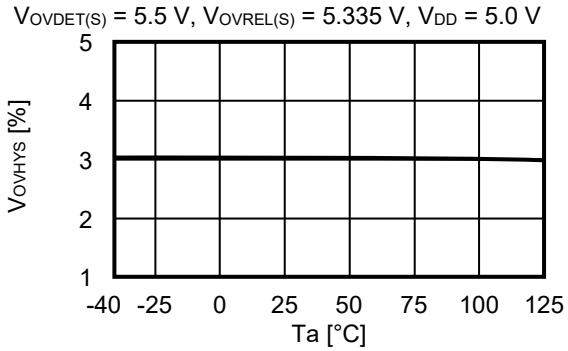
3. 1 Undervoltage detection





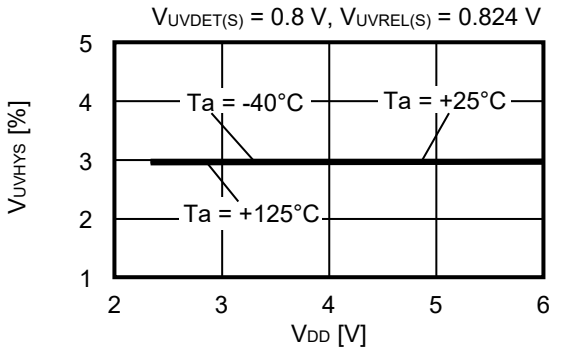
3. 2 Overvoltage detection

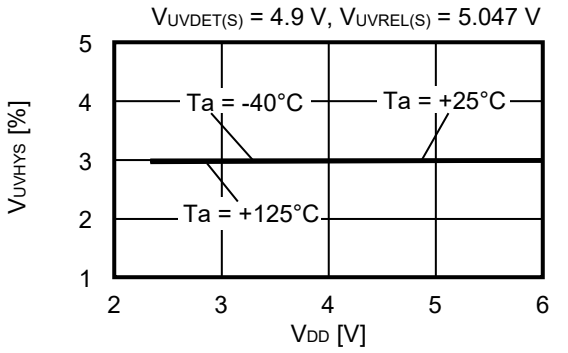




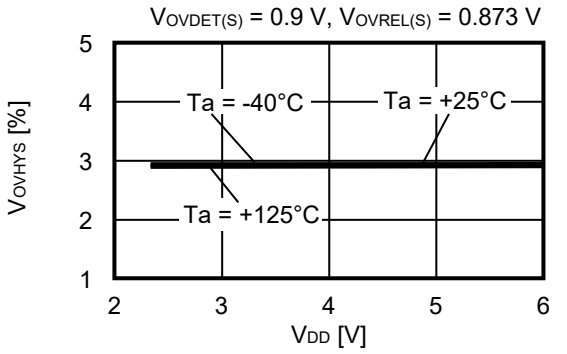
4. Hysteresis width (V_{UVHYS}, V_{OVHYS}) vs. Power supply voltage (V_{DD})

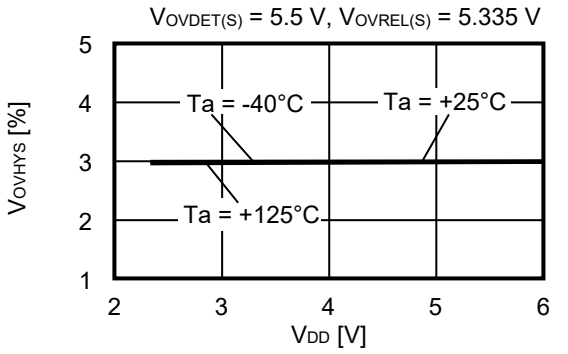
4. 1 Undervoltage detection





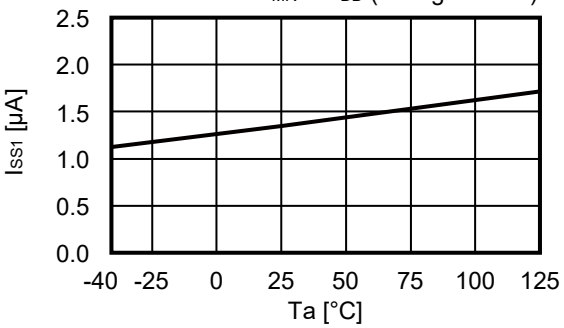
4. 2 Overvoltage detection



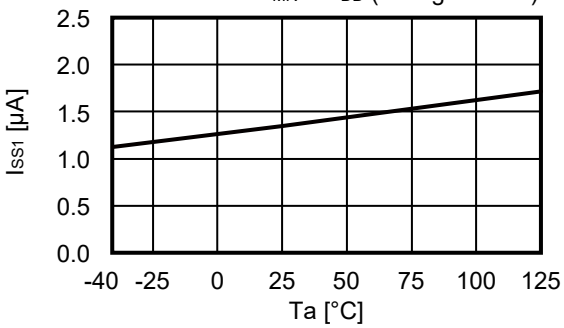


5. Current consumption (I_{SS1}) vs. Temperature (Ta)

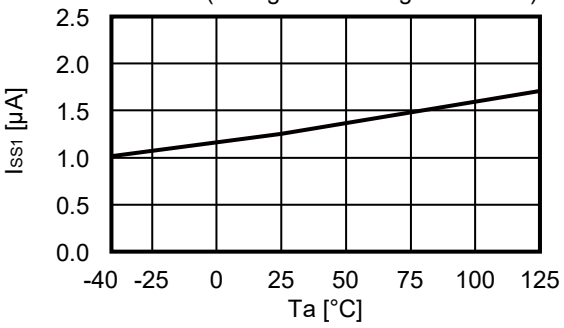
$V_{UVDET(S)}$ = 0.8 V, $V_{OVDET(S)}$ = 0.9 V,
V_{DD} = 5.0 V, V_{SENSE} = ($V_{UVREL(S)}$ + $V_{OVREL(S)}$) / 2,
V_{MR} = V_{DD} (during release)



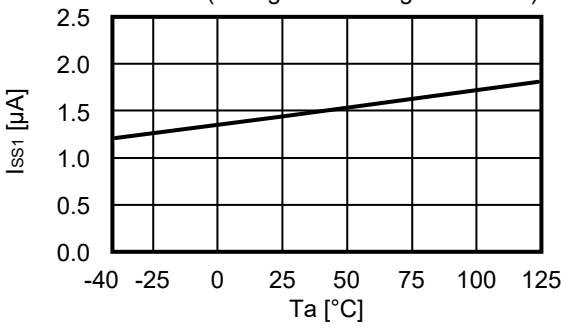
$V_{UVDET(S)}$ = 4.9 V, $V_{OVDET(S)}$ = 5.5 V,
V_{DD} = 5.0 V, V_{SENSE} = ($V_{UVREL(S)}$ + $V_{OVREL(S)}$) / 2,
V_{MR} = V_{DD} (during release)



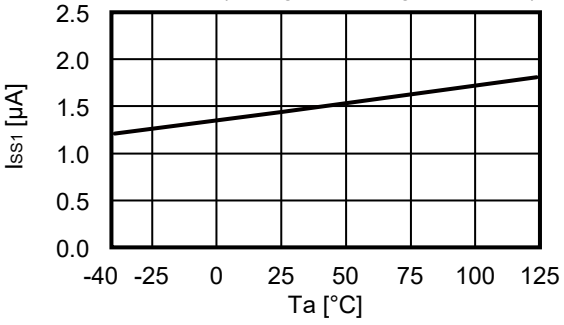
$V_{UVDET(S)}$ = 0.8 V, $V_{OVDET(S)}$ = 0.9 V,
V_{DD} = 5.0 V, V_{SENSE} = 0.0 V,
V_{MR} = V_{DD} (during undervoltage detection)



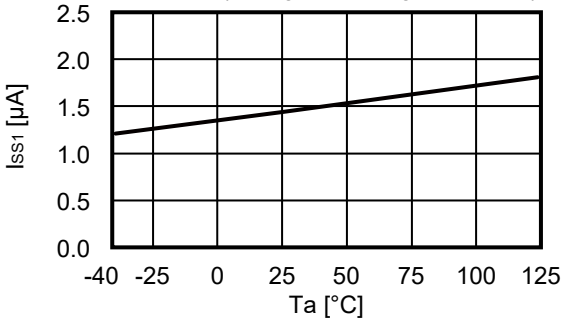
$V_{UVDET(S)}$ = 4.9 V, $V_{OVDET(S)}$ = 5.5 V,
V_{DD} = 5.0 V, V_{SENSE} = 3.9 V,
V_{MR} = V_{DD} (during undervoltage detection)



$V_{UVDET(S)}$ = 0.8 V, $V_{OVDET(S)}$ = 0.9 V,
V_{DD} = 5.0 V, V_{SENSE} = 1.9 V,
V_{MR} = V_{DD} (during overvoltage detection)

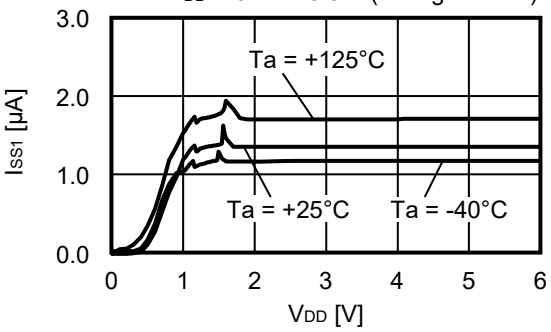


$V_{UVDET(S)}$ = 4.9 V, $V_{OVDET(S)}$ = 5.5 V,
V_{DD} = 5.0 V, V_{SENSE} = 6.0 V,
V_{MR} = V_{DD} (during overvoltage detection)

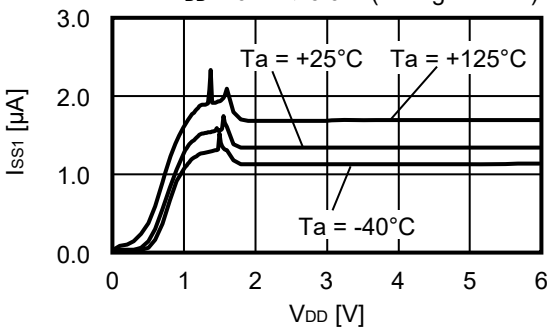


6. Current consumption (I_{SS1}) vs. Power supply voltage (V_{DD})

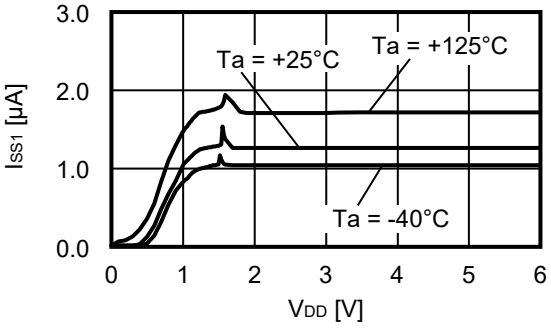
$V_{UVDET(S)}$ = 0.8 V, $V_{OVDET(S)}$ = 0.9 V,
V_{SENSE} = ($V_{UVREL(S)}$ + $V_{OVREL(S)}$) / 2,
V_{DD} = 0 V → 6.0 V (during release)



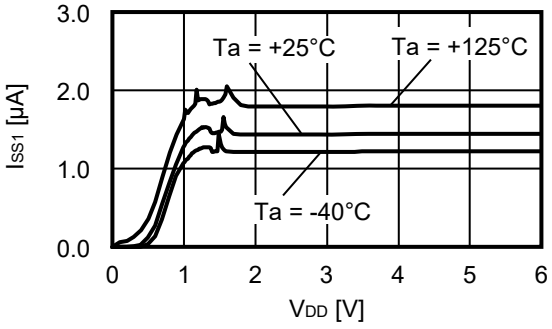
$V_{UVDET(S)}$ = 4.9 V, $V_{OVDET(S)}$ = 5.5 V,
V_{SENSE} = ($V_{UVREL(S)}$ + $V_{OVREL(S)}$) / 2,
V_{DD} = 0 V → 6.0 V (during release)



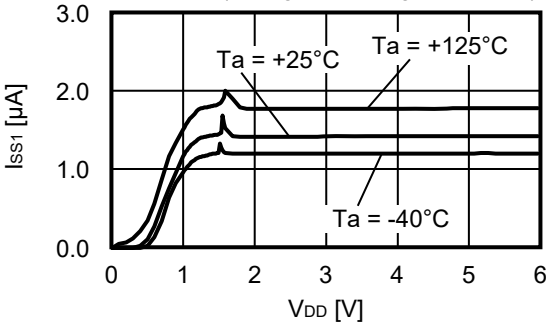
$V_{UVDET(S)}$ = 0.8 V, $V_{OVDET(S)}$ = 0.9 V,
V_{SENSE} = 0.0 V,
V_{DD} = 0 V → 6.0 V (during undervoltage detection)



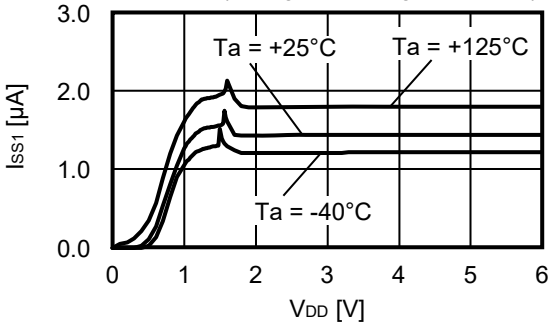
$V_{UVDET(S)}$ = 4.9 V, $V_{OVDET(S)}$ = 5.5 V,
V_{SENSE} = 3.9 V,
V_{DD} = 0 V → 6.0 V (during undervoltage detection)



$V_{UVDET(S)}$ = 0.8 V, $V_{OVDET(S)}$ = 0.9 V,
V_{SENSE} = 1.9 V,
V_{DD} = 0 V → 6.0 V (during overvoltage detection)

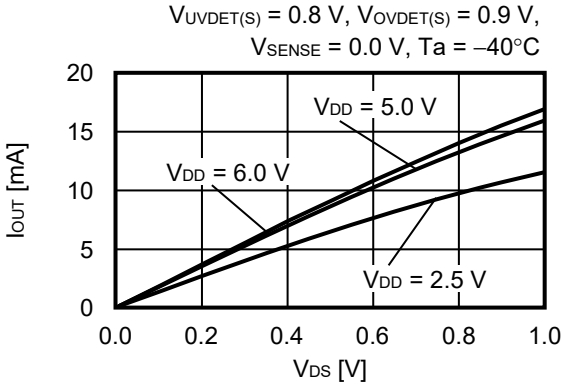


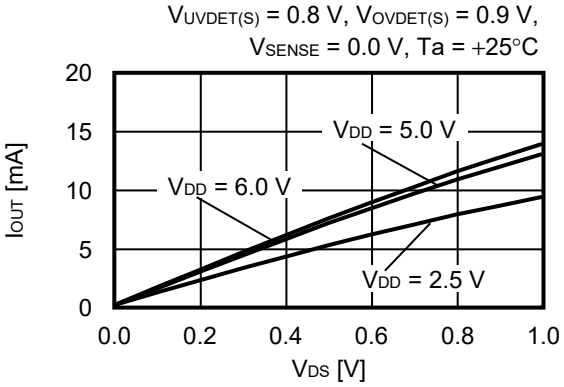
$V_{UVDET(S)}$ = 4.9 V, $V_{OVDET(S)}$ = 5.5 V,
V_{SENSE} = 6.0 V,
V_{DD} = 0 V → 6.0 V (during overvoltage detection)

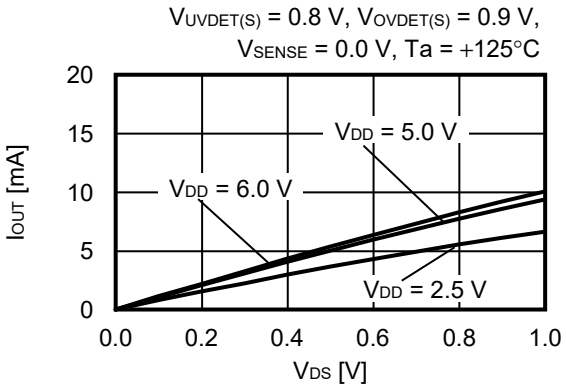


7. Nch transistor output current (I_{OUT}) vs. V_{DS}

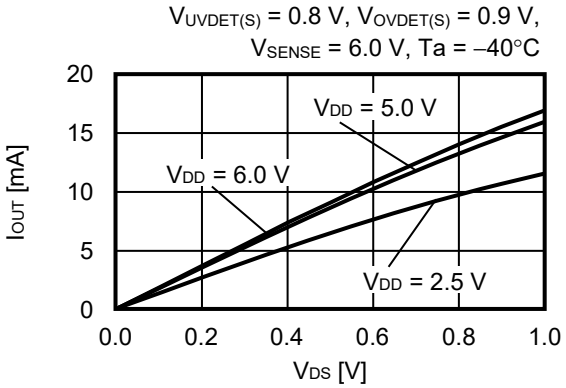
7. 1 Undervoltage detection

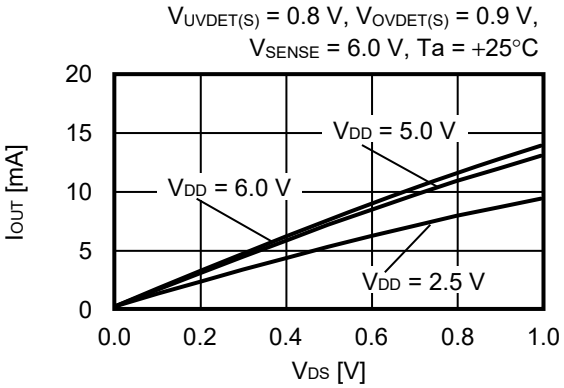


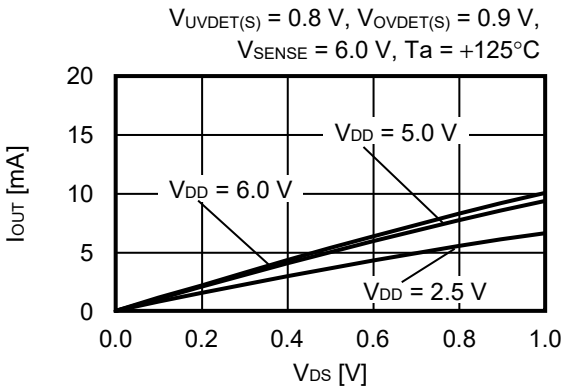




7. 2 Overvoltage detection



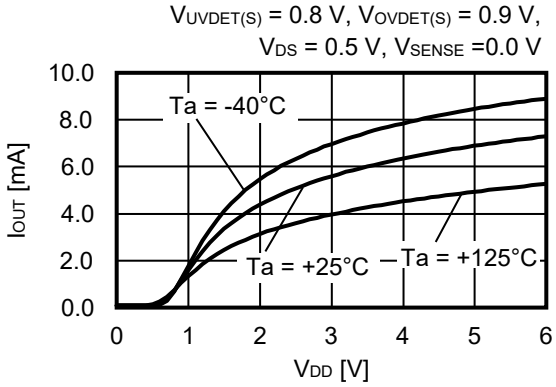




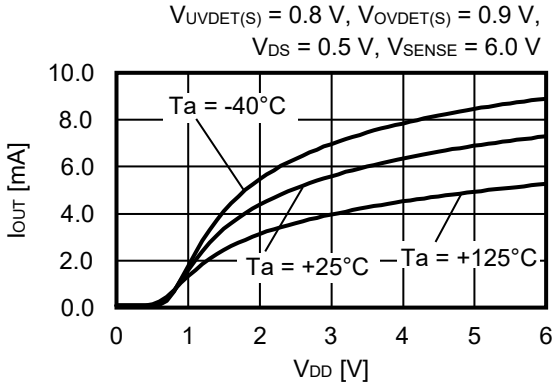
Remark V_{DS}: Drain-to-source voltage of the output transistor

8. Nch transistor output current (I_{OUT}) vs. Power supply voltage (V_{DD})

8. 1 Undervoltage detection



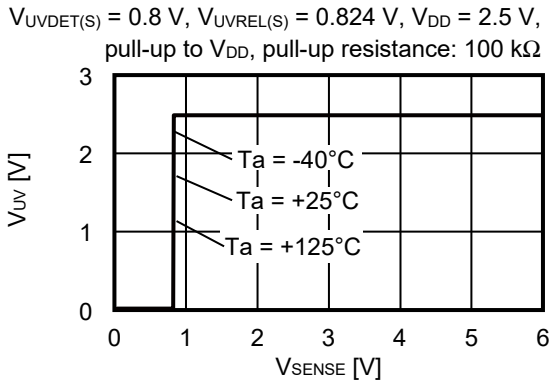
8. 2 Overvoltage detection

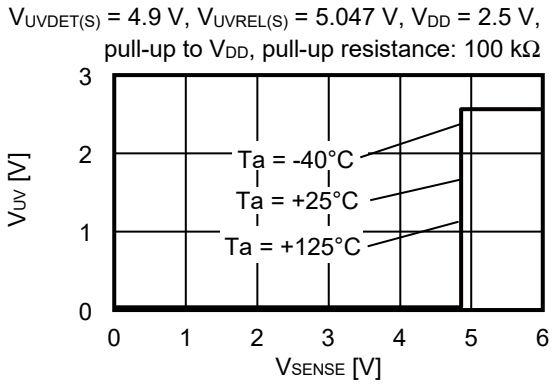


Remark V_{DS}: Drain-to-source voltage of the output transistor

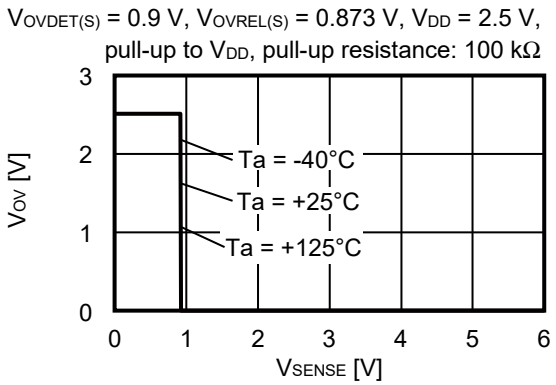
9. Output voltage (V_{UV}, V_{OV}) vs. SENSE pin voltage (V_{SENSE})

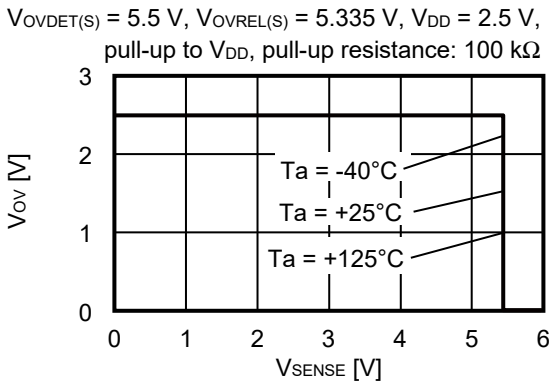
9. 1 Undervoltage detection





9. 2 Overvoltage detection

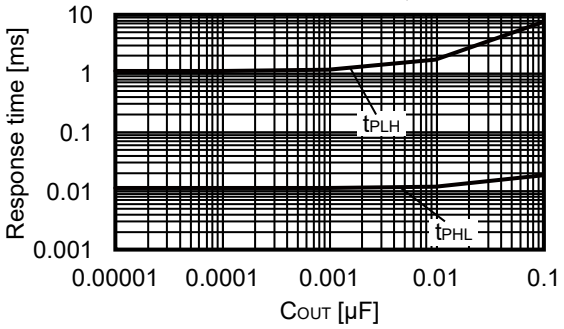




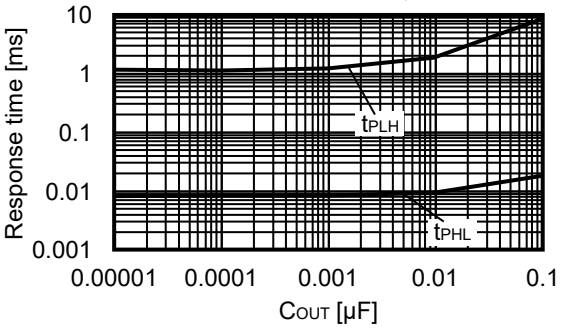
10. Dynamic response vs. Output pin capacitance (C_{OUT}) (CD pin = 0.33 nF)

10. 1 Undervoltage detection

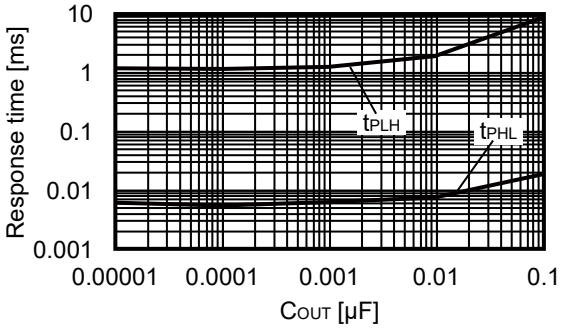
$V_{UVDET(S)}$ = 0.8 V, $V_{UVREL(S)}$ = 0.824 V,
V_{DD} = 5.0 V, Ta = –40°C



$V_{UVDET(S)}$ = 0.8 V, $V_{UVREL(S)}$ = 0.824 V,
V_{DD} = 5.0 V, Ta = +25°C

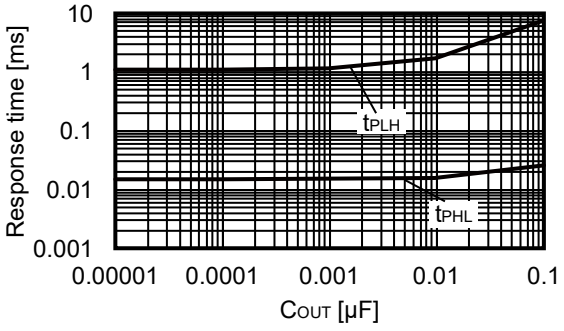


$V_{UVDET(S)}$ = 0.8 V, $V_{UVREL(S)}$ = 0.824 V,
V_{DD} = 5.0 V, Ta = +125°C

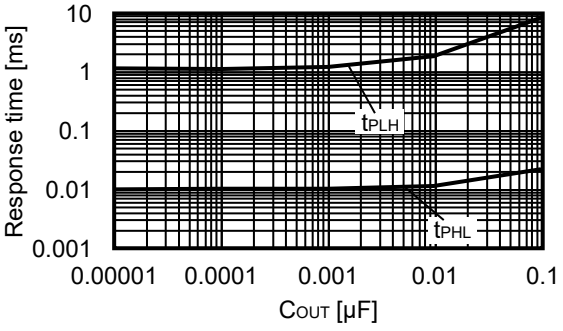


10. 2 Overvoltage detection

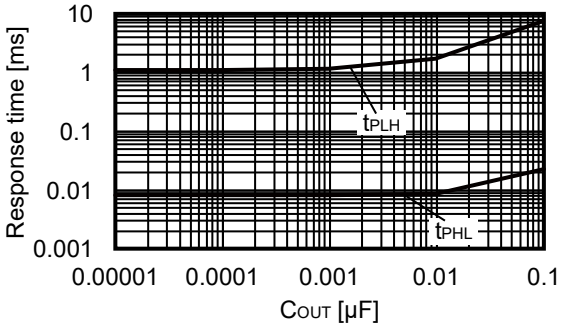
$V_{OVDET(S)}$ = 5.5 V, $V_{OVREL(S)}$ = 5.335 V,
V_{DD} = 5.0 V, Ta = –40°C

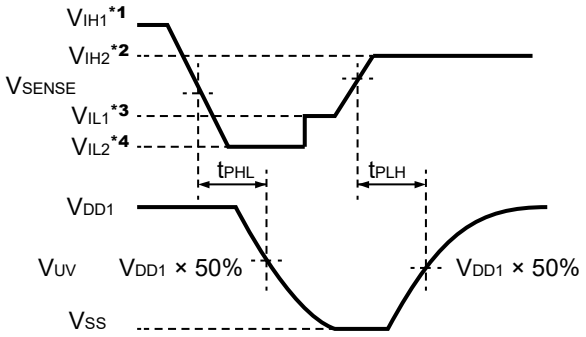


$V_{OVDET(S)}$ = 5.5 V, $V_{OVREL(S)}$ = 5.335 V,
V_{DD} = 5.0 V, Ta = +25°C



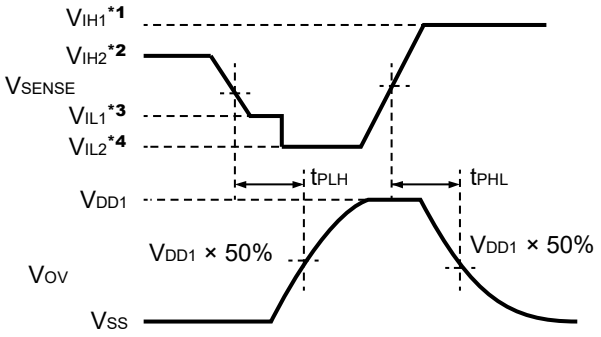
$V_{OVDET(S)}$ = 5.5 V, $V_{OVREL(S)}$ = 5.335 V,
V_{DD} = 5.0 V, Ta = +125°C





***1.** $V_{IH1} = V_{UVDET(S)} + 0.5$ V
***2.** $V_{IH2} = V_{UVREL(S)} \times 1.03$ V
***3.** $V_{IL1} = V_{UVREL(S)} - 0.5$ V
***4.** $V_{IL2} = V_{UVDET(S)} - 0.5$ V

Figure 44 Test Condition of Response Time (Undervoltage Detection)



***1.** $V_{IH1} = V_{OVDET(S)} + 0.5$ V
***2.** $V_{IH2} = V_{OVREL(S)} + 0.5$ V
***3.** $V_{IL1} = V_{OVDET(S)} \times 0.97$ V
***4.** $V_{IL2} = V_{OVREL(S)} - 0.5$ V

Figure 45 Test Condition of Response Time (Overvoltage Detection)

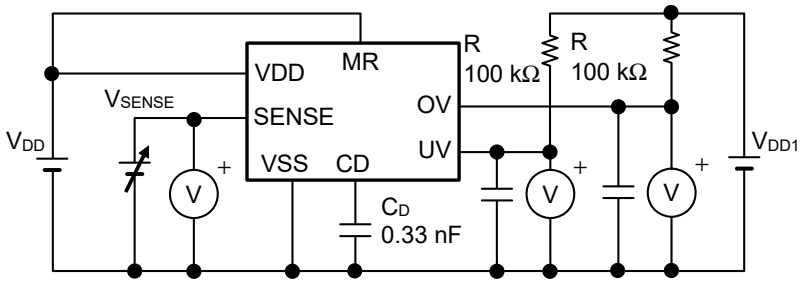


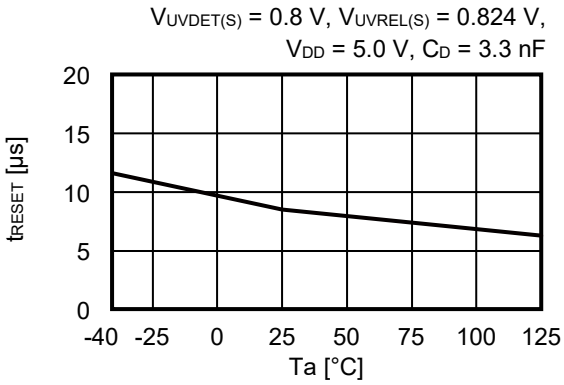
Figure 46 Test Circuit of Response Time

Caution 1. The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation including the temperature characteristics with an actual application to set the constants.
2. When the CD pin is open, a double pulse may appear at release.
To avoid the double pulse, attach 0.33 nF or more capacitor to the CD pin.

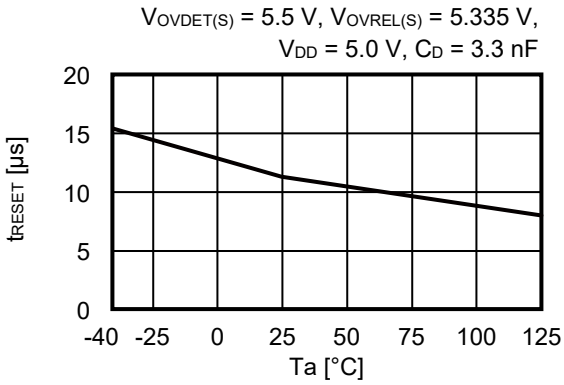
■ Reference Data

1. Detection response time (t_{RESET}) vs. Temperature (Ta)

1. 1 Undervoltage detection

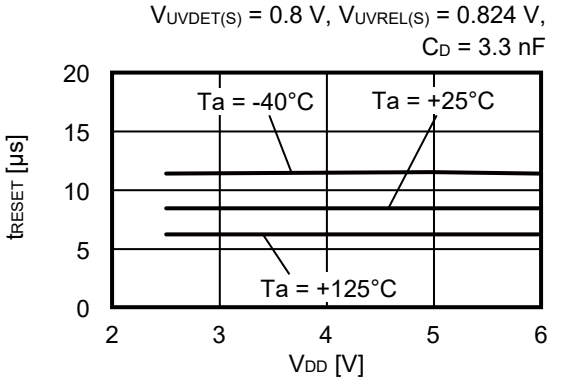


1. 2 Overvoltage detection

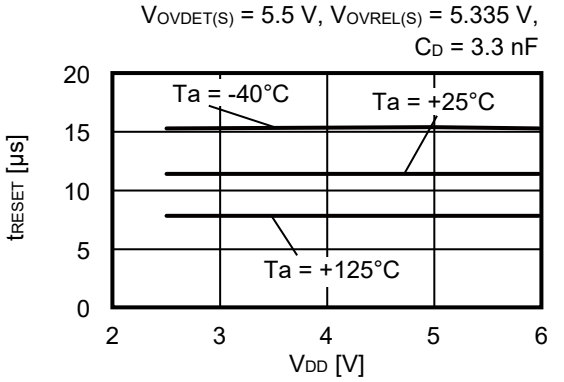


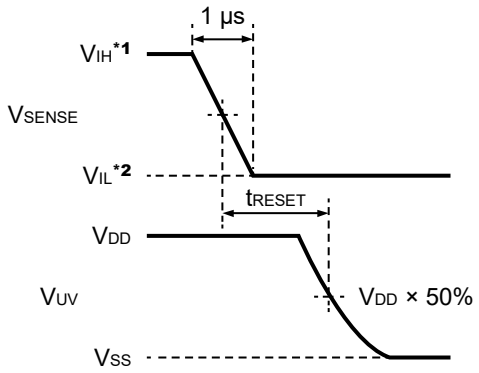
2. Detection response time (t_{RESET}) vs. Power supply voltage (V_{DD})

2. 1 Undervoltage detection



2. 2 Overvoltage detection





*1. $V_{IH} = V_{UVDET(S)} + 0.5$ V
*2. $V_{IL} = V_{UVDET(S)} - 0.5$ V

Figure 47 Test Condition of Detection Response Time (Undervoltage Detection)

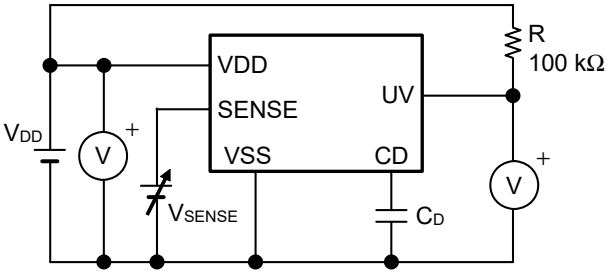
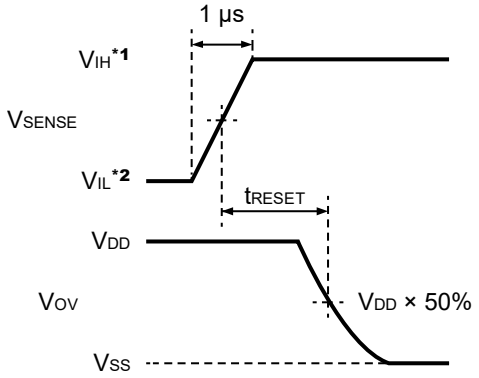


Figure 48 Test Circuit of Detection Response Time (Undervoltage Detection)



*1. $V_{IH} = V_{OVDET(S)} + 0.5$ V
*2. $V_{IL} = V_{OVDET(S)} - 0.5$ V

Figure 49 Test Condition of Detection Response Time (Overvoltage Detection)

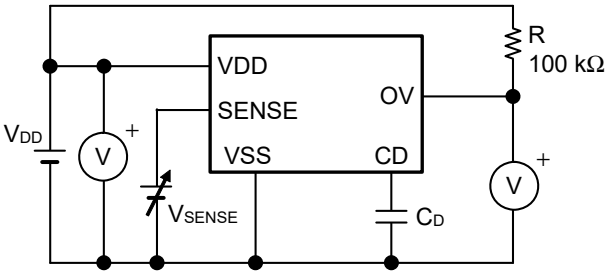
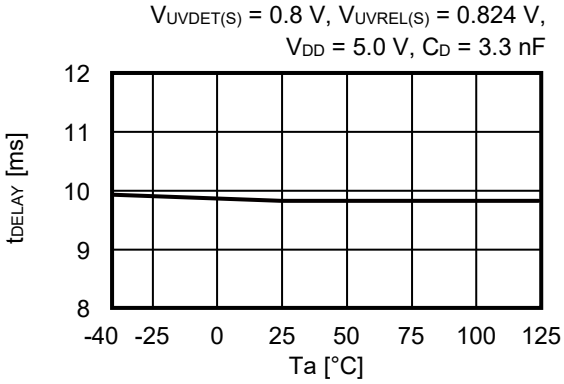


Figure 50 Test Circuit of Detection Response Time (Overvoltage Detection)

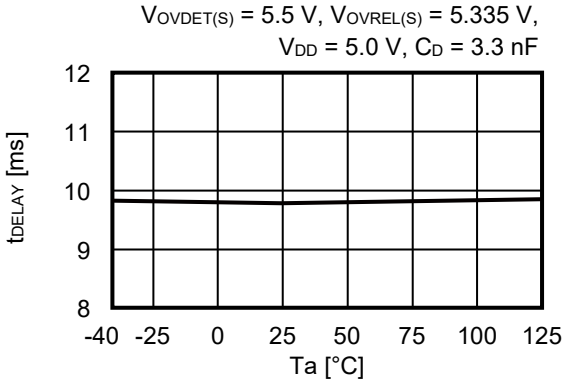
Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation including the temperature characteristics with an actual application to set the constants.

3. Release delay time (t_{DELAY}) vs. Temperature (Ta)

3. 1 Undervoltage detection

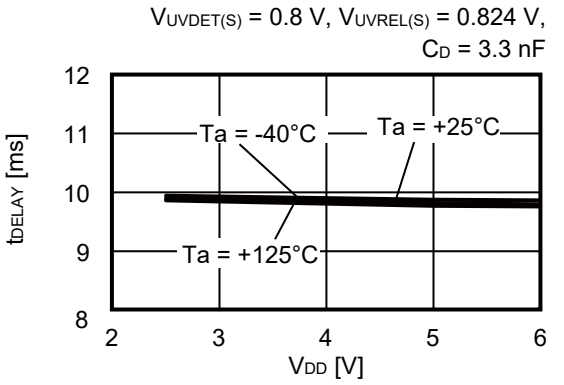


3. 2 Overvoltage detection

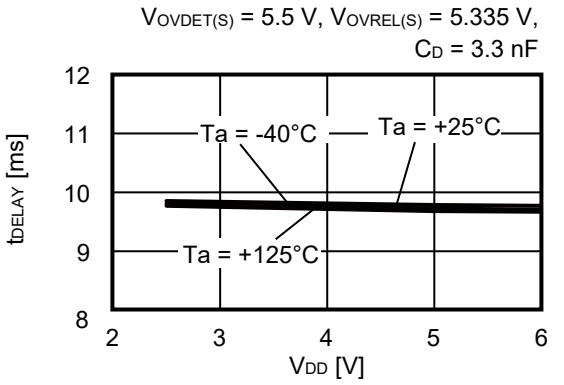


4. Release delay time (t_{DELAY}) vs. Power supply voltage (V_{DD})

4. 1 Undervoltage detection

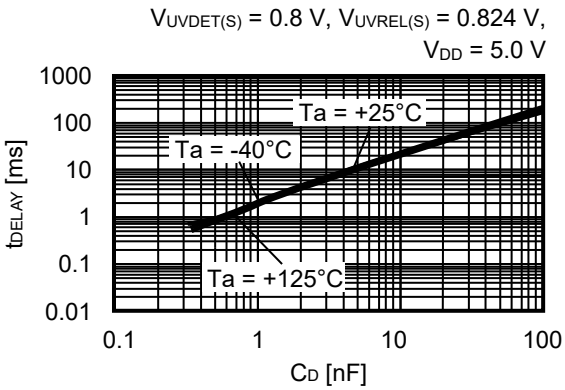


4. 2 Overvoltage detection

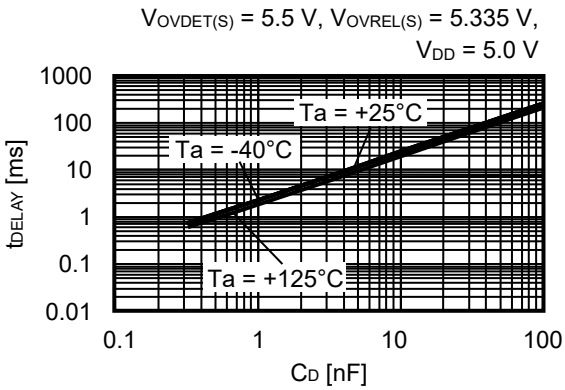


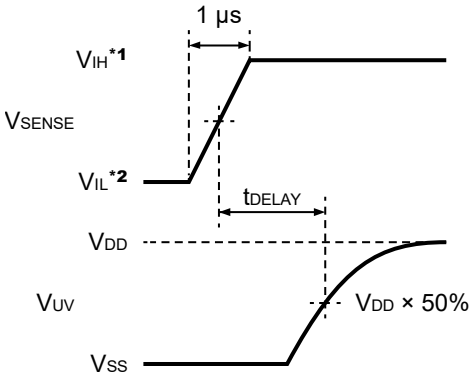
5. Release delay time (t_{DELAY}) vs. CD pin capacitance (C_D) (Without output pin capacitance)

5. 1 Undervoltage detection



5. 2 Overvoltage detection





*1. $V_{IH} = V_{UVREL(S)} \times 1.03$ V
*2. $V_{IL} = V_{UVREL(S)} - 0.5$ V

Figure 51 Test Condition of Release Delay Time (Undervoltage Detection)

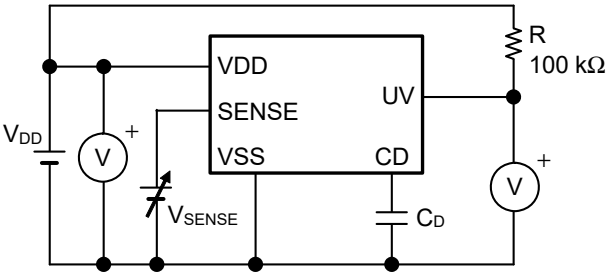
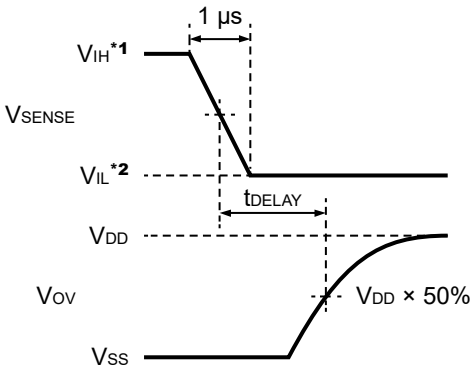


Figure 52 Test Circuit of Release Delay Time (Undervoltage Detection)



*1. $V_{IH} = V_{OVREL(S)} + 0.5$ V
*2. $V_{IL} = V_{OVREL(S)} \times 0.97$ V

Figure 53 Test Condition of Release Delay Time (Overvoltage Detection)

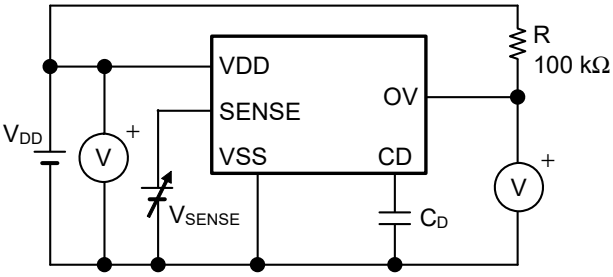
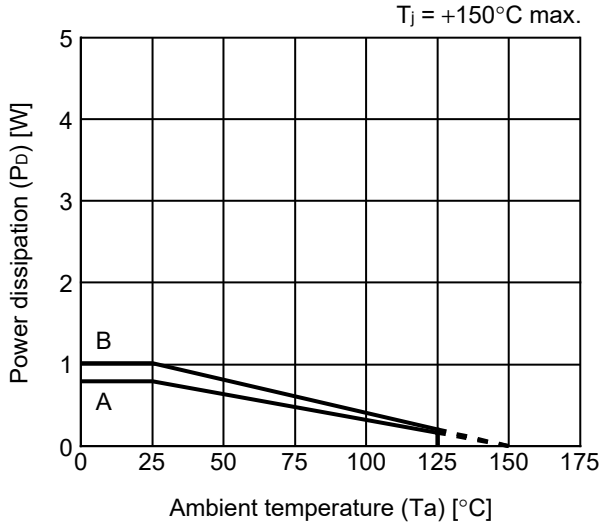


Figure 54 Test Circuit of Release Delay Time (Overvoltage Detection)

Caution 1. The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation including the temperature characteristics with an actual application to set the constants.
2. When the CD pin is open, a double pulse may appear at release.
To avoid the double pulse, attach 0.33 nF or more capacitor to the CD pin.

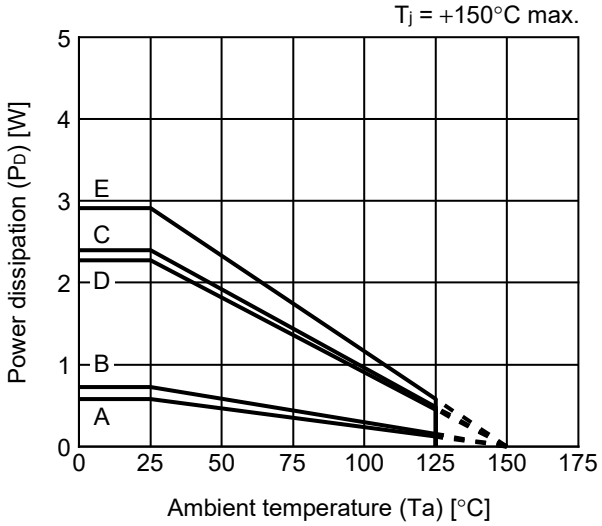
■ Power Dissipation

SOT-23-6



Board	Power Dissipation (P_D)
A	0.79 W
B	1.01 W
C	–
D	–
E	–

HSNT-8(1616)B

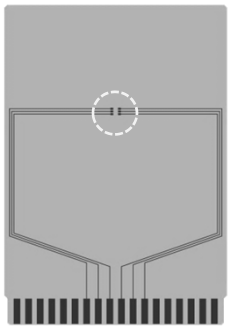


Board	Power Dissipation (P_D)
A	0.58 W
B	0.73 W
C	2.40 W
D	2.27 W
E	2.91 W

SOT-23-3/3S/5/6 Test Board

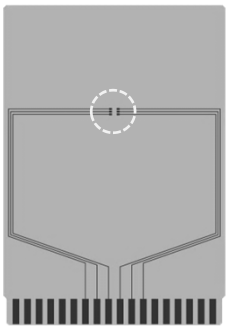
IC Mount Area

(1) Board A



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



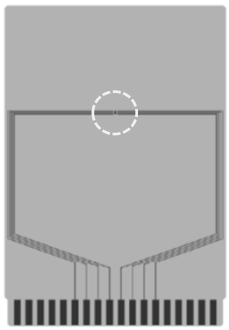
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

No. SOT23x-A-Board-SD-2.0

HSNT-8(1616)B Test Board

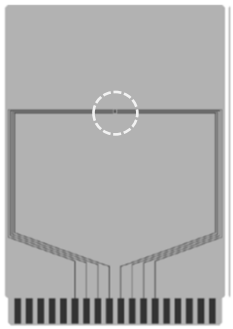
IC Mount Are

(1) Board A



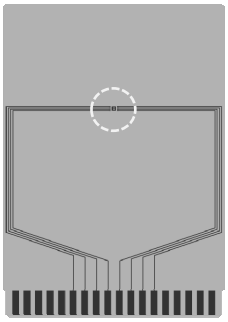
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C



enlarged view

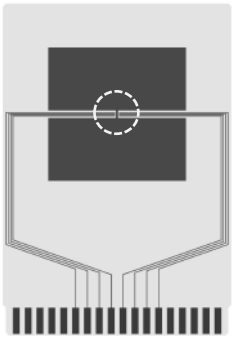
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

No. HSNT8-C-Board-SD-1.0

HSNT-8(1616)B Test Board

IC Mount Are

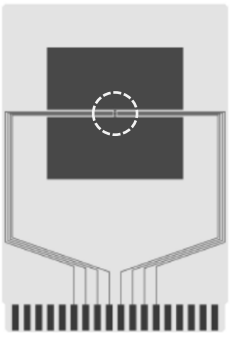
(4) Board D



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

enlarged view

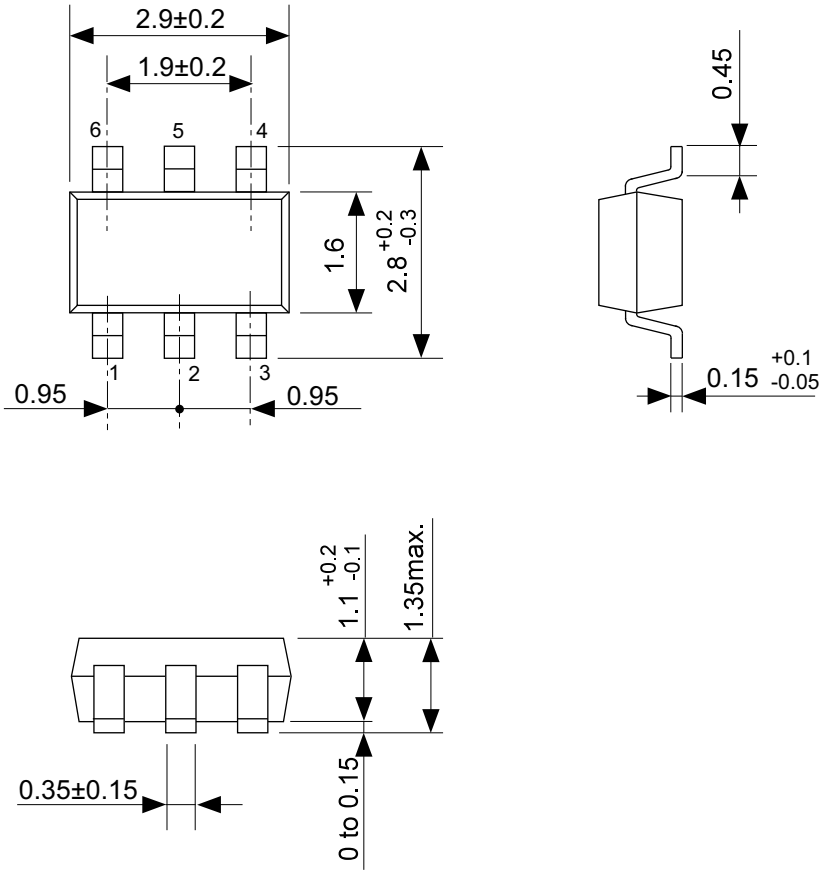
(5) Board E



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

enlarged view

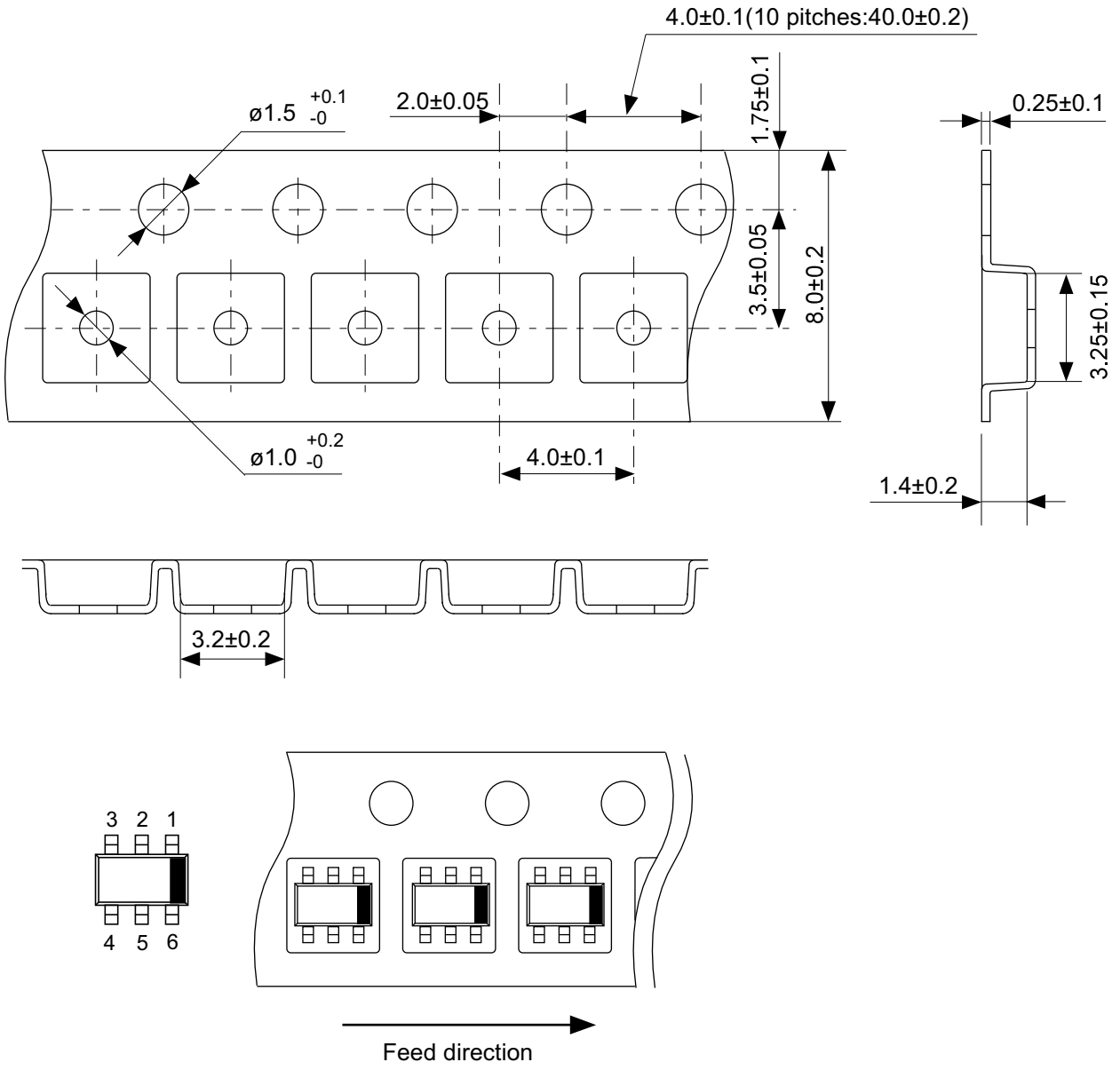
No. HSNT8-C-Board-SD-1.0



No. MP006-A-P-SD-2.1

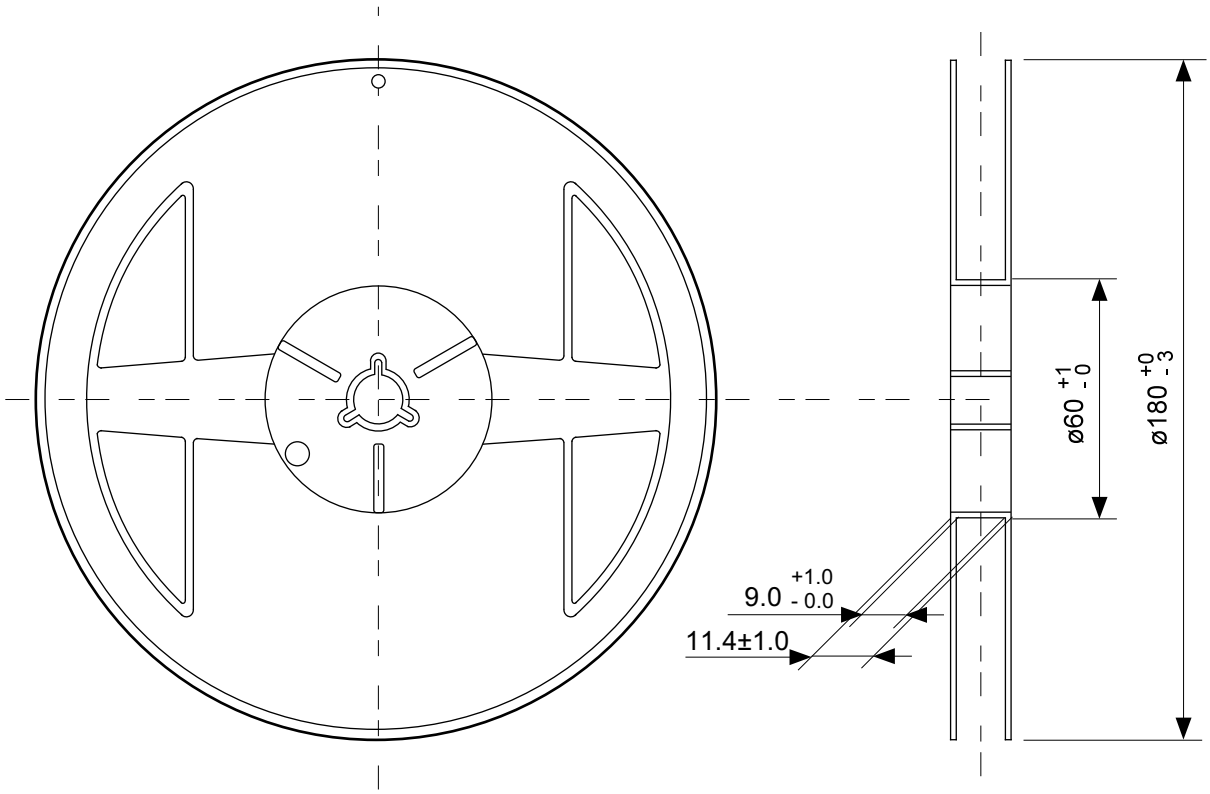
TITLE	SOT236-A-PKG Dimensions
No.	MP006-A-P-SD-2.1
ANGLE	
UNIT	mm

ABLIC Inc.

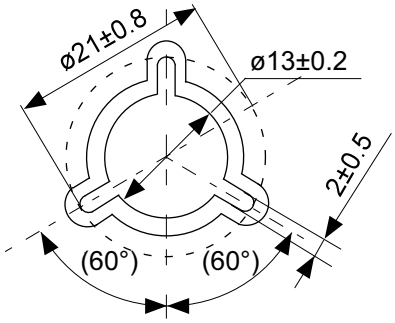


No. MP006-A-C-SD-3.1

TITLE	SOT236-A-Carrier Tape
No.	MP006-A-C-SD-3.1
ANGLE	
UNIT	mm
ABLIC Inc.	

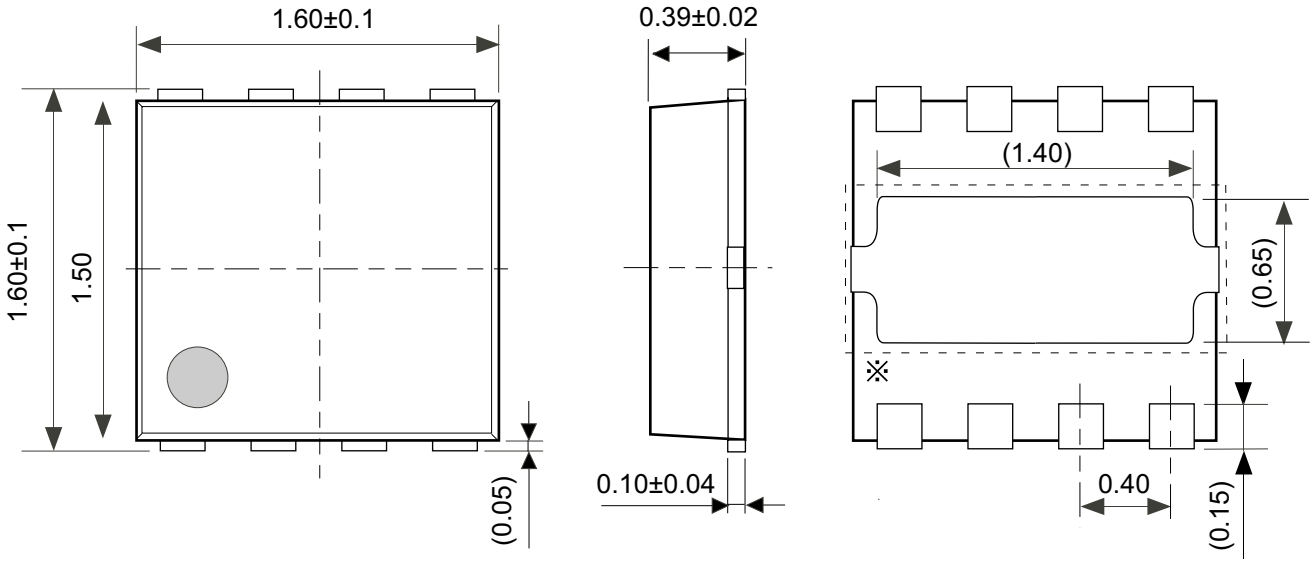


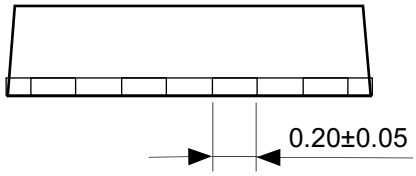
Enlarged drawing in the central part



No. MP006-A-R-SD-3.0

TITLE	SOT236-A-Reel		
No.	MP006-A-R-SD-3.0		
ANGLE		QTY	3,000
UNIT	mm		
ABLIC Inc.			

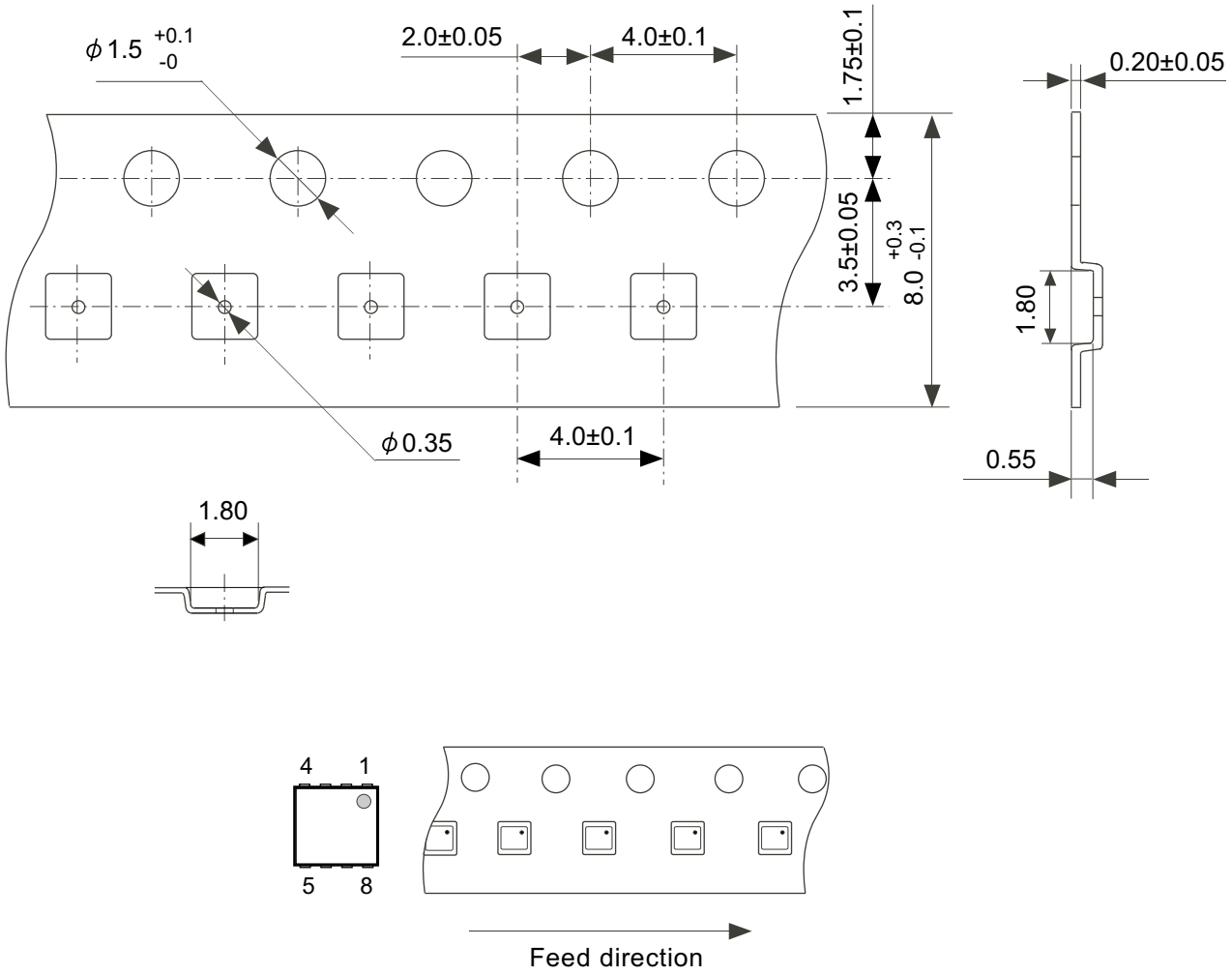




※ The heat sink of back side has different electric potential depending on the product.
Confirm specifications of each product.
Do not use it as the function of electrode.

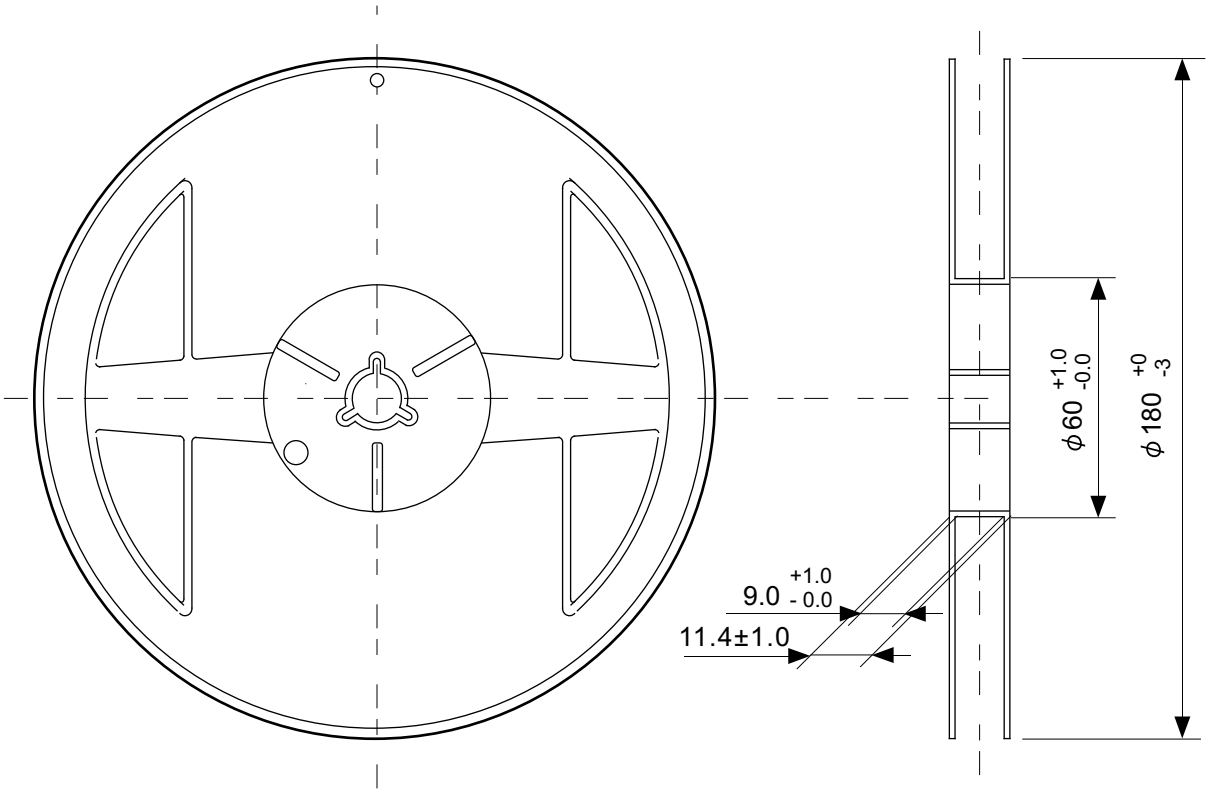
No. PY008-B-P-SD-1.0

TITLE	HSNT-8-C-PKG Dimensions
No.	PY008-B-P-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

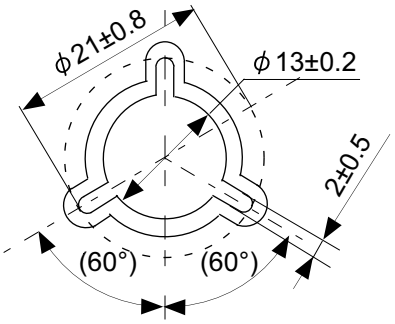


No. PY008-B-C-SD-1.0

TITLE	HSNT-8-C-Carrier Tape
No.	PY008-B-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	



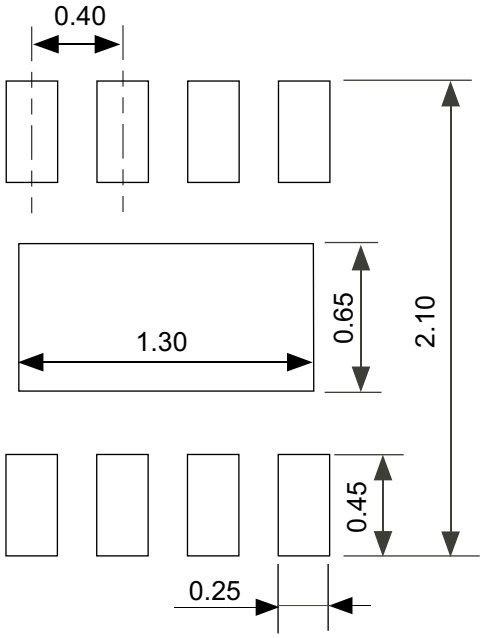
Enlarged drawing in the central part



No. PY008-B-R-SD-1.0

TITLE	HSNT-8-C-Reel		
No.	PY008-B-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			

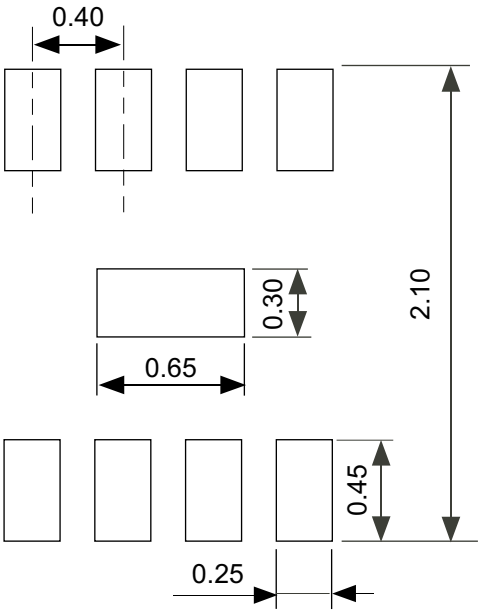
Land Pattern



Cauion It is recommended to solder the heat sink to a board in order to ensure the heat radiation.

注意 放熱性を確保する為に、PKGの裏面放熱板（ヒートシンク）を基板に半田付けする事を推奨いたします。

Metal Mask Pattern



Caution ① Mask aperture ratio of the lead mounting part is 100%.
② Mask aperture ratio of the heat sink mounting part is 20%.
③ Mask thickness: t0.10 mm

注意 ①リード実装部のマスク開口率は100%です。
②放熱板実装のマスク開口率は20%です。
③マスク厚み：t0.10 mm

No. PY008-B-L-SD-1.0

TITLE	HSNT-8-C -Land Recommendation
No.	PY008-B-L-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

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2.4-2019.07

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