High-Side or Low-Side Measurement, Bi-Directional Current and Power Monitor with 16 Bit ADC and Alert

General Description

The RT6056 is a high accuracy current-sense monitor with an I^2C and SMBUS interface, and the device provides full information for system by reading out the load current and power.

The device monitors both of the drops across sense resistor and the BUS voltage, converts into the current in amperes, and power in watts through internal analog-to-digital converter ADC. The programmable calibration, adjustable conversion time, and averaging function are also built in for more design flexibility.

The RT6056 provides a wide temperature environment from –40°C to 125°C and operates with an input voltage from 2.7V to 5.5V. The device senses the current on common-mode bus voltage with 0V to 36V.

The RT6056 also provides an alert function with open-drain output, and it provides the full protection by giving a warning to host from over-current, over-voltage and over-power situation.

The RT6056 is available in a small MSOP-10 package.

The recommended junction temperature range is –40°C to 125°C.

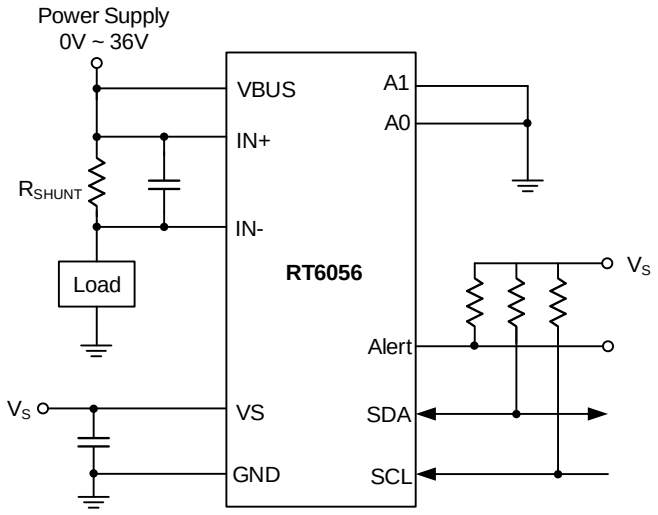
Features

- **I^2C and SMBUS Compatible Interface**
- **Bi-Direction Current Sensing, Available for High-Side or Low-Side Sensing**
- **2.7V to 5.5V Operation Supply Voltage Range**
- **Monitor Bus Voltage from 0V to 36V**
- **High Accuracy, Max 0.12% Gain Error**
- **Low Offset Voltage, Max 10μV Offset**
- **Current, Bus Voltage and System Power Reporting**
- **Programmable Warning Threshold**
- **Over-Current, Over-Voltage and Over-Power Alert**
- **MSOP-10 Package**

Applications

- Servers, Storage and Network Equipment
- Portable, Battery-Powered Systems
- Point of Load (POL) Power Modules
- Notebook Computers
- High End Digital TV

Simplified Application Circuit



Ordering Information

RT6056 □□

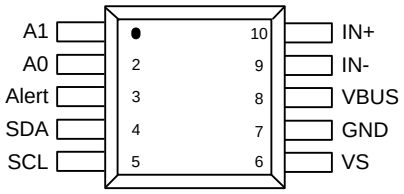
- Package Type
  F: MSOP-10
- Lead Plating System
  G: Richtek Green Policy Compliant

Note:

Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020

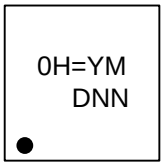
Pin Configuration

(TOP VIEW)



MSOP-10

Marking Information

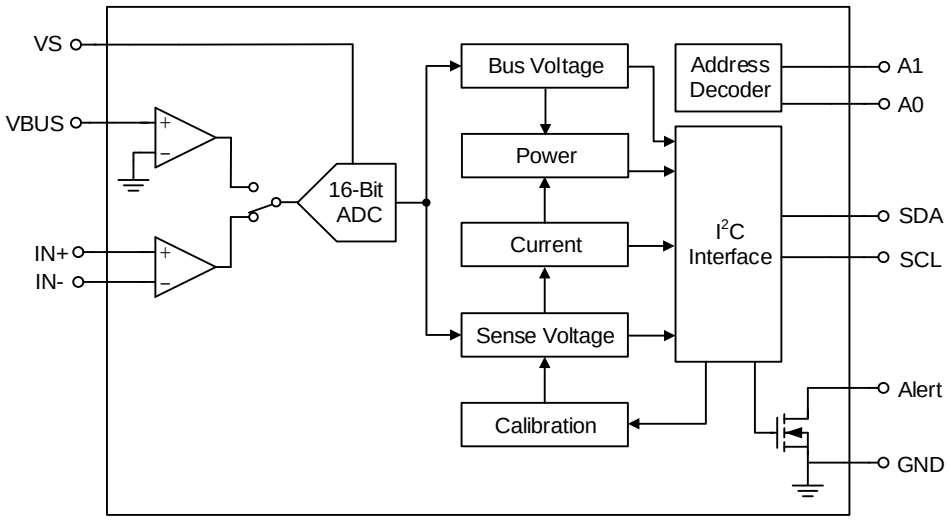


0H= : Product Code
YMDNN : Date Code

Functional Pin Description

Pin No.	Pin Name	I/O	Pin Function
1	A1	Digital Input	Address pin. Connect to GND, SCL, SDA, or VS.
2	A0	Digital Input	Address pin. Connect to GND, SCL, SDA, or VS.
3	Alert	Digital Output	Multi-functional alert, open-drain output.
4	SDA	Digital IN/OUT	Bi-directional serial data interface.
5	SCL	Digital Input	Serial clock interface.
6	VS	Power	Supply voltage, 2.7 V to 5.5 V. Connect a 0.1μF capacitor as close to the VS pin as possible.
7	GND	Ground	Ground.
8	VBUS	Analog Input	Bus voltage input.
9	IN-	Analog Input	Negative current-sensing input. Connect load side to external sense resistor.
10	IN+	Analog Input	Positive current-sensing input. Connect power side to external sense resistor.

Functional Block Diagram



Operation

The RT6056 is a high-side/low-side current and power monitor with an integrated 16-bit ADC and an internal open-drain for alert indicator. The device is ideal for a variety of industrial and telecom equipment applications.

The RT6056 operates over a wide 0V to 36V input common-mode voltage range, and an internal 16-bit integrating analog-to-digital converter (ADC) allows the user to read data such as voltage, current and power. The full-scale voltage from -81.9175mV 81.92mV and calibration function allow for a wide dynamic range current measurement and application flexibility in choosing sense resistor values.

Mode Configuration

RT6056 provides ADC configuration function through Configuration Register (00h); the device includes all-register reset, ADC conversion times, averaging mode and operating mode configuration.

The device has several operating modes for ADC operation, including continuous mode, trigger mode and shutdown mode; when the device is in default operating mode (continuous mode), it continuously converts the sense voltage and bus voltage; after the voltage is read, the current is calculated by the value of calibration setting and further used to calculate the power.

When the device operates in trigger mode, the data in the registers remains; the ADC only executes data updating after the Configuration Register (00h) executes a new “WRITE” format.

The device also provides shutdown mode to reduce the input quiescent current; when the device operates in shutdown mode, the write and read are available for the register. The device keeps in shutdown mode until one of the continuous mode or triggered mode is selected.

Conversion Time and Averaging

RT6056 provides configurable conversion time and averaging time through Configuration Register (00h); it allows the user to optimize the design according to the accuracy and system-timing requirement. The conversion time setting for both of sense voltage and bus voltage can be selected from 139μs to 8.205ms; the longer conversion time results in higher noise immunity, but it needs more time for data updating. Figure 1 shows the performance of noise vs. conversion time.

The averaging function also improves the measurement accuracy by effectively filtering the signal. This approach allows the device to reduce any noise in the measurement that may be caused by noise coupling into the signal. A greater number of averages enables the device to be more effective in reducing the noise component of the measurement.

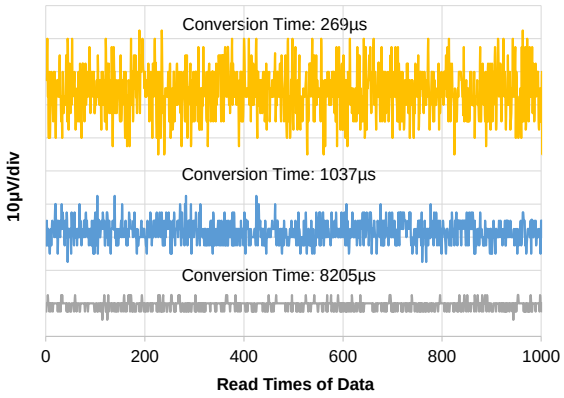


Figure 1. Noise vs. Conversion Time

Calibration and Current Calculation

The Calibration Register (05h) is calculated based on the shunt resistor and required current resolution; the equation is shown as below :

$$\text{Calbration Setting (dec)} = \frac{0.00512}{R_{SHUNT} \times I_{LSB}}$$

Where

- 0.00512 is an internal fixed value
- I_{LSB} is the resolution of measurement current

The highest resolution for the Current Register (04h) can be obtained by using the smallest allowable Current_LSB based on the maximum output current, the equation is shown as below :

$$\text{Current resolution} = \frac{\text{Maximum Current}}{2^{15}}$$

While the highest resolution is lower than the expected resolution, it is common to select a value for the Current_LSB to the nearest round number and above the highest resolution to simplify the conversion of the Current in amperes and power in watts respectively.

After programming the Calibration Register (05h), the

Current Register (04h) is calculated by multiplying the decimal value of the Sense Voltage Register (01h) contents by the decimal value of the Calibration Register and then dividing by 2048; the equation is shown as below :

$$\text{Current} = \frac{\text{Sense Voltage} \times \text{Calbration Setting}}{2048}$$

After the device power on, the Current Register (04h) and Power Register (03h) remain at zero, Current Register (04h) and Power Register (03h) update based on the corresponding sense voltage and bus voltage.

Power Calculation

After the Current Register (04h) update, the power is calculated by multiplying the decimal value of the Bus Voltage Register (02h) contents by the decimal value of the Current Register and then dividing by 20000, the equation is shown as below :

$$\text{Power} = \frac{\text{Bus Voltage} \times \text{Current}}{20000}$$

Programing Example

Table 1. shows an example for register data in real application.

Table 1. Power Calculation Procedure

Conditions : V_{CM} = V_{BUS} = 12V, R_{SHUNT} = 2mΩ, Load current = 10A						
Procedure	**Register**	**Address**	**Data (Hex)**	**Data (Dec)**	**LSB**	**Value**
Step 1	Configuration	00h	4127	--	--	--
Step 2	Sense Voltage	01h	1F40	8000	2.5μV	20mV
Step 3	Bus Voltage	02h	2580	9600	1.25mV	12V
Step 4	Calibration	05h	A00	2560	--	--
Step 5	Current	04h	2710	10000	1mA	10A
Step 6	Power	03h	12C0	4800	25mV	120W

Alert Indicator

The RT6056 provides a flexible response function that can be approached by multi-functional indicator pin; the user can monitor five alert functions or conversion Ready notification through the Mask/Enable register (06h), and the threshold can be programed in the Alert Limit Register (07h). From the Mask/Enable register (06h), one of the five alert events can be selected at a time, when the monitoring event selected in the Mask/Enable register exceeds the values programing in the Alert Limit Register (07h), the open-drain output of Alert pin is pulled low. The five alert functions are listed below :

- Sense Voltage Over-Limit (SOL)
- Sense Voltage Under-Limit (SUL)
- Bus Voltage Over-Limit (BOL)
- Bus Voltage Under-Limit (BUL)
- Power Over-Limit (POL)

If multiple alert functions are enabled, the selected function in the highest significant bit position takes priority and responds to the Alert Limit Register value. For example, if the Sense Voltage Over-Limit function and the Sense Voltage Under-Limit function are selected at the same time, the Alert pin asserts when the Sense Voltage Register exceeds the value in the Alert Limit Register.

RT6056 asserts warning alert by comparing the “mathematics value”. The sign bit is also considered, which means when the indicator is set to response sense voltage over-Limit (SOL), the positive value is always higher than negative value. The examples are shown in Figure 2.

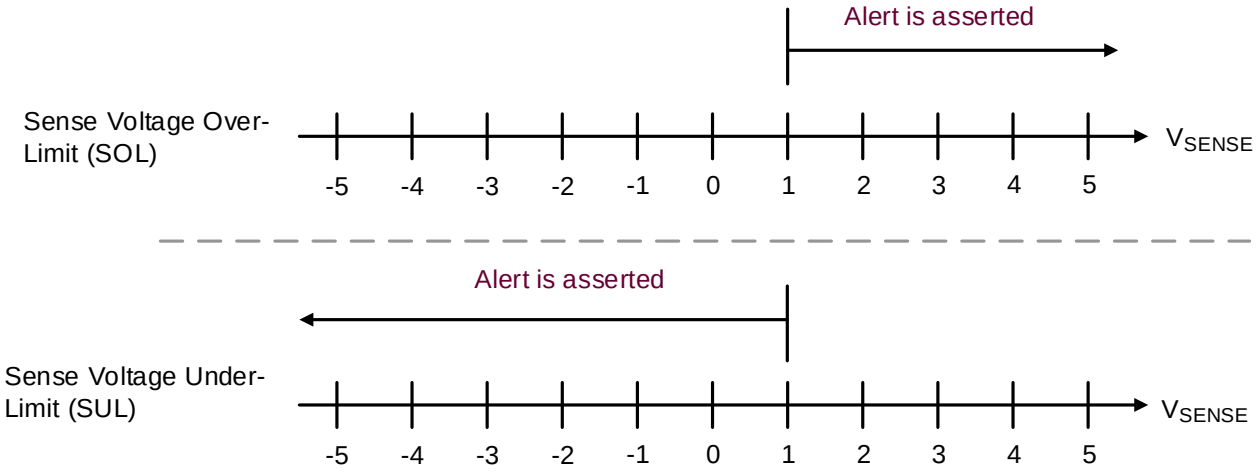


Figure 2. Alert Pin Response to SOL and SUL When the Alert Limit Register (07h) is Set to 1

Conversion Ready Indicator

The Conversion Ready state of the device can also be monitored at the Alert pin to inform the user when the device has completed the previous conversion and is ready to begin a new conversion. Conversion Ready can be monitored at the Alert pin along with one of the alert functions. If an alert function and the Conversion Ready are both enabled to be monitored at the Alert pin, after the Alert pin is asserted, the Mask/Enable Register must be read following the alert to determine the source of the alert. By reading the Conversion Ready Flag (CVRF, bit3), and the Alert Function Flag (AFF, bit 4) in the Mask/Enable Register, the source of the alert can be determined. If the Conversion Ready feature is not desired and the CNVR bit is not set, the Alert pin only responds to an exceeded alert limit based on the alert function enabled.

If the alert function is not used, the Alert pin can be left floating without impacting the operation of the device.

Digital Interface

The RT6056A supports general-purpose serial interface to I^2C bus and SMBus to control and monitor the configuration registers. The device supports the protocol with fast mode (1kHz to 400kHz), and high-speed mode (1kHz to 2940kHz).

Table 2 shows the timing requirements in fast mode and high-speed mode.

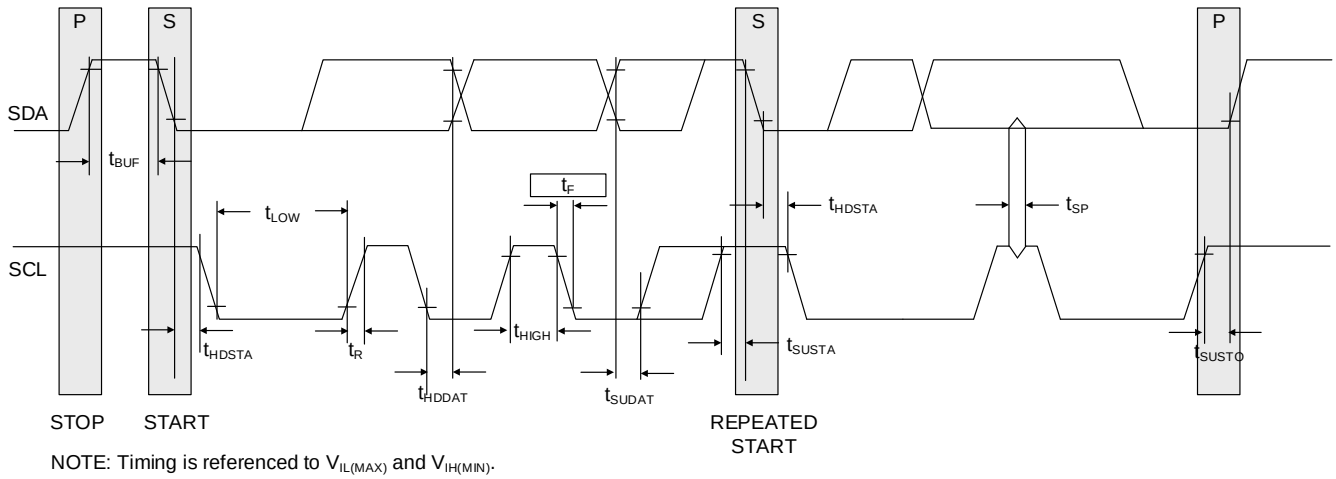


Figure 3. Bus Timing Diagram

Table 2. Timing Requirements

Parameter	Symbol	FAST MODE		HIGH-SPEED MODE		Unit
		Min	Max	Min	Max	
SCL Clock Rate	f_{SCL}	1	400	1	2940	kHz
Hold Time (Repeated) Start Condition. After this period, the first clock is generated.	t_{HDSTA}	0.1	--	0.1	--	µs
Low Period of the SCL Clock	t_{LOW}	1.3	--	0.2	--	µs
High Period of the SCL Clock	t_{HIGH}	0.6	--	0.06	--	µs
Set-Up Time for a Repeated START Condition	t_{SUSTA}	0.1	--	0.1	--	µs
Data hold time	t_{HDDAT}	10	900	10	100	ns
Data set-up time	t_{SUDAT}	100	--	20	--	ns
Set-Up Time for STOP Condition	t_{SUSTO}	0.1	--	0.1	--	µs
Bus Free Time Between STOP and START Condition	t_{BUF}	0.6	--	0.16	--	µs
Clock fall time	t_F	--	300	--	80	ns
Data fall time	t_F	--	300	--	40	ns
Clock rise time	t_R	--	300	--	40	ns
Data rise time for $f_{SCL} \leq 100kHz$	t_R	--	1000	--	--	ns

Serial Bus Address

16 distinct slave addresses are configurable using two pins for address configuration, A1 and A0; the system is able to control maximum 16 ICs of RT6056 in one I^2C bus. The device samples the state of pins A0 and A1 on every bus communication. Configure the slave address before any activity on the interface occurs. Table 3 lists the 16 addresses with A1/A0 pins combination.

Table 3. Slave Addresses Selection

A1	A0	Slave Address	Slave Address (Hex)
GND	GND	1000000	40
GND	VS	1000001	41
GND	SDA	1000010	42
GND	SCL	1000011	43
VS	GND	1000100	44
VS	VS	1000101	45
VS	SDA	1000110	46
VS	SCL	1000111	47
SDA	GND	1001000	48
SDA	VS	1001001	49
SDA	SDA	1001010	4A
SDA	SCL	1001011	4B
SCL	GND	1001100	4C
SCL	VS	1001101	4D
SCL	SDA	1001110	4E
SCL	SCL	1001111	4F

Write Protocol

The master begins communication with a START condition followed by the 7-bit slave address with the R$\overline{W}$ bit set to low. The RT6056 acknowledges the address and then the master sends a command byte indicates the address of the register. The RT6056 acknowledges the command byte and then updates the register pointer into the desired register. The master then delivers the next two data bytes to the register addressed by the register pointer, and the RT6056 acknowledges receipt of each data byte. The transmission is ended when the master sends a start or stop condition.

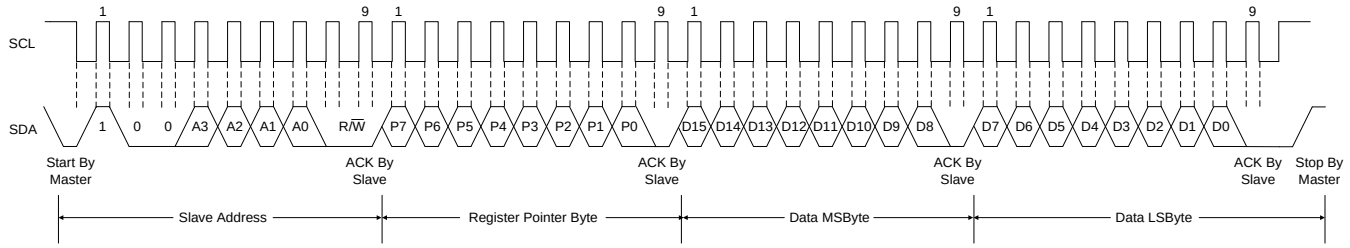


Figure 4. Timing Diagram for Write Word Format

Read Protocol

The master begins a read operation with a START condition followed by the 7-bit slave address and the R$\overline{W}$ bit set to low. During read operation, the last value stored in the register pointer by a write operation determines which register is read. To change the register pointer for a read operation, a new value must be written to the register

pointer.

This write is accomplished by issuing a slave address byte with the $R\overline{W}$ bit low, followed by the register pointer byte. No additional data are required. The master then generates a start condition and sends the slave address byte with the $R\overline{W}$ bit high to initiate the read command. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the register pointer. This byte is followed by an Acknowledge from the master; then the slave transmits the least significant byte. The master acknowledges receipt of the data byte. The master may terminate data transfer by generating a Not-Acknowledge after receiving any data byte, or generating a start or stop condition. If repeated reads from the same register are desired, it is not necessary to continually send the register pointer bytes; the device retains the register pointer value until it is changed by the next write operation.

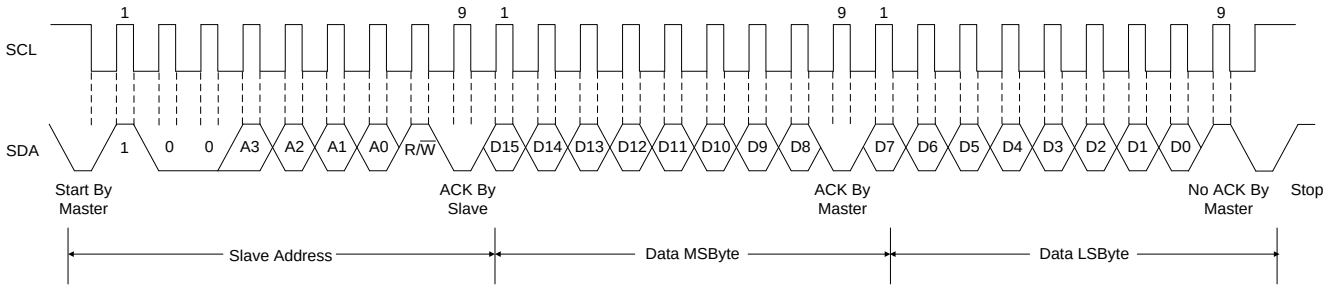


Figure 5. Timing Diagram for Read Word Format

SMBus Alert Response

The SMBus-alert feature provides a quick method to identify alarming devices on a shared interrupt. Upon receiving an interrupt signal, the Master can broadcast a receive byte request to the alert-response slave address. Any slave device that generates an interrupt attempts to identify itself by putting its own address on the bus. The alert response can activate several different slave devices simultaneously. If more than one slave attempts to respond, bus arbitration rules apply, and the device with the lower address wins a consequence of the open-collector bus. The losing device does not generate an acknowledgement and continues to hold the Alert pin low until serviced. Successful reading of the alert response address de-asserts Alert indicator.

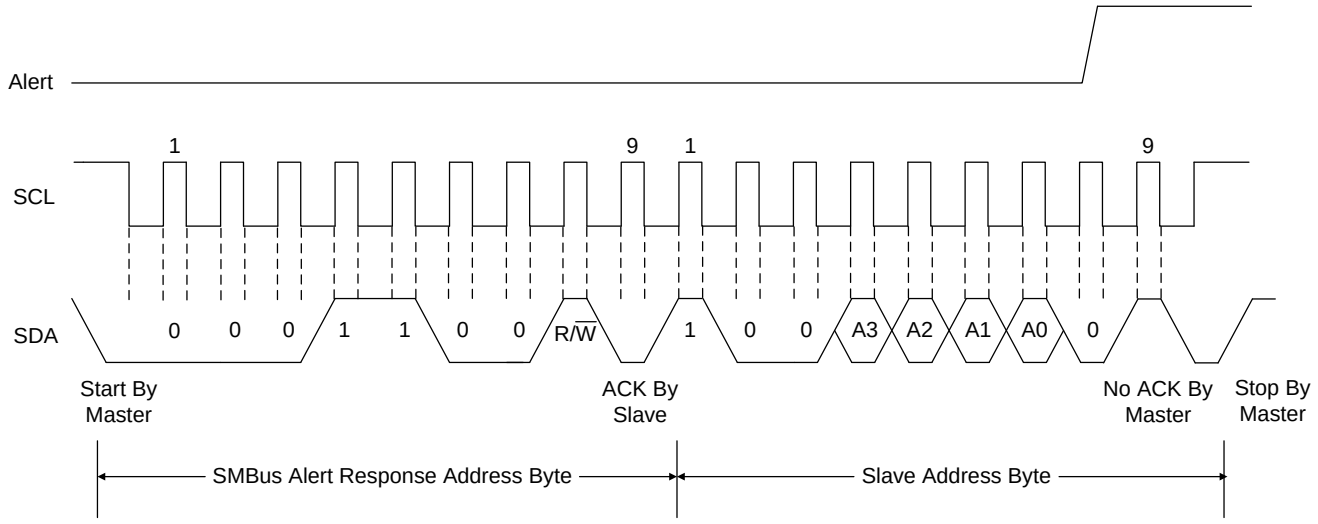


Figure 6. Timing Diagram for SMBus Alert

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_S ---------- –0.3V to 6V
- Power Sensing Pins, Common Mode (V_{IN+} + V_{IN-}) / 2, V_{CM} ---------- –0.3V to 40V
- Power Sensing Pins, different mode (V_{IN+} - V_{IN-}), V_{SENSE} (Note 2) ---------- –40V to 40V
- Bus Voltage, V_{BUS} ---------- –0.3V to 40V
- Other Pins, ---------- –0.3 to 6V
- Input Current into any Pin, I_{IN} ---------- 5mA
- Open-Drain Digital Output Current, I_{OUT} ---------- 10mA
- Power Dissipation, P_D @ T_A = 25°C

  MSOP-10 ---------- 0.51W
- Package Thermal Resistance (Note 3)

  MSOP-10, θ_{JA} ---------- 195°C/W

  MSOP-10, θ_{JC} ---------- 64°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 5)

- Common-Mode Input Voltage, V_{CM} ---------- 12V
- Operating Supply Voltage, V_S ---------- 3.3V
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_S = 3.3V, V_{IN+} = 12V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0mV and V_{BUS} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply						
Operating Supply Range	V_S		2.7	--	5.5	V
Quiescent Current	I_Q		--	550	650	μA
	I_{Q_SD}	power-down (shutdown) mode	--	3.5	6	μA
Power-On Reset Threshold	V_{POR}		--	2	--	V
Input						
Sense Voltage Input Range	V_{SENSE}		–81.92	--	81.92	mV
Bus Voltage Input Range	V_{BUS}		0	--	36	V
Common-Mode Rejection (Note 7)	CMRR	0 V ≤ V_{IN+} ≤ 36 V	126	140	--	dB

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Sense Offset Voltage, RTI	V_{S_OS}		--	±2.5	±10	μV
Sense Offset Voltage, RTI vs Power Supply	PSRR	2.7 V ≤ V_S ≤ 5.5 V	--	2.5	--	μV/V
Bus Offset Voltage, RTI	V_{B_OS}		--	±1.25	±7.5	mV
Bus Offset Voltage, RTI vs Power Supply (Note 7)	PSRR	2.7 V ≤ V_S ≤ 5.5 V	--	0.5	--	mV/V
Input Bias Current (I_{IN}+ or I_{IN}– pins)	I_B		--	35	--	μA
VBUS Input Impedance			--	830	--	kΩ
Input Leakage		(IN+ pin) + (IN– pin), power-down mode	--	0.1	0.5	μA
DC Accuracy						
ADC Native Resolution			--	16		Bits
1 LSB Step Size		Sense voltage	--	2.5		μV
		Bus voltage	--	1.25		mV
Sense Voltage Gain Error			--	0.02	0.12	%
Sense Voltage Nonlinearity			--	0.05	--	%
Bus Voltage Gain Error			--	0.02	0.4	%
Bus Voltage Nonlinearity (Note 7)			--	0.05	--	%
ADC Conversion Time, Continuous Mode	t_{CT1}	bit = 000	--	139	--	μs
		bit = 001	--	203	--	μs
		bit = 010	--	269	--	μs
		bit = 011	--	525	--	μs
		bit = 100	--	1037	--	μs
		bit = 101	--	2061	--	μs
		bit = 110	--	4109	--	μs
		bit =111	--	8205	--	μs
I^2C/SMBus						
Timeout			--	37	--	ms
Digital Input / Output						
Input Capacitance			--	5	--	pF
Leakage Input Current	I_{LEAK}	0 ≤ Input Pin Voltage ≤ V_S	--	0.1	--	μA
High-Level Input Voltage	V_{IH}		1.2	--	--	V
Low-Level Input Voltage	V_{IL}		--	--	0.6	V
Low-Level Output Voltage, SDA, Alert	V_{OL}	I_{OL} = 3mA	--	--	0.4	V

Note 1. Stresses listed as the above under "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. The voltage at IN+ and IN– pins must not exceed the range –0.3V to 40V.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

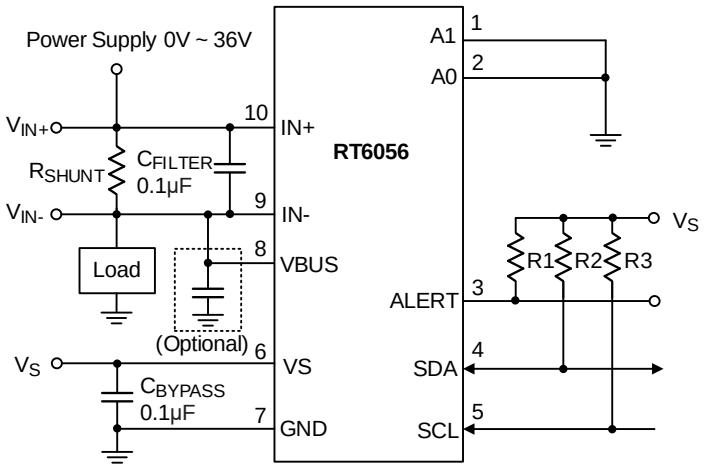
Note 5. The device is not guaranteed to function outside its operating conditions.

Note 6. RTI = Referred to input.

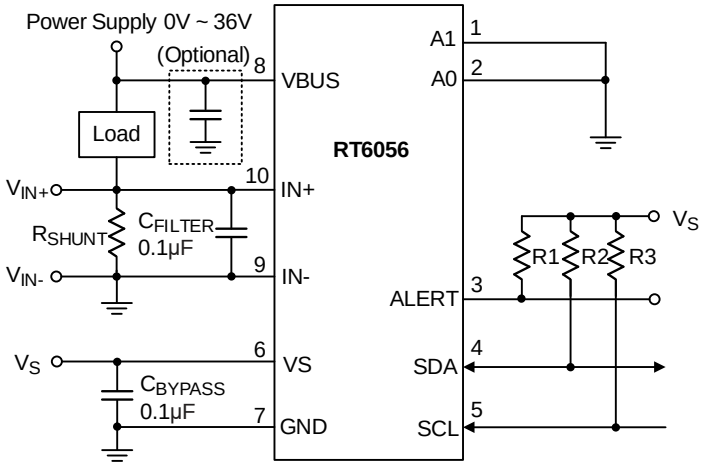
Note 7. Specifications are guaranteed by design, not production test.

Typical Application Circuit

High-Side Sensing Circuit Application

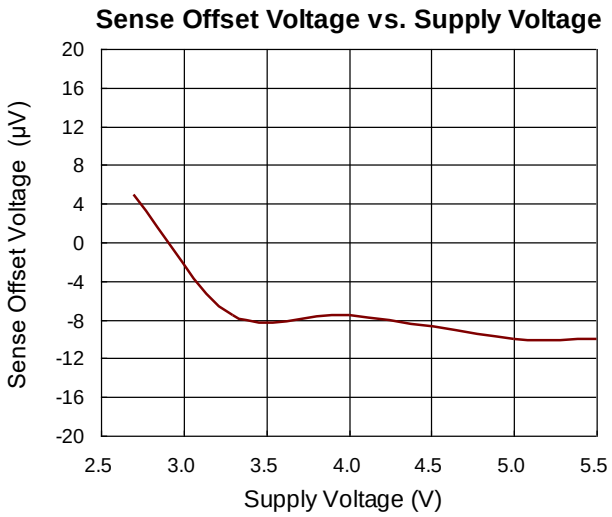


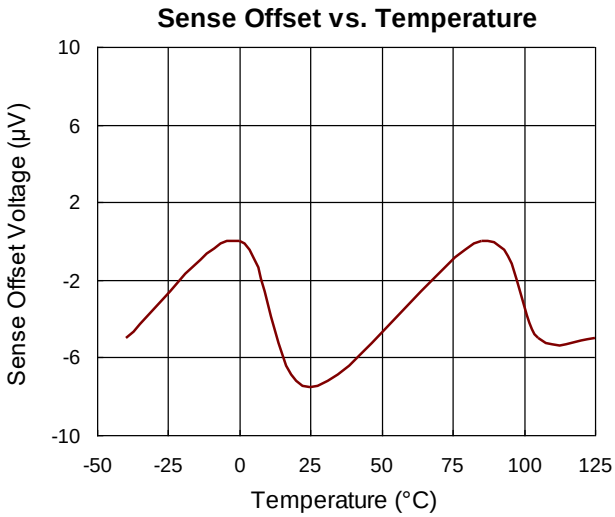
Low-Side Sensing Circuit Application

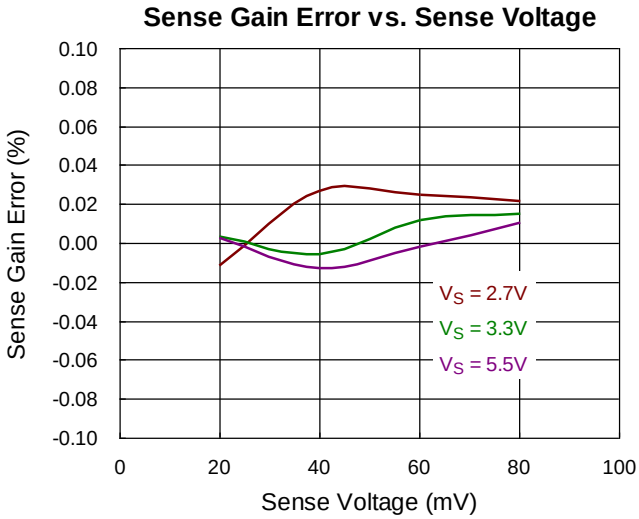


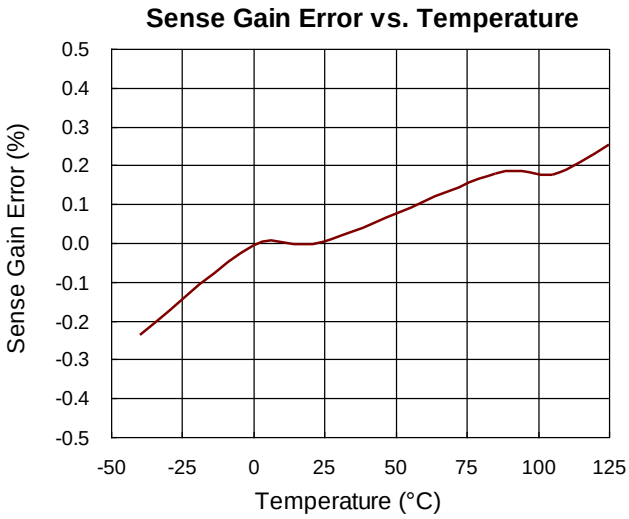
Note : All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC Bias.

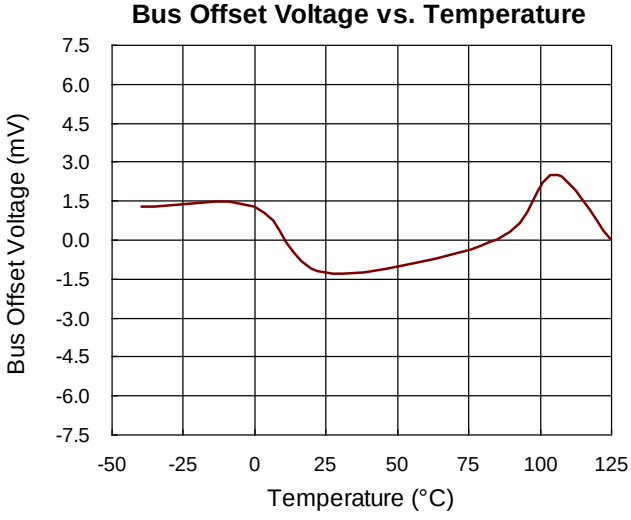
Typical Operating Characteristics

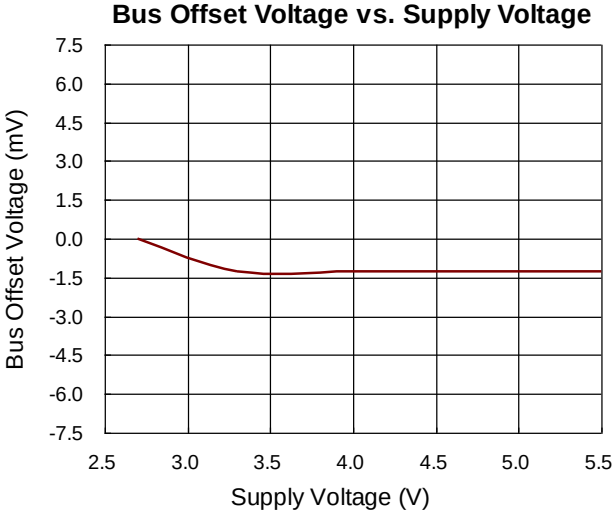




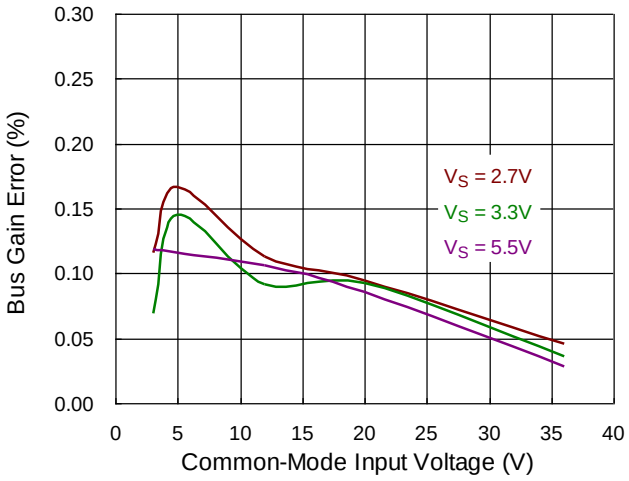




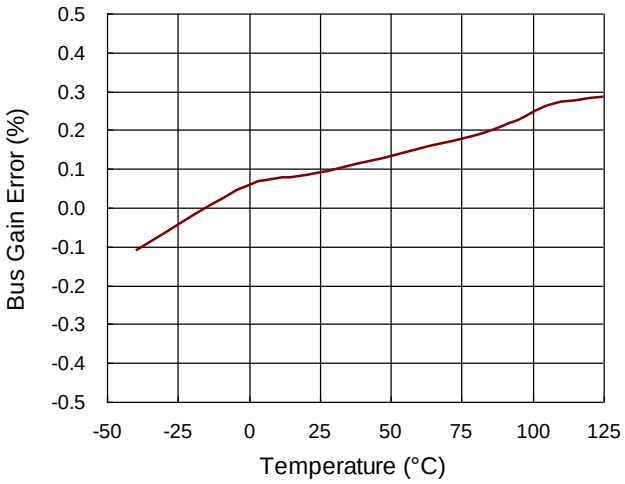




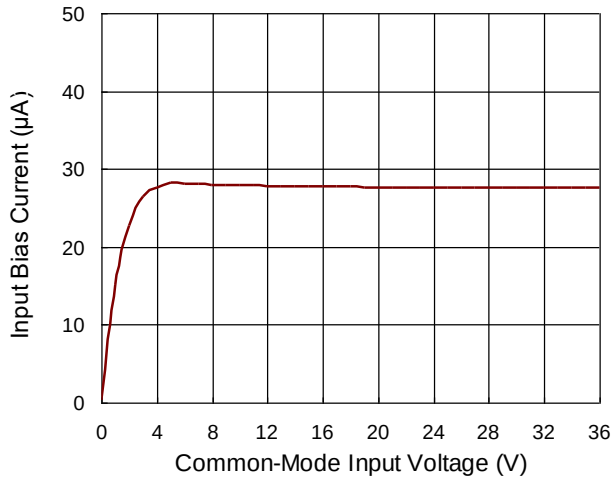
Bus Gain Error vs. Common-Mode Input Voltage



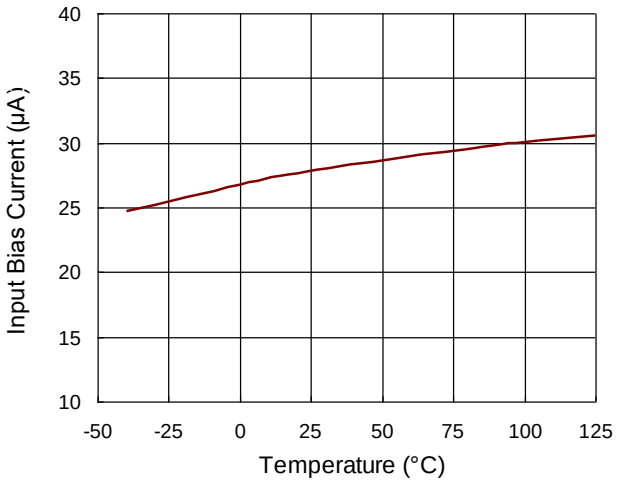
Bus Gain Error vs. Temperature



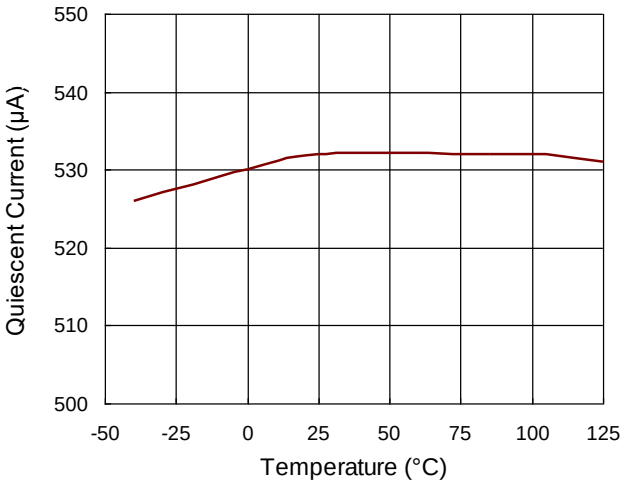
Input Bias Current vs. Common-Mode Input Voltage



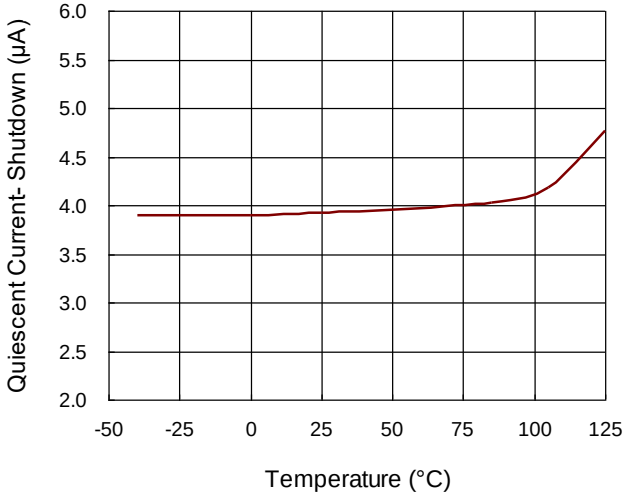
Input Bias Current vs. Temperature



Quiescent Current vs. Temperature



Quiescent Current-Shutdown vs. Temperature



Register Maps

Table 4 shows the summary of the RT6056 registers. These registers are two bytes with I^{2}C interface.

Table 4. The Summary of the RT6056 Registers

CMD CODE	COMMAND Name	Access	Command Description	Default Value
00h	Configuration	R/W	Operating mode configuration, conversion times and averaging setting	4127h
01h	Sense Voltage	R	Sense voltage measurement data.	0000h
02h	Bus Voltage	R	Bus voltage measurement data.	0000h
03h	Power	R	Calculated power data	0000h
04h	Current	R	Calculated current data	0000h
05h	Calibration	R/W	Current Calibration	0000h
06h	Mask/Enable	R/W	Alert configuration	0000h
07h	Alert Limit	R/W	Limit threshold setting	0000h
FEh	Manufacturer ID	R	Manufacturer identification number.	1214h
FFh	Die ID	R	Die identification number.	2260h

Configuration Register (00h)

Description : The Configuration Register settings control the operating modes for the device. This register controls the conversion time settings for both the sense and bus voltage measurements as well as the averaging mode used. The operating mode that controls what signals are selected to be measured is also programmed in the Configuration Register.

The Configuration Register can be read from at any time without impacting or affecting the device settings or a conversion in progress. Writing to the Configuration Register halts any conversion in progress until the write sequence is completed, resulting in a new conversion starting based on the new contents of the Configuration Register (00h). This halt prevents any uncertainty in the conditions used for the next completed conversion.

Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	RST	X	X	X	AVG2	AVG1	AVG0	VBUSCT2	VBUSCT1	VBUSCT0	VSENCT2	VSHNCT1	VSENCT0	MODE3	MODE2	MODE1
Value	0	1	0	0	0	0	0	1	0	0	1	0	0	1	1	1

Bits	Name	Description
15	Reset Bit (RST)	Set this bit to '1' to reset all registers as default value. This bit self-clears.
11:9	Averaging Mode (AVG)	Determines the number of samples that are collected and averaged. Table 5 shows all the AVG bit settings and related number of averages for each bit setting.

Table 5. AVG Bit Settings [11:9] Combinations

Averaging	AVG2	AVG1	AVG0
1 (default)	0	0	0
4	0	0	1
16	0	1	0
64	0	1	1
128	1	0	0
256	1	0	1
512	1	1	0
1024	1	1	1

<table>
<tr>
<td>8:6</td>
<td>Bus Voltage Conversion Time (VBUSCT)</td>
<td>Sets the conversion time for the bus voltage measurement. Table 6 shows the VBUSCT bit options and related conversion times for each bit setting.
Table 6. VBUSCT Bit Settings [8:6] Combinations
<table>
<tr><th>Conversion Time (μs)</th><th>VBUSCT2</th><th>VBUSCT1</th><th>VBUSCT0</th></tr>
<tr><td>139</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>203</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>269</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>525</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1037 (default)</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>2061</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>4109</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>8205</td><td>1</td><td>1</td><td>1</td></tr>
</table>
</td>
</tr>
<tr>
<td>5:3</td>
<td>Sense Voltage Conversion Time (VSENCT)</td>
<td>Sets the conversion time for the sense voltage measurement. Table 7 shows the VSENCT bit options and related conversion times for each bit setting.
Table 7. VSENCT Bit Settings [8:6] Combinations
<table>
<tr><th>Conversion Time (μs)</th><th>VSENCT2</th><th>VSENCT1</th><th>VSENCT0</th></tr>
<tr><td>139</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>203</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>269</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>525</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1037 (default)</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>2061</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>4109</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>8205</td><td>1</td><td>1</td><td>1</td></tr>
</table>
</td>
</tr>
<tr>
<td>2:0</td>
<td>Operating Mode (MODE)</td>
<td>Selects continuous, triggered, or power-down mode of operation. These bits default to continuous sense and bus measurement mode. The mode settings are shown in Table 8.
Table 8. Mode Settings [2:0] Combinations
<table>
<tr><th>Mode Setting</th><th>MODE3</th><th>MODE2</th><th>MODE1</th></tr>
<tr><td>Shutdown Mode</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Sense Voltage, Triggered</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>Bus Voltage, Triggered</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Sense and Bus Voltage, Triggered</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Shutdown Mode</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>Sense Voltage, Continuous</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>Bus Voltage, Continuous</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>Sense and Bus Voltage, Continuous (default)</td><td>1</td><td>1</td><td>1</td></tr>
</table>
</td>
</tr>
</table>

Sense Voltage Register (01h)																
Description: The Sense Voltage Register stores the current Sense voltage reading, V_{SENSE}. Negative numbers are represented in two's complement format. Generate the two's complement of a negative number by complementing the absolute value binary number and adding 1. An MSB = '1' denotes a negative number.																
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	SIGN	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	Sign Bit (SIGN)	SIGN Bit 0 : Positive value 1 : Negative value
14:0	Sense Voltage	**Example**: For a value of V_{SENSE} = –80mV : 1. Take the absolute value: 80mV 2. Translate this number to a whole decimal number (80mV ÷ 2.5μV) = 32000 3. Convert this number to binary = 0111 1101 0000 0000 4. Complement the binary result = 1000 0010 1111 1111 5. Add '1' to the complement to create the two's complement result = 1000 0011 0000 0000 = 8300h If averaging is enabled, this register displays the averaged value. Full-scale range = 81.92 mV (decimal = 7FFF); LSB: 2.5μV.

Bus Voltage Register (02h)																
Description: The Bus Voltage Register stores the most recent bus voltage reading, VBUS. If averaging is enabled, this register displays the averaged value.																
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	X	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	Bus Voltage	Note. Bit15 is always zero because bus voltage can only be positive.

Power Register (03h)																
Description: If averaging is enabled, this register displays the averaged value. The Power Register LSB is internally programmed to equal 25 times the programmed value of the Current_LSB. The Power Register records power in Watts by multiplying the decimal values of the Current Register with the decimal value of the Bus Voltage Register.																
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	Power	Note. The power is always positive value.

Current Register (04h)																
Description: If averaging is enabled, this register displays the averaged value. The value of the Current Register is calculated by multiplying the decimal value in the Sense Voltage Register with the decimal value of the Calibration Register.																
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	SIGN	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	Sign Bit (SIGN)	SIGN Bit 0 : Positive value 1 : Negative value
14:0	Current	The current value

Calibration Register (05h)																
Description: This register provides the device with the value of the Sense resistor that is present to create the measured differential voltage. It also sets the resolution of the Current Register. Programming this register sets the Current_LSB and the Power_LSB. This register is also suitable for use in overall system calibration. See the Programming the Calibration Register section for additional information on programming the Calibration Register.																
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	X	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	Calibration	Note. Bit15 is always zero.

Mask/Enable (06h)																
Description: The Mask/Enable Register selects the function that is enabled to control the Alert pin as well as how that pin functions. If multiple functions are enabled, the highest significant bit position Alert Function (Bit15-Bit11) takes priority and responds to the Alert Limit Register.																
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	SOVL	SUVL	BOVL	BUVL	OPL	CNVR	X	X	X	X	X	AFF	CNRF	OVF	APO	ALE
Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	Sense Over-Voltage Limit (SOVL)	Setting this bit high configures the Alert pin to be asserted if the sense voltage measurement following a conversion exceeds the value programmed in the Alert Limit Register.
14	Sense Under-Voltage Limit (SUVL)	Setting this bit high configures the Alert pin to be asserted if the sense voltage measurement following a conversion drops below the value programmed in the Alert Limit Register.
13	Bus Over-Voltage Limit (BOVL)	Setting this bit high configures the Alert pin to be asserted if the bus voltage measurement following a conversion exceeds the value programmed in the Alert Limit Register.
12	Bus Under-Voltage Limit (BUVL)	Setting this bit high configures the Alert pin to be asserted if the bus voltage measurement following a conversion drops below the value programmed in the Alert Limit Register.
11	Over-Power Limit (OPL)	Setting this bit high configures the Alert pin to be asserted if the Power calculation made following a bus voltage measurement exceeds the value programmed in the Alert Limit Register.
10	Conversion Ready (CNVR)	Setting this bit high configures the Alert pin to be asserted when the Conversion Ready Flag, Bit 3, is asserted indicating that the device is ready for the next conversion.
4	Alert Function Flag (AFF)	While only one Alert Function can be monitored at the Alert pin at a time, the Conversion Ready can also be enabled to assert the Alert pin. Reading the Alert Function Flag following an alert allows the user to determine if the Alert Function was the source of the Alert. When the Alert Latch Enable bit is set to Latch mode, the Alert Function Flag bit clears only when the Mask/Enable Register is read. When the Alert Latch Enable bit is set to Transparent mode, the Alert Function Flag bit is cleared following the next conversion that does not result in an Alert condition.
3	Conversion Ready Flag (CNRF)	Although the device can be read at any time, and the data from the last conversion is available, the Conversion Ready Flag bit is provided to help coordinate one-shot or triggered conversions. The Conversion Ready Flag bit is set after all conversions, averaging, and multiplications are complete. Conversion Ready Flag bit clears under the following conditions: 1.) Writing to the Configuration Register (except for Power-Down selection) 2.) Reading the Mask/Enable Register
2	Math Overflow Flag (OVF)	This bit is set to '1' if an arithmetic operation results in an overflow error. It indicates that current and power data may be invalid.
1	Alert Polarity bit (APO)	1 = Inverted (active-high open collector) 0 = Normal (active-low open collector) (default)

Bits	Name	Description
0	Alert Latch Enable (ALE)	1 = Latch enabled 0 = Transparent (default) When the Alert Latch Enable bit is set to Transparent mode, the Alert pin and Flag bit reset to the idle states when the fault has been cleared. When the Alert Latch Enable bit is set to Latch mode, the Alert pin and Alert Flag bit remain active following a fault until the Mask/Enable Register has been read.

Alert Limit Register (07h)

Description: The Alert Limit Register contains the value used to compare to the register selected in the Mask/Enable Register to determine if a limit has been exceeded.

Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:0	Alert Limit	Stores the alert limit values

Manufacturer ID Register (FEh)

Description: The Manufacturer ID Register stores a unique identification number for the manufacturer.

Bit .	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Value	0	0	0	1	0	0	1	0	0	0	0	1	0	1	0	0

Bits	Name	Description
15:0	Manufacturer ID	Stores the manufacturer identification bits

Die ID Register (FFh)																
Description: The Die ID Register stores a unique identification number and the revision ID of the die.																
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Value	0	0	1	0	0	0	1	0	0	1	1	0	0	0	0	0

Bits	Name	Description
15:4	Die ID	Stores the device identification bits
3:0	Die Revision ID	Stores the device revision identification bits

Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and reserve suitable design margin to ensure the functional suitability of their components and systems.

Power Up

The VS pin must exceed the Power-On Reset threshold (V_{POR}) of 2V to keep the RT6056 out of power-on reset. Power-on reset will clear all of the register data.

Choosing the Sense Resistor

A high R_{SHUNT} value causes the power-source voltage to drop due to IR loss. For minimal voltage loss, use the lowest R_{SHUNT} value. V_{SENSE} full scale should be less than the full code of −81.9175mV to 81.92mV. For best performance with a 3.3V supply voltage, select R_{SHUNT} to provide approximately 40mV~60mV of sense voltage for the full-scale current in each application.

At low current levels, a high R_{SHUNT} value allows lower currents more accurately because offsets are less significant when the sense voltage is larger.

At high current levels, the I^2R loss in R_{SHUNT} can be significant. Notice the resistor value and power dissipation rating when choosing. Also, the sense resistor's value might drift if it is allowed to heat up excessively. The precision V_{OS} 10μV (max) and Gain Error 0.12% (max) of the RT6056 allows the use of small sense resistors to reduce power dissipation and reduce hot spots.

Filtering and Input Considerations

The RT6056 provides several methods to reduce the effect from the input noise; for example, conversion time and averaging mode can be flexibly chosen through the register (00h). However, in order to prevent device damaging from the load dumps, reverse battery protection, fast load-switching and inductive kickback voltages, the input filter and input voltage clamping schemes are needed to protect the device during such conditions.

Figure 7 shows the recommended schematic for input filtering. Filtering at the input means current noise is not amplified and the RT6056 can drive a cleaner signal into the ADC without an output filter loading down the ADC.

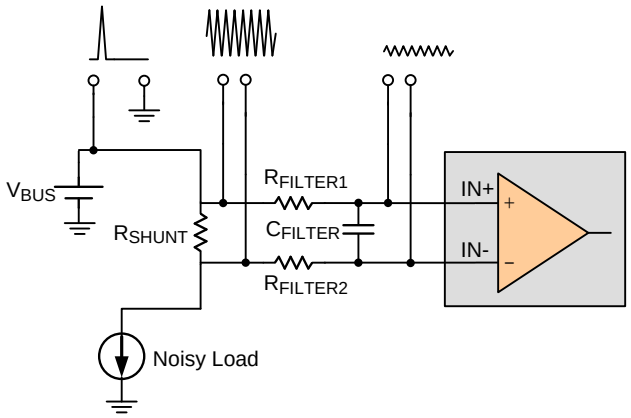


Figure 7. Input Filter

If the chosen device states that the Absolute Maximum Common-Mode Voltage rating cannot exceed system maximum expected voltage surge, then it needs input protection. Along with some passives, the current sensor needs transient voltage suppression (TVS) or Zener diodes at the inputs for protection. Figure 8 shows an example using the cost-optimized current sensor.

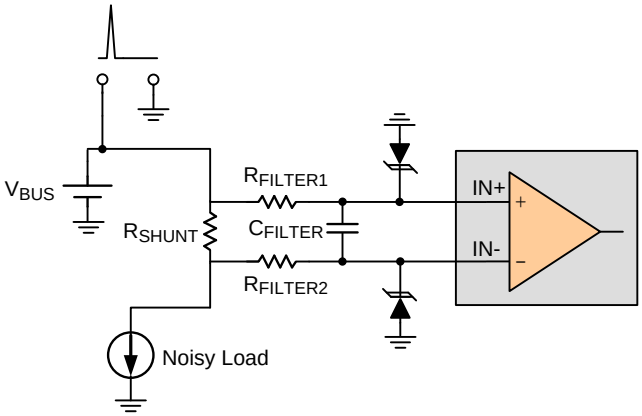


Figure 8. RT6056 with Input Protection

Total Error Analysis

In order to optimize the design, the first is to analyze the contribution of each error; the main influences of sense voltage errors can be identified as follows :

- The tolerance of shunt resistor (R_{SHUNT})
- Sense offset voltage, V_{S_OS}. When the sense voltage is small, especially low load current and small shunt resistance, the error is dominated by the input offset error.
- Gain Error, GE%
- PSRR of offset voltage, PSRR
- Common mode rejection, CMRR
- The offset voltage caused by input bias current
- Nonlinearity Error, NLIN%

Max Output Error Estimation

This section gives an example. The system bus voltage for IN+ = 36V, supply voltage V_S = 5V, shunt resistor is accuracy 1% 2mΩ, the load current is 25A. To set the design goals, the maximum output voltage errors are calculated as follows:

Input offset voltage error

The rate of offset error in the total error can be estimated directly from the specification table. The input offset voltage is 10μV at T_A = 25°C, the error due to offset can be obtained by the equation below :

$$V_{OS\_err} = \frac{V_{OS(MAX)}}{V_{SENSE}} \times 100\% = \frac{10\mu V}{2m\Omega \times 25A} \times 100\% = 0.02\%$$

Sense Voltage Gain Error

From the electrical characteristics, the max gain error is 1%.

PSRR Error

The PSRR error is to estimate the error caused by different supply voltage; the RT6056 device specification gives the specified power supply voltage for the input offset voltage specification as V_S = 3.3V; when the system supply voltage is not exactly 3.3V, it may result in an additional error. RT6056 device gives the maximum PSRR as 2.5μV/V. Calculate the PSRR error by the equation below :

$$PSRR\_err = \frac{\left|V_{S\_DS} - V_{S\_SYS}\right| \times PSRR}{V_{SENSE}} \times 100\%$$

$$= \frac{\left|3.3 - 5\right| \times 2.5\frac{\mu V}{V}}{2m\Omega \times 25A} \times 100\% = 0.0085\%$$

CMRR Error

The CMRR error means the input offset error is influenced by the variation of common-mode voltage; in real conditions, calculate the maximum input offset by determining the actual common-mode voltage as applied to RT6056. According to the RT6056 device specification, it gives the common-mode rejection ratio minimum as 126dB (0.501μV/V). The offset voltage in the data sheet is specified with a common-mode voltage that is 12V. To calculate the actual common-mode error at system bus voltage :

$$126dB \text{ can be converted to } \mu V/V = \frac{1}{10^{\left(\frac{126dB}{20}\right)}} \times 10^6 \times \frac{\mu V}{V}$$

$$= 0.501\frac{\mu V}{V}$$

$$CMRR\_err = \frac{\left|V_{CM\_DS} - V_{CM\_SYS}\right| \times CMRR}{V_{SENSE}} \times 100\%$$

$$= \frac{\left|12 - 36\right| \times 0.501\frac{\mu V}{V}}{2m\Omega \times 25A} \times 100\% = 0.024\%$$

Input Bias Current Error

The input bias current flows into shunt resistor to cause additional offset; this error is calculated with respect to the ideal voltage across the sense voltage.

$$I_{B\_err} = \frac{I_B \times R_{SHUNT}}{V_{SENSE}} \times 100\% = \frac{35\mu A \times 2m\Omega}{2m\Omega \times 25A} \times 100\% = 0.0001\%$$

Nonlinearity Error

For ideal cases, the voltage gain is constant over full sense ranges, but in the real application, the voltage gain is not exactly constant, the nonlinearity gain may cause some additional errors. In the specification, the RT6056 gives the nonlinearity error as 0.1% over sense voltage from 20mV to 80mV.

Total Error

The equation below can calculate the worst case of total error.

$$\text{Total\_err} = \sqrt{(\text{GE\%})^2 + (\text{R\%})^2 + (V_{OS\_err})^2 + (\text{PSR\_err})^2 + (\text{CMR\_err})^2 + (I_{B\_err})^2 + (\text{NLIN\%})^2}$$

$$= \sqrt{(0.12\%)^2 + (1\%)^2 + (0.05\%)^2 + (0.021\%)^2 + (0.06\%)^2 + (0.00035\%)^2 + (0.045\%)^2}$$

$$= 1.01\%$$

Layout Guidelines

- A Kelvin sense arrangement is required for best performance. Connect the input pins (IN+ and IN-) to the sensing resistor using a 4-wire connection.
- PCB trace resistance from the sense resistor to the IN+ and IN- pins can affect the power measurement accuracy. Place the sense resistors as close as possible to the RT6056 and not to use minimum width PCB traces.
- Place the power-supply bypass capacitor as close as possible to the supply and ground pins.

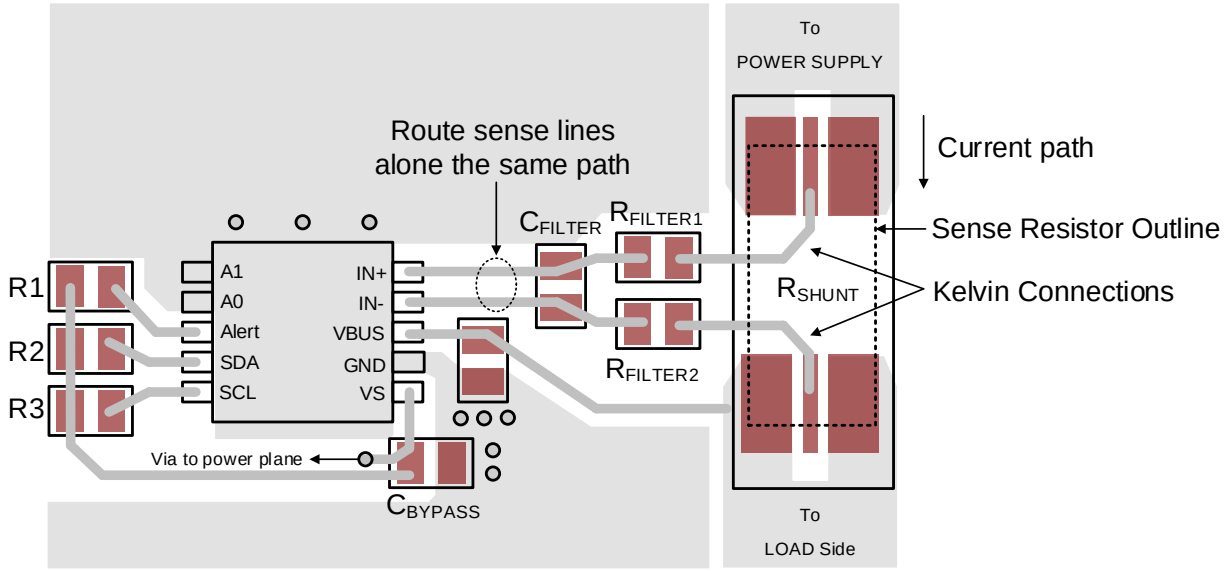
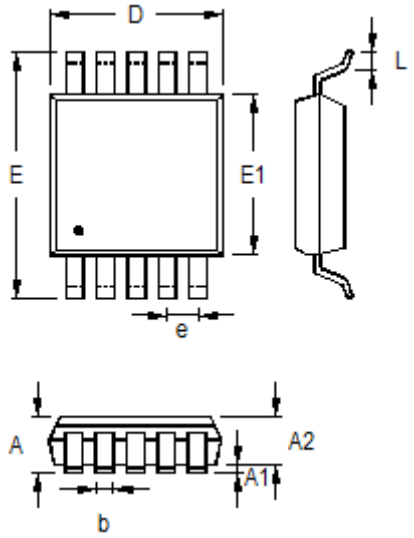


Figure 9. PCB Layout Guide

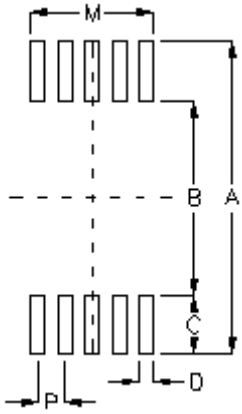
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.810	1.100	0.032	0.043
A1	0.000	0.150	0.000	0.006
A2	0.750	0.950	0.030	0.037
b	0.170	0.270	0.007	0.011
D	2.900	3.100	0.114	0.122
e	0.500		0.020	
E	4.800	5.000	0.189	0.197
E1	2.900	3.100	0.114	0.122
L	0.400	0.800	0.016	0.031

10-Lead MSOP Plastic Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)						Tolerance
		P	A	B	C	D	M	
MSOP-10	10	0.50	5.80	3.60	1.10	0.25	2.25	±0.10

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Datasheet Revision History

Version	Date	Description	Item
01	2024/1/15	Modify	Title on P1 General Description on P1 Ordering Information on P2 Operation on P6 Electrical Characteristics on P11 Typical Application Circuit on P13 Application Information on P23, 24, 25

Mouser Electronics

Authorized Distributor

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