iND83213A Datasheet
Rev 1.1

1 Document Revision History

Rev #	Date	Action
0.1	2022/1	Draft
0.2	2022/6	Update EC table and description after G1
0.5	2022/10	Update EC table and description after G3
0.9	2022/10	Update EC table and description
0.91	2023/1	Insert register map
0.92	2023/2	Update pinout
0.93	2023/3	Change maximum VBAT voltage to 20V
0.94	2023/4	Change the standard package specification to 3000 pcs per tape & reel
0.95	2023/6	Update clock trimming register
0.96	2023/7	Remove LIN master feature
1.0	2023/10	Update EC table and description after G4
1.1	2023/11	SDIO timing description updated in register map

2 Table of Contents

3 System Overview

3.1 Introduction

The iND83213A is an automotive LED lighting integrated device that combines an ASIC die (including 24 channels of 50mA current source, LDO, LIN controller, LIN transceiver, clock, 16-bit PWM, 12-bit SAR ADC, LED PN voltage detection) and an MCU die (including ARM Cortex-M0 CPU core, 64KB flash memory, 16KB SRAM) together.

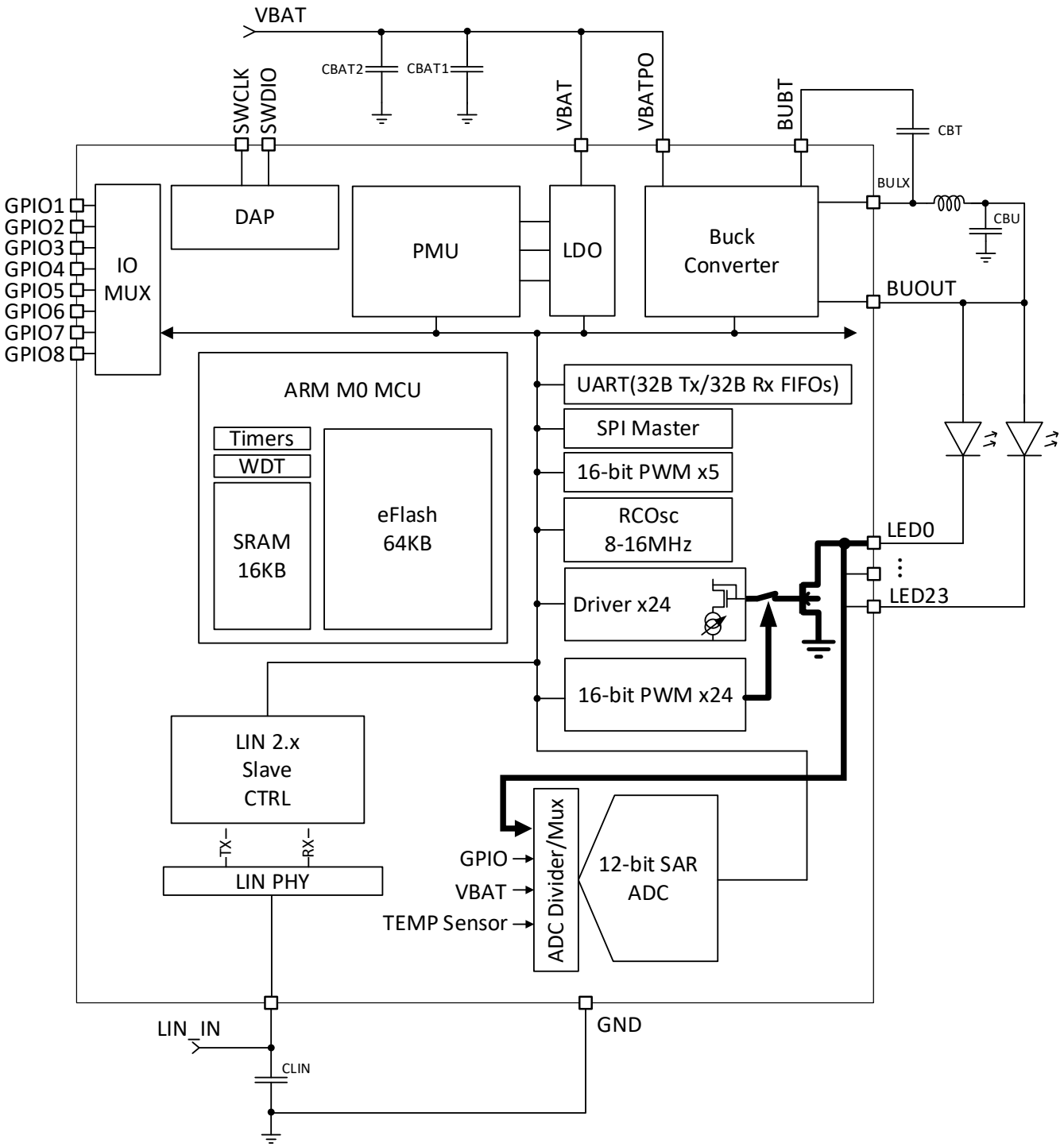
3.2 Main Features

- Full automotive qualification AEC-Q100 Grade 1
- Functional safety enhancement
  - Hardware LIN TX monitor for LINS to prevent a dominant bus caused by internal malfunction
- Buck
  - Period & VDAC configuration hardware check
  - Buck clock is independent from system clock configuration
- LIN bus idle timeout monitors
  - Always active, even the chip is in hibernate mode
  - For preventing a fast discharge of the car battery, if a short to ground is detected, the following options are available
    - Automatically switch off LIN slave's pull-up
  - Auto-recovery if the failure condition disappears
- CPU architecture
  - ARM Cortex-M0 processor
  - SysTick timer (24-bit, interruptible)
  - Serial Wire Debug port (SWD)
  - Built-in Nested Vectored Interrupt Controller (NVIC)
  - Single-cycle 32-bit x 32-bit multiply instruction
  - Programmable watchdog timer
  - 3 programmable timers
- Memory
  - 64KB of flash memory, 10 years retention in automotive environment
  - 16KB of SRAM
- Peripherals/Digital features
  - Clock and reset manager
    - RCO: system and always on (wake up support)
    - Reset POR and BOR (no external reset)
  - One SAE J2602/LIN2.2 LIN slave controller and transceiver
  - Watchdog timer (ASIC side)
  - 24x16-bit PWM to control the LED current drivers

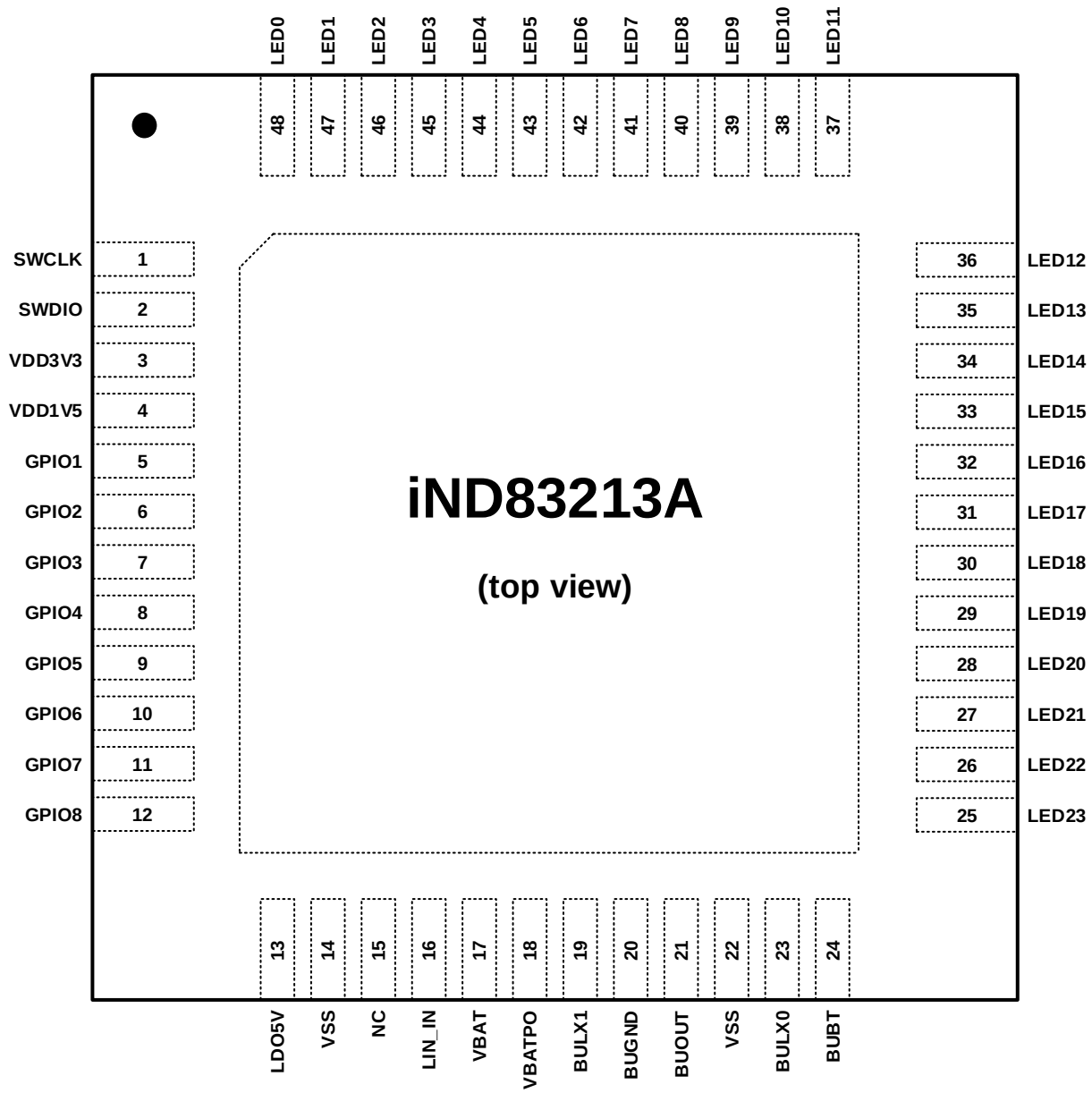
        - Shared prescaler and 16-bit counter
        - Support power balancing with independent rise/fall timing configuration
    - 5x16-bit auxiliary PWM to control the GPIOs, with 2 shared prescalers and 16-bit counters
    - Serial communication interfaces
        - Integrated UART controller with two independent FIFOs(TX: 32 bytes, RX: 32 bytes)
        - Integrated SPI master controller
    - Up to 8 GPIOs with flexible configurations
        - Generic GPIOs with pull-up & pull-down
        - Analog input mode
        - Support edge detects
        - Wake-up sources in hibernate mode
- Peripherals/Analog features
    - 24 programmable 50mA max constant current low voltage (VDD5P0) IO open drain
        - Drain voltage that ensures < 1V
        - Integrated pull-up capability
    - PN voltage measurement for temp compensation
        - Integrated a dedicated 2.5mA current source
        - Fully differential measurement
    - Temperature sensor/monitor with ADC
    - Battery voltage detection and monitoring
    - Hardware over temperature protection
    - 12-bit SAR ADC
        - Up to 4 continuous conversion channels
            - Separated reference voltage configuration for each channel
            - Separated gain selection for each channel
        - Up to 43 mux channels
            - Buffered bandgap voltage
            - Junction temperature
            - Forward voltages of external LEDs
            - GPIO
            - Accurate VBAT voltage
            - LDO voltage
            - Buck output voltage
            - Self-calibration channels
    - Fully integrated step-down buck converter
        - Integrated synchronous buck converter
        - Operation frequency: 400kHz

        - Output voltage adjustable: 3.0V-5.5V
        - OCP/dead short protection with hiccup support
        - Independent SSC clock
        - Internal ZCD/NCD detection
    - Integrated voltage regulators
        - LDO 3.3V (ASIC core, IO supply and MCU I/O)
        - LDO 1.5V (MCU core and flash memory)
        - LDO 5.0V (Pre-regulator for 1.5V and 3.3V LDO)
- QFN-48, 6*6mm

3.3 Functional Block Diagram



3.4 Pin Configuration and Function



No.	Name	Type	Description
1	SWCLK	Input	SWD clock input, weak pulled-down internally(1)
2	SWDIO	I/O	SWD data I/O, weak pulled-up internally(1)
3	VDD3V3	Power	Internal 3.3V LDO output. The pin requires a ceramic capacitor with a minimum value of 2.2μF or greater(2)
4	VDD1V5	Power	Internal 1.5V LDO output. The pin requires a ceramic capacitor with a minimum value of 2.2μF or greater(2)
5	GPIO1	I/O	GPIOA0/PWM0/debugging
6	GPIO2	I/O	GPIOA1/PWM1/SPI_SS/debugging
7	GPIO3	I/O	GPIOA2/PWM2/LINS_RXD/SPI_SCK/debugging
8	GPIO4	I/O	GPIOA3/PWM3/UART_RXD/SPI_MOSI/debugging
9	GPIO5	I/O	GPIOA4/PWM4/UART_TXD/LINS_TXD/SPI_MISO/debugging

10	GPIO6	I/O	GPIOA5/PWM1/SPI_MISO/debugging
11	GPIO7	I/O	GPIOA6/PWM2/LINS_RXD/SPI_SCK/debugging
12	GPIO8	I/O	GPIOA7/PWM3/UART_RXD/SPI_MOSI/debugging
13	LDO5V	Power	Internal 5V LDO output. The pin requires a ceramic capacitor with a minimum value of 2.2μF or greater(2)
14	VSS	Ground	Bonding with ground plane
15	NC	NC	No connection
16	LIN_IN	I/O	LIN bus line I/O, can be controlled by LIN slave controller or GPIOB1
17	VBAT	Power	power input for all internal circuit except for buck
18	VBATPO	Power	power input for buck
19	BULX1	Analog	Connect to the external inductor
20	BUGND	Ground	Buck power ground
21	BUOUT	Analog	Buck output (internal), also is feedback input (external)
22	VSS	Ground	Bonding with ground plane
23	BULX0	Analog	Connected to BULX1 internally, connect to the bootstrap capacitor
24	BUBT	Analog	Connect a 100nF bootstrap capacitor to the BULX0 pin
25	LED23	Analog	Current regulated sink
26	LED22	Analog	Current regulated sink
27	LED21	Analog	Current regulated sink
28	LED20	Analog	Current regulated sink
29	LED19	Analog	Current regulated sink
30	LED18	Analog	Current regulated sink
31	LED17	Analog	Current regulated sink
32	LED16	Analog	Current regulated sink
33	LED15	Analog	Current regulated sink
34	LED14	Analog	Current regulated sink
35	LED13	Analog	Current regulated sink
36	LED12	Analog	Current regulated sink
37	LED11	Analog	Current regulated sink
38	LED10	Analog	Current regulated sink
39	LED9	Analog	Current regulated sink
40	LED8	Analog	Current regulated sink
41	LED7	Analog	Current regulated sink
42	LED6	Analog	Current regulated sink
43	LED5	Analog	Current regulated sink
44	LED4	Analog	Current regulated sink
45	LED3	Analog	Current regulated sink
46	LED2	Analog	Current regulated sink
47	LED1	Analog	Current regulated sink
48	LED0	Analog	Current regulated sink
EPAD	Ground	Ground	Connect to system ground

Note:

1. LDO5V, VDD3V3 and VDD1V5 has only very limited load capacity, the peak current of external load should not exceed 10mA in total, and should never apply any external power on these pins
2. SWD debugging/flashing port must keep disconnected before the IC start-up sequence finished, preventing the reversed current from the SWD pins damages the IC

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Voltages referenced to ground.

Names	Conditions	Min.	Max.	Unit
V_{BAT}/V_{BATPO} to ground	No damage, t<5min	-0.3	+40	V
	No damage, t<5ms	-1.1		V
	No damage, t<20ns	-4.0		V
	No damage, ISO 7637-2 pulse 1, V_{BAT}=13.5V, T_A=23°C±5°C, test pulse applied to V_{BAT} via reverse polarity diode and more than 4.7µF capacitor	-100		V
	No damage, ISO 7637-2 pulse 2, V_{BAT}=13.5V, T_A=23°C±5°C, test pulse applied to V_{BAT} via reverse polarity diode and more than 4.7µF capacitor		+40	V
	No damage, ISO 7637-2 pulses 3A, 3B, V_{BAT}=13.5V, T_A=23°C±5°C, test pulse applied to V_{BAT} via reverse polarity diode and more than 4.7µF capacitor	-150	+100	V
	No damage, ISO 7637-2 pulses 5b, V_{BAT}=13.5V, T_A=23°C±5°C, test pulse applied to V_{BAT} via reverse polarity diode and more than 4.7µF capacitor		+40	V
LIN to ground	No damage, t<500ms	-40	+40	V
	No damage, ISO 7637-3 pulse 1, V_{BAT}=13.5V, T_A=23°C±5°C, test pulse applied to LIN via 1nF capacitor	-100		V
	No damage, ISO 7637-2 pulse 2, V_{BAT}=13.5V, T_A=23°C±5°C,		+40	V

	test pulse applied to LIN via 1nF capacitor			
	No damage, ISO 7637-2 pulses 3A, 3B, V_{BAT}=13.5V, T_A=23°C±5°C, test pulse applied to LIN via 1nF capacitor	-150	+100	V
LED0~LED23 to ground	No damage	-0.3	5.5	V
BUOUT to ground	No damage	-0.3	5.5	V
BULX to ground	No damage	-0.3	42	V
BUBT to BULX	No damage	-0.3	5.5	V
SWCLK, SWDIO, GPIO1~GPIO8 to ground	No damage	-0.3	3.6	V
VBAT/VBATPO/LININ/LINOUT/GND	ESD HBM	-2	+2	kV
All pins except VBAT/VBATPO and LIN	ESD HBM	-2	+2	kV
All pins	ESD CDM	-750	+750	V
Junction temperature, T_j		-40	150	°C

Note:
Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. The absolute maximum ratings provided in the table above are limiting values that do not lead to a permanent damage of the part. But functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4.2 Thermal Information

Parameter	Conditions	Min.	Typ.	Max.	Unit
Operating temperature, T_a		-40	25	125	°C
Storage temperature		-55		150	°C
Package thermal resistance	Junction to board thermal resistance (ThetaJB)		10		K/W
	Junction to ambient thermal resistance (ThetaJA)		27		K/W

4.3 Current Consumption

Names	Descriptions	Min.	Typ.	Max.	Unit
Normal	MCU running, no flash writing, LED off, ADC, VBAT monitor, over-temperature monitor and WDT on T_a=125°C, V_{BAT}=18V, R_{CO}=16MHz			10	mA
Sleep mode 1	Main regulator (5V) ON, load dump protection active, overvoltage/undervoltage detection, PWM, LED driver, temperature sensor and ADC are OFF except GPIO toggling and wake-up timer T_a=125°C max, V_{BAT}=13.5V		60		μA

Sleep mode 2	Main regulator (5V) ON, load dump protection active, overvoltage/undervoltage detection, PWM, LED driver, temperature sensor and ADC are off except one LIN RX on and GPIO toggling and wake-up timer T_a=125°C max, V_{BAT}=13.5V		70		µA

4.4 Electrical Characteristics

V_{IN} = 14V, For digital outputs, C_{LOAD} = 20pF (Unless otherwise noted).

Parameter	Conditions/Comments	Min.	Typ.	Max.	Unit
VBAT		4	13.5	20	V
ASIC core supply		1.35	1.5	1.65	V
MCU core supply	MCU core supply including SRAM and flash memory	1.35	1.5	1.65	V
Flash Memory					
Sector endurance		20k			Cycles
Data retention	At 25°C	100			Years
Data retention	At 85°C	25			Years
Buck Converter					
Input supply	V_{BATPO} input supply (Maximum range)	4.2	13.5	40	V
	V_{BATPO} input supply (Recommended range)	4.2	13.5	20	V
Output voltage	V_{BAT}=13.5V, configurable range of V_{BUOUT}	3.0	5.0	5.5	V
Output voltage accuracy	V_{BAT}=13.5V, V_{BUOUT}=5.0V, I_{load}=500mA	-1.5		+1.5	%
Output load current (I_{load})	V_{BAT}=13.5V, V_{BUOUT}=5.0V			1.2	A
	V_{BAT}=6V, V_{BUOUT}=5.0V			1.0	A
Switching frequency	SSC is disabled	380	400	420	kHz
Peak efficiency	V_{BUOUT}=5.0V, I_{load}=500mA, V_{BAT} from 8V to 19V	90			%
High side MOSFET ON resistance	Include bonding wire		320		mΩ
Low side MOSFET ON resistance	Include bonding wire		220		mΩ
Quiescent current	No output load		8		mA
Switching SSC		-5		+5	%
Ripple	V_{BAT}=13.5V, V_{BUOUT}=5.0V, I_{load}=300mA			60	mV
Load regulation	V_{BAT}=13.5V, V_{BUOUT}=5.0V, I_{load} from 1µA to 500mA			50	mV
Line regulation	I_{load}=500mA, V_{BAT} from 8V to 19V			20	mV
Soft start	V_{BAT}=13.5V, I_{load}<200mA, V_{BUOUT} from 0 to 5V			10	ms

Parameter	Conditions/Comments	Min.	Typ.	Max.	Unit
Inductor	L nominal value		10		μH
Output capacitor	C_{OUT} nominal value		44		μF
Input capacitor	C_{IN} nominal value, place near VBATPO as close as possible.		10		μF
Buck monitor over voltage threshold			110		%
Buck input under voltage threshold			4		V
I_{HSLMT}	High-side current limit		2		A
T_{ON_MIN}	Minimum on-time		80		ns
T_{OFF_MIN}	Minimum off-time		80		ns
T_{ON_MAX}	Maximum on-time		3.3		μs
T_{SS}	Internal soft-start unit time(total time=unit time***VDAC_TRIM**) 2-bit configurable	7.8	15.6	62.4	μs
T_{HIC}	Hiccup recovery time, configurable through register **HICCUP_DWELL** by 1ms step	1		16	ms
Clocks					
System clock frequency	8-bit configurable through register **TRIM_HF_RC**	12	16	20	MHz
System clock accuracy	F_{sys}=16MHz	-7		+7	%
System clock start-up time			10		μs
Auxiliary clock frequency	Used in sleep mode		250		kHz
5V LDO					
Output voltage		4.65	4.9	5.1	V
Decoupling capacitor		2.2		10	μF
3.3V LDO					
Output voltage		3.3	3.4	3.5	V
Decoupling capacitor		2.2		10	μF
1.5V LDO					
Output voltage		1.5	1.55	1.6	V
Decoupling capacitor		2.2		10	μF
POR/BOR					
POR (LDO5V) rise threshold		2.8	3.0	3.3	V
POR (LDO5V) hysteresis			0.16		V
BOR VDD3V3 rise threshold	register **S_BOR_3V3**=4	2.9	3.1	3.2	V
BOR VDD3V3 hysteresis			0.2		V
BOR VDD1V5 rise threshold	register **S_BOR_1V5**=5	1.31	1.35	1.38	V
BOR VDD1V5 hysteresis			0.1		V
BG core/V2I					
BG core output voltage	After trimming		1.214		V
Battery Monitor					
Under voltage rise threshold	register **UVLEVEL**=10	5.5	5.7	6.0	V

Parameter	Conditions/Comments	Min.	Typ.	Max.	Unit
Under voltage fall threshold		5.3	5.4	5.5	V
Under voltage hysteresis	Programmable through register **UVHYS**		0.29		V
Under voltage digital debounce time	For signal rise and fall, 62.5ns or 62.5µs steps, programmable through register **UVTHRES0** and **UVTHRES1**			16	ms
Over voltage threshold range	Programmable through register **OVLEVEL**	14		19	V
Over voltage hysteresis	Programmable through register **OVHYS**	0.4	1.1	2.4	V
Over voltage digital debounce time	For signal rise and fall, 62.5ns or 62.5µs steps, programmable through register **OVTHRES0** and **OVTHRES1**			16	ms
Current Source LED(Low Voltage Pins)					
LED voltage	Minimum voltage to allow current regulation			0.5	V
	Recommended minimum voltage to ensure sink current error < 4%			0.7	V
Sink current	V_{BAT}>6V, Programmable through registers **TRIM0**-**TRIM23**	0.1		50	mA
Sink current step size			100		µA
Sink current error	T_a=25°C, LED voltage>1.0V	-4		+4	%
Temperature drift	-40°C~150°C	-9		+9	%
Over Temperature Monitor					
Over temperature threshold	Programmable through register **TS_CFG**	90		160	°C
Over temperature hysteresis			10		°C
Temperature Sensor					
Temperature range	ADC channel	-40		150	°C
Temperature accuracy		-10		+10	°C
Differential Amplifier for LED V_{FW} measurement					
Input voltage range (V_{IN})	Gain=1/5 or 2/5	0		V_{BUCK}	V
Output voltage range	Internal output range of LED measurement	0	V_{in}*Gain	V_{ref} (ADC)	V
Output voltage relative error				0.1	%
Gain	Programmable		1/5		
Wake-up					
T_{WAKEUP}	LIN_IN, programmable	30	150	200	µs
SAR ADC					

Parameter	Conditions/Comments	Min.	Typ.	Max.	Unit
Resolution	Differential measurement		12		bits
	Single-ended measurement for positive signal		11		bits
V_{ref}	Internal 2.4V reference voltage for ADC		2.425		V
Available mux channels	24 differential LED PN voltage channels, 8 single-ended GPIO channels, 5 single-ended power voltage channels, 3 self-calibration channels, 2 differential temperature sensor channels, 1 differential GPIO channels		43		
ENOB	Effective number of bits		9		bits
t_{conv}	ADC conversion time			20	µs
LIN specified with V_{BAT}=8V to 16V – refer to LIN 2.x specification, V_{BUS}=LIN pin/line					
V_{SUP}	Supply voltage range	6	13.5	19	V
I_{BUS_LIM}	Current limitation for driver dominant state driver on: V_{BAT} = 18V, V_{BUS} = 18V	40		200	mA
$I_{BUS\_PAS\_dom}$	Input leakage current at the receiver including pull-up resistor Driver off, V_{BAT} = 12V, V_{BUS} = 0V	-1			mA
$I_{BUS\_PAS\_rec}$	Driver off, VBUS>VBAT V_{BAT}= 7V, V_{BUS} = 18V			20	µA
$I_{BUS\_NO\_GND}$	Control unit disconnected from ground GND_{Device} = V_{BAT} = 12V, 0V < V_{BUS} < 18V Loss of local ground must not affect communication in the residual network	-1		+1	mA
$I_{BUS\_NO\_BAT}$	V_{BAT} disconnected V_{BAT_Device} = 0V, 0 < V_{BUS} < 18V Node must sustain the current that can flow under this condition. Bus must remain operational under this condition			100	µA
V_{BUSdom} (Transmitter)	Transmitter dominant voltage Load 500Ω, driver open drain active	0.0		0.2	V_{BAT}
V_{BUSrec} (Transmitter)	Transmitter recessive voltage	0.8		1.0	V_{BAT}

Parameter	Conditions/Comments	Min.	Typ.	Max.	Unit
	Driver open drain high impedance				
C_{SLAVE}	LIN pin input capacitance Note that LIN 2.2A spec 220pF typ, 250pF max as total node capacitance at the connector including the physical bus driver and all other components including C_{LIN}			100	pF
V_{BUSdom}	Receiver dominant state			0.4	V_{BAT}
V_{BUSrec}	Receiver recessive state	0.6			V_{BAT}
V_{BUS_CNT}	Center point receiver V_{BUS_CNT} =(V_{th_dom}+ V_{th_rec})/2	0.475	0.5	0.525	V_{BAT}
V_{HYS}	Receiver hysteresis V_{HYS} = V_{th_rec} -V_{th_dom}			0.175	V_{BAT}
t_{rx_pd}	propagation delay of receiver C_{RXD} load 20pF (RX output of transceiver, internal node, access in test mode)			6	µs
t_{rx_sym}	symmetry of receiver propagation delay C_{RXD} load 20pF (RX output of transceiver, internal node, access in test mode)	-2		+2	µs
R_{slave}	LIN slave pull-up resistor	20	30	60	kΩ
LIN Timing parameters (CBUS ; RBUS): (1nF; 1kΩ) / (6.8nF;660Ω) / (10nF;500Ω)					
D1, duty cycle 1 (20kBit/s)	$TH_{Rec(max)}$ = 0.744 x V_{BAT}; $TH_{Dom(max)}$ = 0.581 x V_{BAT}; V_{BAT} = 7.0V...18V; t_{Bit} = 50µs; D1 = $t_{Bus\_rec(min)}$ / (2 x t_{Bit})	0.396			-
D2, duty cycle 2 (20kBit/s)	TH_{Rec}(min) = 0.422 x V_{BAT}; TH_{Dom}(min) = 0.284 x V_{BAT}; V_{BAT} = 7.6V...18V;t_{Bit} = 50µs; D2 = t_{Bus_rec}(max) / (2 x t_{Bit})			0.581	-
D3, duty cycle 3 (10.4kBit/s)	$TH_{Rec(max)}$ = 0.778 x V_{BAT}; $TH_{Dom(max)}$ = 0.616 x V_{BAT}; V_{BAT} = 7.0V...18V; t_{Bit} = 96µs; D3 = $t_{Bus\_rec(min)}$ / (2 x t_{Bit})	0.417			-
D4, duty cycle 4 (10.4kBit/s)	$TH_{Rec(min)}$ = 0.389 x V_{BAT}; $TH_{Dom(min)}$ = 0.251 x V_{BAT}; V_{BAT} = 7.6V...18V; t_{Bit} = 96µs; D4 = $t_{Bus\_rec(max)}$ / (2 x t_{Bit})			0.590	-
GPIO					
V_{IH}	High-level input voltage threshold	2		VDD3V3+0.3	V

Parameter	Conditions/Comments	Min.	Typ.	Max.	Unit
V_{IL}	Low-level input voltage threshold	-0.3		0.8	V
I_{OH}	High-level output current PDRV=0,V_{OH}=VDD3V3-0.8V	4			mA
	High-level output current PDRV=1,V_{OH}=VDD3V3-0.8V	8			mA
	High-level output current PDRV=2,V_{OH}=VDD3V3-0.8V	12			mA
	High-level output current PDRV=3,V_{OH}=VDD3V3-0.8V	16			mA
I_{OL}	Low-level output current PDRV=0,V_{OL}=0.5V	4			mA
	Low-level output current PDRV=1,V_{OL}=0.5V	8			mA
	Low-level output current PDRV=2,V_{OL}=0.5V	12			mA
	Low-level output current PDRV=3,V_{OL}=0.5V	16			mA
I_{IH}	Input leakage current V_{LDO5V}=5.5V, V_{PIN}=5.5V	-1		1	μA
R_{PU}	Pull-up resistor on GPIOx pin		100		kΩ
R_{PD}	Pull-down resistor on GPIOx pin		100		kΩ
R_{PU_SWDIO}	Pull-up resistor on SWDIO pin	22		110	kΩ
R_{PD_SWCLK}	Pull-down resistor on SWCLK pin	22		110	kΩ

Note:

1. Electrical characteristics are valid over the full temperature range of Tj = -40°C to +150°C and a supply range of 6V <= VBAT <= 19V unless otherwise noted
2. The figure below shows the relation between the propagation delay, the TX thresholds and associated receiver duty cycles. Refer to D1 to D4 duty cycles in the table above for THRec and THDom threshold levels

5 MCU Feature Description

5.1 Cortex-M0 Processor

The iND83213A features with one ARM Cortex-M0 processor. The processor supports SysTick timer and single-cycle 32-bit x 32-bit multiply instruction.

5.2 SRAM

The MCU implements 16KB of SRAM. MCU can execute codes from the SRAM. The available address of SRAM is from 0x20000000 to 0x20003FFF.

5.3 Flash Memory

The MCU implements 64KB of flash memory. MCU can execute codes from the flash memory. The available address of flash memory is from 0x00000000 to 0x0000FFFF. The flash memory has x32 configuration, sector and chip erase and byte program capability. It also integrates extra five sectors of 512 bytes non-volatile registers (NVR) to store factory trim data.

In normal operation, the MCU core only fetches instructions or loads data from the flash memory but it is also possible for a program to alter the content of the flash memory. The following operations can be performed in the flash memory:

- Byte write
- Sector erase
- Block erase
- Code protect

For a description of the flash memory registers, please refer to the product register map. Here is a simple description of the basic features supported:

- Registers support to write/erase data to a byte, sector address
- Support programmable read wait states (1)
- Support system clock divider for write/erase functions
- Protection mechanism to unlock flash memory write and start flash memory byte-write
- Protection mechanism to unlock flash memory sector erase

Note:

1. The design is implemented such that the timings associated with the flash macro meet the maximum speed of the system clock requirements

5.4 Vector Table

The address starts with 0x00000000 is the vector table defined by Cortex-M0 architecture. The first 148-byte space of flash memory is used on the device, including an initial stack pointer value, 5 MCU core interrupt vectors, 16 ASIC peripheral interrupt vectors and 5 MCU peripheral interrupt vectors. The following table shows the definitions of all vectors used by the microcontroller

Word Offset	Address	Definitions
0	0x00000000	Initial MSP value
1	0x00000004	Reset vector
2	0x00000008	Not used (no NMI implemented)
3	0x0000000C	Hard fault vector
4, 5, 6, 7, 8, 9, 10	0x00000010 to 0x00000028	Not used
11	0x0000002C	SVC vector
12, 13	0x00000030 to 0x00000034	Not used
14	0x00000038	PendSV vector
15	0x0000003C	SysTick vector
16	0x00000040	Wake up LIN slave
17	0x00000044	Auxiliary PWM interrupt vector
18	0x00000048	Wake up timer interrupt vector
19	0x0000004C	BOR interrupt vector
20	0x00000050	Over/under voltage interrupt vector
21	0x00000054	Over temperature interrupt vector
22	0x00000058	ASIC watchdog interrupt vector
23	0x0000005C	GPIO interrupt vector
24	0x00000060	LIN slave interrupt vector
25	0x00000064	Reserved
26	0x00000068	UART interrupt vector
27	0x0000006C	ADC interrupt vector
28	0x00000070	PWM interrupt vector
29	0x00000074	Buck interrupt vector
30	0x00000078	SPI interrupt vector
31	0x0000007C	Lullaby interrupt vector
32	0x00000080	Timer0 interrupt vector
33	0x00000084	Timer1 interrupt vector
34	0x00000088	Timer2 interrupt vector
35	0x0000008C	MCU watchdog interrupt vector
36	0x00000090	BTE interrupt vector
37	0x00000094	Reserved

5.5 Interrupt

The Cortex-M0 core implements an NVIC (Nested Vector Interrupt Controller) peripheral capable of handling up to 32 peripheral's interrupts. Upon reset the microcontroller can answer only to Reset, NMI (Non-Maskable Interrupt) and Hard-Fault interrupts/exceptions. All other interrupts must be enabled. To enable and disable the interrupts the user must use access the ISER (Interrupt Set Enable Register) and ICER (Interrupt Clear Enable Interrupt) registers associated with the desired interrupt.

5.6 Code Protection

The controlled access to the flash content is based on disabling all communications with the debug interface, therefore preventing any external attack. Hence, the application code is still able to modify the Flash content.

Upon Power-On Reset or Normal Reset, MCU core disables the communication with the debug interface for a small time interval (8192 system clock cycles). If the application needs to be protected it is mandatory to set the protection register with the appropriate code in the beginning of the initialization process and before the internal hardware enable the debug communication. In other words, if during this time interval the protection register is loaded with a specific pattern, then the communication remains disabled after the end of this interval and stays disabled until this register is loaded with a different pattern. To allow for debug communication the application has only to write a different value in the lock register.

If a part is protected, the emulator can still erase and program the part, but first it will be required to erase the flash memory, therefore protecting it.

5.7 SysTick Timer

SysTick timer is an optional part of the Cortex-M0. SysTick timer has a 24-bit count-down counter and can trigger an interrupt when the counter counts to zero. For more details, please refer to the documentation of Cortex-M0.

5.8 General-purpose Timer

The MCU also implements three simple count-up timers: timer 0, timer 1 and timer 2. All three timers use the system clock as the clock source. They increment at the system clock rate starting from the loaded value in the counter until they overflow from 0xFFFFFFFF to 0x00000000. At this point, an interrupt request generates.

The operation of the timers is quite simple:

1. Load the **TIMERx.COUNT** with the required initial value
2. Enable the timer by writing 1 to **TIMERx.ENA**
3. Enable the related interrupt in NVIC register if needed

Please be aware that the general-purpose timers will increment from 0x00000000 after the counter overflows. It's recommended to reload the value in the interrupt routine.

5.9 MCU Watchdog Timer

The MCU implements a WDT (watchdog timer) that can operate in one of two ways:

- Interrupt Mode: In the event of a WDT rollover, an interrupt will be generated
- Reset Mode: In the event of a WDT rollover, the microcontroller will reset

The WDT supports Reset, Enable, status/flag and clear functions. It integrates a prescaler that can divide the system clock by 2^{13}, 2^{19}, 2^{22} or 2^{32}. It means that the WDT internal counter will count from 0 to the pre-scaler value at the system clock speed and trigger if not cleared.

For instance, a system running from a 16MHz system clock and 222 prescaler value will trigger the WDT after approximately 0.26 seconds if not cleared properly and in time by the application.

5.10 MCU Core to ASIC Interface

The ASIC die will be communicating to the MCU die with Cortex-M0 processor through a proprietary interface. The interface used with MCU should be fully kept as is to enable any swap between ASIC die and MCU die.

6 ASIC Feature Description

6.1 Clock

Two clock sources are integrated in the device. The system clock is based on a RC network and will be trimmed to meet the accuracy requirements specified in the EC table. Additionally, an auxiliary clock will be used during sleep.

6.2 Reset

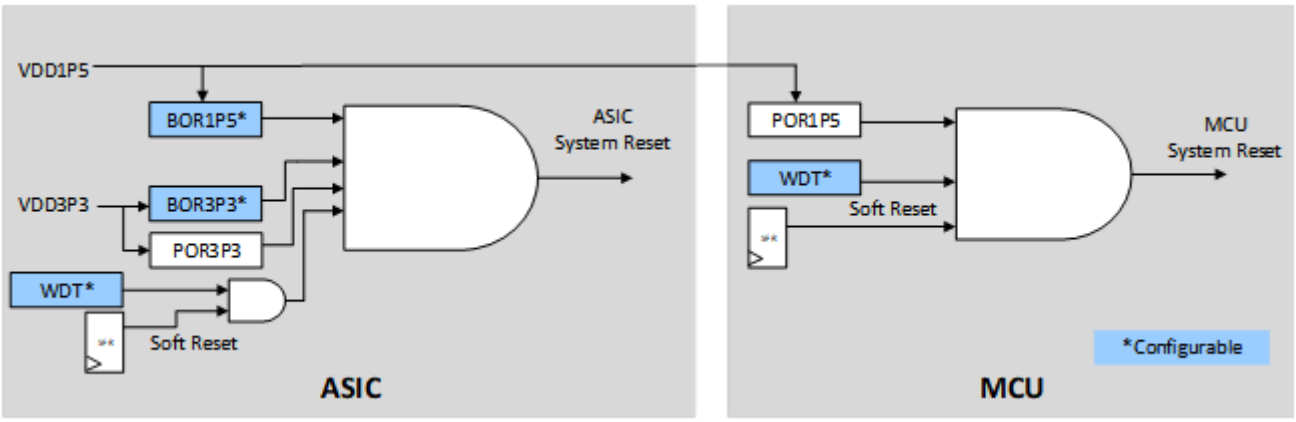
Both ASIC and MCU integrates Power on Reset (POR) circuitry: MCU POR monitors its input supply and generate a reset every time the MCU supply is recycled. ASIC POR monitors the main 3V3 LDO supply and generate a reset every time the LDO supply is recycled. Both POR maintain their output reset active if the monitored supply voltage is not above the minimum supply level to ensure safe logic operation of the power management unit (PMU) including the necessary analog features such as clock generator, bandgap, etc. This level is hardcoded and process technology dependent.

Additionally, the ASIC integrates BOR (brown out reset) circuit detectors that are configurable by SW (enable/disable as well as threshold programmable for the main ASIC core supply) and are actively monitored by the ASIC power management unit (PMU). In case any BOR is triggered, the PMU can be configured to either do the following (per BOR blocks).

- Trigger a system reset
- Generate an interrupt to the MCU for further actions
- Do nothing

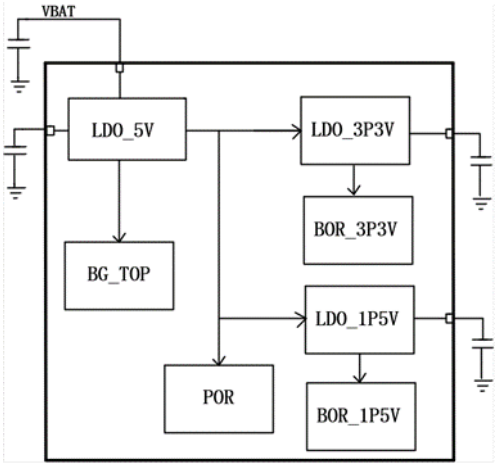
Finally, the MCU watchdog timer (if configured to do so) or a reset instruction can reset the MCU logic while on the ASIC side the watchdog timer (if configured to do so) or a reset register write can reset the ASIC system.

The block diagram below illustrates the possible triggers of a reset on both side of the design: ASIC and MCU.



6.3 PMU and Load Dump Protect Circuits

The iND83213A can withstand wide voltage transients during load-dump and cold-crank conditions due to its internal wide input range (up to 40V) PMU block. Specifically, the PMU block includes:



1. LDO5V: It is an always-on block and regulates the voltage from VIN to 5.0V. Most of analog blocks are powered by the main LDO. The output pin of main LDO needs a 4.7μF (typ.) off-chip capacitor. It has internal output over current limit protection (OCP), which can protect the LDO from start-up over-voltage damage and short-GND damage.

2. VDD1V5: it regulates the voltage from VDD5P0 to 1.5V as the power supply of digital part and the MCU. It needs a 2.2μF off-chip capacitor. It has internal output over current limit protection.

3. VDD3V3: it regulates the voltage from VDD5P0 to 3.3V as the power supply of GPIO part and the MCU. It needs a 2.2μF off-chip capacitor. It has internal output over current limit protection.

4. POR and BOR: All the LDOs output are detected by POR or BOR circuit. It can release the according part when LDO exceed POR(BOR) threshold, or reset it when LDO under POR(BOR) threshold, which can insure the analog and digital parts powered by LDO work under appropriate voltage.

5. Bandgap: the internal high-precise bandgap is used for ADC and other detection blocks as voltage or bias current reference.

6.4 LIN Transceiver

Supports LIN protocol controller according to LIN 2.x and SAE J2602 (rev J2602-1_201211). The IC contains an integrated PHY for low-speed vehicle serial data network communication using the LIN protocol.

6.4.1 LIN RxD Debounce

For preventing RxD spikes in case of RF interferences and automotive pulses, two digital glitch filters are integrated in the data pathes of LIN RxD.

Debounce thresholds for low to high and high to low can be programmable independently.

$$T_{thres} = \left(T_{hfosc}\right) \times LINDBNCTHRESx$$

For instance, the default DBNCTHRES value is 0x30 and HFOSC freq is 16MHz.Thus the default debounce threshold is 62.5ns * 48 = 3 us.

6.4.2 LIN TxD Timeout Monitor

Two TxD timeout monitors are integrated to prevent dominant bus due to internal malfunction. LIN TX is controlled by TxD signal from LIN controller or GPIO (Selected by bit LINS_HWMODE in IOCTRLA->LIN). If TxD is stuck at low over a specified TxD timeout time due to a crash of

MCU/GPA/LIN controller, the integrated TxD monitor will switch off the LIN TX output automatically until a low to high transition of TxD.

6.4.3 Short LIN Bus to Ground

If the bus idle timeout monitor detects the bus is shorted to ground, LIN slave's 30k pull-up resistor will be automatically switched off to prevent a fast discharge of the car battery.

If enabled, the feature is always on even the chip is in hibernate mode.

6.4.4 External LIN Transceiver Mode

In this mode, the internal LIN transceiver is bypassed and the RxD/TxD of LIN controller is connected to an external transceiver through GPIO.

6.5 LIN Controller

6.5.1 Overview

The IC contains a LIN slave core. The LIN core is a communication controller that performs serial communication. It implements the datalink layer of the LIN protocol specification. LIN uses a single master / multiple slave concept for the message transfer between nodes of the LIN network. The LIN controller core comprises an interface to connect a micro controller that accesses the LIN core registers to control the transmission and reception of message frame.

Features:

- LIN slave controller
  - Support of LIN specification 2.2A/SAE J2602
  - Backward compatibility to LIN 1.3
- Automatic bit rate detection
- 8-byte data buffer
- 8-bit host controller interface

6.5.2 Data Length Register and Enhanced Checksum

The host controller must define the length of the data field of the current LIN frame by adjusting the data length register **LENGTH**. If the data length bits[3:0] are loaded with the value "1111b" the length of the data field is decoded from bit 5 and 4 of the identifier register (**ID**) according to table below (e.g. compatibility to LIN specification 1.1). Otherwise, the amount of data bytes can be written directly to the data length register (**LENGTH**) (supported values are 0...8).

ID (Bit 5)	ID (Bit 4)	Number of Bytes in the data field
0	0	2
0	1	2
1	0	4
1	1	8

The LIN core supports classic checksum (Spec 1.3, inverted eight-bit sum with carry over all data bytes) and enhanced checksum (Spec. 2.0, inverted eight-bit sum with carry over all data bytes and protected identifier). The host controller must set the checksum type used in the current frame by adjusting bit **ENCHK** in the data length register (set 1 for enhanced checksum, set 0 for classic checksum).

6.5.3 Timing Settings for "Wake up Repeat Time" and "Bus Inactivity Time"

The time for repeating of wake up because of no reaction on the bus and for go to sleep because of inactivity on the bus can be optionally written by the host controller to registers **WUPREPEAT** and **BUSINACTIVE** (address 0x0F).

WUPREPEAT [1:0]	LIN Wake-Up Repeat Time (msec.)
00	180
01	200
10	220
11	240

BUSINACTIVE [1:0]	LIN Inactivity Time (s)
00	4
01	6
10	8
11	10

6.5.4 Bit Time Settings

The bit rate of the LIN system must be defined in the bit timing registers.

Name	Description	Width(bits)
BTDIV	Bit time divider	9
PRESCL	Clock prescaler	2

The LIN bit rate f_{bit} can be calculated from system clock f_{clock} and bit timing registers according to the following general equation:

$$f_{bit} = \frac{f_{clock}}{2^{prescl} * bt_{div} * (bt_{mul} + 1)}$$

For the slave controller, the bit timing registers adjustment of slave is the following:

The steps for adjusting the bit timing registers of the LIN slave are explained below.

Note:

1. The LIN core slave synchronizes to any bit rate between 1 kbit/s and 20 kbit/s. Nevertheless, the bit timing registers must be adjusted to adapt the LIN core to the used system clock frequency.

Setting up the pre-scaler register depending on system clock according to the following equation; the value must be rounded down to the next integer value:

$$PRESCL = \ln\left(\frac{f_{clock}}{20kHz * 200}\right) * \frac{1}{\ln 2}$$

Adjusting the bit time divider depending on system clock and pre-scaler according to the following equation; the value must be rounded down to the next integer value:

$$BT_{DIV} = \frac{f_{clock}}{2^{prescl} * 20kHz}$$

System Clock	PRESCL	BTDIV
8MHz	1	200
12MHz	1	300
16MHz	2	200

6.5.5 Controlling The LIN Core (Slave) by a Host Controller

The first step before transmitting messages with the LIN core is setting up the bit rate of the LIN system. For that, the host controller must load the bit time registers. After that, the message transfer can be started. The LIN core slave detects the header of the message frame sent by the LIN master and synchronizes its internal bit time to the master bit time. An interrupt to the host controller is requested after the reception of the **ID** field, after the reception of a wake-up signal (if the slave is in sleep mode), when an error is detected or when the message transfer is completed.

The following steps should be done by the host controller when an interrupt is requested.

1. Check bit **DATAREQ** in the status register (it is 1 when the **ID** field has been received). Proceed with the following if **DATAREQ** is set else proceed with step 2
   a) Load the identifier from the ID register and process it
   b) Adjust the bit **TRANSMIT** in the control register (1 - if the current frame is a transmit operation for the slave, 0 - if the current frame is a receive operation for the slave)
   c) Load the data length in the data LENGHT register (number of data bytes or value "1111b" if the data length should be decoded from the identifier) and set the checksum type (enhanced checksum (Bit **ENHCHK** = 1) or classic checksum (Bit **ENHCHK** = 0))
   d) Load the data to transmit into the data buffer (for transmit operation only)
   e) Set the bit **DATAACK** in the control register
2. Check bit **ERROR** in the status register. Perform error handling and proceed with step 6 if bit ERROR is set else proceed with step 3.
3. Check bit **BUSIDLETIMEOUT** in the status register and activate the sleep mode by setting bit **SLEEP** in the control register if **BUSIDLETIMEOUT** is set.
4. Check bit **WAKEUP** in the status register (it is set if the slave has received a wake-up signal). If **WAKEUP** is set proceed with step 6 else proceed with step 5.
5. Check bit **COMPLETE** in the status register (it is set if the transmission was successful). If **COMPLETE** is set and the current frame was a receive operation for the slave, load the received data bytes from the data buffer.
6. Set the bits **RSTINT** (reset interrupt) and **RSTERR** (reset error) in the control register to reset the interrupt request and the error flags.

Note:

1. Steps a..e have to be done during the in-frame response space, if the current frame is a transmit operation for the slave; otherwise a timeout will be detected by the master. If the current frame

is a receive operation for the slave, steps a..e have to be finished until the reception of the first byte after the identifier field (**ID**). Otherwise, the internal receive buffer of the slave core will be overwritten and a timeout error will be detected in the slave core.

2. If the host controller of the slave detects an unknown identifier (e.g. extended identifier) it has to write a '1' to bit "stop" in control register instead of setting bit **DATAACK** (steps b .. e can be skipped). In that case the LIN core slave stops the processing of the LIN communication until the next break-sync field is received.
3. Bit **TIMEOUT** in the error register and bit **WAKEUP** in the status register are set if the slave has sent a wake-up signal but the master did not respond within 150ms
4. Bit **COMPLETE** in the status register is not changed when a wake-up signal is transmitted or received. Therefore, bit **WAKEUP** has to be checked before bit **COMPLETE**

6.5.6 Sleep Mode and Wakeup

To reduce the systems power consumption the LIN protocol specification defines a sleep mode. The message used to broadcast a sleep mode request has to be started by the host controller of the LIN core master in the same way as a normal transmit message. The host controller of the LIN core slave has to decode the sleep mode frame from identifier and data bytes. After that, it has to put the LIN slave node into the sleep mode by setting bit **SLEEP** in the control register. If bit **SLEEP** in the control register of the LIN core slave is not set and there is no bus activity for 4s to 10s (specified bus idle timeout), bit **SLEEP** & **BUSIDLETIMOUT** are set and an interrupt request is generated. After that application has to understand that the LIN bus is in sleep mode. The bus inactivity time which should be defined as bus idle timeout for the slave can optionally set to values 4s, 6s, 8s or 10s as possible accordingly with specification 2.2A.

After receiving a wake-up signal from the master or any slave node a wake-up request is generated, the host controller terminates the sleep mode of the LIN bus by clearing bit **SLEEP** in the control register.

Note:

(1) Don't enter hibernate mode when bit **SLEEP** = 0, because in this state dominant signal will not be taken as a wake-up request.

To send a wake-up signal, the host controller of the LIN core must set the bit **WAKEUPREQ** in the control register. After successful transmission of the wake-up signal with the LIN core master the **WAKEUP** bit in the status register of the sending LIN core master is set and an interrupt request is generated. The LIN core slave does not generate an interrupt request after successful transmission of the wake-up signal but it generates an interrupt request if the master does not respond to the wake-up signal within 150ms to 250ms. This value can be set optionally to 180ms, 200ms, 220ms or 240ms as it is possible accordingly with specification 2.2A. In that case, bit **ERROR** and bit **TIMEOUT** are set. The host controller must decide whether to transmit another wake-up signal or not.

6.5.7 Error Detection and Handling

The LIN core generates an interrupt request and stops the processing of the current frame if it detects the following errors:

- BITMON: The bit value monitored on the bus is different from the sent bit value
- Timeout caused by wake-up repeat timeout
- BUS IDLE timeout

The errors detected in break/sync field will be ignored by LIN controller. The other errors happen in ID/data field will be recorded. In DataReq interrupt routine, the application must check the type of error by processing the **ERROR** register. After that, it must reset the **ERROR** register and the **ERROR** bit in status register by writing a 1 to bit **RSTERR** in control register.

6.6 Buck Regulator

The chip has a high-integrated, synchronous, step-down DC/DC converter. With integrated high-side and low-side power MOSFETs, up to 1.2A of output current is delivered over a wide input voltage range of 4.2V to 40V and an output voltage range of 3.0V to 5.5V. The buck uses peak-current-mode control to provide optimal efficiency and output voltage accuracy.

The buck regulator works in FPWM mode, which works with constant switching frequency at 400kHz during the whole load range, to meet the EMI standard requirements.

To start the buck regulator, the following sequences are recommended:

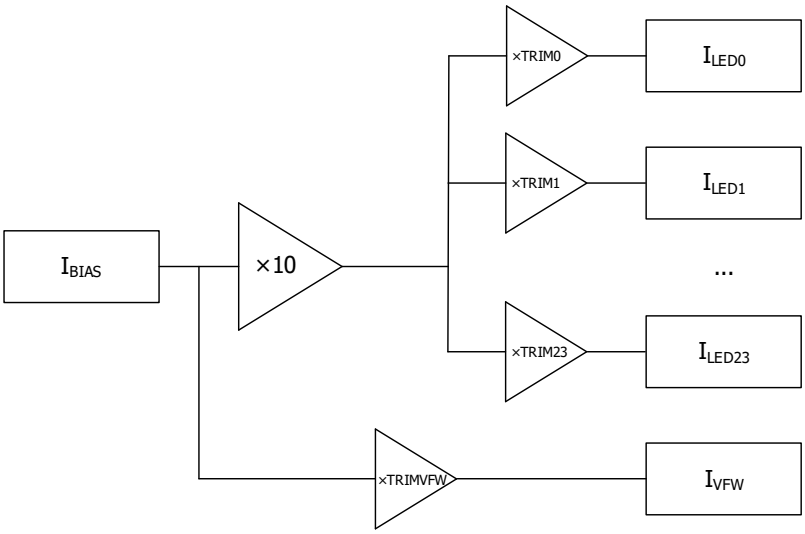
1. Set the output voltage. **VDAC_TRIM** controls the voltage of output reference, the formula below calculates the output voltage, for example, V_{BUOUT} = 5.0V when **VDAC_TRIM** = 32

$$V_{BUOUT} = \frac{\text{VDAC\_TRIM}}{6.4} V$$

2. Update the output reference by writing 1 to **RAMP_UPDATE** and wait until **RAMP_UPDATE** back to 0
3. If spread spectrum feature is needed, configurate **SEL_SSC_STEP** and write 1 to **SSC_ENA**. Otherwise, write 0 to **SSC_ENA**
4. Start buck converter by writing 1 to **BUCK_ENA**

6.7 LED Current Source

ASIC integrates a high precision open drain LED driver stage that allows for tuning LED currents in a wide range up to 50mA and precise step in 100μA step.



All the LED current sources share a single factory-calibrated precise bias current source (I_{BIAS}), the typical value is 10μA for default value **LEDBIASTRIM=128**, the tuning step is about 50nA.

The driver stages allow a linearly control of LED driver current (I_{LED}) with 100μA step. The desired current is provided according the formula below:

$$I_{LED} = TRIM[8:0] * I_{BIAS} * 10 = TRIM[8:0] * 100\mu A$$

The LED forward voltage measurement bias is also derived from the precise bias current source (I_{BIAS}).

$$I_{VFW} = TRIMVFW[7:0] * I_{BIAS} = TRIMVFW[7:0] * 10\mu A$$

The table below shows the typical value for some common conditions:

Item	LEDBIASTRIM register	TRIM register	TRIMVFW register
I_{LED}=30mA	128	300	
I_{VFW}=2mA			200

Due to the mismatch of the process, the **LEDBIASTRIM**, **TRIMVFW** and **TRIM0** - **TRIM23** value will be calibrated for I_{LED}=30mA, and I_{VFW}=2mA condition. Any other I_{LED} or I_{VFW} current for the corresponding channel can be linearly converted from the factory-calibrated trim code. Only the factory-calibrated value should be applied for **LEDBIASTRIM** register for best performance.

For example, to change the LED current to 45mA, the value written to **TRIMx** register should be:

$$TRIM_X = \frac{TRIM_{X\_30mA} * 45mA}{30mA}$$

At the same time, the register **LEDBIASTRIM** should be kept as factory-trimmed 10μA code.

6.8 Analog-to-digital Converter (ADC)

Features:

- 12-bit resolution, single ended input
- Bandgap voltage reference
- Up to 43 available channels
  - 24 differential LED PN voltage channels
  - 8 single-ended GPIO channels
  - 5 single-ended power voltage channels
    - V_{buck} (Gain=1/4)
    - V_{LDO5V} (Gain=1/4)
    - V_{VDD3V3}
    - V_{VDD1V5}
    - V_{BAT} (Gain=1/14 or 1/28)
  - 3 self-calibration channels
    - P: ADC_REFp, N: ADC_REFp
    - P: ADC_REFp, N: VREF_GND
    - P: VREF_GND, N: ADC_REFp
  - 2 differential temperature sensor channels
    - LED temperature sensor
    - Buck temperature sensor
  - 1 differential GPIO channels
    - P: GPIO6, N: GPIO7

- Up to 3 ADC reference voltages for each channel
  - V_{bg} (1.2V)
  - 2*V_{bg} (2.4V)
  - VDD_{3V3} (3.3V)
- Up to 3 ADC gain selection for each channel
  - 14/32
  - 22/32
  - 31/32
- ADC system capable of being configured for single or automatic multiple channels(up to 4 channels) conversion (VBAT, LED and temperature sensor)
- Interrupt on conversion complete regardless of digital comparator configuration

6.9 Over and Under Voltage Detection (VBAT)

The over and under voltage comparators are based on comparing a divided voltage from the load dump limiter output feeding an analog comparator with hysteresis (refer to EC table for electrical parameters and PMU description). The over and under voltage events generate Interrupts to the interrupt controller.

6.10 Temperature Monitor

The MCU is in charge to pull the ADC related data from temperature sensor and in case the measured data is too high, MCU will reduce power profile to reduce heat.

6.11 Over Temperature Detection

The over temperature comparator monitors the junction temperature with hysteresis. The over temperature event generates reset or interrupt to the interrupt controller.

6.12 General-purpose I/O

The GPIOs support digital input, digital output, ADC input and can be multiplexed to other peripheral.

Features:

- Up to 8 GPIOs available
- External interrupt for both rising edge and falling edge
- Gated clock to save power
- Read/write multiple GPIOs in a single operation with the **GPxDATA** register matrix
- Output drive strength supports 4mA, 8mA, 12mA, 16mA controlled by **PDVR1** and **PDVR0** registers
- Adjustable slew rate controlled by **SL** register (fast/slow)
- Both internal pull-up and pull-down resistor is supported (100kΩ typ.) and controlled by **PUENA** and **PDENA** register
- Standard 3.3V IO, not 5V input tolerant
- One pair of GPIOs support differential ADC input
- All GPIOs support single-ended ADC input
- All GPIOs can be multiplexed as PWM output (up to 5 PWM channels)

There are two GPIO controller units, each unit can manage up to 8 GPIOs. All GPIOs in a unit can be operated in a single operation. The register **GPADATA** and **GPBDATA** are register matrices which both occupy 1024 bytes address space (10-bit).

GPIO Controller Address	GPIO Pin Name
GPA[0]	GPIO1
GPA[1]	GPIO2
GPA[2]	GPIO3
GPA[3]	GPIO4
GPA[4]	GPIO5
GPA[5]	GPIO6
GPA[6]	GPIO7
GPA[7]	GPIO8
GPB[0]	Reserved
GPB[1]	LIN_IN
GPB[2]	Reserved
GPB[3]	Not used
GPB[4]	Not used
GPB[5]	Not used
GPB[6]	Not used
GPB[7]	Not used

In the GPIO register matrix operation, the more significant 8 bits of address controls the select signal and the 8-bit value is the level signal. For example, write (1<<0|0<<2) to the **GPADATA** register with word offset (1<<0|1<<2) will change GPIO1 to low level and change GPIO3 to high level without any influence on other GPIOs. Read/Write the **GPADATA** register with the word offset 0xFF will read/write all GPIOs at the same time.

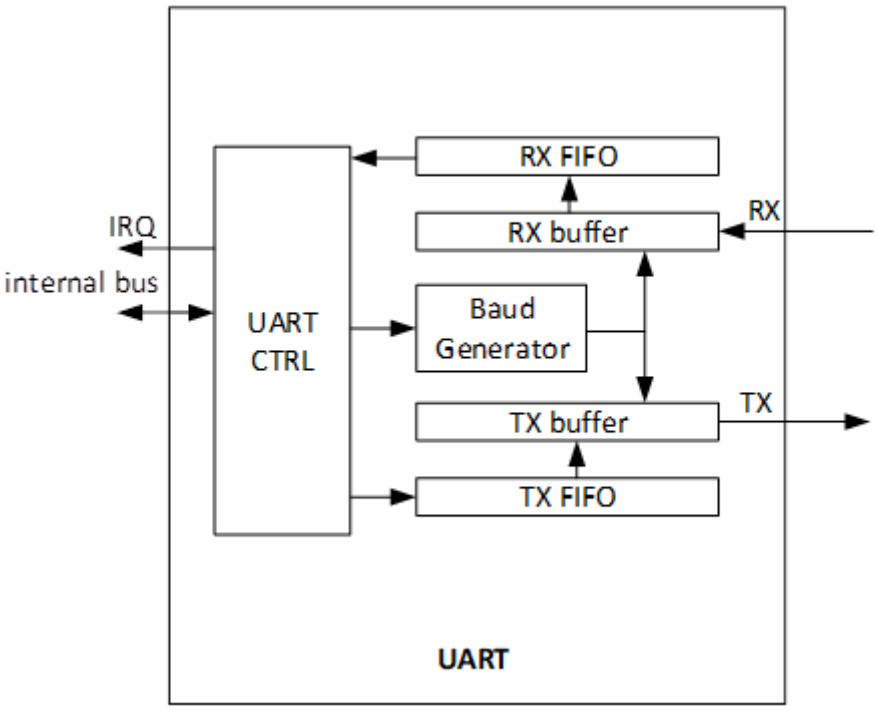
There are all available registers about GPIO configuration:

- **GPIO.GPxENA** (x=A,B) enables the gated clock of GPIO unit
- **GPIO.GPxDIR[n]** (x=A,B and n=0,1,2,3,4,5,6,7) enables the push-pull output
- **IOCTRLA.GPIOx.RDENA** (n=1,2,3,4,5,6,7,8) enables the input path
- **GPIO.GPxDATA<1024>** (x=A,B) reads/writes the level of GPIO input/output
- **IOCTRLA.GPIOx.PDVR0** and **IOCTRLA.GPIOx.PDVR1** (n=1,2,3,4,5,6,7,8) controls the GPIO output drive strength
- **IOCTRLA.GPIOx.SL** (n=1,2,3,4,5,6,7,8) controls the output slew rate
- **IOCTRLA.GPIOx.CS** (n=1,2,3,4,5,6,7,8) enables the input Schmitt trigger
- **IOCTRLA.GPIOx.PUENA** and **IOCTRLA.GPIOx.PDENA** (n=1,2,3,4,5,6,7,8) enables the pull-up and pull-down
- **GPIO.GPxIE[n]** (x=A,B and n=0,1,2,3,4,5,6,7) enables the edge interrupt
- **GPIO.GPxRE[n]** (x=A,B and n=0,1,2,3,4,5,6,7) enables the rising edge interrupt
- **GPIO.GPxFE[n]** (x=A,B and n=0,1,2,3,4,5,6,7) enables the falling edge interrupt
- **GPIO.GPxACTDET[n]** (x=A,B and n=0,1,2,3,4,5,6,7) indicates the interrupt flag
- **GPIO.GPxCLR[n]** (x=A,B and n=0,1,2,3,4,5,6,7) clears the interrupt flag
- **IOCTRLA.GPIOx.HWMODE** (n=1,2,3,4,5,6,7,8) controls the digital multiplexing selection
- **SAR_CTRL.CHn_SEL** (n=1,2,3,4) enables the analog path from GPIO to ADC

All GPIO interrupts share a same interrupt number, users must check the **GPIO.GPxACTDET[n]** registers to determine the actual interrupt source.

6.13 Universal Asynchronous Receiver Transmitter (UART)

The UART circuit includes a 'baud' rate generator with software-programmable divider ratios for rates from 100kHz to 2MHz. The UART features a 32-bytes-deep receive/transmit FIFO that minimizes the microcontroller overhead command and provides a set of maskable interrupt support to monitor and manage TX and RX data paths. The UART does not include any HW to filter out received messages that are not matching the LIN ID address. In other words, the address associated with the master command will have to be decoded and executed if the ID matches. It is expected that given the clock source, the embedded FW may have to compensate for clock frequency drift over temperature to keep a reliable communication path between nodes.



6.14 Serial Peripheral Interface (SPI)

The digital engine supports an SPI interface for system expansion. The microcontroller serves as the master. A GPIO pin can be used to gate power to an external SPI device. The SPI signal pins, may also be configured as GPIO pins.

The Serial Peripheral Interface (SPI) is a synchronous full-duplex serial interface. It communicates in master/slave mode where the master initiates the data transfer. For this SPI interface, only the master mode is implemented.

Features:

- Compatible with an Industry Standard SPI interface
- 32-byte deep reception FIFO, shared with UART
- 32-byte deep transmission FIFO, shared with UART
- Interrupt upon events related to transmission, reception, and error:
  - Write Collision
  - Transmission FIFO full and empty
  - Reception FIFO full and empty

6.15 LED PWM

LED PWMs are used to control the light intensity accurately.

Features:

- 24x16-bit PWM channels with shared period length, independent pulse rise and independent pulse fall timestamps
- Frequency and duty cycle of PWM waveform support up to a maximum resolution of 16 bits. The resolution is 16-bit only when the PWM counter period register **PERIOD** is the maximum value
- Programmable pre-scaler: system clock division **PRESCALESEL** (PWM_{DIV})
- Programmable PWM period register **PERIOD** (PWM_{PER})

$$Period = \frac{1 + (PWM_{PER} \times PWM_{DIV})}{F_{sys}}$$

- Programmable duty cycle 0 to 100% (PWM_{PW})

$$PulseWidth = \frac{1 + \left((PWM_{PFALL} - PWM_{PRISE}) \times PWM_{DIV}\right)}{F_{sys}}$$

- Pre-scaler, period, pulse rise & pulse fall configurations will be updated at the end of the current output period if there is a pending **UPDATE** bit
- Support interrupt generation when new programmed PWM control data become active. After new pulse parameters (Period, pulse rise & pulse fall) have been loaded into their respective registers, an **UPDATE** bit can be set to 1 that will trigger the activation of the new parameters at the end of the current pulse as not to affect the pulse shape.
- PWM frequency range from 80Hz to 250Hz
- Parameter cases for different P_{RISE}, P_{FALL}, listed in priority:
  - $P_{RISE} = 0, P_{FALL} = PERIOD$: 100% on
  - $P_{RISE} < P_{FALL}$: Normal case. on at P_{RISE}, off at P_{FALL}.
  - $P_{RISE} = 0, P_{FALL} = 0$: equivalent to $P_{RISE} = 0, P_{FALL} = 1$
  - $P_{RISE} \geq P_{FALL}$: 100% off

6.16 Auxiliary PWM

The auxiliary PWM generates PWM waveform to GPIO.

Features:

- 2 shared PWM counter, each channel and counter can be attached freely
- 5x16-bit PWM channels with shared PWM counter, independent pulse rise and independent pulse fall timestamps
- Frequency and duty cycle of PWM waveform support up to a maximum resolution of 16 bits. The resolution is 16-bit only when the PWM counter period register **PERIOD** is the maximum value
- Programmable pre-scaler: system clock division **PRESCALESEL** (PWM_{DIV})
- Programmable PWM period register **PERIOD** (PWM_{PER})

$$Period = \frac{1 + (PWM_{PER} \times PWM_{DIV})}{F_{sys}}$$

- Programmable duty cycle 0 to 100% (PWM_{PW})

$$PulseWidth = \frac{1 + \left((PWM_{PFALL} - PWM_{PRISE}) \times PWM_{DIV}\right)}{F_{sys}}$$

- Pre-scaler, period, pulse rise & pulse fall configurations will be updated at the end of the current output period if there is a pending **UPDATE** bit
- Support interrupt generation when new programmed PWM control data become active. After new pulse parameters (Period, pulse rise & pulse fall) have been loaded into their respective registers, an **UPDATE** bit can be set to 1 that will trigger the activation of the new parameters at the end of the current pulse as not to affect the pulse shape.
- PWM frequency range from 80Hz to 250Hz
- Parameter cases for different P_{RISE}, P_{FALL}, listed in priority:
  - $P_{RISE} = 0, P_{FALL} = PERIOD$: 100% on
  - $P_{RISE} < P_{FALL}$: Normal case. on at P_{RISE}, off at P_{FALL}.
  - $P_{RISE} = 0, P_{FALL} = 0$: equivalent to $P_{RISE} = 0, P_{FALL} = 1$
  - $P_{RISE} \geq P_{FALL}$: 100% off

6.17 Hibernate Mode

IC must be able to enter sleep mode through SW request. The device should be able to come out of sleep with either the slow auxiliary clock or the system clock. It's up to the SW to select which clock shall be used after a wake event is detected. The SW should not have to request to go to sleep with the same clock selected for wake up.

6.18 Wake-up Mode

Coming out from sleep mode can happen through the following events:

- After a low pulse on the LIN pin such that a dominant (low) voltage level is applied for longer than T_{WAKEUP} time.
- GPIOs pin toggling either from high to low or low to high levels (V_{IL}/V_{IH}) and maintaining the active state for more than T_{WAKEUP} time.
- Wake up timer. Programmable range, refer the EC Table. Wake up timer should have the option to be disabled.

MCU should be able to check which wake up events triggered the system through a status register read. GPIOs trigger should be consolidated into 1 status register. MCU to clear the register after status check.

6.19 ASIC Watchdog Timer

While it exists a watchdog timer in the MCU, the ASIC integrates another watchdog timer that is intended to be used to recover from a situation where there may have been a software fault or other system failure where the software has ceased to operate correctly. If the timer is not reset by software periodically, it will time out, and this event can be used to reset the system or generate an interrupt.

Features:

- Programmable timeout period with instantaneous access to the value of watchdog timeout counter
- Running with 16kHz clock derived from the auxiliary clock independent of system clock
- Status flag, stop and clear/reset control registers
- The watchdog timer is by default active after power up and set to its maximum duration setting
- Window mode supported: If enabled, WDTA can only be cleared after the watchdog window opened and before time-out period; Otherwise, WDTA will issue a system reset or an interrupt.

7 Register Map

Peripherals List		
Address	**Peripheral**	**Description**
0x50000000 - 0x5000003F	CRGA	Clock & Reset Generator
0x50000040 - 0x5000005F	PMUA	Power Management Unit
0x50000060 - 0x5000007F	EVTHOLD	Event Hold Control
0x50000080 - 0x500000FF	BTE	Block Transfer Engine registers
0x50010100 - 0x500101FF	WICA	WakeUp Interrupt Controller
0x50010200 - 0x500102FF	WDTA	Watchdog Timer Registers
0x50010300 - 0x500103FF	LINS	LIN slave interface registers
0x50010500 - 0x500105FF	BUCK_INF	BUCK Interface Registers
0x50010600 - 0x500106FF	SAR_CTRL	SAR ADC Interface registers
0x50010700 - 0x500107FF	SPI	SPIM Interface registers
0x50010800 - 0x500108FF	UART	UART Interface registers
0x50010900 - 0x500109FF	PWM_AUX	Control (and status) registers for the pulse width modulation waveform generator.
0x50011000 - 0x50011FFF	PWM	Control (and status) registers for the pulse width modulation waveform generator.
0x50012000 - 0x50012FFF	IOCTRLA	I/O configuration and DFT pin control
0x50013000 - 0x50013FFF	SYSCTRLA	System configuration and retention memory
0x50014000 - 0x50014FFF	GPIO	GPIO bit control and configuration
0x50015000 - 0x50015FFF	PMUAPRE5V	Power Management Unit of 5V domain
0x50020000 - 0x50020007	TIMER0	General purpose timer 0 registers
0x50020008 - 0x5002000F	TIMER1	General purpose timer 1 registers
0x50020010 - 0x50020017	TIMER2	General purpose timer 2 registers
0x50020018 - 0x5002001F	WDT1	The watchdog timer that is local to VERNE MCU
0x50020020 - 0x5002005F	FLASH	FLASH Memory registers

7.1 CRGA

CRGA		
Address	**Register**	**Description**
0x50000000	LFCLKCTRL	Low frequency clock control
0x50000004	SYSCLKCTRL	System clock control
0x50000008	RESETCTRL	Reset control
0x5000000C	MODULERST	Module Reset control
0x50000010	WDTACTION	Watchdog action
0x50000014	LFCLKKILL	Low frequency clock kill
0x50000018	OVTEMPACTION	OVTEMP action
0x5000001C	OVTEMPCONFIG	OVTEMP configuration
0x50000020	OVUVACTION	OVUV action
0x50000024	MODULEGATEENA	Module Gate control

7.1.1 LFCLKCTRL

0x50000000 **LFCLKCTRL**

Low frequency clock control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F8	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F8	CLKLFSEL	LF Clock Source select. Used to select lf osc mode between, NOTE:The write operation of this field register takes effect by configuring 'SYSCTRLA_SFRS->DEBUG_ACCESS_KEY.DEBUG_ACCESS_KEY = 0x05' 0x0: CLK_LF(LF OSC out) is 256KHz, slow system clock freq is Freq_CLK_LF/2 = 128KHz. 0x1: CLK_LF(LF OSC out) is 256KHz, slow system clock freq is Freq_CLK_LF/16= 16KHz.	1	rw	0x1

F0	LFRCSTS	Slow oscillator status. Will be high when the Low Frequency oscillator is selected	1	ro	0x0

7.1.2 SYSCLKCTRL

0x50000004																SYSCLKCTRL															
System clock control.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	F20		-	F16			-	-	-	-	-	-	-	F8	-	-	-	-	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F20	HF_RC_LDO_VSEL	24MHz RC OSC LDO output select. 0x0: 1V45 Selected 0x1: 1V50 Selected 0x2: 1V55 Selected 0x3: 1V65 Selected	2	rw	0x1
F16	DIVSYSCLK	Clock div select. Select the divider ratio on the system clock when using fast oscillator 0x0: No Division. Full Clock speed. 0x1: Div by 2. 0x2: Div by 3. 0x3: Div by 4. 0x4: Div by 5. 0x5: Div by 6. 0x6: Div by 7. 0x7: Div by 8.	3	rw	0x0
F8	SYSCLKSEL	Clock select. Used to switch between the fast and slow system clocks 0x0: Slow clock 0x1: Fast clock	1	rw	0x0
F1	HFRCSTS	Fast oscillator status. Will be high when High Frequency oscillator is enabled	1	ro	0x0
F0	HFRCENA	Fast oscillator enable. Setting this bit when the High Frequency oscillator is not running will cause the oscillator to start (the PMU may have already started it). Even though the fast oscillator is running, its output is only used when selected via the clock mux - see CLKSEL. This bit is cleared automatically on entering SLEEP mode	1	rw	0x0

7.1.3 RESETCTRL

0x50000008																															
Reset control.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F24	-	-	-	-	-	-	-	F16	-	F14	F13	-	F11	-	F9	F8	-	F6	F5	-	F3	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F24	SOFTRSTREQ	Soft reset request. Set to trigger a soft reset of chip Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F16	HARDRSTREQ	Hard reset request. Set to trigger a hard reset of chip	1	wo	0x0
F14	OVTEMPFLAGCLR	OVTEMP flag clear. Set to clear the OVTEMP flag	1	wo	0x0
F13	WDTFLAGCLR	WDT flag clear. Set to clear the WDT flag	1	wo	0x0
F11	UVFLAGCLR	UV flag clear. Set to clear the UV flag	1	wo	0x0
F9	OVFLAGCLR	OV flag clear. Set to clear the OV flag	1	wo	0x0
F8	PORFLAGCLR	POR flag clear. Set to clear the POR flag	1	wo	0x0
F6	OVTEMPFLAG	Over Temp Violation flag. Set by the hardware when the over temp condition is detected.	1	ro	N/A
F5	WDTFLAG	Watchdog bark flag. Set by the hardware when the watchdog barks.	1	ro	N/A
F3	UVFLAG	Under Voltage Monitor flag. Set by the hardware when the under voltage monitor.	1	ro	N/A
F1	OVFLAG	Over Voltage Monitor flag. Set by the hardware when the over voltage monitor.	1	ro	N/A
F0	PORFLAG	Power on reset flag. Set by the hardware during power-on reset	1	ro	N/A

7.1.4 MODULERST

0x5000000C	MODULERST																													
Module Reset control.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	MODULERSTREQ	Module Soft reset request. Set to trigger a soft reset of module below. 0x1: ADC Soft reset request 0x2: BUCK Soft reset request 0x8: LINS soft reset request 0x10: PWM_AUX soft reset request 0x20: PWM soft reset request 0x40: SPI soft reset request 0x80: UART soft reset request Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	8	wo	0x0

7.1.5 WDTACTION

0x50000010	WDTACTION																													
Watchdog action.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	WDTACTION	Watchdog action. Defines the consequences of watchdog bark being detected by the hardware. 0x0: IRQ generated 0x1: Hard reset generated	1	rw	0x1

7.1.6 LFCLKKILL

0x50000014	LFCLKKILL																													
Low frequency clock kill.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	KILLLFRC	Kill slow RC oscillator. Setting this bit gates the low frequency RC oscillator input. NOTE:The write operation of this field register takes effect by configuring 'SYSCTRLA_SFRS->DEBUG_ACCESS_KEY.DEBUG_ACCESS_KEY = 0x05'	1	rw	0x0

7.1.7 OVTEMPACTION

0x50000018	OVTEMPACTION																													
OVTEMP action.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0	

#	Field Name	Field Description	Width	Access	Reset
F31	OVTEMP_LOCK	Set Only bit. Set this bit to lock OVTEMP related bits.	1	rw	0x0
F0	OVTEMP	Over Temperature action. Defines the consequences of over temp condition detected by the hardware. 0x2: No action 0x1: IRQ generated 0x0: Hard reset generated	2	rw	0x2

7.1.8 OVTEMPCONFIG

0x5000001C	OVTEMPCONFIG

OVTEMP configuration.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F4		-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F4	SEL_TSCH	Selecting the temperature sensor channel. Selecting the temperature sensor channel 0x0: channel 1 0x1: channel 2 0x2: channel 3 0x3: channel 4	2	rw	0x0

7.1.9 OVUVACTION

0x50000020	OVUVACTION

OVUV action.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	F27	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F4	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F31	UV_LOCK	Set Only bit. Set this bit to lock UV ACTION related bits.	1	rw	0x0
F27	OV_LOCK	Set Only bit. Set this bit to lock OV ACTION related bits.	1	rw	0x0
F4	UV_ACTION	Under Voltage action. Defines the consequences of under voltage condition detected by the hardware. 0x1: No action 0x0: Hard reset generated	1	rw	0x1
F0	OV_ACTION	Over Voltage action. Defines the consequences of over voltage condition detected by the hardware. 0x1: No action 0x0: Hard reset generated	1	rw	0x1

7.1.10 MODULEGATEENA

0x50000024	MODULEGATEENA

Module Gate control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0				

#	Field Name	Field Description	Width	Access	Reset
F0	MODULEGATEENA	Module Gate enable request. Set to enable the clock gate of module below. 0x1: GPIO clock gate Soft enable request 0x2: PWM clock gate Soft enable request 0x4: PWM_AUX clock gate soft enable request 0x8: UART clock gate soft enable request 0x10: SPI clock gate soft enable request	5	rw	0x1F

7.2 PMUA

PMUA		
Address	**Register**	**Description**
0x50000040	CTRL	Control
0x50000044	PMUTRIM	PMU Trim Register
0x50000048	DWELL	Dwell
0x5000004C	VBATCTRL	VBAT Monitor Register
0x50000050	VBATTRIM	VBAT Monitor Trim Register
0x50000054	VBATDBNC	VBAT Debounce Register
0x50000058	VBATDBNCTHRES	VBAT Monitor Threshold Register
0x5000005C	PMUIRQ	Voltage Monitor interrupts

7.2.1 CTRL

0x50000040	CTRL

Control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F7	F6	F5	-	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F7	DBG_OT_COMP	Enable to test the comparator of over temperature function.	1	rw	0x0
F6	DBG_IPRE	EN test IBIAS_PRE 1uA current.	1	rw	0x0
F5	DBG_1P3V	LDO_1V5 output 1.35V, Set to 1V5-LDO output 1V35.	1	rw	0x0
F3	IGNORE_CIFS	Ignore QACKs. Setting a bit in this register prevents PMUA from waiting for the assertion of the corresponding 'Quiescent State Acknowlege' signal when before transitioning towards the Hibernate state.	1	rw	0x0
F2	BG_OK	the flag of bandgap OK. the flag of bandgap OK	1	ro	N/A
F1	FASTBOOT	Fast boot. Set to enable used of the fast clock during subsequent power-up sequences (including the portion consumed by the Clough boot sequence). The set value brings the system up with the slow clock to make the initial boot and any boot after a hard reset (e.g. after a brownout) as safe as possible.	1	rw	0x1
F0	HIBERNATE	Hibernate. Set to put the chip into HIBERATE mode. Before setting this bit, ensure that wake interrupt controller HOLD bit has been set (and that a corresponding Lullaby interrupt has been received).	1	wo	0x0

7.2.2 PMUTRIM

0x50000044 **PMUTRIM**

PMU Trim Register
NOTE:The write operation of this field register takes effect by configuring 'SYSCTRLA_SFRS->PMU_ACCESS_KEY.PMU_ACCESS_KEY = 0x0A'.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	F28			-	-	F24		-	-	-	-	-	-	-	-	-	-	-	-	-	-	F8		F4				-	F0		

#	Field Name	Field Description	Width	Access	Reset
F28	VDD3V3_LDO_TRIM	3.3V LDO output trim. at PMU debug mode 0x0: 3.00V 0x1: 3.09V 0x2: 3.18V 0x3: 3.28V 0x4: 3.40V (default) 0x5: 3.52V 0x6: 3.65V 0x7: 3.80V	3	rw	0x4
F24	VDD1V5_LDO_TRIM	1.5V LDO output trim. at PMU debug mode 0x0: 1.500V 0x1: 1.545V(default) 0x2: 1.606V 0x3: 1.606V	2	rw	0x1
F8	OCP_CTRL_1V5	OCP trim for 1.5V LDO(default 30mA). 0x0: 17 mA 0x1: 30 mA (default) 0x2: 46 mA 0x3: 60 mA	2	rw	0x1
F4	OCP_CTRL_3V3	OCP trim for 3V3 LDO(default 30mA). 0x0: 9.5 mA 0x1: 11.8 mA 0x2: 14.0 mA 0x3: 16.5 mA 0x4: 18.8 mA 0x5: 21.2 mA 0x6: 23.6 mA 0x7: 26.0 mA 0x8: 28.3 mA 0x9: 30.0 mA (default) 0xa: 33.0 mA 0xb: 35.4 mA 0xc: 38.0 mA 0xd: 40.0 mA 0xe: 42.5 mA 0xf: 45.0 mA	4	rw	0x9

F0	OCP_CTRL_5V0	OCP trim for 5V LDO(default 80mA). 0x0: 53 mA 0x1: 44 mA 0x2: 35 mA 0x3: 25 mA 0x4: 115 mA 0x5: 80 mA(default) 0x6: 72 mA 0x7: 62 mA	3	rw	0x5

7.2.3 DWELL

0x50000048 **DWELL**

Dwell
NOTE:The write operation of this field register takes effect by configuring 'SYSCTRLA_SFRS->TRIM_ACCESS_KEY.TRIM_ACCESS_KEY = 0x0E'. Minimum times spent in various PMUA states. Please Note- The STARTUP_BIAS_DWELL state timeout is hardcoded to a value of 0xC. A value of 0xC in the STARTUP_BIAS_DWELL state @ 16KHz yields a delay of 1.5 milliseconds

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F12				F8				F4				F0			

#	Field Name	Field Description	Width	Access	Reset
F12	POWER_DOWN_MCU	Power down MCU dwell time. Defines the amount of time spent in the 'Power down MCU' state. Pausing here allows the MCU supplies to discharge (to guarantee subsequent POR)	4	rw	0x4
F8	ATTACH_3V3	Attach 3.3V dwell time. Defines the amount of time spent in the 'Attach 3V3' state. State Attaches 3.3V to MCU.	4	rw	0x4
F4	ATTACH_1V5	Attach 1.5V dwell time. Defines the amount of time spent in the 'Attach 1V5' state. State Attaches 1.5V to MCU.	4	rw	0x4
F0	ENABLE_1V5	Enable 1.5V dwell time. Defines the amount of time spent in the 'Enable 1V5' state. Allows 3v3 and 1v5 regs to settle	4	rw	0x4

7.2.4 VBATCTRL

0x5000004C **VBATCTRL**

VBAT Monitor Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	F27	F26	F25	F24	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F27	HIGH_DBNC	Battery Voltage High Status after deboucing. Battery monitor over voltage event signal coming from the debouncer of analog comparator circuit.	1	ro	0x0
F26	LOW_DBNC	Battery Voltage Low Status after debouncing. Battery monitor under voltage event signal coming from the debouncer of analog comparator circuit.	1	ro	0x0
F25	HIGH	Battery Voltage High Status. RAW battery monitor over voltage event signal coming from the analog comparator circuit.	1	ro	0x0
F24	LOW	Battery Voltage Low Status. RAW battery monitor under voltage event signal coming from the analog comparator circuit.	1	ro	0x0
F3	OV_POL	Battery Voltage Monitor Over Voltage Interrupt Event Polarity. Flips the over voltage event signal coming from the analog comparator circuit which feeds into the interrupt generator. 0x0: Native Polarity 0x1: Flip Polarity	1	rw	0x0
F2	UV_POL	Battery Voltage Monitor Under Voltage Interrupt Event Polarity. Flips the under voltage event signal coming from the analog comparator circuit which feeds into the interrupt generator. 0x0: Native Polarity 0x1: Flip Polarity	1	rw	0x0
F1	BAT_OV_EN	Battery Over Voltage Monitor Enable. Set to enable the vbat over voltage monitor analog comparator circuit.	1	rw	0x0
F0	BAT_UV_EN	Battery Under Voltage Monitor Enable. Set to enable the vbat under voltage monitor analog comparator circuit.	1	rw	0x0

7.2.5 VBATTRIM

0x50000050	VBATTRIM																													
VBAT Monitor Trim Register.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	F24		-	-	-	-	F16				-	-	-	-	-	-	F8		-	-	F0					

#	Field Name	Field Description	Width	Access	Reset
F24	OVHYS	Battery Voltage Monitor Over Voltage Hysterisis Select. Selects the hysterisis level for the Over Voltage monitor. 0x0: 0.359V 0x1: 0.720V 0x2: 1.080V 0x3: 1.440V	2	rw	0x1
F16	OVLEVEL	Battery Voltage Monitor Over Voltage Select. Selects the reference level for the Over Voltage monitor to output one-hot Configuration to Analog Module.(If OVLEVEL>9, the actual analog trim value is the same as default value:OVLEVEL=0x07) 0x0: Over Voltage Threshold- 10'h001: 14.67V 0x1: Over Voltage Threshold- 10'h002: 15.16V 0x2: Over Voltage Threshold- 10'h004: 15.68V 0x3: Over Voltage Threshold- 10'h008: 16.23V 0x4: Over Voltage Threshold- 10'h010: 16.83V 0x5: Over Voltage Threshold- 10'h020: 17.48V 0x6: Over Voltage Threshold- 10'h040: 18.17V 0x7: Over Voltage Threshold- 10'h080: 18.93V(default) 0x8: Over Voltage Threshold- 10'h100: 19.75V 0x9: Over Voltage Threshold- 10'h200: 20.64V	4	rw	0x7
F8	UVHYS	Battery Voltage Monitor Under Voltage Hysterisis Select. Selects the hysterisis level for the Under Voltage monitor. 0x0: 0.475V 0x1: 0.835V 0x2: 1.225V 0x3: 1.635V	2	rw	0x1
F0	UVLEVEL	Battery Voltage Monitor Under Voltage Select. Selects the reference level for the Under Voltage monitor. If UVLEVEL[5:3]>0x04, the actual analog trim value is the same as UVLEVEL=0x0A. The UVLEVEL threshold is mononically increased with the setting. 0x0: Vf: 4.615V 0x1: Vf: 4.685V 0x7: Vf: 5.135V 0x8: Vf: 5.225V 0x9: Vf: 5.135V 0xa: Vf: 5.405V(default) 0xf: Vf: 5.895V 0x10: Vf: 6.015V 0x11: Vf: 6.125V 0x17: Vf: 6.925V 0x18: Vf: 7.075V 0x19: Vf: 7.235V 0x1f: Vf: 8.385V 0x20: Vf: 8.605V 0x21: Vf: 8.845V 0x27: Vf:10.610V	6	rw	0xA

7.2.6 VBATDBNC

0x50000054	VBATDBNC																													
VBAT Debounce Register.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F5	OVSTRB1SEL	Low frequency strobing select for debouncing. Enables strobing 1 with the Low frequency clock(16K) instead of just clocking with High frequency Clock(16M). Default is set to 0 for quick acknowledgement of OV event.	1	rw	0x0
F4	OVSTRB0SEL	Low frequency strobing select for debouncing. Enables strobing 0 with the Low frequency clock(16K) instead of just clocking with High frequency Clock(16M). Default is set to 1 for debouncing of OV.	1	rw	0x1

F3	UVSTRB1SEL	Low frequency strobing select for debouncing. Enables strobing 1 with the Low frequency clock(16K) instead of just clocking with High frequency Clock(16M). Default is set to 0 for quick acknowledgement of UV event.	1	rw	0x0
F2	UVSTRB0SEL	Low frequency strobing select for debouncing. Enables strobing 0 with the Low frequency clock(16K) instead of just clocking with High frequency Clock(16M). Default is set to 1 for debouncing of UV.	1	rw	0x1
F1	OV	over voltage signal debounce enable. if set to '1, debounces the over voltage signal before going to over voltage interrupt generation else the signal bypass the debouncer	1	rw	0x1
F0	UV	under voltage signal debounce enable. if set to '1, debounces the under voltage signal before going to under voltage interrupt generation else the signal bypass the debouncer	1	rw	0x1

7.2.7 VBATDBNCTHRES

0x50000058 **VBATDBNCTHRES**

VBAT Monitor Threshold Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F24								F16								F8								F0							

#	Field Name	Field Description	Width	Access	Reset
F24	OVTHRES0	Over Voltage debouncing threshold for 1to0 Transition. Sets the threshold for debouncing the over voltage event going from 1 to 0. It will require the ov event to stay high for the (OVTHRES0+1) number of LF/HF clocks to transit from a 1 to 0.	8	rw	0xFF
F16	UVTHRES0	Under Voltage debouncing threshold for 1to0 Transition. Sets the threshold for debouncing the under voltage event going from 1 to 0. It will require the uv event to stay high for the (UVTHRES0+1) number of LF/HF clocks to transit from a 1 to 0.	8	rw	0xFF
F8	OVTHRES1	Over Voltage debouncing threshold for 0to1 Transition. Sets the threshold for debouncing the over voltage event going from 0 to 1. It will require the ov event to stay high for the (OVTHRES1+1) number of LF/HF clocks to transit from a 0 to 1.	8	rw	0x1
F0	UVTHRES1	Under Voltage debouncing threshold for 0to1 Transition. Sets the threshold for debouncing the under voltage event going from 0 to 1. It will require the uv event to stay high for the (UVTHRES1+1) number of LF/HF clocks to transit from a 0 to 1.	8	rw	0x1

7.2.8 PMUIRQ

0x5000005C **PMUIRQ**

Voltage Monitor interrupts. Contains the the enable, clear, status and active flag for the Battery Voltage interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	F25	F24	-	-	-	-	-	-	F17	F16	-	-	-	-	-	-	F9	F8	-	-	-	-	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F25	OV	over voltage interrupt active.	1	ro	0x0
F24	UV	under voltage interrupt active.	1	ro	0x0
F17	OV	over voltage interrupt status.	1	ro	0x0
F16	UV	under voltage interrupt status.	1	ro	0x0
F9	OV	over voltage interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F8	UV	under voltage interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F1	OV	over voltage interrupt enable.	1	rw	0x0
F0	UV	under voltage interrupt enable.	1	rw	0x0

7.3 EVTHOLD

EVTHOLD		
Address	**Register**	**Description**
0x50000060	HOLD	Hold

7.3.1 HOLD

0x50000060																															
HOLD																															
Hold.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	HOLD	Hold. Set to prevent serialisation of new non-wakeup events in prepartion for hibernate mode. At the point of becoming set, a request to send the lullaby interrupt is automatically generated. The lullaby handler can then safely assert the PMUA->CTRL.HIBERNATE bit in order to put the device into hibernate mode.	1	wo	0x0

7.4 BTE

BTE		
Address	**Register**	**Description**
0x50000080	BTE_CTRL	BTE Control Register
0x50000084	BTE_SRAM_ADDR	BTE SRAM Address Register

7.4.1 BTE_CTRL

0x50000080																															
BTE_CTRL																															
BTE Control Register. This register can only be written if there is no ongoing transfer. If the BTE is transferring data, any writes to this register will be ignore																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	F27	F26	F25	F24	F16								F0															

#	Field Name	Field Description	Width	Access	Reset
F27	START	An operation is initiated when this bit is set. The bit auto-clears when the block is complete.	1	rw	0x0
F26	BLOCKING	If set then the block transfer has priority over the MCU. If the MCU tries to use the bus, it will stall until the block transfer is complete. If not set, then the MCU waits only until the remainder of the current word completes and then waits until the bus is idle again before continuing.	1	rw	0x0
F25	TX_DIR	Transfer direction. If set then SRAM->ASIC otherwise ASIC->SRAM	1	rw	0x0
F24	INC_ADDR	if set then ASIC die address increments at the end of each transfer. Set to zero if the peripheral is a FIFO.	1	rw	0x0
F16	BXNUM	Number of 32-bit words to transfer.	8	rw	0x0
F0	BXADD	Address of the ASIC die (LSB). This is the lower 16 bits of the ASIC die address. The MSBs are 0x5001.	16	rw	0x0

7.4.2 BTE_SRAM_ADDR

0x50000084																															
BTE_SRAM_ADDR																															
BTE SRAM Address Register.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	BXSRAMADDR	Address of the SRAM (LSB). This is the lower 16 bits of the SRAM address. The MSBs are 0x2000.	16	rw	0x0

7.5 WICA

WICA		
Address	**Register**	**Description**
0x50010100	CTRL	Wakeup Control Register
0x50010104	STATUS	Wakeup Status Register

7.5.1 CTRL

0x50010100	**CTRL**																													
Wakeup Control Register. This is the control register for wakeup via gpio or lin or wut																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F15	F14	-	F12	F11	F10	-	F8	F4				-	F2	-	-

#	Field Name	Field Description	Width	Access	Reset
F14	TIMERIRQCLR	clear the wutimer_irq. writting a '1 to this register will clear the wutimer_irq	1	wo	0x0
F12	LINSIRQCLR	clear the wulin_irq. writting a '1 to this register will clear the wulins_irq	1	wo	0x0
F10	TIMERIRQENA	Timer Wakeup Interrupt Enable. if set, wutimer_irq is asserted if wakeup timer matches the tapsel	1	rw	0x1
F8	LINSIRQENA	LIN Slave Wakeup Interrupt Enable. if set, wulin_irq is asserted if a wakeup signal is detected on the LIN_IN bus	1	rw	0x1
F4	TIMERTAPSEL	WakeUp Timer Tap Select. Wakeup Time = 2^(WUT_TAPSEL) x Tlfclk(62.5us)	4	rw	0x4
F2	TIMERENA	Wakeup Timer Enable. it enables the wakeup timer	1	rw	0x0

7.5.2 STATUS

0x50010104	**STATUS**																													
Wakeup Status Register. This is the status register for wakeup via gpio or lin or wut																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																-	-	-	-	-	-	-	-	-	-	-	-	F3	F2	-	F0

#	Field Name	Field Description	Width	Access	Reset
F16	TIMERCNT	Wakeup Timer Counter Value. Counter Value of the Wakeup Timer	16	ro	0x0
F2	TIMER	Wakeup Timer Status. This gets set if a wakeup timer is enabled and the count matches the tapsel setting during hibernate, CLRIRQ clears this Register	1	ro	0x0
F0	LINS	LIN Slave Wakeup Status. This gets set if a wakeup signal is detected on the LIN_IN bus when LINS SLEEP bit is set. CLRIRQ clears this Register	1	ro	0x0

7.6 WDTA

WDTA		
Address	**Register**	**Description**
0x50010200	CTRL	Control
0x50010204	STOP	Stop
0x50010208	CLEAR	Clear
0x5001020C	CNTVAL	Counter value
0x50010210	INT	WDTA Interrupts

7.6.1 CTRL

0x50010200	**CTRL**																													
Control.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F14	F12		F11	F8			-	-	-	-	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F31	STOP_LOCK	Set Only bit. Set this bit to lock STOP bits.	1	rw	0x0

F14	WDTA_WINOPEN_FLAG	Window open flag. A flag that indicates when the watchdog window is open. It only can be cleared by Reg CLEAR! 0x0: Window is Closed 0x1: Window is Open	1	ro	0x0
F12	WDTA_WINOPEN_SEL	Window Mode open select. Defines the watchdog window open time (the time between the watchdog start and the window open). 0x0: 1/2 * WDT timeout 0x1: 1/4 * WDT timeout 0x2: 1/8 * WDT timeout 0x3: 1/16* WDT timeout	2	rw	0x0
F11	WDTA_WINOPEN_ENA	Window Mode Enable. Enables Window Mode. 1'b1: Enable the Window mode of Watchdog, if the WDT is cleared before the time window opens, the WDT will issue a system reset. 1'b0: Disable the Window mode of Watchdog.	1	rw	0x0
F8	WDTA_TIMEOUT_SEL	Timeout select. Defines the watchdog timeout period (the time between a clear operation and the next timeout). 0x0: 2^11 * 62.5us ~= 128 ms 0x1: 2^12 * 62.5us ~= 256 ms 0x2: 2^13 * 62.5us ~= 512 ms 0x3: 2^14 * 62.5us ~= 1.024s 0x4: 2^15 * 62.5us ~= 2.048s 0x5: 2^16 * 62.5us ~= 4.096s 0x6: 2^17 * 62.5us ~= 8.192s 0x7: 2^18 * 62.5us ~= 16.384s	3	rw	0x7
F1	UPDATE	Window Mode Enable. Set to update Analog-Watchdog Configurations. NOTE: DO NOT change the CTRL register when it is high, which indicates there is an update in progress, It gets cleared by the core when the current update is done	1	dual	0x0
F0	WDTA_RUNNING	Analog-Watchdog Running status. A flag that indicates when the Analog-Watchdog timer is enabled. 0x0: Analog-Watchdog timer is stopped and cleared 0x1: Analog-Watchdog timer is running	1	ro	0x0

7.6.2 STOP

0x50010204	**STOP**				
Stop.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
F0					
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	STOP	Stop. Write the *stop* code (0x6da475c3) to this register to reset the timer and disable the watchdog (e.g. during debug). If any other value is written to this register the watchdog will be enabled.	32	rw	0x0

7.6.3 CLEAR

0x50010208	**CLEAR**				
Clear.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
F0					
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	CLEAR	Clear. Write the value 0x3c574ad6 (as a single word access) to reset the watchdog timer. Periodically performing this action is the expected method of preventing the watchdog from timing out (and resetting the MCU).	32	wo	0x0

7.6.4 CNTVAL

0x5001020C	**CNTVAL**				
Counter value.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
F0					
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	CNTVAL	Counter value. The instantaneous value of watchdog timeout counter	32	ro	0x0

7.6.5 INT

0x50010210																													
INT																													
WDTA Interrupts. Contains the ENABLE, CLEAR, STATUS and IRQ for the UART interrupt sources.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	F25	F24	-	-	-	-	-	-	F17	F16	-	-	-	-	-	-	F9	F8	-	-	-	-	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F25	WINOPEN	Window Open Interrupt. Set by WDTA timeout	1	ro	0x0
F24	WDTA	WDTA timeout Interrupt. Set by WDTA timeout	1	ro	0x0
F17	WINOPEN	Window Open Status. Set by WDTA timeout	1	ro	0x0
F16	WDTA	WDTA timeout Status. Set by WDTA timeout	1	ro	0x0
F9	WINOPEN	Window Open Interrupt Clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F8	WDTA	WDTA timeout Interrupt Clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F1	WINOPEN	Window Open Interrupt Enable.	1	rw	0x0
F0	WDTA	WDTA timeout Interrupt Enable.	1	rw	0x0

7.7 LINS

LINS		
Address	**Register**	**Description**
0x50010300	DATABYTE1	Data Byte 1
0x50010304	DATABYTE2	Data Byte 2
0x50010308	DATABYTE3	Data Byte 3
0x5001030C	DATABYTE4	Data Byte 4
0x50010310	DATABYTE5	Data Byte 5
0x50010314	DATABYTE6	Data Byte 6
0x50010318	DATABYTE7	Data Byte 7
0x5001031C	DATABYTE8	Data Byte 8
0x50010320	CTRL	Control Register
0x50010324	STATUS	Status
0x50010328	ERROR	Error Register
0x5001032C	DL	DATA Length Register
0x50010330	BTDIV07	Bit time Divider Register
0x50010334	BITTIME	Control Settings
0x50010338	ID	ID Register
0x5001033C	BUSTIME	Lin Bus Timing Register
0x50010340	STATUSEXT	Extended Status
0x50010348	CONF	Extended Configuration Register for compatibility issue
0x5001034C	BAUDCTRL	BaudRate Control

7.7.1 DATABYTE1

0x50010300																													
DATABYTE1																													
Data Byte 1. DATA_BUF1~4 could be read/written through one word access to this register.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F24								F16								F8								F0							

#	Field Name	Field Description	Width	Access	Reset
F24	DATABUF4SHADOW	Data Buffer 2 Shadow. Shadow register of 4th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	dual	0x0
F16	DATABUF3SHADOW	Data Buffer 2 Shadow. Shadow register of 3rd byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	dual	0x0

F8	DATABUF2SHADOW	Data Buffer 2 Shadow. Shadow register of 2nd byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	dual	0x0
F0	DATABUF1	Data Buffer 1. 1st byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

7.7.2 DATABYTE2

0x50010304	DATABYTE2				
Data Byte 2.					
31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0		
- - - - - - - -	- - - - - - - -	- - - - - - - -	F0		
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	DATABUF2	Data Buffer 2. 2nd byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

7.7.3 DATABYTE3

0x50010308	DATABYTE3				
Data Byte 3.					
31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0		
- - - - - - - -	- - - - - - - -	- - - - - - - -	F0		
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	DATABUF3	Data Buffer 3. 3rd byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

7.7.4 DATABYTE4

0x5001030C	DATABYTE4				
Data Byte 4.					
31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0		
- - - - - - - -	- - - - - - - -	- - - - - - - -	F0		
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	DATABUF4	Data Buffer 4. 4th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

7.7.5 DATABYTE5

0x50010310	DATABYTE5				
Data Byte 5.					
31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0		
F24	F16	F8	F0		
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F24	DATABUF8SHADOW	Data Buffer 8 Shadow. Shadow register of 8th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	dual	0x0
F16	DATABUF7SHADOW	Data Buffer 7 Shadow. Shadow register of 7th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	dual	0x0
F8	DATABUF6SHADOW	Data Buffer 6 Shadow. Shadow register of 6th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	dual	0x0
F0	DATABUF5	Data Buffer 5. 5th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

7.7.6 DATABYTE6

0x50010314	DATABYTE6				
Data Byte 6.					
31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0		
- - - - - - - -	- - - - - - - -	- - - - - - - -	F0		
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**

F0	DATABUF6	Data Buffer 6. 6th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

7.7.7 DATABYTE7

0x50010318	DATABYTE7				
Data Byte 7.					

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF7	Data Buffer 7. 7th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

7.7.8 DATABYTE8

0x5001031C	DATABYTE8				
Data Byte 8.					

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF8	Data Buffer 8. 8th byte of the 8-byte Data Buffer. Only writable when the transaction is idle.	8	rw	0x0

7.7.9 CTRL

0x50010320	CTRL				
Control Register.					

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F7	F6	F5	F4	F3	F2	F1	-

#	Field Name	Field Description	Width	Access	Reset
F7	STOP	Stop Register. The host controller of the LIN slave has set this register if it handles a data request interrupt and can not make use of the frame content with the received identifier(e.g. extended identifiers). For that case the LIN slave stops the processing of the LIN communication until the next SYNC BREAK is detected. A read access to this bit delivers always the value 0 Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F6	SLEEP	Sleep Request. The bit is used by the LIN core to determine whether the LIN bus is in Sleep Mode or not. The host controller has to set the bit after sending or receiving a Sleep Mode frame. If DIS_AUTOSLEEP = 0, the bit will be set automatically by the LIN core if a bus idle timeout is detected. The host controller has to clear the bit after a wakeup signal is detected.	1	rw	0x1
F5	TRANSMIT	Transmit Operation. The bit determines whether the current frame is a transmit frame or a receive frame for the LIN node. It has to be set by the host controller. 0x0: receive operation 0x1: transmit operation	1	rw	0x0
F4	DATAACK	Data Acknowledgement. The bit has to be set by the host controller of a LIN slave after handling a data request interrupt (compare STATUS.DATA_REQ register). The bit will be reset by the LIN core.	1	rw	0x0
F3	RSTINT	Reset interrupt. The host controller has to set this bit to reset the STATUS.INTR register and the interrupt request output of the LIN core. A read access to this bit delivers always the value 0.	1	wo	0x0
F2	RSTERR	Reset Error. The host controller has to set this bit to reset the error bits in status register and error register. A read access to this bit delivers always the value 0.	1	wo	0x0
F1	WAKEUPREQ	WakeUp Request. The bit has to be set by the host controller to terminate the Sleep Mode of the LIN bus by sending a Wakeup signal. The bit will be reset by the LIN core.	1	rw	0x0

7.7.10 STATUS

0x50010324	STATUS																													
Status.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F7	F6	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F7	ACTIVE	Lin Bus Active. The bit indicates whether the LIN bus is active or not. Note: For the LIN slave, this bit is set after the detection of a correct SYNC BREAK / SYNC FIELD sequence and it is reset at the end of the transmission or if the processing of the current frame is stopped by the host controller 0x0: no Lin bus activity 0x1: transmission on the LIN bus is active	1	ro	0x0
F6	BUSIDLETIMEOUT	BUS Idle Timeout. This bit is set by the LIN core if LIN is in hardware mode and no bus activity is detected for 4s~10s. In addition, an interrupt request to the host controller is generated in that case. After that, It is assumed that the LIN bus is in sleep mode and CTRL.SLEEP register will be set by the LIN core. The bit has to be reset by the host controller by setting the bit CTRL.RST_INT register.	1	ro	0x0
F5	ABORTED	Aborted. The bit is set if the processing of the current frame has been stopped by setting CTRL.STOP register. The bit is cleared by the LIN core after receiving a correct SYNC BREAK / SYNC FIELD sequence	1	ro	0x0
F4	DATAREQ	Data Request. The LIN core slave sets the bit after receiving the Identifier and requests an interrupt to the host controller. The host controller has to decode the Identifier to decide whether the current frame is a transmit or a receive operation. It has to adjust CTRL.TRANSMIT register and to load the data length. For transmit operations it has to load the data buffer too. After that the host controller has to set CTRL.DATA_ACK register	1	ro	0x0
F3	INTR	Interupt Request. The LIN core sets the bit when it requests an interrupt to the host controller. It has the same value as the interrupt output INTR. The bit has to be reset by the host controller by setting the bit CTRL.RST_INT register	1	ro	0x0
F2	ERROR	Lin Error. The LIN core sets the bit if an error has been detected (compare error register). The bit has to be reset by the host controller by setting the bit CTRL.RST_ERR register	1	ro	0x0
F1	WAKEUP	WakeUp. The bit is set when the LIN core is transmitting a Wakeup signal.	1	ro	0x0
F0	COMPLETE	Complete. The LIN core will set the bit after a transmission has been successfully finished and it will reset it at the start of a transmission	1	ro	0x0

7.7.11 ERROR

0x50010328	ERROR																													
Error Register.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F8	F7	F6	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F8	BITMONDATA	Bit Monitor Error occurred in Start or Data Bits. The Bit value monitored on the bus is different from the sent bit value and the error occurrs on the start or data bits.	1	ro	0x0
F7	BITMONSTOP	Bit Monitor Error occurred in Stop Bit. The Bit value monitored on the bus is different from the sent bit value and the error occurrs on the stop bit. In SAE2602, the error belongs to framing error.	1	ro	0x0
F6	FRAMEERR	Byte Field Framing Error. This bit is set by the LIN core slave if a transmission is aborted after the beginning of the data field due to a timeout or an incomplete frame	1	ro	0x0
F5	SBITERR	Start Bit Error in Byte field. Start Bit Error in Byte field, i.e., invalid start bit.	1	ro	0x0
F4	BITMON	Bit Monitor Error. The Bit value monitored on the bus is different from the sent bit value, bit monitor error will trigger an interrupt	1	ro	0x0
F3	PARITY	Parity Error. Identifier parity error	1	ro	0x0
F2	TIMEOUT	Timeout Error. There are several reason that can cause a timeout error: The master detects a timeout error if it is expecting data from the bus but no slave does respond. If the slave responds to late and the frame is not	1	ro	0x0

		finished within the maximum frame length TFRAME_MAX a timeout error will be detected too. The slave detects a timeout error if it is requesting a data acknowledge to the host controller (for selecting receive or transmit, data length and loading data), and the host controller does not set CTRL.DATA_ACK or CTRL.STOP register until the end of the reception of the first byte after the identifier. The slave detects a timeout error if it has transmitted a wakeup signal and it detects no sync field (from the master) within 150 ms. Note: The slave does not perform an exact check of the frame length TFRAME_MAX but a timeout is detected after 200 bit times, if the slave is in receive mode and there are missing data fields or a missing ID field from the master.			
F1	CHK	Checksum Error. Checksum Error	1	ro	0x0
F0	BITERR	Bit Error in Byte field. Bit Error in Byte field, i.e., invalid stop bit.	1	ro	0x0

7.7.12 DL

0x5001032C	DL

DATA Length Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F7	F6	F5	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F7	ENHCHK	Enhancement Check. The host controller has to set the checksum type used in the current frame by adjusting this register. 0x0: for classic checksum 0x1: for enhanced checksum	1	rw	0x0
F6	DISBITMON	Disable Bit Monitor. Set to disable the bit monitor during transmission. The bit must be set in case that RXD/TXD are separated.	1	rw	0x0
F5	DISAUTOSLEEP	Disable Auto Sleep. Set to Disable auto sleep.	1	rw	0x0
F0	LENGTH	Data Length. The host controller has to define the length of the data field of the current LIN frame by adjusting the data length register. If the data length is loaded with the value 1111b the length of the data field is decoded from Bit 5 and 4 of the identifier register id according to the Table below (e.g. compatibility to LIN specification 1.1). Otherwise the amount of data bytes can be written directly to the data length register (supported values are 0..8).	4	rw	0x0

ID (Bit 5)	ID (Bit 4)	Number of Bytes in the data field
0	0	2
0	1	2
1	0	4
1	1	8

7.7.13 BTDIV07

0x50010330	BTDIV07

Bit time Divider Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	BTDIV07	Bt Div LSBs. Bit time divider [7:0]	8	rw	0xFF

7.7.14 BITTIME

0x50010334	BITTIME

Control Settings.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F6		-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F6	PRESCL	Prescaler Register. Prescaler Setting	2	rw	0x3
F0	BTDIV8	Bt Div Most Significant bit. Bit time divider [8]	1	rw	0x1

7.7.15 ID

0x50010338	ID

ID Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0					

#	Field Name	Field Description	Width	Access	Reset
F0	ID	ID. ID register	6	rw	0x0

7.7.16 BUSTIME

0x5001033C	BUSTIME

Lin Bus Timing Register. Table 2-9 Control of time settings for wup_repeat_time and bus_inactivity_time

Bit 3	Bit 2	Bit 1	Bit 0	Time
0	0	0	0	Reset value
0	0			4 s (bus_inactivity_time)
0	1			6 s (bus_inactivity_time)
1	0			8 s (bus_inactivity_time)
1	1			10 s (bus_inactivity_time)
		0	0	180 ms (wup_repeat_time)
		0	1	200 ms (wup_repeat_time)
		1	0	220 ms (wup_repeat_time)
		1	1	240 ms (wup_repeat_time)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F2		F0	

#	Field Name	Field Description	Width	Access	Reset
F2	BUSINACTIVE	Bus Inactivity Time.	2	rw	0x0
F0	WUPREPEAT	wakeup repeat time.	2	rw	0x0

7.7.17 STATUSEXT

0x50010340	STATUSEXT

Extended Status.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F2		F1	F0

#	Field Name	Field Description	Width	Access	Reset
F2	BUSIDLEMONITOR	Bus Idle Monitor Status. If LIN is in hardware mode, BIT[0] is set by the lin core if the bus has no activity for 4s~10s and BIT[1] is set by the lin core if LIN is stuck at dominant inactivity state for 4s~10s. Any bus transition will clear these two bits. LIN Slave's pullup will be disabled.	2	ro	0x0
F1	BUSIDLETIMEOUTDOMINANT	Dominant Bus Idle Timeout. The bit is set by the lin core if LIN is in hardware mode & the bus is stuck at dominant inactivity state for 4s~10s. The bit has to be reset by the host controller by setting the bit CTRL.RST_INT register.	1	ro	0x0
F0	COMPLETETX	Complete TX. The LIN core will set the bit after a TX transmission has been successfully finished and it will reset it at the start of a transmission.	1	ro	0x0

7.7.18 CONF

0x50010348	CONF

Extended Configuration Register for compatibility issue.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	F18	F17	F16	-	-	-	-	-	-	-	F8	-	-	-	-	-	-	F0	

#	Field Name	Field Description	Width	Access	Reset
F18	DISBIT2CHECK	Disable Two Bits Width Check. Set to disable two bits width check for sync field.	1	rw	0x0

		0x0: Default.If the width mismatch is >25% between any two close bits and the 1st two bits, the byte will not be taken as a sync field. 0x1: Disabled. Recommended for the fast mode case that its baud rate is >=250KHz.			
F17	DUTYMAXSEL	Maximum Duty Select. Select the maximum duty constraint for sync field check. 0x0: Default. Check will fail if Duty > 68.75%. 0x1: Check will fail if Duty > 62.5%.	1	rw	0x0
F16	DUTYMINSEL	Minimum Duty Select. Select the minimum duty constraint for sync field check. 0x0: Default. Check will fail if Duty < 31.25%. 0x1: Check will fail if Duty < 37.5%.	1	rw	0x0
F8	BITMONMODE	BIT Monitor Mode. Control the exit timing when bit monitor error occured. Only writable when the transaction is idle. 0x0: Default. The transmission finished immediately if bit_mon is detected. 0x1: Even bit_mon is detected, the transmission will not be finished until the byte transfer is completed.	1	rw	0x0
F0	INTERBYTECNT	Inter-Byte Space Bit Count. Bit count of inter-byte space. >= 1bit inter-byte space is required by some legacy LIN devices. Only writable when the transaction is idle.	2	rw	0x1

7.7.19 BAUDCTRL

0x5001034C **BAUDCTRL**

BaudRate Control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0														

#	Field Name	Field Description	Width	Access	Reset
F0	BTDIVSYNC	Bit BaudRate Divider. Bit BaudRate = Fsys/(2**PRESCL)/BT_DIV_SYNC. The register is automatically updated once a legal sync field is received.	15	rw	0x7FFF

7.8 BUCK_INF

BUCK_INF

Address	Register	Description
0x50010508	BUCK_CFG0	BUCK configuration register0
0x5001050C	BUCK_CFG1	BUCK configuration register1
0x50010510	BUCK_CFG2	BUCK configuration register2
0x50010514	BUCK_CFG3	BUCK configuration register3
0x50010518	BUCK_CFG4	BUCK configuration register4
0x50010520	BUCK_CFG6	BUCK configuration register6
0x50010528	BUCK_STS0	BUCK status register0
0x5001052C	BUCK_STS1	BUCK status register1
0x50010530	BUCK_CTRL_INT	BUCK control & interrupt register

7.8.1 BUCK_CFG0

0x50010508 **BUCK_CFG0**

BUCK configuration register0.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	F28	-	-	F25	F24	F20				F19	F18	F16		-	-	F8						-	-	F0					

#	Field Name	Field Description	Width	Access	Reset
F24	RAMP_UPDATE	Update VDAC ramp parameters. Set high then set low to launch a ramp update.	1	rw	0x0
F19	BUCKDIS_RAMPDOWN_ENA	Enable of Ramp down after Core Buck disable. set 1'b1 to enable	1	rw	0x0
F18	RAMP_ENA	Enable the Ramp feature for VDAC. If set enables the core to ramp the VDAC at a rate set by RAMP_RATE, till the VDAC reach the set code in VDAC_TRIM. if set to '1 the ramped value will be available on VDAC bus, if set to '0 the vdac_trim will be available on VDAC bus	1	rw	0x1

F16	RAMP_RATE	VDAC ramp rate to reach to VDAC_TRIM. When RAMP_ENA is set, the register decides the rate at which the VDAC ramp up/down to reach the set VDAC_TRIM 0x0: 7.8us per step 0x1: 15.6us per step 0x2: 31.2us per step 0x3: 62.4us per step	2	rw	0x1
F0	VDAC_TRIM	TRIM code for VDAC. Set the VDAC trim code, which decides BUCK output voltage. VBUCK_OUT = (0.15625*VDAC_TRIM) V. The trim code is range from 0 to VBUCK_DAC_MAX. If the trim code is bigger than VBUCK_DAC_MAX, the trim code would be forced to VBUCK_DAC_MAX.	6	rw	0x20

7.8.2 BUCK_CFG1

0x5001050C **BUCK_CFG1**

BUCK configuration register1.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F28				F24				F20				F16				F12				F8				F4				F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F28	HICCUP_DWELL	HICCUP Timeout Setting. Timeout wait time = (HICCUP_DWELL + 1)*1ms.	4	rw	0x3
F24	START_OK_PRE_DWELL	START_OK_PRE Timeout Setting. Timeout wait time = (START_OK_PRE_DWELL + 1)*(2^RAMP_RATE)*31.2us.	4	rw	0x8
F20	START_DRV_DWELL	START_DRV Timeout Setting. Timeout wait time = (START_DRV_DWELL + 1)*(2^RAMP_RATE)*7.8us.	4	rw	0x9
F16	START_PWM_DWELL	START_PWM Timeout Setting. Timeout wait time = (START_PWM_DWELL + 1)*7.8us.	4	rw	0x8
F12	START_ENA_DWELL	START_ENA Timeout Setting. Timeout wait time = (START_ENA_DWELL + 1)*7.8us.	4	rw	0x8
F8	DET_LOW_DWELL	DET_LOW Timeout Setting. Timeout wait time = (DET_LOW_DWELL + 1)*1ms.	4	rw	0x3
F4	PRE_ENA_DWELL	PRE_ENA Timeout Setting. Timeout wait time = (PRE_ENA_DWELL + 1)*3.9us.	4	rw	0x1

7.8.3 BUCK_CFG2

0x50010510 **BUCK_CFG2**

BUCK configuration register2.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	F28			-	-	F25	F24	F16								F15	F14	F13	F12	F11	F8			-	-	-	F4	F0			

#	Field Name	Field Description	Width	Access	Reset
F28	BUCK_ERROR_CLR	BUCK error flag clear. Set high then set low to launch a clear operation. BIT[0] : clear error flag: VOUT OVP can't release before BUCK startup BIT[1] : clear error flag: VOUT SHORT can't release after BUCK startup for a while BIT[2] : clear error flag: Vout OK detect fail	3	rw	0x0
F25	SET_VOUT_PD	SET_VOUT_PD. Set 1 to pull down BUCK output.	1	rw	0x0
F24	BUCK_ENA	BUCK enable request. Setting this bit to '1 will kickstart the statup sequence for the buck regulator. Setting this bit to '0 will start the off sequence for the buck regulator. Auto clearred if hiccup is disabled & error conditions are encountered.	1	rw	0x0
F13	DIS_VOUT_OV	Set VOUT OV option. 1'b0: enable VOUT OV detection.1'b1: disable VOUT OV detection	1	rw	0x0
F12	CFG_UVLO	Set UVLO threshold. 1'b0: VIN UVLO=4V.1'b1: VIN UVLO=6V	1	rw	0x0
F11	SR_CTRL	Set slew rate.	1	rw	0x0
F8	CFG_CLPUP	Set clamp up configuration.	3	rw	0x4
F4	HICCUP_ENA	BUCK HICCUP Enable. Set this bit to high will enable the hiccup control of BUCK FSM.	1	rw	0x1
F0	BUCK_IGNORE	BUCK Status ignore. BIT[0] : ignore vin uvlo detection BIT[1] : ignore vout low detection	4	rw	0x0

		BIT[2] : ignore vout short detection BIT[3] : ignore vout ok detection			

7.8.4 BUCK_CFG3

0x50010514		BUCK_CFG3			
BUCK configuration register3.					
31 30 29 28 27 26 25 24		23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
F28 F24		F20 F16	- - F13 F12 F11 F10 F9 F8	- - F5 F4 F3 F2 F1 F0	
#	Field Name	Field Description	Width	Access	Reset
F28	VOUT_LOW_DBNC_THRES0	VOUT_LOW debounce threshold from 1 to 0. The deglitch width to detect 0 is from 62.4us to 998.4us.	4	rw	0x3
F24	VOUT_LOW_DBNC_THRES1	VOUT_LOW debounce threshold from 0 to 1. The deglitch width to detect 1 is from 62.4us to 998.4us.	4	rw	0x3
F20	IDLE_HOLD_DBNC_THRES0	IDLE_HOLD debounce threshold from 1 to 0. The deglitch width to detect 0 is from 3.9us to 62.4us.	4	rw	0x0
F16	IDLE_HOLD_DBNC_THRES1	IDLE_HOLD debounce threshold from 0 to 1. The deglitch width to detect 1 is from 3.9us to 62.4us.	4	rw	0x5
F13	VOUT_OV_POL	The valid level polarity for BUCK VOUT OV signal. 1'b0: the valid level polarity is high. 1'b1: the valid level polarity is low.	1	rw	0x0
F12	VOUT_OK_POL	The valid level polarity for BUCK VOUT OK signal. 1'b0: the valid level polarity is high. 1'b1: the valid level polarity is low.	1	rw	0x0
F11	VOUT_SHORT_POL	The valid level polarity for BUCK VOUT SHORT signal. 1'b0: the valid level polarity is high. 1'b1: the valid level polarity is low.	1	rw	0x0
F10	VIN_UV_POL	The valid level polarity for BUCK VIN UVLO signal. 1'b0: the valid level polarity is high. 1'b1: the valid level polarity is low.	1	rw	0x0
F9	VOUT_LOW_POL	The valid level polarity for BUCK VOUT LOW signal. 1'b0: the valid level polarity is high. 1'b1: the valid level polarity is low.	1	rw	0x1
F8	IDLE_HOLD_POL	The valid level polarity for IDLE_HOLD signal. 1'b0: the valid level polarity is high. 1'b1: the valid level polarity is low.	1	rw	0x0
F5	VOUT_OV_DBNC_ENA	VOUT_OV debounce enable. 1'b0: disable VOUT_OV debounce function. 1'b1: enable VOUT_OV debounce function.	1	rw	0x1
F4	VOUT_OK_DBNC_ENA	VOUT_OK debounce enable. 1'b0: disable VOUT_OK debounce function. 1'b1: enable VOUT_OK debounce function.	1	rw	0x1
F3	VOUT_SHORT_DBNC_ENA	VOUT_SHORT debounce enable. 1'b0: disable VOUT_SHORT debounce function. 1'b1: enable VOUT_SHORT debounce function.	1	rw	0x1
F2	VIN_UV_DBNC_ENA	VIN_UV debounce enable. 1'b0: disable VIN UVLO debounce function. 1'b1: enable VIN UVLO debounce function.	1	rw	0x1
F1	VOUT_LOW_DBNC_ENA	VOUT_LOW debounce enable. 1'b0: disable VOUT_LOW debounce function. 1'b1: enable VOUT_LOW debounce function.	1	rw	0x1
F0	IDLE_HOLD_DBNC_ENA	IDLE_HOLD debounce enable. 1'b0: disable IDLE_HOLD debounce function. 1'b1: enable IDLE_HOLD debounce function.	1	rw	0x1

7.8.5 BUCK_CFG4

0x50010518	BUCK_CFG4
BUCK configuration register4.	
31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
F28 F24	F20 F16 F12 F8 F4 F0

#	Field Name	Field Description	Width	Access	Reset
F28	VOUT_OV_DBNC_THRES0	VOUT_OV debounce threshold from 1 to 0. The deglitch width to detect 0 is from 7.8us to 124.8us.	4	rw	0x1
F24	VOUT_OV_DBNC_THRES1	VOUT_OV debounce threshold from 0 to 1. The deglitch width to detect 1 is from 31.2us to 499.2us.	4	rw	0x3
F20	VOUT_OK_DBNC_THRES0	VOUT_OK debounce threshold from 1 to 0. The deglitch width to detect 0 is from 7.8us to 124.8us.	4	rw	0x7
F16	VOUT_OK_DBNC_THRES1	VOUT_OK debounce threshold from 0 to 1. The deglitch width to detect 1 is from 7.8us to 124.8us.	4	rw	0x7
F12	VOUT_SHORT_DBNC_THRES0	VOUT_SHORT debounce threshold from 1 to 0. The deglitch width to detect 0 is from 3.9us to 62.4us.	4	rw	0x3
F8	VOUT_SHORT_DBNC_THRES1	VOUT_SHORT debounce threshold from 0 to 1. The deglitch width to detect 1 is from 31.2us to 499.2us.	4	rw	0x3
F4	VIN_UV_DBNC_THRES0	VIN_UV debounce threshold from 1 to 0. The deglitch width to detect 0 is from 249.6us to 3993.6us.	4	rw	0x3
F0	VIN_UV_DBNC_THRES1	VIN_UV debounce threshold from 0 to 1. The deglitch width to detect 1 is from 3.9us to 62.4us.	4	rw	0x1

7.8.6 BUCK_CFG6

0x50010520	BUCK_CFG6

BUCK configuration register6.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	F24				F20				F16				-	-	-	F8					-	-	-	F4	F3	F0		

#	Field Name	Field Description	Width	Access	Reset
F24	TRIM_IS_LSTRIG_PBIAS2	Trim the upper limit of the curve of LS current limit vs VEA-VCP_L.	4	rw	0x0
F20	TRIM_IS_LSTRIG_PBIAS1	Trim the upper limit of the curve of LS current limit vs VEA-VCP_L.	4	rw	0x0
F16	TRIM_IS_LSTRIG	Trim the derivative of the curve of LS current limit vs VEA-VCP_L.	4	rw	0x0
F4	SOFT_RSTN_REQ	Generate a pulse used to reset BUCK 5V logic. Pull up and then pull down to generate a pulse.	1	rw	0x0
F3	SSC_ENA	SSC enable.	1	rw	0x1
F0	SEL_SSC_STEP	Set step period used in SSC. 3'b000: 8 steps per period . 3'b001: 4 steps per period . 3'b010: 2 steps per period . 3'b011: 1 steps per period . 3'b100: 1 step per 2 periods . 3'b101: 1 step per 3 periods . 3'b110: 1 step per 4 periods . 3'b111: 1 step per 5 periods .	3	rw	0x5

7.8.7 BUCK_STS0

0x50010528	BUCK_STS0

BUCK status register0.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	F26	F25	F24	-	-	-	-	-	F18	F17	F16	-	F14	F13	F12	F11	F10	F9	F8	-	F6	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F18	BUCK_IDLE	Status of Buck idle. When BUCK_IDLE becomes 1, The FSM of BUCK is located in IDLE state.	1	ro	N/A
F17	BUCK_READY	Status of Buck ready. When BUCK_READY becomes 1, The FSM of BUCK is located in START_OK/ENA_L state.	1	ro	N/A
F16	BUCK_OFF	Status of Buck off. When BUCK_OFF becomes 1, The FSM of BUCK is located in IDLE/HICCUP/PRE_ENA/DET_VIN/DET_LOW/ENA_L_ERR state.	1	ro	N/A
F14	PWM_COMP_OUT_RAW	Raw status of Buck PWM Comparator output.	1	ro	N/A
F13	VBTPORN_RAW	Raw status of voltage for VBT.	1	ro	N/A
F12	CLP_L_RAW	Raw status of clamp low for EA.	1	ro	N/A
F11	ZCD_COMP_OUT_RAW	Raw status of ZCD comparator output.	1	ro	N/A

F10	ZCD_RAW	Raw status of Buck Low Side NMOS is reach to zero current.	1	ro	N/A
F9	LS_ILMT_RAW	Raw status of Buck Low Side NMOS Over Current.	1	ro	N/A
F8	HS_ILMT_RAW	Raw status of Buck High Side NMOS Over Current.	1	ro	N/A
F6	LS_ON_RAW	Raw status of Buck Low Side NMOS ON.	1	ro	N/A
F5	HS_ON_RAW	Raw status of Buck High Side NMOS ON.	1	ro	N/A
F4	VOUT_OV_RAW	Raw status of Buck Output over-voltage.	1	ro	N/A
F3	VOUT_OK_RAW	Raw status of Buck Output voltage OK.	1	ro	N/A
F2	VOUT_SHORT_RAW	Raw status of Buck Output short.	1	ro	N/A
F1	VIN_UV_RAW	Raw status of Buck Input UVLO.	1	ro	N/A
F0	VOUT_LOW_RAW	Raw status of Buck output low.	1	ro	N/A

7.8.8 BUCK_STS1

0x5001052C **BUCK_STS1**

BUCK status register1.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F8			F4				F0			

#	Field Name	Field Description	Width	Access	Reset
F8	BUCK_ERROR	BUCK error flag. bit[0] : VOUT OVP can't release before BUCK startup. bit[1] : VOUT SHORT can't release after BUCK startup for a while. bit[2] : VOUT OK detect fail.	3	ro	N/A
F4	BUCK_STATE	BUCK FSM state. BUCK FSM state, which can be used for debug. 0x0: IDLE 0x1: HICCUP 0x2: PRE_ENA 0x3: DET_VIN 0x4: DET_LOW 0x5: START_ENA 0x6: START_PWM 0x7: START_DRV 0x8: START_OK_PRE 0x9: START_OK 0xa: ENA_L 0xb: ENA_L_ERR	4	ro	N/A

7.8.9 BUCK_CTRL_INT

0x50010530 **BUCK_CTRL_INT**

BUCK control & interrupt register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	F30	F29	F28	F27	F26	F25	F24	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F29	INT_VOUT_OC_IRQ	Vout over-current interrupt activity.	1	ro	0x0
F28	INT_VOUT_OV_IRQ	Vout over-voltage interrupt activity.	1	ro	0x0
F27	INT_VOUT_OK_IRQ	Vout soft start OK interrupt activity.	1	ro	0x0
F26	INT_VOUT_SHORT_IRQ	Vout short interrupt activity.	1	ro	0x0
F25	INT_VIN_UV_IRQ	Vin under-voltage interrupt activity.	1	ro	0x0
F24	INT_START_ERROR_IRQ	BUCK start error interrupt activity.	1	ro	0x0
F21	INT_VOUT_OC_STS	Vout over-current interrupt status.	1	ro	0x0
F20	INT_VOUT_OV_STS	Vout over-voltage interrupt status.	1	ro	0x0
F19	INT_VOUT_OK_STS	Vout soft start OK interrupt status.	1	ro	0x0
F18	INT_VOUT_SHORT_STS	Vout short interrupt status.	1	ro	0x0
F17	INT_VIN_UV_STS	Vin under-voltage interrupt status.	1	ro	0x0
F16	INT_START_ERROR_STS	BUCK start error interrupt status.	1	ro	0x0
F13	INT_VOUT_OC_CLR	Vout over-current interrupt clear.	1	wo	N/A
F12	INT_VOUT_OV_CLR	Vout over-voltage interrupt clear.	1	wo	N/A

F11	INT_VOUT_OK_CLR	Vout soft start OK interrupt clear.	1	wo	N/A
F10	INT_VOUT_SHORT_CLR	Vout short interrupt clear.	1	wo	N/A
F9	INT_VIN_UV_CLR	Vin under-voltage interrupt clear.	1	wo	N/A
F8	INT_START_ERROR_CLR	BUCK start error interrupt clear.	1	wo	N/A
F5	INT_VOUT_OC_ENA	Vout over-current interrupt enable.	1	rw	0x0
F4	INT_VOUT_OV_ENA	Vout over-voltage interrupt enable.	1	rw	0x0
F3	INT_VOUT_OK_ENA	Vout soft start OK interrupt enable.	1	rw	0x0
F2	INT_VOUT_SHORT_ENA	Vout short interrupt enable.	1	rw	0x0
F1	INT_VIN_UV_ENA	Vin under-voltage interrupt enable.	1	rw	0x0
F0	INT_START_ERROR_ENA	BUCK start error interrupt enable.	1	rw	0x0

7.9 SAR_CTRL

SAR_CTRL		
Address	**Register**	**Description**
0x50010600	SAR_CTRL	SAR ADC Control
0x50010604	SAR_CFG0	SAR Configuration Register0
0x50010608	SAR_CFG1	SAR Configuration Register1
0x5001060C	SAR_CFG2	SAR Configuration Register2
0x50010610	OT_CTRL_CFG	Over-temperature detection control & Configuration
0x50010614	SAR_CHAN_CFG	SAR Channel Configuration
0x50010618	ADC_DATA0	ADC_DATA0,
0x5001061C	ADC_DATA1	ADC_DATA1,
0x50010620	ADC_OT_DATA	ADC_OT_DATA,
0x50010624	SAR_INT	SAR Interrupts

7.9.1 SAR_CTRL

0x50010600 **SAR_CTRL**

SAR ADC Control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	F28	F24				-	-	-	F16					-	F14	F12		-	-	-	F8	-	-	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F28	ADC_SEL_VIN_VCM_EXT	Select External Inputs to ADC. choose ADC input common voltage. 0: choose internal vin_vcm, equals to (vinp+vinn)/2; 1: choose external vin_vcm, for PN detect.	1	rw	0x0
F24	TRIGSEL	SAR Converion Trigger Selects. Selects the trigger condition of SAR ADC. Don't change the bits during an ADC conversion sequence is ongoing. 0x1: Triggered through writing 1 to conversion bit. 0x2: Triggered by the PWM posedge. 0x4: Triggered by the PWM negedge. 0x8: Triggered by PWM period.	4	rw	0x0
F16	PWMSEL	PWM Trigger Signal Selects. Selects the source PWM channel.	5	rw	0x0
F14	EN_AVER	Enable sample data average.	1	rw	0x0
F12	AVER_SEL	Select average numbers of adc sample data. 0x0: Average numbers of adc sample data: 4 0x1: Average numbers of adc sample data: 8 0x2: Average numbers of adc sample data: 16 0x3: Average numbers of adc sample data: 32	2	rw	0x0
F8	CONT	Continuous Conversion Enable. If this bit has been set before an ADC conversion sequence trigged by CONVERT bit, the sequence will be treated as a sequential conversion, rather than a single conversion, only value when auto_trg_en is disable.	1	rw	0x0
F5	SAR_BUSY	SAR ADC busy. When SAR ADC is running, the flag is set	1	ro	0x0
F4	DIG_RESET	SAR Digital Part Reset. Resets SAR digital parts. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0

F3	CONVERT	ADC START Register. Set 1 to start a new adc conversion. NOTE: THAT BIT SHOULD NOT BE SET UNTIL ALL OTHER CONFIG BITS BE SETTED Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F2	SAR_AFE_EN	ADC AFE Enable. adc afe enable. If vinp, vinn and vin vcm all choose external, adc afe should be disabled: adc_adc_en=0, otherwise, adc afe must be enabled: adc_afe_en=1.	1	rw	0x0
F1	SAR_PREAMP_EN	adc pre-amp enable. 0:disable, 1:enable	1	rw	0x0
F0	SAR_ENA_REQ	SAR ADC Enable. Set to enable the SAR analog & digital part	1	rw	0x0

7.9.2 SAR_CFG0

0x50010604 **SAR_CFG0**

SAR Configuration Register0.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	F22		F20		F18		F16		F14		F12		F10		F8		F6		F4		F2		F0	

#	Field Name	Field Description	Width	Access	Reset
F22	SAR_INPUT_MODE_CH4	ADC AFE Input Modes for channel 4. Select ADC AFE Input Modes. 0x0: All external. 0x1: VINP buffered, VINN external. 0x2: VINN buffered, VINP external. 0x3: Both VINP & VINN buffered.	2	rw	0x1
F20	SAR_INPUT_MODE_CH3	ADC AFE Input Modes for channel 3. Select ADC AFE Input Modes. 0x0: All external. 0x1: VINP buffered, VINN external. 0x2: VINN buffered, VINP external. 0x3: Both VINP & VINN buffered.	2	rw	0x1
F18	SAR_INPUT_MODE_CH2	ADC AFE Input Modes for channel 2. Select ADC AFE Input Modes. 0x0: All external. 0x1: VINP buffered, VINN external. 0x2: VINN buffered, VINP external. 0x3: Both VINP & VINN buffered.	2	rw	0x1
F16	SAR_INPUT_MODE_CH1	ADC AFE Input Modes for channel 1. Select ADC AFE Input Modes. 0x0: All external. 0x1: VINP buffered, VINN external. 0x2: VINN buffered, VINP external. 0x3: Both VINP & VINN buffered.	2	rw	0x1
F14	SAR_INPUT_GAIN_CH4	choose ADC input gain for channel 4. 0x0: 14/32 0x1: 22/32 0x2: 31/32 0x3: 31/32	2	rw	0x3
F12	SAR_INPUT_GAIN_CH3	choose ADC input gain for channel 3. 0x0: 14/32 0x1: 22/32 0x2: 31/32 0x3: 31/32	2	rw	0x3
F10	SAR_INPUT_GAIN_CH2	choose ADC input gain for channel 2. 0x0: 14/32 0x1: 22/32 0x2: 31/32 0x3: 31/32	2	rw	0x1
F8	SAR_INPUT_GAIN_CH1	choose ADC input gain for channel 1. 0x0: 14/32 0x1: 22/32 0x2: 31/32 0x3: 31/32	2	rw	0x3
F6	ADC_VREF_SEL_CH4	adc vref select for channel 4. 0x0: adc_vref = vbg when sar_ena_req=1 0x1: adc_vref = 2*vbg when sar_ena_req=1 0x2: adc_vref = VDD_3V3 when sar_ena_req=1 0x3: adc_vref = VDD_3V3 when sar_ena_req=1	2	rw	0x1

F4	ADC_VREF_SEL_CH3	adc vref select for channel 3. 0x0: adc_vref = vbg when sar_ena_req=1 0x1: adc_vref = 2*vbg when sar_ena_req=1 0x2: adc_vref = VDD_3V3 when sar_ena_req=1 0x3: adc_vref = VDD_3V3 when sar_ena_req=1	2	rw	0x1
F2	ADC_VREF_SEL_CH2	adc vref select for channel 2. 0x0: adc_vref = vbg when sar_ena_req=1 0x1: adc_vref = 2*vbg when sar_ena_req=1 0x2: adc_vref = VDD_3V3 when sar_ena_req=1 0x3: adc_vref = VDD_3V3 when sar_ena_req=1	2	rw	0x1
F0	ADC_VREF_SEL_CH1	adc vref select for channel 1. 0x0: adc_vref = vbg when sar_ena_req=1 0x1: adc_vref = 2*vbg when sar_ena_req=1 0x2: adc_vref = VDD_3V3 when sar_ena_req=1 0x3: adc_vref = VDD_3V3 when sar_ena_req=1	2	rw	0x1

7.9.3 SAR_CFG1

0x50010608 **SAR_CFG1**

SAR Configuration Register1.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	F20				F16				F12				F8				-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F20	SAMPCYC_CH4	Sample cycle for channel 4. Set sampling time from 1 to 16 sar clock cycles. 0x0: 1 Cycle 0x1: 2 Cycle 0x2: 3 Cycle 0xf: 16 Cycle	4	rw	0x8
F16	SAMPCYC_CH3	Sample cycle for channel 3. Set sampling time from 1 to 16 sar clock cycles. 0x0: 1 Cycle 0x1: 2 Cycle 0x2: 3 Cycle 0xf: 16 Cycle	4	rw	0x8
F12	SAMPCYC_CH2	Sample cycle for channel 2. Set sampling time from 1 to 16 sar clock cycles. 0x0: 1 Cycle 0x1: 2 Cycle 0x2: 3 Cycle 0xf: 16 Cycle	4	rw	0x8
F8	SAMPCYC_CH1	Sample cycle for channel 1. Set sampling time from 1 to 16 sar clock cycles. 0x0: 1 Cycle 0x1: 2 Cycle 0x2: 3 Cycle 0xf: 16 Cycle	4	rw	0x8
F0	ROUND	ADC round enable. Enable ADC round. 0x0: No round. 0x1: Negative code+1	1	rw	0x1

7.9.4 SAR_CFG2

0x5001060C **SAR_CFG2**

SAR Configuration Register2.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F24								F16								-	-	-	-	F11	F10	F9	F8	-	-	-	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F24	TRIG_DLY_TS	Trigger delay used for temp sensor sampling channel. Set trigger delay time from 1 to 256 sar clock cycles.	8	rw	0x20
F16	TRIG_DLY	Trigger delay used for non temp sensor sampling channel. Set trigger delay time from 1 to 256 sar clock cycles.	8	rw	0x14
F11	TS_SEL_CH4	Temp sensor select for channel 4. 1'b0: Temp sensor located in BUCK; 1'b1: Temp sensor located in LED.	1	rw	0x0

		The value is only valid when Temp Sensor differential channel of CH4 is selected.			
F10	TS_SEL_CH3	Temp sensor select for channel 3. 1'b0: Temp sensor located in BUCK; 1'b1: Temp sensor located in LED. The value is only valid when Temp Sensor differential channel of CH3 is selected.	1	rw	0x0
F9	TS_SEL_CH2	Temp sensor select for channel 2. 1'b0: Temp sensor located in BUCK; 1'b1: Temp sensor located in LED. The value is only valid when Temp Sensor differential channel of CH2 is selected.	1	rw	0x0
F8	TS_SEL_CH1	Temp sensor select for channel 1. 1'b0: Temp sensor located in BUCK; 1'b1: Temp sensor located in LED. The value is only valid when Temp Sensor differential channel of CH1 is selected.	1	rw	0x0
F0	SAR_CLK_DIV	SAR ADC reference clock div select. Select the divisor on the system clock after perscale. The sar adc clock = sysclk(16Mhz)/((CRGA.DIVSYSCLK+1)*(SAR_CLK_DIV+1)). The sar adc clock frequence must be no more than 4Mhz. The default sar adc clock: 1Mhz.	4	rw	0xF

7.9.5 OT_CTRL_CFG

0x50010610 **OT_CTRL_CFG**

Over-temperature detection control & Configuration.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	F27	F26	F25	F24	-	-	-	-	-	-	F17	F16	-	-	-	-	-	-	F9	F8	F6		F4		-	F0		

#	Field Name	Field Description	Width	Access	Reset
F27	OT_BUSY	OT_BUSY. When over-temperature sensor is working, the bit is set to high.	1	ro	N/A
F26	ADC_SAMP_OT_ENA	ADC sampling temperature sensor enable.	1	rw	0x0
F25	AUTO_OT_DET_ENA	Auto OT detection enable.	1	rw	0x0
F24	START_OT_DET	Set 1 to launch a OT detect operation. It's a pulse signal and no need to clear it.	1	wo	N/A
F17	DBG_TS_CH	Select temperature sensor channel. Only used to test OT in debug mode.	1	rw	0x0
F16	DBG_OT	OT debug enable signal. Only used to test OT in debug mode.	1	rw	0x0
F9	EN_OVERTEMP	Enable over temperature sensor.	1	rw	0x0
F8	EN_COMPOT	Enable the comparator of over temperature function.	1	rw	0x0
F6	SEL_OT_DBNC_THRES0	Select OT flag debounce threshold when a 1 turns into a 0. 0x0: 32us 0x1: 64us 0x2: 96us 0x3: 128us	2	rw	0x3
F4	SEL_OT_DBNC_THRES1	Select OT flag debounce threshold when a 0 turns into a 1. 0x0: 32us 0x1: 64us 0x2: 96us 0x3: 128us	2	rw	0x3
F0	TS_CFG	Choose the OT level from 90~160 degree. 0x0: 160 degree 0x1: 150 degree 0x2: 140 degree 0x3: 130 degree 0x4: 120 degree 0x5: 110 degree 0x6: 100 degree 0x7: 90 degree	3	rw	0x0

7.9.6 SAR_CHAN_CFG

0x50010614 **SAR_CHAN_CFG**

SAR Channel Configuration.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

F31	-	F24	-	-	F16	-	-	F8	F2	F0

#	Field Name	Field Description	Width	Access	Reset
F31	TEST_BATTERY_GAIN_CHOOSE	VBAT Gain Select. 0: gain=1/14, vbat max 30V/14=2.14v, under ADC vref=2.4v 1: gain=1/28, vbat max 30V/28=1.07v, under ADC vref=1.2v	1	rw	0x0
F24	CH4_SEL	Channel4 Selection. Refer to Channel1 Selects.	6	rw	0x8
F16	CH3_SEL	Channel3 Selection. Refer to Channel1 Selects.	6	rw	0x7
F8	CH2_SEL	Channel2 Selection. Refer to Channel1 Selects.	6	rw	0x6
F2	CH1_SEL	Channel1 Selection. Channel1 Selects. 0x0: adc_vinp=adc_refp, adc_vinn=adc_refp (all shot to adc_ref(2.4V) for adc channel offset K) 0x1: adc_vinp=adc_refp, adc_vinn=vref_gnd (for adc channel +gain error K) 0x2: adc_vinp=vref_gnd, adc_vinn=adc_refp (for adc channel -gain error K) 0x3: adc_vinp=GPIO6, adc_vinn=GPIO7,differential channel 0x4: Temp Sensor differential channel 0x5: adc_vinp=VDD_1V5, adc_vinn=vref_gnd 0x6: adc_vinp=VDD_3V3, adc_vinn=vref_gnd 0x7: adc_vinp=VDD_PRE5V(1/4), adc_vinn=vref_gnd 0x8: adc_vinp=VBAT ACCURATE (gain selected by TEST_BATTERY_GAIN_CHOOSE), adc_vinn=vref_gnd 0x9: adc_vinp=GPIO6, adc_vinn=vref_gnd. 0xa: adc_vinp=GPIO7, adc_vinn=vref_gnd. 0xb: adc_vinp=GPIO8, adc_vinn=vref_gnd. 0xc: adc_vinp=GPIO1, adc_vinn=vref_gnd. 0xd: adc_vinp=GPIO2, adc_vinn=vref_gnd. 0xe: adc_vinp=GPIO3, adc_vinn=vref_gnd. 0xf: adc_vinp=GPIO4, adc_vinn=vref_gnd. 0x10: adc_vinp=GPIO5, adc_vinn=vref_gnd. 0x12: adc_vinp=VBUCK 5V(1/4), adc_vinn=vref_gnd. 0x13: adc_vinp=VBUCK, adc_vinn=LED PN channel 0 . 0x14: adc_vinp=VBUCK, adc_vinn=LED PN channel 1 . 0x2a: adc_vinp=VBUCK, adc_vinn=LED PN channel 23.	6	rw	0x5
F0	CHAN_SEQ_NUM	Channel Sequence number. Select the sequence number of channels to be converted. 0x0: CH1 only 0x1: CH1->CH2 0x2: CH1->CH2->CH3 0x3: CH1->CH2->CH3->CH4	2	rw	0x3

7.9.7 ADC_DATA0

0x50010618	ADC_DATA0

ADC_DATA0,.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	DATA1	Data1 of ADC conversion	16	ro	0x0
F0	DATA0	Data0 of ADC conversion	16	ro	0x0

7.9.8 ADC_DATA1

0x5001061C	ADC_DATA1

ADC_DATA1,.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	DATA3	Data3 of ADC conversion	16	ro	0x0
F0	DATA2	Data2 of ADC conversion	16	ro	0x0

7.9.9 ADC_OT_DATA

0x50010620	ADC_OT_DATA																													
ADC_OT_DATA,.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0														

#	Field Name	Field Description	Width	Access	Reset
F16	DATA_OT1	Data of ADC conversion for OT channel 1	16	ro	0x0
F0	DATA_OT0	Data of ADC conversion for OT channel 0	16	ro	0x0

7.9.10 SAR_INT

0x50010624	SAR_INT																													
SAR Interrupts. Contains the enable, status and clear for the SAR interrupt sources.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	F25	F24	-	-	-	-	-	F18	F17	F16	-	-	-	-	-	-	F9	F8	-	-	-	-	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F25	INT_OT_IRQ	Over-temperature interrupt.	1	ro	N/A
F24	INT_SAR_DONE_IRQ	SAR convert done interrupt.	1	ro	N/A
F18	INT_OT1_STS	Over-temperature flag of OT channel 1. Set when an Over-temperature happens.	1	ro	N/A
F17	INT_OT0_STS	Over-temperature flag of OT channel 0. Set when an Over-temperature happens.	1	ro	N/A
F16	INT_SAR_DONE_STS	SAR convert done flag status. Set by the SAR when an conversion is done.	1	ro	N/A
F9	INT_OT_CLR	Over-temperature interrupt clear.	1	wo	N/A
F8	INT_SAR_DONE_CLR	SAR convert done interrupt clear.	1	wo	N/A
F1	INT_OT_ENA	Over-temperature interrupt enable.	1	rw	0x0
F0	INT_SAR_DONE_ENA	SAR convert done interrupt enable.	1	rw	0x0

7.10 SPI

SPI		
Address	**Register**	**Description**
0x50010700	SPIRXDATA	Serial Peripheral Rx Data Register
0x50010704	SPITXDATA	Serial Peripheral Tx Data Register
0x50010708	SPICTRL	Serial Peripheral Control Register
0x5001070C	SPISTATUS	Serial Peripheral Status Register
0x50010710	SPIINTSTATUS	SPI Interrupt Status
0x50010714	SPIINTENABLE	SPI Interrupt Enable
0x50010718	SPIINTCLEAR	SPI Interrupt Clear

7.10.1 SPIRXDATA

0x50010700	SPIRXDATA																													
Serial Peripheral Rx Data Register.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	RXDATA	Rx Data buffer. Received Data Register. A read from this register will return data from current read pointer on the receive FIFO. A read from this register will increment the read pointer on the receive FIFO.	8	ro	0x0

7.10.2 SPITXDATA

0x50010704	SPITXDATA

Serial Peripheral Tx Data Register.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	TXDATA	Tx Data buffer. Transmit Data Register. Used for data that is to be transmitted. A write to this register will place data into the transmit FIFO and increment the write pointer for the transmit FIFO.	8	wo	0x0

7.10.3 SPICTRL

0x50010708	SPICTRL

Serial Peripheral Control Register.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F24	-	-	-	-	-	-	-	F16	-	-	-	-	-	-	F8		F6		F5	F4	F2		F1	F0

#	Field Name	Field Description	Width	Access	Reset
F24	FIFOSOFTRESET	FIFO Soft Reset. FIFO Soft Reset bit (active high). Writing a one here will clear the FIFO pointers. This bit automatically clears to zero.	1	wo	0x0
F16	LPBK	Port wired-OR mode bit. 0x0: master_in = miso 0x1: master_in = mosi	1	rw	0x0
F8	ICNT	Interrupt counter bits. 0x0: Interrupt is set after every completed transfer 0x1: Interrupt is set after two completed transfers 0x2: Interrupt is set after three completed transfers 0x3: Interrupt is set after four completed transfers	2	rw	0x0
F6	SCKEXT	Extended clock divider. SPR - Standard Clock Rate Divider Select SPRE (SCKEXT) - Extended Clock Rate Select Bits {SPRE, SPR} = Clock Divide Result {00, 00}: System Clock / 2 {00, 01}: System Clock / 4 {00, 10}: System Clock / 8 {00, 11}: System Clock / 32 {01, 00}: System Clock / 64 {01, 01}: System Clock / 16 {01, 10}: System Clock / 128 {01, 11}: System Clock / 256 {10, 00}: System Clock / 512 {10, 01}: System Clock / 1024 {10, 10}: System Clock / 2048 {10, 11}: System Clock / 4096 {11, xx}: Reserved	2	rw	0x0
F5	CPOL	SPI clock polarity (Motorola SPI Frame Format). 0x0: The base value of the clock is zero 0x1: The base value of the clock is one	1	rw	0x0
F4	CPHA	SPI clock phase. 0x0: Data is captured on clock transition from base and data is propagated on the clock transition to base 0x1: Data is captured on clock transition to base and data is propagated on the clock transition from base	1	rw	0x0
F2	SPR	Standard clock divider selection. Please refer to SPRE register for system clock.	2	rw	0x0
F1	ENA_STS	SPI enable status. Status of SPI enable	1	ro	0x0
F0	ENA_REQ	SPI enable request. Enables the SPI interface. When SPI enable is deasserted the Tx and Rx FIFO's are still operable. Careful- If data is present in the Tx FIFO prior to enabling SPI, then once SPI is enabled it will begin transmitting the data present in the Tx FIFO.	1	rw	0x0

7.10.4 SPISTATUS

0x5001070C	SPISTATUS

Serial Peripheral Status Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	F16		-	-	-	-	-	-	F8		-	F6	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F16	TXFIFOCOUNT	Transmit FIFO Count. Signal indicates active number of bytes in the FIFO. Increments on Push. Decrements on Pop.	2	ro	0x0
F8	RXFIFOCOUNT	Reception FIFO Count. Signal indicates active number of bytes in the FIFO. Increments on Push. Decrements on Pop.	2	ro	0x0
F6	TXFIFOFULL	Transmit FIFO full. 0x0: FIFO is NOT full 0x1: FIFO is full	1	ro	0x0
F5	TXFIFOEMPTY	Transmit FIFO empty. 0x0: FIFO is NOT empty 0x1: FIFO is empty	1	ro	0x1
F4	RXFIFOFULL	Reception FIFO full. 0x0: FIFO is NOT full 0x1: FIFO is full	1	ro	0x0
F3	RXFIFOEMPTY	Reception FIFO empty. 0x0: FIFO is NOT empty 0x1: FIFO is empty	1	ro	0x1
F2	TXFIFOOF	Transmit FIFO overflow. 0x0: overflow inactive 0x1: overflow active	1	ro	0x0
F1	RXFIFOUF	Reception FIFO underflow. 0x0: underflow inactive 0x1: underflow active	1	ro	0x0
F0	XFERCNT	Completed Transfer Count. Signal is set after a programmable amount of completed transfer. See SPI_CTRL register field ICNT.	1	ro	0x0

7.10.5 SPIINTSTATUS

0x50010710 **SPIINTSTATUS**

SPI Interrupt Status. Read this register to establish the reason for an SPI interrupt. This interrupt status is reporting the status after the interrupt enable. All interrupts are OR'ed together into a single SPI IRQ signal.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F2	INTTXFIFOOF	Transmit FIFO Overflow Interrupt. Interrupt is set when Transmit FIFO is full and a write transaction occurs. (WRITE COLLISION)	1	ro	0x0
F1	INTRXFIFOUF	Reception FIFO Underflow Interrupt. Interrupt is set when Receive FIFO is empty and a read transaction occurs. (READ COLLISION)	1	ro	0x0
F0	INTXFERCNT	SPI Transfer Count Interrupt. Interrupt is set after a programmable amount of completed transfer. See SPI_CTRL register field ICNT.	1	ro	0x0

7.10.6 SPIINTENABLE

0x50010714 **SPIINTENABLE**

SPI Interrupt Enable. SPI Interrupt Enable Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F2	INTTXFIFOOFENA	Transmit FIFO Overflow Interrupt Enable.	1	rw	0x0
F1	INTRXFIFOUFENA	Reception FIFO Underflow Interrupt Enable.	1	rw	0x0
F0	INTXFERCNTENA	SPI Transfer Count Interrupt Enable.	1	rw	0x0

7.10.7 SPIINTCLEAR

0x50010718 **SPIINTCLEAR**

SPI Interrupt Clear. SPI Interrupt Clear Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F2	INTTXFIFOOFCLR	Transmit FIFO Overflow Interrupt. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F1	INTRXFIFOUFCLR	Reception FIFO Underflow Interrupt. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F0	INTXFERCNTCLR	SPI Transfer Count Interrupt. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0

7.11 UART

UART		
Address	**Register**	**Description**
0x50010800	DATA	Data
0x50010804	UARTDATARECEIVESTATUS	Data Receive Status
0x50010808	MSGCTRL	Message control
0x5001080C	UARTINT	UART Interrupts
0x50010810	UARTINT2	Extended UART Interrupts
0x50010814	UARTBAUD	UART Baud rate
0x50010818	UARTFIFOSTATUS	UART FIFO STATUS
0x5001081C	UARTFIFOLEVELCTL	UART FIFO Level Control

7.11.1 DATA

0x50010800 **DATA**

Data.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F9				F0							

#	Field Name	Field Description	Width	Access	Reset
F9	DATARECEIVESTATUS	Data Receive Status. Mirror for DATA_RECEIVE_STATUS: This register contains the receive status associated with the current byte read from the UART_DATA register. The Data Receive Status register is updated only after a read from the UART_DATA register. Example- Read UART_DATA byte first. Then read UART_DATA_RECEIVE_STATUS register second.	3	ro	0x0
F0	BYTE	Data. Used for both received data(ONLY bit0~7 are available) and data that is to be transmitted(bit0~8 are available): Transmit: the MSB-bit[8] is only available for Transmitter, and it indicates this data used for sending BREAK or Not 1'b1 : this DATA is used for sending BREAK; 1'b0 : this DATA is used for sending Normal Data. Receive: the MSB-bit[7] indicates the mode Match Address: 1'b0 : Normal mode, the following Rxd Datas will be received with the condition of 7bits-[6:0] matched; 1'b1 : Broadcast mode, the following Rxd Datas will be received without the condition of 7bits-[6:0] matched.	9	dual	0x0

7.11.2 UARTDATARECEIVESTATUS

0x50010804 **UARTDATARECEIVESTATUS**

Data Receive Status. This register contains the receive status associated with the current byte read from the UART_DATA register.
The Data Receive Status register is updated only after a read from the UART_DATA register.
Example- Read UART_DATA byte first. Then read UART_DATA_RECEIVE_STATUS register second.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset

F2	BREAKERROR	Break Error. This bit is set to 1 if a break condition was detected, indicating that the received data input was held LOW for longer than a full-word transmission time (defined as start, data, parity, and stop bits).	1	ro	0x0
F1	PARITYERROR	Parity Error. When this bit is set to 1, it indicates that the parity of the received data character does not match the parity selected as defined by bits 2 and 7 of the UARTLCR_H register.	1	ro	0x0
F0	FRAMEERROR	Framing Error. When this bit is set to 1, it indicates that the received byte did not have a valid stop bit (a valid stop bit is 1).	1	ro	0x0

7.11.3 MSGCTRL

0x50010808 **MSGCTRL**

Message control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	F24							F23	-	-	-	-	-	-	-	-	-	F13	F12	F11	F10	F8		F6		F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F24	ADDR_MATCH	Match Address. Match Address, Only 7bit is available	7	rw	0x0
F23	LOOPENA	Loopback enable. Set to enable loopback	1	rw	0x0
F13	STICKENA	Sticky parity enable. Set to enable sticky parity	1	rw	0x0
F12	PARODD	Odd parity. 0x0: ODD Parity 0x1: EVEN parity	1	rw	0x0
F11	PARENA	Parity enable. Set to enable parity (see PARODD for odd/even)	1	rw	0x0
F10	STOP	Stop bit control. 0x0: One stop bit 0x1: If a 5-bit transmission it selects 1.5 stop bits, otherwise 2 stop bits (6, 7 & 8 bits)	1	rw	0x0
F8	SIZE	Transmission word size. 0x0: 5-bit(only available for Receive mode) 0x1: 6-bit(only available for Receive mode) 0x2: 7-bit(available for Receive and Transmit mode) 0x3: 8-bit(available for Receive and Transmit mode)	2	rw	0x3
F6	MAX_BYTES_RXD	Set Max Byte number of DATA in a rxd frame 0x0: 15-Bytes 0x1: 31-Bytes 0x2: 63-Bytes 0x3: 127-Bytes	2	rw	0x3
F5	ENA_ADDR_MATCH	Set to enable Address Match	1	rw	0x0
F4	TXXFERCNTCLR	TX Transfer Counter Clear. Clear TX Multi Transfer Counter to zero Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F3	RXXFERCNTCLR	RX Transfer Counter Clear. Clear RX Multi Transfer Counter to zero Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F2	UFIFOSOFTRESET	FIFO SOFT RESET. Resets FIFO pointers to zero and initializes FIFO contents to zero Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F1	ENABLE_STS	Enable status. Status of UART enable	1	ro	0x0
F0	ENABLE	Enable. Set to enable the UART	1	rw	0x0

7.11.4 UARTINT

0x5001080C **UARTINT**

UART Interrupts. Contains the enable, status and clear for the UART interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	F30	F29	F28	F27	F26	F25	F24	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F31	TXMULTDONE	Multiple Transmit Transactions Done Interrupt. Set by the UART when the programmed number of transmit transactions have completed. See UART_FIFO_LEVEL_CTL register.	1	ro	0x0

F30	RXMULTDONE	Multiple Receive Transactions Done Interrupt. Set by the UART when the programmed number of receive transactions have completed. See UART_FIFO_LEVEL_CTL register	1	ro	0x0
F29	TXDONE	Transmission done Interrupt. Set by the UART when the transmission is done	1	ro	0x0
F28	BREAKKERR	Break Error Interrupt. Set by the UART when a break error occurs	1	ro	0x0
F27	PRTYERR	Parity Error Interrupt. Set by the UART when a parity error occurs	1	ro	0x0
F26	FRMERR	Framing error Interrupt. Set by the UART when a framing error occurs	1	ro	0x0
F25	OVRUNERR	Overrun error Interrupt. Set by the UART when an overrun error occurs	1	ro	0x0
F24	RXDONE	Rx Data ready Interrupt. Set by the UART when Rx data is ready	1	ro	0x0
F23	TXMULTDONE	Multiple Transmit Transactions Done. Set by the UART when the programmed number of transmit transactions have completed. See UART_FIFO_LEVEL_CTL register.	1	ro	0x0
F22	RXMULTDONE	Multiple Receive Transactions Done. Set by the UART when the programmed number of receive transactions have completed. See UART_FIFO_LEVEL_CTL register	1	ro	0x0
F21	TXDONE	Transmission is done. Set by the UART when the transmit is done	1	ro	0x0
F20	BREAKKERR	Break IRQ. Set by the UART when a break error occurs	1	ro	0x0
F19	PRTYERR	Parity Error. Set by the UART when a parity error occurs	1	ro	0x0
F18	FRMERR	Framing error. Set by the UART when a framing error occurs	1	ro	0x0
F17	OVRUNERR	Overrun error. Set by the UART when an overrun error occurs	1	ro	0x0
F16	RXDONE	Rx Data ready. Set by the UART when Rx data is ready	1	ro	0x0
F15	TXMULTDONE	Multiple Transmit Transactions Done Interrupt Clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F14	RXMULTDONE	Multiple Receive Transactions Done Interrupt Clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F13	TXDONE	Transmission done Interrupt Clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F12	BREAKKERR	Break Error Interrupt Clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F11	PRTYERR	Parity Error Interrupt Clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F10	FRMERR	Framing error Interrupt Clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F9	OVRUNERR	Overrun error Interrupt Clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F8	RXDONE	Rx Data ready Interrupt Clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F7	TXMULTDONE	Multiple Transmit Transactions Done Interrupt Enable.	1	rw	0x0
F6	RXMULTDONE	Multiple Receive Transactions Done Interrupt Enable.	1	rw	0x0
F5	TXDONE	Transmission done Interrupt Enable.	1	rw	0x0
F4	BREAKKERR	Break Error Interrupt Enable.	1	rw	0x0
F3	PRTYERR	Parity Error Interrupt Enable.	1	rw	0x0
F2	FRMERR	Framing error Interrupt Enable.	1	rw	0x0
F1	OVRUNERR	Overrun error Interrupt Enable.	1	rw	0x0
F0	RXDONE	Rx Data ready Interrupt Enable.	1	rw	0x0

7.11.5 UARTINT2

0x50010810	UARTINT2

Extended UART Interrupts. Contains the enable, status and clear for the extended UART interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F24	-	-	-	-	-	-	-	F16	-	-	-	-	-	-	-	F8	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F24	RXTOUT	Rx Time-out Interrupt. Set by the UART when RXTOUT flag is set and RXOUT interrupt is enabled.	1	ro	0x0
F16	RXTOUT	Rx Time-out. Set by the UART when timeout of 4 data frame times without reception, and data received(one or three bytes received,programmable)	1	ro	0x0
F8	RXTOUT	Rx Time-out Interrupt Clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F0	RXTOUT	Rx Time-out Interrupt Enable.	1	rw	0x0

7.11.6 UARTBAUD

0x50010814 **UARTBAUD**

UART Baud rate. The controls in this register define the relationship between the system clock and the UART baud rate. The baud rate is given by the following equation. baud_rate = Fclk/(OSR*(BAUDDIV+1+FDIV/8)) where Fclk is the frequency of the system clock, and OSR , FDIV and BAUDDIV are the fields of this register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	F29	F28	-	F24			-	-	-	F16					F0															

#	Field Name	Field Description	Width	Access	Reset
F29	URETARD	Retard Register. Retards the sample window by 1 cycle. For Debug.	1	rw	0x0
F28	UADVANCE	Advance Register. Advances the sample window by 1 cycle. For Debug.	1	rw	0x0
F24	FDIV	Fractional divider.	3	rw	0x0
F16	OSR	Over-sampling ratio. Valid OSR Range: 6 to 16.	5	rw	0x10
F0	BAUDDIV	Baud rate divider.	16	rw	0x0

7.11.7 UARTFIFOSTATUS

0x50010818 **UARTFIFOSTATUS**

UART FIFO STATUS. The FIFO status register is read-only and gives the current state of the Receive and Transmit FIFO's.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	F24				-	-	-	-	-	F18	F17	F16	-	-	F8						-	-	-	-	-	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F24	TXCOUNT	Transmit FIFO current count.	4	ro	0x0
F18	TXFULL	Transmit FIFO full.	1	ro	0x0
F17	TXEMPTY	Transmit FIFO empty.	1	ro	0x0
F16	TXOF	Transmit FIFO overflow.	1	ro	0x0
F8	RXCOUNT	Reception FIFO current count.	6	ro	0x0
F2	RXFULL	Reception FIFO empty.	1	ro	0x0
F1	RXEMPTY	Reception FIFO empty.	1	ro	0x0
F0	RXUF	Reception FIFO underflow.	1	ro	0x0

7.11.8 UARTFIFOLEVELCTL

0x5001081C **UARTFIFOLEVELCTL**

UART FIFO Level Control. The FIFO Level Control register defines the trigger points for the transmit and receive interrupts.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F8				-	-	F0					

#	Field Name	Field Description	Width	Access	Reset
F8	TXMULTIPLEXFERDONECNT	Transmit Data Count Interrupt. Number of bytes transmitted from the transmit FIFO before a INT_TX_MULTIPLE_XFER_DONE interrupt is asserted. Example: A value of 4 would be used to compare to the number of completed transfers (pops from the Tx FIFO).	4	rw	0x1

		Valid Range: 1 to 8, NOTE: Invalid configuration value '0' will be forced to '1'			
F0	RXMULTIPLEXFERDONECNT	Receive Data Count Interrupt. Minimum number of bytes in the receive FIFO before a INT_RX_MULTIPLE_XFER_DONE interrupt is asserted. Example: A value of 4 would be used to compare to the number of receive transactions (pushes to the Rx FIFO). Valid Range: 1 to 32, NOTE: Invalid configuration value '0' will be forced to '1'	6	rw	0x1

7.12 PWM_AUX

PWM_AUX		
Address	**Register**	**Description**
0x50010900	BASE0	Base 0 functions
0x50010904	PWMCNT0	PWM Count Value
0x50010908	BASE1	Base 1 functions
0x5001090C	PWMCNT1	PWM Count Value
0x50010910	BASESEL	Base Timer Select for individual Channels
0x50010914	ENAREQ	Enable request
0x50010918	ENASTS	Enable status
0x5001091C	INIT	Intial State of Outputs
0x50010920	INV	Invert
0x50010924	UPDATE	Update
0x50010928	PULSE0	PWM0 pulse setup
0x5001092C	PULSE1	PWM1 pulse setup
0x50010930	PULSE2	PWM2 pulse setup
0x50010934	PULSE3	PWM3 pulse setup
0x50010938	PULSE4	PWM4 pulse setup
0x5001093C	INTPOSEDGENA	PWM posedge interrupt enable
0x50010940	INTNEGEDGENA	PWM negedge interrupt enable
0x50010944	INTPOSEDGCLR	PWM posedge interrupt control
0x50010948	INTNEGEDGCLR	PWM negedge interrupt control
0x5001094C	INTPOSEDGSTS	PWM posedge interrupt status
0x50010950	INTNEGEDGSTS	PWM negedge interrupt status
0x50010954	INTPOSEDGIRQ	PWM posedge interrupt active
0x50010958	INTNEGEDGIRQ	PWM negedge interrupt active
0x5001095C	INTPERIOD	PWM Period interrupt control
0x50010960	INTUPDATED	PWM Updated interrupt control

7.12.1 BASE0

0x50010900	BASE0				
Base 0 functions.					
31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11	10 9 8	7 6	5 4 3 2 1 0
F16		- - - - -	F8	- -	- - - - - -

#	Field Name	Field Description	Width	Access	Reset
F16	PERIOD0	Period. Specifies the period of the output waveform in terms of a number of prescaler output cycles.	16	rw	0x0
F8	PRESCALESEL0	Prescaler select. Defines the ratio between the system clock and the clock used for the waveform generator. 0x0: Divide by 1 0x1: Divide by 2 0x2: Divide by 4 0x3: Divide by 8 0x4: Divide by 16 0x5: Divide by 64 0x6: Divide by 256 0x7: Divide by 1024	3	rw	0x0

7.12.2 PWMCNT0

0x50010904	PWMCNT0																													
PWM Count Value.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	PWMCNT0	PWM counter value to give a sense about the current period	16	ro	0x0

7.12.3 BASE1

0x50010908	BASE1																													
Base 1 functions.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																-	-	-	-	-	F8			-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F16	PERIOD1	Period. Specifies the period of the output waveform in terms of a number of prescaler output cycles.	16	rw	0x0
F8	PRESCALESEL1	Prescaler select. Defines the ratio between the system clock and the clock used for the waveform generator. 0x0: Divide by 1 0x1: Divide by 2 0x2: Divide by 4 0x3: Divide by 8 0x4: Divide by 16 0x5: Divide by 64 0x6: Divide by 256 0x7: Divide by 1024	3	rw	0x0

7.12.4 PWMCNT1

0x5001090C	PWMCNT1																													
PWM Count Value.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	PWMCNT1	PWM counter value to give a sense about the current period	16	ro	0x0

7.12.5 BASESEL

0x50010910	BASESEL																													
Base Timer Select for individual Channels.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0				

#	Field Name	Field Description	Width	Access	Reset
F0	BASE_SEL	Base Timer Selects:1=Select BASE1, 0=Select BASE0.	5	rw	0x0

7.12.6 ENAREQ

0x50010914	ENAREQ																													
Enable request.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	F26	F25	F24	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0				

#	Field Name	Field Description	Width	Access	Reset
F26	FORCEINACTIVE	Set to force PWM signals return to initial value immediately.	1	rw	0x0
F25	CLRREQALL	Write 1 to clear all ENA_REQ bits; Write 0 has no effects.	1	wo	0x0
F24	ENAREQALL	Write 1 to enable all ENA_REQ bits; Write 0 has no effects.	1	wo	0x0
F0	ENAREQ	Set to enable the waveform generator.	5	rw	0x0

7.12.7 ENASTS

0x50010918	ENASTS																													
Enable status.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0				

#	Field Name	Field Description	Width	Access	Reset
F0	ENASTS	Status of enable in the waveform generator.	5	ro	0x0

7.12.8 INIT

0x5001091C	INIT																													
Intial State of Outputs.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0				

#	Field Name	Field Description	Width	Access	Reset
F0	INIT	Set to initialise the output waveform.	5	rw	0x0

7.12.9 INV

0x50010920	INV																													
Invert.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0				

#	Field Name	Field Description	Width	Access	Reset
F0	INVERT	Set to invert the output waveform.	5	rw	0x0

7.12.10 UPDATE

0x50010924	UPDATE																													
Update.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0	

#	Field Name	Field Description	Width	Access	Reset
F0	UPDATE	Set to trigger consumption of new PULSE parameters (invert,prescale_sel,period,pulse start & stop). The flag is automatically cleared by the hardware when the settings are consumed, so reading a high value indicates that an update is still pending.	2	dual	0x0

7.12.11 PULSE0

0x50010928	PULSE0																													
PWM0 pulse setup.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0														

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE0	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL0	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

7.12.12 PULSE1

0x5001092C	PULSE1

PWM1 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE1	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL1	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

7.12.13 PULSE2

0x50010930 **PULSE2**

PWM2 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE2	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL2	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

7.12.14 PULSE3

0x50010934 **PULSE3**

PWM3 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE3	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL3	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

7.12.15 PULSE4

0x50010938 **PULSE4**

PWM4 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE4	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL4	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

7.12.16 INTPOSEDGENA

0x5001093C **INTPOSEDGENA**

PWM posedge interrupt enable. Contains the enable for the PWM posedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0				

#	Field Name	Field Description	Width	Access	Reset

F0	INTPOSEDGENA	Interrupt enable. bit[4:0]: posedge interrupt enable.	5	rw	0x0

7.12.17 INTNEGEDGENA

0x50010940																															
INTNEGEDGENA																															
PWM negedge interrupt enable. Contains the enable for the PWM negedge interrupt sources.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0				

#	Field Name	Field Description	Width	Access	Reset
F0	INTNEGEDGENA	Interrupt enable. bit[4:0]: negedge interrupt enable.	5	rw	0x0

7.12.18 INTPOSEDGCLR

0x50010944																															
INTPOSEDGCLR																															
PWM posedge interrupt control. Contains the clear for the PWM posedge interrupt sources.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0				

#	Field Name	Field Description	Width	Access	Reset
F0	INTPOSEDGCLR	Interrupt clear. bit[4:0] : posedge interrupt clear.	5	wo	0x0

7.12.19 INTNEGEDGCLR

0x50010948																															
INTNEGEDGCLR																															
PWM negedge interrupt control. Contains the clear for the PWM negedge interrupt sources.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0				

#	Field Name	Field Description	Width	Access	Reset
F0	INTNEGEDGCLR	Interrupt clear. bit[4:0] : negedge interrupt clear.	5	wo	0x0

7.12.20 INTPOSEDGSTS

0x5001094C																															
INTPOSEDGSTS																															
PWM posedge interrupt status. Contains the status for the PWM posedge interrupt sources.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0				

#	Field Name	Field Description	Width	Access	Reset
F0	INTPOSEDGSTS	Interrupt status. bit[4:0] : posedge interrupt status.	5	ro	N/A

7.12.21 INTNEGEDGSTS

0x50010950																															
INTNEGEDGSTS																															
PWM negedge interrupt status. Contains the status for the PWM negedge interrupt sources.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0				

#	Field Name	Field Description	Width	Access	Reset
F0	INTNEGEDGSTS	Interrupt status. bit[4:0] : negedge interrupt status.	5	ro	N/A

7.12.22 INTPOSEDGIRQ

0x50010954																															
INTPOSEDGIRQ																															
PWM posedge interrupt active. Contains the active for the PWM posedge interrupt sources.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0				

#	Field Name	Field Description	Width	Access	Reset
F0	INTPOSEDGIRQ	Interrupt active. bit[4:0] : posedge interrupt active.	5	ro	N/A

7.12.23 INTNEGEDGIRQ

0x50010958	INTNEGEDGIRQ

PWM negedge interrupt active. Contains the active for the PWM negedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0				

#	Field Name	Field Description	Width	Access	Reset
F0	INTNEGEDGIRQ	Interrupt active. bit[4:0] : negedge interrupt active.	5	ro	N/A

7.12.24 INTPERIOD

0x5001095C	INTPERIOD

PWM Period interrupt control. Contains the enable, clear, status and active for the PWM period interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	F24		-	-	-	-	-	-	F16		-	-	-	-	-	-	F8		-	-	-	-	-	-	F0	

#	Field Name	Field Description	Width	Access	Reset
F24	PERIOD	Period Interrupt active.	2	ro	N/A
F16	PERIOD	Period Interrupt status.	2	ro	N/A
F8	PERIOD	Period Interrupt clear.	2	wo	0x0
F0	PERIOD	Period Interrupt enable.	2	rw	0x0

7.12.25 INTUPDATED

0x50010960	INTUPDATED

PWM Updated interrupt control. Contains the enable, clear, status and active for the PWM updated interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	F24		-	-	-	-	-	-	F16		-	-	-	-	-	-	F8		-	-	-	-	-	-	F0	

#	Field Name	Field Description	Width	Access	Reset
F24	UPD	Updated Interrupt active.	2	ro	N/A
F16	UPD	Updated Interrupt status.	2	ro	N/A
F8	UPD	Updated Interrupt clear.	2	wo	0x0
F0	UPD	Updated Interrupt enable.	2	rw	0x0

7.13 PWM

PWM		
Address	**Register**	**Description**
0x50011000	BASE	Base functions
0x50011004	PWMCNT	PWM Count Value
0x50011008	ENAREQ	Enable request
0x5001100C	ENASTS	Enable status
0x50011010	INIT	Intial State of Outputs
0x50011014	INV	Invert
0x50011018	UPDATE	Update
0x5001101C	PULSE0	PWM0 pulse setup
0x50011020	PULSE1	PWM1 pulse setup
0x50011024	PULSE2	PWM2 pulse setup
0x50011028	PULSE3	PWM3 pulse setup
0x5001102C	PULSE4	PWM4 pulse setup
0x50011030	PULSE5	PWM5 pulse setup
0x50011034	PULSE6	PWM6 pulse setup
0x50011038	PULSE7	PWM7 pulse setup
0x5001103C	PULSE8	PWM8 pulse setup

0x50011040	PULSE9	PWM9 pulse setup
0x50011044	PULSE10	PWM10 pulse setup
0x50011048	PULSE11	PWM11 pulse setup
0x5001104C	PULSE12	PWM12 pulse setup
0x50011050	PULSE13	PWM13 pulse setup
0x50011054	PULSE14	PWM14 pulse setup
0x50011058	PULSE15	PWM15 pulse setup
0x5001105C	PULSE16	PWM16 pulse setup
0x50011060	PULSE17	PWM17 pulse setup
0x50011064	PULSE18	PWM18 pulse setup
0x50011068	PULSE19	PWM19 pulse setup
0x5001106C	PULSE20	PWM20 pulse setup
0x50011070	PULSE21	PWM21 pulse setup
0x50011074	PULSE22	PWM22 pulse setup
0x50011078	PULSE23	PWM23 pulse setup
0x5001107C	INTPOSEDGENA	PWM posedge interrupt enable
0x50011080	INTNEGEDGENA	PWM negedge interrupt enable
0x50011084	INTPOSEDGCLR	PWM posedge interrupt control
0x50011088	INTNEGEDGCLR	PWM negedge interrupt control
0x5001108C	INTPOSEDGSTS	PWM posedge interrupt status
0x50011090	INTNEGEDGSTS	PWM negedge interrupt status
0x50011094	INTPOSEDGIRQ	PWM posedge interrupt active
0x50011098	INTNEGEDGIRQ	PWM negedge interrupt active
0x5001109C	INTPWM	PWM interrupt control

7.13.1 BASE

0x50011000 **BASE**

Base functions.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																-	-	-	-	-	F8			-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F16	PERIOD	Period. Specifies the period of the output waveform in terms of a number of prescaler output cycles.	16	rw	0x0
F8	PRESCALESEL	Prescaler select. Defines the ratio between the system clock and the clock used for the waveform generator. 0x0: Divide by 1 0x1: Divide by 2 0x2: Divide by 4 0x3: Divide by 8 0x4: Divide by 16 0x5: Divide by 64 0x6: Divide by 256 0x7: Divide by 1024	3	rw	0x0

7.13.2 PWMCNT

0x50011004 **PWMCNT**

PWM Count Value.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	PWMCNT	PWM counter value to give a sense about the current period	16	dual	0x0

7.13.3 ENAREQ

0x50011008 **ENAREQ**

Enable request.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	F26	F25	F24	F0																							

#	Field Name	Field Description	Width	Access	Reset
F26	FORCEINACTIVE	Set to force PWM signals return to initial value immediately.	1	rw	0x0
F25	CLRREQALL	Write 1 to clear all ENA_REQ bits; Write 0 has no effects.	1	wo	0x0
F24	ENAREQALL	Write 1 to enable all ENA_REQ bits; Write 0 has no effects.	1	wo	0x0
F0	ENAREQ	Set to enable the waveform generator.	24	rw	0x0

7.13.4 ENASTS

0x5001100C **ENASTS**

Enable status.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	F0																							

#	Field Name	Field Description	Width	Access	Reset
F0	ENASTS	Status of enable in the waveform generator.	24	ro	0x0

7.13.5 INIT

0x50011010 **INIT**

Intial State of Outputs.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	F0																							

#	Field Name	Field Description	Width	Access	Reset
F0	INIT	Set to initialise the output waveform.	24	rw	0x0

7.13.6 INV

0x50011014 **INV**

Invert.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	F0																							

#	Field Name	Field Description	Width	Access	Reset
F0	INVERT	Set to invert the output waveform.	24	rw	0x0

7.13.7 UPDATE

0x50011018 **UPDATE**

Update.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	UPDATE	Set to trigger consumption of new PULSE parameters (invert,prescale_sel,period,pulse start & stop). The flag is automatically cleared by the hardware when the settings are consumed, so reading a high value indicates that an update is still pending.	1	dual	0x0

7.13.8 PULSE0

0x5001101C **PULSE0**

PWM0 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE0	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0

F0	PFALL0	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

7.13.9 PULSE1

0x50011020	PULSE1				
PWM1 pulse setup.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0			
F16	F0				
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F16	PRISE1	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL1	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

7.13.10 PULSE2

0x50011024	PULSE2				
PWM2 pulse setup.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0			
F16	F0				
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F16	PRISE2	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL2	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

7.13.11 PULSE3

0x50011028	PULSE3				
PWM3 pulse setup.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0			
F16	F0				
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F16	PRISE3	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL3	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

7.13.12 PULSE4

0x5001102C	PULSE4				
PWM4 pulse setup.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0			
F16	F0				
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F16	PRISE4	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL4	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

7.13.13 PULSE5

0x50011030	PULSE5

PWM5 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE5	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL5	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

7.13.14 PULSE6

0x50011034	PULSE6

PWM6 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE6	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL6	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

7.13.15 PULSE7

0x50011038	PULSE7

PWM7 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE7	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL7	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

7.13.16 PULSE8

0x5001103C	PULSE8

PWM8 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE8	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL8	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

7.13.17 PULSE9

0x50011040	PULSE9

PWM9 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE9	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL9	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

7.13.18 PULSE10

0x50011044 **PULSE10**

PWM10 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE10	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL10	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

7.13.19 PULSE11

0x50011048 **PULSE11**

PWM11 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE11	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL11	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

7.13.20 PULSE12

0x5001104C **PULSE12**

PWM12 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE12	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL12	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

7.13.21 PULSE13

0x50011050 **PULSE13**

PWM13 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset

F16	PRISE13	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL13	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

7.13.22 PULSE14

0x50011054	PULSE14

PWM14 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE14	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL14	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

7.13.23 PULSE15

0x50011058	PULSE15

PWM15 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE15	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL15	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

7.13.24 PULSE16

0x5001105C	PULSE16

PWM16 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE16	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL16	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

7.13.25 PULSE17

0x50011060	PULSE17

PWM17 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE17	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0

F0	PFALL17	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

7.13.26 PULSE18

0x50011064 **PULSE18**

PWM18 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE18	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL18	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

7.13.27 PULSE19

0x50011068 **PULSE19**

PWM19 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE19	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL19	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

7.13.28 PULSE20

0x5001106C **PULSE20**

PWM20 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE20	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL20	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

7.13.29 PULSE21

0x50011070 **PULSE21**

PWM21 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE21	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL21	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

7.13.30 PULSE22

0x50011074	PULSE22

PWM22 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE22	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL22	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

7.13.31 PULSE23

0x50011078	PULSE23

PWM23 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE23	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL23	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

7.13.32 INTPOSEDGENA

0x5001107C	INTPOSEDGENA

PWM posedge interrupt enable. Contains the enable for the PWM posedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	F0																							

#	Field Name	Field Description	Width	Access	Reset
F0	INTPOSEDGENA	Interrupt enable. bit[23:0]: posedge interrupt enable.	24	rw	0x0

7.13.33 INTNEGEDGENA

0x50011080	INTNEGEDGENA

PWM negedge interrupt enable. Contains the enable for the PWM negedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	F0																							

#	Field Name	Field Description	Width	Access	Reset
F0	INTNEGEDGENA	Interrupt enable. bit[23:0]: negedge interrupt enable.	24	rw	0x0

7.13.34 INTPOSEDGCLR

0x50011084	INTPOSEDGCLR

PWM posedge interrupt control. Contains the clear for the PWM posedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	F0																							

#	Field Name	Field Description	Width	Access	Reset
F0	INTPOSEDGCLR	Interrupt clear. bit[23:0] : posedge interrupt clear.	24	wo	0x0

7.13.35 INTNEGEDGCLR

0x50011088	INTNEGEDGCLR

PWM negedge interrupt control. Contains the clear for the PWM negedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	F0																							

#	Field Name	Field Description	Width	Access	Reset
F0	INTNEGEDGCLR	Interrupt clear. bit[23:0] : negedge interrupt clear.	24	wo	0x0

7.13.36 INTPOSEDGSTS

0x5001108C **INTPOSEDGSTS**

PWM posedge interrupt status. Contains the status for the PWM posedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	F0																							

#	Field Name	Field Description	Width	Access	Reset
F0	INTPOSEDGSTS	Interrupt status. bit[23:0] : posedge interrupt status.	24	ro	N/A

7.13.37 INTNEGEDGSTS

0x50011090 **INTNEGEDGSTS**

PWM negedge interrupt status. Contains the status for the PWM negedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	F0																							

#	Field Name	Field Description	Width	Access	Reset
F0	INTNEGEDGSTS	Interrupt status. bit[23:0] : negedge interrupt status.	24	ro	N/A

7.13.38 INTPOSEDGIRQ

0x50011094 **INTPOSEDGIRQ**

PWM posedge interrupt active. Contains the active for the PWM posedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	F0																							

#	Field Name	Field Description	Width	Access	Reset
F0	INTPOSEDGIRQ	Interrupt active. bit[23:0] : posedge interrupt active.	24	ro	N/A

7.13.39 INTNEGEDGIRQ

0x50011098 **INTNEGEDGIRQ**

PWM negedge interrupt active. Contains the active for the PWM negedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	F0																							

#	Field Name	Field Description	Width	Access	Reset
F0	INTNEGEDGIRQ	Interrupt active. bit[23:0] : negedge interrupt active.	24	ro	N/A

7.13.40 INTPWM

0x5001109C **INTPWM**

PWM interrupt control. Contains the enable, clear, status and active for the PWM period & updated interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	F25	F24	-	-	-	-	-	-	F17	F16	-	-	-	-	-	-	F9	F8	-	-	-	-	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F25	UPD	Updated Interrupt active.	1	ro	N/A
F24	PERIOD	Period Interrupt active.	1	ro	N/A
F17	UPD	Updated Interrupt status.	1	ro	N/A
F16	PERIOD	Period Interrupt status.	1	ro	N/A
F9	UPD	Updated Interrupt clear.	1	wo	0x0
F8	PERIOD	Period Interrupt clear.	1	wo	0x0

F1	UPD	Updated Interrupt enable.	1	rw	0x0
F0	PERIOD	Period Interrupt enable.	1	rw	0x0

7.14 IOCTRLA

IOCTRLA		
Address	**Register**	**Description**
0x50012000	GPIO1	GPIO Pin 1 Control
0x50012004	GPIO2	GPIO Pin 2 Control
0x50012008	GPIO3	GPIO Pin 3 Control
0x5001200C	GPIO4	GPIO Pin 4 Control
0x50012010	GPIO5	GPIO Pin 5 Control
0x50012014	GPIO6	GPIO Pin 6 Control
0x50012018	GPIO7	GPIO Pin 7 Control
0x5001201C	GPIO8	GPIO Pin 8 Control
0x50012024	LIN	LIN Pin Control
0x50012028	LINSGFCONF	LINS Glitch Filter Configuration in active mode
0x5001202C	LINSGFCONF1	LINS Glitch Filter Configuration in active mode
0x50012038	LINTXDMONITOR	LIN TXD Dominant Timeout
0x5001203C	LEDPIN	LED Pin Control
0x50012040	LEDHWMODE	LED HW mode
0x50012044	LEDDATA	LED Data Out
0x50012048	LEDPUENA	LED Data Out
0x5001204C	ANALOGTESTMUXOVERRIDE1	Analog Testmux Override 1
0x50012050	ANALOGTESTMUXOVERRIDE2	Analog Testmux Override 2
0x50012054	ANALOGTESTMUXOVERRIDE3	Analog Testmux Override 3
0x50012058	IRQ	IOCTRLA LINS TXD Dominant Monitor interrupts
0x5001205C	FILT_ACCESS	Glitch Filter access key
0x50012060	MCU_INF_CONF	Mcu interface access config

7.14.1 GPIO1

0x50012000 **GPIO1**

GPIO Pin 1 Control. GPIO Pin 1 has four seperate drivers: GPIO Controller, PWM Controller ,Testmux.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	F24						-	-	-	-	-	-	-	-	-	-	-	-	-	-	F9	F8	F7	F6	F5	F4	F3	F0		

#	Field Name	Field Description	Width	Access	Reset
F24	MUXSEL	Selects debug signal to be output on gpio1. 0x0: PMUA (Power Management Unit Asic) qacks[0] 0x1: PMUA (Power Management Unit Asic) daffodil[0] 0x2: PMUA (Power Management Unit Asic) snowflake[0] 0x3: CRGA (Clock Reset Generation Asic) lf_rc_clk 0x4: CRGA (Clock Reset Generation Asic) hf_rc_clk 0x5: CRGA (Clock Reset Generation Asic) lf_rc_sts 0x6: CRGA (Clock Reset Generation Asic) hf_rc_sts 0x7: CRGA (Clock Reset Generation Asic) clk_sys_gated 0x8: CRGA (Clock Reset Generation Asic) (a_por_n) 0x9: CRGA (Clock Reset Generation Asic) (bor_3v3_n) 0xa: CRGA (Clock Reset Generation Asic) (ovtemp_flag) 0xb: CRGA (Clock Reset Generation Asic) (bor_1v5_n) 0xc: CRGA (Clock Reset Generation Asic) (wdt_bark) 0xd: Reserved 0xe: ADC ctrl (Analog to Digital Converter Controller) adc_done 0xf: ADC ctrl (Analog to Digital Converter Controller) sar_dout 0x10: ADC ctrl (Analog to Digital Converter Controller) sar_smp_vcm 0x11: ADC ctrl (Analog to Digital Converter Controller) sar_div_clk 0x14: LINS Controller rxd 0x15: LINS Controller txd 0x16: BOR CONTROL STATE MACHINE state[0] 0x17: BOR CONTROL STATE MACHINE state[1] 0x18: BOR CONTROL STATE MACHINE bor_bias_ena	6	rw	0x0

		0x19: BOR CONTROL STATE MACHINE bor_bias_ena_l 0x1a: BOR CONTROL STATE MACHINE pmua_bor_bias_ena 0x1b: BOR CONTROL STATE MACHINE hf_clk_allowed 0x1c: BOR CONTROL STATE MACHINE hf_active 0x1d: BOR CONTROL STATE MACHINE pmua_bor_arm_sync 0x1e: BATTERY VOLTAGE MONITOR raw output from vbat low comp 0x1f: BATTERY VOLTAGE MONITOR raw output from vbat high comp 0x20: BATTERY VOLTAGE MONITOR synchronised vbat low signal with polarity adjusted 0x21: BATTERY VOLTAGE MONITOR synchronised vbat high signal with polarity adjusted 0x22: BATTERY VOLTAGE MONITOR debounced synchronised vbat low signal 0x23: BATTERY VOLTAGE MONITOR debounced synchronised vbat high signal 0x24: BUCK dtb[0] 0x25: BUCK dtb[1] 0x26: Output of LINS 1st Stage Glitch Filter 0x27: Output of LINS 2nd Stage Glitch Filter 0x28: Output of LINS 3rd Stage Glitch Filter 0x29: Input of LINS 1st Stage Glitch Filter 0x2a: LINS PHY TXD			
F9	PDVR1	GPIO output drive strength MSB selector. GPIO output drive strength MSB selector. PDRV1 | PDRV0 | Output drive strength 0 | 0 | 4mA 0 | 1 | 8mA 1 | 0 | 12mA 1 | 1 | 16mA	1	rw	0x1
F8	PDVR0	GPIO output drive strength LSB selector. GPIO output drive strength LSB selector.	1	rw	0x0
F7	CS	input schmitt trigger enable. 0x0: Disable schmitt trigger 0x1: Enable schmitt trigger.	1	rw	0x1
F6	SL	slewrate ctrl. 0x0: Fast Slewrate on the GPIO 0x1: Slow Slewrate on the GPIO	1	rw	0x0
F5	RDENA	read enable. 0x0: Disable Read path on the GPIO 0x1: Enable Read path on the GPIO	1	rw	0x0
F4	PDENA	pulldown enable. 0x0: Disable 100K Ohm Pull Down 0x1: Enable 100K Ohm Pull Down	1	rw	0x0
F3	PUENA	pullup enable (active-low). 0x0: Enable 100K Ohm Pull Up 0x1: Disable 100K Ohm Pull Up	1	rw	0x1
F0	HWMODE	hardware mode. 0x0: GPA[0] Mode. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is controlled by GPIO Barium via the direction bit. Read Enable, Pull-Up, and Pull-Down are controlled by GPIO register in IOCTRLA. 0x1: PWM[0] Mode. 'PWM Barium' writes data to the GPIO. 0x2: Testmux Mode. 'Digital Testmux' writes data to the GPIO. DEBUG Access must be enabled in the system control block to allow testmux outputs. 0x5: Output of LINS 3rd Stage Glitch Filter.	3	rw	0x0

7.14.2 GPIO2

0x50012004 **GPIO2**

GPIO Pin 2 Control. GPIO Pin 2 has five seperate drivers: GPIO Controller, PWM Controller ,Testmux and SPI_SS.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F9	F8	F7	F6	F5	F4	F3	F0		

#	Field Name	Field Description	Width	Access	Reset
F9	PDVR1	GPIO output drive strength MSB selector. GPIO output drive strength MSB selector. PDRV1 | PDRV0 | Output drive strength	1	rw	0x1

		0 0 4mA 0 1 8mA 1 0 12mA 1 1 16mA			
F8	PDVR0	GPIO output drive strength LSB selector. GPIO output drive strength LSB selector.	1	rw	0x0
F7	CS	input schmitt trigger enable. 0x0: Disable schmitt trigger 0x1: Enable schmitt trigger.	1	rw	0x1
F6	SL	slewrate ctrl. 0x0: Fast Slewrate on the GPIO 0x1: Slow Slewrate on the GPIO	1	rw	0x0
F5	RDENA	read enable. 0x0: Disable Read path on the GPIO 0x1: Enable Read path on the GPIO	1	rw	0x0
F4	PDENA	pulldown enable. 0x0: Disable 100K Ohm Pull Down 0x1: Enable 100K Ohm Pull Down	1	rw	0x0
F3	PUENA	pullup enable (active-low). 0x0: Enable 100K Ohm Pull Up 0x1: Disable 100K Ohm Pull Up	1	rw	0x1
F0	HWMODE	hardware mode. 0x0: GPA[1] Mode. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is controlled by GPIO Barium via the direction bit. Read Enable, Pull-Up, and Pull-Down are controlled by GPIO register in IOCTRLA. 0x1: PWM[1] Mode. 'PWM Barium' writes data to the GPIO. 0x2: Testmux Mode. GPIO input connects to LINS PHY TXD. DEBUG Access must be enabled in the system control block to allow testmux outputs. 0x4: SPI Master Slave Select. 0x5: bor_3v3_n, BOR 3V3 reset. 0x6: bor_1v5_n, BOR 1V5 reset. 0x7: Input of LINS 1st Stage Glitch Filter.	3	rw	0x0

7.14.3 GPIO3

0x50012008 **GPIO3**

GPIO Pin 3 Control. GPIO Pin 3 has six seperate drivers: GPIO Controller, PWM Controller , Testmux , LINS_RXD and SPI_SCK.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F9	F8	F7	F6	F5	F4	F3	F0		

#	Field Name	Field Description	Width	Access	Reset
F9	PDVR1	GPIO output drive strength MSB selector. GPIO output drive strength MSB selector. PDRV1 PDRV0 Output drive strength 0 0 4mA 0 1 8mA 1 0 12mA 1 1 16mA	1	rw	0x1
F8	PDVR0	GPIO output drive strength LSB selector. GPIO output drive strength LSB selector.	1	rw	0x0
F7	CS	input schmitt trigger enable. 0x0: Disable schmitt trigger 0x1: Enable schmitt trigger.	1	rw	0x1
F6	SL	slewrate ctrl. 0x0: Fast Slewrate on the GPIO 0x1: Slow Slewrate on the GPIO	1	rw	0x0
F5	RDENA	read enable. 0x0: Disable Read path on the GPIO 0x1: Enable Read path on the GPIO	1	rw	0x0
F4	PDENA	pulldown enable. 0x0: Disable 100K Ohm Pull Down 0x1: Enable 100K Ohm Pull Down	1	rw	0x0

F3	PUENA	pullup enable (active-low). 0x0: Enable 100K Ohm Pull Up 0x1: Disable 100K Ohm Pull Up	1	rw	0x1
F0	HWMODE	hardware mode. 0x0: GPA[2] Mode. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is controlled by GPIO Barium via the direction bit. Read Enable, Pull-Up, and Pull-Down are controlled by GPIO register in IOCTRLA. 0x1: PWM[2] Mode. 'PWM Barium' writes data to the GPIO. 0x3: LINS controller RXD Input from GPIO(External PHY). 0x4: LINS Single wire mode, LINS PHY RXD/LINS PHY TXD, Open-drain output. 0x5: SPI Master Clock Out. 0x6: Output of LINS 1st Stage Glitch Filter.	3	rw	0x0

7.14.4 GPIO4

0x5001200C **GPIO4**

GPIO Pin 4 Control. GPIO Pin 4 has five seperate drivers: GPIO Controller, PWM Controller ,UART_RXD_IN ,LINS_TXD and SPI_MOSI.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F9	F8	F7	F6	F5	F4	F3	F0		

#	Field Name	Field Description	Width	Access	Reset
F9	PDVR1	GPIO output drive strength MSB selector. GPIO output drive strength MSB selector. PDRV1 / PDRV0 / Output drive strength: 0 / 0 / 4mA 0 / 1 / 8mA 1 / 0 / 12mA 1 / 1 / 16mA	1	rw	0x1
F8	PDVR0	GPIO output drive strength LSB selector. GPIO output drive strength LSB selector.	1	rw	0x0
F7	CS	input schmitt trigger enable. 0x0: Disable schmitt trigger 0x1: Enable schmitt trigger.	1	rw	0x1
F6	SL	slewrate ctrl. 0x0: Fast Slewrate on the GPIO 0x1: Slow Slewrate on the GPIO	1	rw	0x0
F5	RDENA	read enable. 0x0: Disable Read path on the GPIO 0x1: Enable Read path on the GPIO	1	rw	0x0
F4	PDENA	pulldown enable. 0x0: Disable 100K Ohm Pull Down 0x1: Enable 100K Ohm Pull Down	1	rw	0x0
F3	PUENA	pullup enable (active-low). 0x0: Enable 100K Ohm Pull Up 0x1: Disable 100K Ohm Pull Up	1	rw	0x1
F0	HWMODE	hardware mode. 0x0: GPA[3] Mode. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is controlled by GPIO Barium via the direction bit. Read Enable, Pull-Up, and Pull-Down are controlled by GPIO register in IOCTRLA. 0x1: PWM[3] Mode. 'PWM Barium' writes data to the GPIO. 0x2: UART RXD Input from GPIO 0x3: UART Single Wire Mode 0x4: SPI Master MOSI 0x6: Output of LINS 2nd Stage Glitch Filter.	3	rw	0x0

7.14.5 GPIO5

0x50012010 **GPIO5**

GPIO Pin 5 Control. GPIO Pin 5 has five seperate drivers: GPIO Controller, PWM Controller ,UART_TXD_OUT , LINS_TXD and SPI MISO.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F10	F9	F8	F7	F6	F5	F4	F3	F0		

#	Field Name	Field Description	Width	Access	Reset

F10	UART_TXD_IDLE_DIR	Control the direction of PAD for UART TXD Idle. 0x0: Hold the UART TXD Pad to output when TXD is idle, 0x1: Switch the TXD Pad to input When TXD is idle.	1	rw	0x0
F9	PDVR1	GPIO output drive strength MSB selector. GPIO output drive strength MSB selector. PDRV1 / PDRV0 / Output drive strength 0 / 0 / 4mA 0 / 1 / 8mA 1 / 0 / 12mA 1 / 1 / 16mA	1	rw	0x1
F8	PDVR0	GPIO output drive strength LSB selector. GPIO output drive strength LSB selector.	1	rw	0x0
F7	CS	input schmitt trigger enable. 0x0: Disable schmitt trigger 0x1: Enable schmitt trigger.	1	rw	0x1
F6	SL	slewrate ctrl. 0x0: Fast Slewrate on the GPIO 0x1: Slow Slewrate on the GPIO	1	rw	0x0
F5	RDENA	read enable. 0x0: Disable Read path on the GPIO 0x1: Enable Read path on the GPIO	1	rw	0x0
F4	PDENA	pulldown enable. 0x0: Disable 100K Ohm Pull Down 0x1: Enable 100K Ohm Pull Down	1	rw	0x0
F3	PUENA	pullup enable (active-low). 0x0: Enable 100K Ohm Pull Up 0x1: Disable 100K Ohm Pull Up	1	rw	0x1
F0	HWMODE	hardware mode. 0x0: GPA[4] Mode. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is controlled by GPIO Barium via the direction bit. Read Enable, Pull-Up, and Pull-Down are controlled by GPIO register in IOCTRLA. 0x1: PWM[4] Mode. 'PWM Barium' writes data to the GPIO. 0x2: UART TXD Output to GPIO 0x3: LINS PHY TXD Output to GPIO. 0x4: SPI Master MISO. 0x6: Output of LINS 1st Stage Glitch Filter.	3	rw	0x0

7.14.6 GPIO6

0x50012014 **GPIO6**

GPIO Pin 6 Control. GPIO Pin 6 has five seperate drivers: GPIO Controller, PWM Controller ,Testmux and SPI_SS.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F10	F9	F8	F7	F6	F5	F4	F3	F0		

#	Field Name	Field Description	Width	Access	Reset
F10	UART_RXO_SW	UART RX output Switch. 0x0: Bypass UART RXD 0x1: Force UART RXD output to Reset Value-'1'	1	rw	0x0
F9	PDVR1	GPIO output drive strength MSB selector. GPIO output drive strength MSB selector. PDRV1 / PDRV0 / Output drive strength 0 / 0 / 4mA 0 / 1 / 8mA 1 / 0 / 12mA 1 / 1 / 16mA	1	rw	0x1
F8	PDVR0	GPIO output drive strength LSB selector. GPIO output drive strength LSB selector.	1	rw	0x0
F7	CS	input schmitt trigger enable. 0x0: Disable schmitt trigger 0x1: Enable schmitt trigger.	1	rw	0x1
F6	SL	slewrate ctrl. 0x0: Fast Slewrate on the GPIO 0x1: Slow Slewrate on the GPIO	1	rw	0x0

F5	RDENA	read enable. 0x0: Disable Read path on the GPIO 0x1: Enable Read path on the GPIO	1	rw	0x0
F4	PDENA	pulldown enable. 0x0: Disable 100K Ohm Pull Down 0x1: Enable 100K Ohm Pull Down	1	rw	0x0
F3	PUENA	pullup enable (active-low). 0x0: Enable 100K Ohm Pull Up 0x1: Disable 100K Ohm Pull Up	1	rw	0x1
F0	HWMODE	hardware mode. 0x0: GPA[5] Mode. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is controlled by GPIO Barium via the direction bit. Read Enable, Pull-Up, and Pull-Down are controlled by GPIO register in IOCTRLA. 0x1: PWM[1] Mode. 'PWM Barium' writes data to the GPIO. 0x2: Testmux Mode. Output of LINS 3rd Stage Glitch Filter. 0x4: SPI Master MISO. 0x5: UART RXD Output to GPIO. 0x6: Output of LINS 2nd Stage Glitch Filter.	3	rw	0x0

7.14.7 GPIO7

0x50012018 **GPIO7**

GPIO Pin 7 Control. GPIO Pin 7 has six seperate drivers: GPIO Controller, PWM Controller , Testmux , LINS_RXD and SPI_SCK.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F9	F8	F7	F6	F5	F4	F3	F0		

#	Field Name	Field Description	Width	Access	Reset
F9	PDVR1	GPIO output drive strength MSB selector. GPIO output drive strength MSB selector. PDRV1 / PDRV0 / Output drive strength: 0 / 0 / 4mA 0 / 1 / 8mA 1 / 0 / 12mA 1 / 1 / 16mA	1	rw	0x1
F8	PDVR0	GPIO output drive strength LSB selector. GPIO output drive strength LSB selector.	1	rw	0x0
F7	CS	input schmitt trigger enable. 0x0: Disable schmitt trigger 0x1: Enable schmitt trigger.	1	rw	0x1
F6	SL	slewrate ctrl. 0x0: Fast Slewrate on the GPIO 0x1: Slow Slewrate on the GPIO	1	rw	0x0
F5	RDENA	read enable. 0x0: Disable Read path on the GPIO 0x1: Enable Read path on the GPIO	1	rw	0x0
F4	PDENA	pulldown enable. 0x0: Disable 100K Ohm Pull Down 0x1: Enable 100K Ohm Pull Down	1	rw	0x0
F3	PUENA	pullup enable (active-low). 0x0: Enable 100K Ohm Pull Up 0x1: Disable 100K Ohm Pull Up	1	rw	0x1
F0	HWMODE	hardware mode. 0x0: GPA[6] Mode. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is controlled by GPIO Barium via the direction bit. Read Enable, Pull-Up, and Pull-Down are controlled by GPIO register in IOCTRLA. 0x1: PWM[2] Mode. 'PWM Barium' writes data to the GPIO. 0x3: LINS RXD Input from GPIO(External PHY). 0x4: LINS Single wire mode, LINS PHY RXD/LINS PHY TXD, Open-drain output. 0x5: SPI Master Clock Out. 0x6: UART TXD Input from GPIO.	3	rw	0x0

7.14.8 GPIO8

0x5001201C	GPIO8

GPIO Pin 8 Control. GPIO Pin 8 has five seperate drivers: GPIO Controller, PWM Controller ,UART_RXD_IN ,LINS_TXD and SPI_MOSI.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F9	F8	F7	F6	F5	F4	F3	F0		

#	Field Name	Field Description	Width	Access	Reset
F9	PDVR1	GPIO output drive strength MSB selector. GPIO output drive strength MSB selector. PDRV1 / PDRV0 / Output drive strength 0 / 0 / 4mA 0 / 1 / 8mA 1 / 0 / 12mA 1 / 1 / 16mA	1	rw	0x1
F8	PDVR0	GPIO output drive strength LSB selector. GPIO output drive strength LSB selector.	1	rw	0x0
F7	CS	input schmitt trigger enable. 0x0: Disable schmitt trigger 0x1: Enable schmitt trigger.	1	rw	0x1
F6	SL	slewrate ctrl. 0x0: Fast Slewrate on the GPIO 0x1: Slow Slewrate on the GPIO	1	rw	0x0
F5	RDENA	read enable. 0x0: Disable Read path on the GPIO 0x1: Enable Read path on the GPIO	1	rw	0x0
F4	PDENA	pulldown enable. 0x0: Disable 100K Ohm Pull Down 0x1: Enable 100K Ohm Pull Down	1	rw	0x0
F3	PUENA	pullup enable (active-low). 0x0: Enable 100K Ohm Pull Up 0x1: Disable 100K Ohm Pull Up	1	rw	0x1
F0	HWMODE	hardware mode. 0x0: GPA[7] Mode. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is controlled by GPIO Barium via the direction bit. Read Enable, Pull-Up, and Pull-Down are controlled by GPIO register in IOCTRLA. 0x1: PWM[3] Mode. 'PWM Barium' writes data to the GPIO. 0x2: UART RXD Input from GPIO 0x3: UART Single Wire Mode 0x4: SPI Master MOSI 0x5: Output of LINS 2nd Stage Glitch Filter.	3	rw	0x0

7.14.9 LIN

0x50012024	LIN

LIN Pin Control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	F25	-	-	-	-	-	-	-	-	-	-	-	F13	-	-	-	-	F8	-	-	F5	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F25	PMODE	LIN Power Mode. Control LINS power state in hibernate mode. 0x0: Regardless of the related enable bits, LIN TX analog parts will be shut-down in hibernate mode, unless any LIN dominant signal is detected. 0x1: LIN TX analog parts are still controlled by theirs corresponding enable bits.	1	rw	0x0
F5	LINS_TXENA	LIN transmit enable.	1	rw	0x0
F0	LINS_HWMODE	LIN Slave hardware mode. 0x0: Hardware Mode Disabled. GPIO Barium Peripheral GPB[1] writes/reads the LIN I/O pin. 0x1: Hardware Mode Enabled. LIN peripheral writes/reads the LIN I/O pin.	1	rw	0x0

7.14.10 LINSGFCONF

0x50012028	LINSGFCONF

LINS Glitch Filter Configuration in active mode.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

-	-	-	-	-	-	-	-	-	F16	-	F8	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F16	LINS_DBNC_THRES1_1ST	1st Stage LINS Debounce Threshold for 0 to 1. 1st Stage LINS Debounce Threshold for 0 to 1, detect '1' width of (T_clksys*resetvalue = 62.5ns*0 = 0[us].	7	rw	0x0
F8	LINS_DBNC_THRES0_1ST	1st Stage LINS Debounce Threshold for 1 to 0. 1st Stage LINS Debounce Threshold for 1 to 0, detect '0' width of (T_clksys*resetvalue = 62.5ns*8 = 0.5[us].	7	rw	0x8
F0	LINS_RX_GF_ENA	LINS RXD Glitch Filter enables. bit-0: Enable LINS Glitch Filter 1st stage; bit-1: Enable LINS Glitch Filter 2nd stage; bit-2: Enable LINS Glitch Filter 3rd stage; bit-3: Enable LINS Glitch Filter for Sleep Mode NOTE: The write operation of this register takes effect by configuring SYSCTRLA_SFRS->TRIM_ACCESS_KEY.TRIM_ACCESS_KEY, FILT_ACCESS.FILT_UNLOCK	4	rw	0xF

7.14.11 LINSGFCONF1

0x5001202C **LINSGFCONF1**

LINS Glitch Filter Configuration in active mode.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	F24							-	F16							-	F8							-	F0						

#	Field Name	Field Description	Width	Access	Reset
F24	LINS_DBNC_THRES1_3RD	3rd Stage LINS Debounce Threshold for 0 to 1. 3rd Stage LINS Debounce Threshold for 0 to 1, detect '1' width of (T_clksys*resetvalue = 62.5ns*40 = 2.5[us].	7	rw	0x28
F16	LINS_DBNC_THRES0_3RD	3rd Stage LINS Debounce Threshold for 1 to 0. 3rd Stage LINS Debounce Threshold for 1 to 0, detect '0' width of (T_clksys*resetvalue = 62.5ns*40 = 2.5[us].	7	rw	0x28
F8	LINS_DBNC_THRES1_2ND	2nd Stage LINS Debounce Threshold for 0 to 1. 2nd Stage LINS Debounce Threshold for 0 to 1, detect '1' width of (T_clksys*resetvalue = 62.5ns*32 = 2[us].	7	rw	0x20
F0	LINS_DBNC_THRES0_2ND	2nd Stage LINS Debounce Threshold for 1 to 0. 2nd Stage LINS Debounce Threshold for 1 to 0, detect '0' width of (T_clksys*resetvalue = 62.5ns*16 = 1[us].	7	rw	0x10

7.14.12 LINTXDMONITOR

0x50012038 **LINTXDMONITOR**

LIN TXD Dominant Timeout.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F9	F8	-	-	-	-	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F8	LINSTXDTIMEOUTDOMINANT	Tx Dominant Timeout. The bit is set by LINS TxD monitor if LINS's TxD is stuck at dominant output for 64ms. A dominant to recessive transition of the TxD will clear this bit. LIN's TX will be disabled automatically when this bit is set.	1	ro	0x0
F0	LINSTXDMONITORENA	LINS TxD Monitor enable.	1	rw	0x1

7.14.13 LEDPIN

0x5001203C **LEDPIN**

LED Pin Control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F24	F22		-	-	-	F17		F16	F15	-	-	-	F9			F8	-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F24	BUCK_OUT_PORN_STS	BUCK ouput volatage POR flag. 0: BUCKOUT < 2.1V(typ) 1: BUCKOUT > 2.3V	1	ro	0x0
F22	OP_GBW_SEL	LED SENSE OP GBW SEL. PN detect fully differential Op GBW choose 00: 3M	2	rw	0x3

		01: 5M 10: 8M 11: 10M			
F17	PN_OP_START_BIAS_BOOST	PN OP START BIAS BOOST. PN diff OP start bias current 00: 1uA 01: 2uA 10: 3uA 11: 4uA	2	rw	0x0
F16	GAIN_SEL	LED Sense AFE gain select. V_ADC = (vbat-vled)*GAIN , where V_ADC is voltage to ADC LED channle, and GAIN is selected by GAIN_SEL as following: 0x0: GAIN = 2/5 0x1: GAIN = 1/5	1	rw	0x0
F15	VFW_ENA	LED Forward Voltage Current Enable. Set to enable the independent LED VFW current source(maximum=5mA). When ADC CH2 measurement is active, the LED channel selected by CH2_SEL will be driven by LED_VFW current source.	1	rw	0x0
F9	SENSE_CTRL	LED. LED Sense Control bits for override control/debug.	3	rw	0x0
F8	SENSE_ENA	LED Forward Voltage Sense Enable. Set to enable LED forward voltage sense module. After setting this bit, it's recommended to wait ~40us before ADC conversion for LED_SENSE to settle down.	1	rw	0x0

7.14.14 LEDHWMODE

0x50012040	LEDHWMODE			
LED HW mode.				
31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0		
- - - - - - - -	F0			
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	HWMODE	LED hardware mode. LED Hardware Mode Enable. Each bit controls the corresponding LED Channel respectively. 0x0: Hardware Mode Disabled. LED_DATA register drives the LED Data Output pin. Read is not available on this pin. 0x1: Hardware Mode Enabled. PWM_BARIUM peripheral drives the LED Data Output pin. Read is not available on this pin.	24	rw	0x0

7.14.15 LEDDATA

0x50012044	LEDDATA			
LED Data Out.				
31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0		
- - - - - - - -	F0			
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	LEDDATA	LED Data Out. When the LED hardware mode is disabled, then the data in this register bit is used to drive the LED driver. Each bit controls the corresonding LED Channel respectively.	24	rw	0x0

7.14.16 LEDPUENA

0x50012048	LEDPUENA			
LED Data Out.				
31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0		
- - - - - - - -	F0			
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	LEDPUENA	LED Pullup Enable. Set to enable LED Pullup when no LED current source is connected.	24	rw	0x0

7.14.17 ANALOGTESTMUXOVERRIDE1

0x5001204C	ANALOGTESTMUXOVERRIDE1
Analog Testmux Override 1.	

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	F24					F20				F8												-	-	-	-	-	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F24	ADC_LED_REG	Select which channel of LED forward voltage to ADC by firmware. Control which LED channel is selected when the ADC_CON_SEL/ADC_CON_REG[11] are set.	5	rw	0x0
F20	ADC_GPIO_REG	Select which GPIO forward voltage to ADC by firmware. Control which GPIO channel is selected when the ADC_CON_SEL/ADC_CON_REG[9] are set. 0x0: Select GPIO6 0x1: Select GPIO7 0x2: Select GPIO8 0x3: Select GPIO1 0x4: Select GPIO2 0x5: Select GPIO3 0x6: Select GPIO4 0x7: Select GPIO5	4	rw	0x0
F8	ADC_CON_REG	Firmware Debug Value. Contains the output value when the ADC_CON_SEL firmware select bit is set. 0x1: Select All shot to adc_ref(2.4V) for adc channel offset K 0x2: Select adc_vinp= adc_refp, adc_vinn= vref_gnd 0x4: Select adc_vinp= vref_gnd, adc_vinn= adc_refp 0x8: Select GPIO6(adc_vinp)/GPIO7(adc_vinn) to ADC 0x10: Select Tempsensor to ADC 0x20: Select VDD1.5v to ADC 0x40: Select VDD3.3v to ADC 0x80: Select VDD5.0v(1/4) to ADC 0x100: Select Accurate VBAT to ADC 0x200: Select GPIO1~9(determined by CH4_SEL in ADC_CTRL) to ADC 0x400: Select BUCK 5V(1/4) to ADC 0x800: Select LED0~23 Forward Voltage to ADC	12	rw	0x0
F2	ADC_SEL_SEL	Hardware/Firmware Select NOTE:The write operation of this field register takes effect by configuring 'SYSCTRLA_SFRS->DEBUG_ACCESS_KEY.DEBUG_ACCESS_KEY = 0x05'. 0x0: Hardware Controlled. 0x1: ADC_SEL_REG controls output.	1	rw	0x0
F1	GPIO_CON_SEL	Hardware/Firmware Select NOTE:The write operation of this field register takes effect by configuring 'SYSCTRLA_SFRS->DEBUG_ACCESS_KEY.DEBUG_ACCESS_KEY = 0x05'. 0x0: Hardware Controlled. 0x1: GPIO_CON_REG controls output.	1	rw	0x0
F0	ADC_CON_SEL	Hardware/Firmware Select NOTE:The write operation of this field register takes effect by configuring 'SYSCTRLA_SFRS->DEBUG_ACCESS_KEY.DEBUG_ACCESS_KEY = 0x05'. 0x0: Hardware Controlled. 0x1: ADC_CON_REG controls output.	1	rw	0x0

7.14.18 ANALOGTESTMUXOVERRIDE2

0x50012050 **ANALOGTESTMUXOVERRIDE2**

Analog Testmux Override 2.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	F0						

#	Field Name	Field Description	Width	Access	Reset
F16	ADCSELREG	Firmware Debug Value. Need to be configured with gpio_con_reg to enable gpio analog output to ADC. 0x1: Enable GPIO1 analog connection 0x2: Enable GPIO2 analog connection 0x4: Enable GPIO3 analog connection 0x8: Enable GPIO4 analog connection 0x10: Enable GPIO5 analog connection 0x20: Enable GPIO6 analog connection 0x40: Enable GPIO7 analog connection 0x80: Enable GPIO8 analog connection	9	rw	0x0
F0	GPIOCONREG	Firmware Debug Value. GPIO1~8 test MUX select. ADC_SEL_SEL/ADC_SEL_REG need to be configured at the same time to enable required GPIO connection. 0x1: Select VDD 3.3V digital supply to GPIO6, mutually exclusive with	7	rw	0x0

		HVBUCK_ATB01. 0x2: Select 1.5v MCU supply to GPIO6, mutually exclusive with HVBUCK_ATB01. 0x4: Select VDD_PRE5V/4 to GPIO6, mutually exclusive with HVBUCK_ATB01. 0x8: Select BUCK_5V/4 to GPIO6, mutually exclusive with HVBUCK_ATB01. 0x10: Select ADC_REFP to GPIO7, mutually exclusive with HVBUCK_ATB02 and PMU_ATB. 0x20: Select ADC_INP to GPIO7, mutually exclusive with HVBUCK_ATB02 and PMU_ATB. 0x40: Select ADC_INN to GPIO8, mutually exclusive with PMU_ATB1, mutually exclusive with lin_ibg1up_tp.			

7.14.19 ANALOGTESTMUXOVERRIDE3

0x50012054 **ANALOGTESTMUXOVERRIDE3**

Analog Testmux Override 3.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	F0																							

#	Field Name	Field Description	Width	Access	Reset
F0	LEDSEL	LED test analog channel select, one hot code NOTE:exclusive with DFT_MODE_ENA_LED.	24	rw	0x0

7.14.20 IRQ

0x50012058 **IRQ**

IOCTRLA LINS TXD Dominant Monitor interrupts. Contains the the enable, clear, status and active flag for the LINS TXD Dominant Monitor interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	F25	F24	-	-	-	-	-	-	F17	F16	-	-	-	-	-	-	F9	F8	-	-	-	-	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F24	LINS_TXD_DOM	LINS TXD Dominant Monitor interrupt active.	1	ro	0x0
F16	LINS_TXD_DOM	LINS TXD Dominant Monitor interrupt status.	1	ro	0x0
F8	LINS_TXD_DOM	LINS TXD Dominant Monitor interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F0	LINS_TXD_DOM	LINS TXD Dominant Monitor interrupt enable.	1	rw	0x0

7.14.21 FILT_ACCESS

0x5001205C **FILT_ACCESS**

Glitch Filter access key.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F31	FILT_UNLOCK	Set Only bit. Write 1 to this bit to un-lock FILT_CODE bits.	1	rw	0x0

7.14.22 MCU_INF_CONF

0x50012060 **MCU_INF_CONF**

Mcu interface access config.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F12		F10		F8		-	-	-	-	-	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F12	MCU_DATA_PDRV	mcu data drive strength control: 0-4mA 1-8mA 2-12mA 3-16mA	2	rw	0x1
F10	MCU_INT_PDRV	mcu int drive strength control: 0-4mA 1-8mA 2-12mA 3-16mA	2	rw	0x1
F8	MCU_CLK_PDRV	mcu clock drive strength control: 0-4mA 1-8mA 2-12mA 3-16mA	2	rw	0x1
F2	MCU_DATA_SL	mcu data slew rate control: 0-fast 1-slow	1	rw	0x0
F1	MCU_INT_SL	mcu int slew rate control: 0-fast 1-slow	1	rw	0x0

F0	MCU_CLK_SL	mcu clock slew rate control: 0-fast 1-slow	1	rw	0x0

7.15 SYSCTRLA

SYSCTRLA		
Address	**Register**	**Description**
0x50013000	RETAIN1	Retained data 1
0x50013004	DEBUG_ACCESS_KEY	Debug access key
0x50013008	DEBUG_ACCESS_ENABLED	Debug access enabled
0x5001300C	TRIM_ACCESS_KEY	Trim access key
0x50013010	TRIM_ACCESS_ENABLED	Trim access enabled
0x50013014	PMU_ACCESS_KEY	PMU configure access key
0x50013018	PMU_ACCESS_ENABLED	PMU configure access enabled
0x5001301C	HF_OSC_TRIM	Trim controls for the high frequency (16MHz) oscillator
0x50013020	BIAS	Bias Control
0x50013024	TRIMLED0	High Voltage LED trim
0x50013028	TRIMLED1	High Voltage LED trim
0x5001302C	TRIMLED2	High Voltage LED trim
0x50013030	TRIMLED3	High Voltage LED trim
0x50013034	TRIMLED4	High Voltage LED trim
0x50013038	TRIMLED5	High Voltage LED trim
0x5001303C	TRIMLED6	High Voltage LED trim
0x50013040	TRIMLED7	High Voltage LED trim
0x50013044	TRIMLED8	High Voltage LED trim
0x50013048	TRIMLED9	High Voltage LED trim
0x5001304C	TRIMLED10	High Voltage LED trim
0x50013050	TRIMLED11	High Voltage LED trim
0x50013054	TRIMLED12	High Voltage LED trim
0x50013058	TRIMLED13	High Voltage LED trim
0x5001305C	TRIMLED14	High Voltage LED trim
0x50013060	TRIMLED15	High Voltage LED trim
0x50013064	TRIMLED16	High Voltage LED trim
0x50013068	TRIMLED17	High Voltage LED trim
0x5001306C	TRIMLED18	High Voltage LED trim
0x50013070	TRIMLED19	High Voltage LED trim
0x50013074	TRIMLED20	High Voltage LED trim
0x50013078	TRIMLED21	High Voltage LED trim
0x5001307C	TRIMLED22	High Voltage LED trim
0x50013080	TRIMLED23	High Voltage LED trim
0x50013084	TRIMVFW	VFW Current Trim
0x50013088	NAME	ASIC name
0x5001308C	REV	Silicon Revision
0x50013090	TESTMODE	Testmode Enable

7.15.1 RETAIN1

0x50013000 **RETAIN1**

Retained data 1.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	RETAIN1	Firmware scratch register 1 (0x1). Contents retained in Hibernate mode - but lost after any hard or soft reset.	8	rw	0x0

7.15.2 DEBUG_ACCESS_KEY

0x50013004	DEBUG_ACCESS_KEY																													
Debug access key.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		
#	Field Name							Field Description																Width		Access			Reset		
F31	DEBUG_LOCK							Set Only bit. Set this bit to lock DEBUG_CODE bits.																1		rw			0x0		
F0	DEBUG_ACCESS_KEY							Write the value 0x5 to this register to enable debug options. Write any other value to disable the debug options.																4		rw			0x0		

7.15.3 DEBUG_ACCESS_ENABLED

0x50013008	DEBUG_ACCESS_ENABLED																													
Debug access enabled.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0
#	Field Name							Field Description																Width		Access			Reset		
F0	DEBUG_ACCESS_ENABLED							A status flag that is set when debug access is enabled																1		ro			0x0		

7.15.4 TRIM_ACCESS_KEY

0x5001300C	TRIM_ACCESS_KEY																													
Trim access key.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		
#	Field Name							Field Description																Width		Access			Reset		
F31	TRIM_LOCK							Set Only bit. Write 1 to this bit to lock TRIM_CODE bits.																1		rw			0x0		
F0	TRIM_ACCESS_KEY							Write the value 0xe to this register to enable 'trim access' (which allows write access to various trim settings and production test options). Write any other value to disable trim access.																4		rw			0x0		

7.15.5 TRIM_ACCESS_ENABLED

0x50013010	TRIM_ACCESS_ENABLED																													
Trim access enabled.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0
#	Field Name							Field Description																Width		Access			Reset		
F0	TRIM_ACCESS_ENABLED							A status flag that is set when trim access is enabled																1		ro			0x0		

7.15.6 PMU_ACCESS_KEY

0x50013014	PMU_ACCESS_KEY																													
PMU configure access key.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		
#	Field Name							Field Description																Width		Access			Reset		
F31	PMU_LOCK							Set Only bit. Set this bit to lock PMU_CODE bits.																1		rw			0x0		
F0	PMU_ACCESS_KEY							Write the value 0xA to this register to enable 1v5 domain at hibernate. Write any other value to disable the 1v5 domain at hibernate.																4		rw			0x0		

7.15.7 PMU_ACCESS_ENABLED

0x50013018	PMU_ACCESS_ENABLED																													
PMU configure access enabled.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	PMU_ACCESS_ENABLED	A status flag that is set when pmu access is enabled	1	ro	0x0

7.15.8 HF_OSC_TRIM

0x5001301C **HF_OSC_TRIM**

Trim controls for the high frequency (16MHz) oscillator.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	F16								-	-	-	-	F9			F8	F0							

#	Field Name	Field Description	Width	Access	Reset
F16	SSCDIV	SSC Clock Divider. SSC Freq = SYS_FREQ/[(SSC_DIV+1)*(SSC_DEEP+1)*4].	8	rw	0x28
F9	SSCDEEP	SSC Depth Configuration.	3	rw	0x0
F8	SSCENA	SSC Enable.	1	rw	0x0
F0	TRIM_HF_RC	High Frequency RC Oscillator trim. TRIM bits will be changed if SSC is enabled. Reload the trim bits from Flash if SSC is disabled while the change has happened. Following value only used as a reference: 0xa: freq=26.08Mhz 0x80: freq=9.62Mhz 0xfa: freq=5.94Mhz	8	rw	0xA4

7.15.9 BIAS

0x50013020 **BIAS**

Bias Control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F4								-	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F4	LEDBIASTRIM	LED bias current trim. Each code is about 50nA step.	8	rw	0x80
F2	LEDBIASTRIMEN	LED bias trim eanble.	1	rw	0x0
F1	LEDBIASREG	High Voltage LED bias select register. If LED_BIAS_SEL is set, then LED_BIAS_REG allows override access to the LED BIAS signal.	1	rw	0x0
F0	LEDBIASSEL	High Voltage LED bias select. 0x0: The LED Bias is enabled and disabled by the pmu hardware state machine by default. 0x1: The value of the LED_BIAS_REG field is what is used to drive the LED_BIAS signal. (override mode)	1	rw	0x0

7.15.10 TRIMLED0

0x50013024 **TRIMLED0**

High Voltage LED trim.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F16	TRIM0	LED trim (100uA step).	9	rw	0x12C

7.15.11 TRIMLED1

0x50013028 **TRIMLED1**

High Voltage LED trim.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F16	TRIM1	LED trim (100uA step).	9	rw	0x12C

7.15.12 TRIMLED2

0x5001302C																TRIMLED2															
High Voltage LED trim.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
#	Field Name							Field Description																Width		Access			Reset		
F16	TRIM2							LED trim (100uA step).																9		rw			0x12C		

7.15.13 TRIMLED3

0x50013030																TRIMLED3															
High Voltage LED trim.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
#	Field Name							Field Description																Width		Access			Reset		
F16	TRIM3							LED trim (100uA step).																9		rw			0x12C		

7.15.14 TRIMLED4

0x50013034																TRIMLED4															
High Voltage LED trim.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
#	Field Name							Field Description																Width		Access			Reset		
F16	TRIM4							LED trim (100uA step).																9		rw			0x12C		

7.15.15 TRIMLED5

0x50013038																TRIMLED5															
High Voltage LED trim.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
#	Field Name							Field Description																Width		Access			Reset		
F16	TRIM5							LED trim (100uA step).																9		rw			0x12C		

7.15.16 TRIMLED6

0x5001303C																TRIMLED6															
High Voltage LED trim.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
#	Field Name							Field Description																Width		Access			Reset		
F16	TRIM6							LED trim (100uA step).																9		rw			0x12C		

7.15.17 TRIMLED7

0x50013040																TRIMLED7															
High Voltage LED trim.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
#	Field Name							Field Description																Width		Access			Reset		
F16	TRIM7							LED trim (100uA step).																9		rw			0x12C		

7.15.18 TRIMLED8

0x50013044	TRIMLED8

High Voltage LED trim.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F16	TRIM8	LED trim (100uA step).	9	rw	0x12C

7.15.19 TRIMLED9

0x50013048	TRIMLED9

High Voltage LED trim.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F16	TRIM9	LED trim (100uA step).	9	rw	0x12C

7.15.20 TRIMLED10

0x5001304C	TRIMLED10

High Voltage LED trim.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F16	TRIM10	LED trim (100uA step).	9	rw	0x12C

7.15.21 TRIMLED11

0x50013050	TRIMLED11

High Voltage LED trim.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F16	TRIM11	LED trim (100uA step).	9	rw	0x12C

7.15.22 TRIMLED12

0x50013054	TRIMLED12

High Voltage LED trim.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F16	TRIM12	LED trim (100uA step).	9	rw	0x12C

7.15.23 TRIMLED13

0x50013058	TRIMLED13

High Voltage LED trim.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F16	TRIM13	LED trim (100uA step).	9	rw	0x12C

7.15.24 TRIMLED14

0x5001305C	TRIMLED14

High Voltage LED trim.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

-	-	-	-	-	-	-	F16	-	-	-	-	-	-	-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F16	TRIM14	LED trim (100uA step).	9	rw	0x12C

7.15.25 TRIMLED15

0x50013060 **TRIMLED15**

High Voltage LED trim.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F16	TRIM15	LED trim (100uA step).	9	rw	0x12C

7.15.26 TRIMLED16

0x50013064 **TRIMLED16**

High Voltage LED trim.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F16	TRIM16	LED trim (100uA step).	9	rw	0x12C

7.15.27 TRIMLED17

0x50013068 **TRIMLED17**

High Voltage LED trim.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F16	TRIM17	LED trim (100uA step).	9	rw	0x12C

7.15.28 TRIMLED18

0x5001306C **TRIMLED18**

High Voltage LED trim.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F16	TRIM18	LED trim (100uA step).	9	rw	0x12C

7.15.29 TRIMLED19

0x50013070 **TRIMLED19**

High Voltage LED trim.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F16	TRIM19	LED trim (100uA step).	9	rw	0x12C

7.15.30 TRIMLED20

0x50013074 **TRIMLED20**

High Voltage LED trim.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset

F16	TRIM20	LED trim (100uA step).	9	rw	0x12C

7.15.31 TRIMLED21

0x50013078																TRIMLED21													
High Voltage LED trim.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
#	Field Name							Field Description																Width		Access			Reset		
F16	TRIM21							LED trim (100uA step).																9		rw			0x12C		

7.15.32 TRIMLED22

0x5001307C																TRIMLED22													
High Voltage LED trim.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
#	Field Name							Field Description																Width		Access			Reset		
F16	TRIM22							LED trim (100uA step).																9		rw			0x12C		

7.15.33 TRIMLED23

0x50013080																TRIMLED23													
High Voltage LED trim.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
#	Field Name							Field Description																Width		Access			Reset		
F16	TRIM23							LED trim (100uA step).																9		rw			0x12C		

7.15.34 TRIMVFW

0x50013084																TRIMVFW													
VFW Current Trim.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							
#	Field Name							Field Description																Width		Access			Reset		
F0	TRIMVFW							PN Forward Voltage Current trim (10uA step).																8		rw			0xC8		

7.15.35 NAME

0x50013088																NAME													
ASIC name.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																													
#	Field Name							Field Description																Width		Access			Reset		
F0	NAME							ASIC name. A read from this register will return the ASIC name																32		ro			N/A		

7.15.36 REV

0x5001308C																REV													
Silicon Revision.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															
#	Field Name							Field Description																Width		Access			Reset		
F0	REV							Silicon Revision. A read from this register will return the ASCII silicon revision (e.g. ASCII C0 is 0x4330)																16		ro			N/A		

7.15.37 TESTMODE

0x50013090	TESTMODE																													
Testmode Enable.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F9	DBG_VPRE_REG_ATB06	EN test VPRE_REG. MUX VPRE_REG to GPIO7	1	rw	0x0
F8	DBG_IBP_1U_ATB05	EN test IBP_1U. MUX IBP_1U(current) to GPIO7	1	rw	0x0
F7	DBG_VREF_1P2_BUF_ATB04	EN test VREF_1P2_BUF. MUX VREF_1P2_BUF to GPIO7	1	rw	0x0
F6	DBG_VBG_TEST_ATB03	EN test VBG_TEST. MUX VBG_TEST to GPIO7	1	rw	0x0
F5	DBG_ADC_TSP_ATB02	EN test ADC_TSP. Mux ADC_TSP to GPIO8.	1	rw	0x0
F4	DBG_ADC_TSN_ATB01	EN test ADC_TSN. Mux ADC_TSN to GPIO7.	1	rw	0x0
F3	BLANK_OT	blanking the OT signal when the OT channel changes.	1	rw	0x0
F2	EN_BG_HCOMP	Enable the comparator of over temperature function.	1	rw	0x0
F1	EN_COMPOT	Enable the comparator of over temperature function.	1	rw	0x0
F0	ENABORTESTMODE	BOR Testmode Enable. 0x0: BOR Testmode Disabled: Reference Voltage for BOR is from Band Gap (Functional Mode) 0x1: BOR Testmode Enabled: Reference Voltage for BOR is from GPIO7 (Test Mode)	1	rw	0x0

7.16 GPIO

GPIO		
Address	**Register**	**Description**
0x50014000	GPADATA	GPIO Port A Data
0x50014400	GPBDATA	GPIO Port B Data
0x50014800	GPENA	GPIO Port Enables
0x50014804	GPAP03	GPIO Port A Pin 0-3 Control
0x50014808	GPAP47	GPIO Port A Pin 4-7 Control
0x5001480C	GPBP02	GPIO Port B Pin 0-2 Control

7.16.1 GPADATA

0x50014000	GPADATA																													
GPIO Port A Data.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	GPADATA<1024>	Port A data. To aid in the efficiency of software, the GPIO ports allow for the modification of individual bits in the GPIO Data by using bits [9:2] of the address bus as a enable. In this manner, software drivers can modify individual GPIO pins in a single instruction without affecting the state of the other pins. This method is more efficient than the conventional method of performing a read-modify-write operation to set or clear an individual GPIO pin. To write all the bits at the same time use address offset of 0x07F.	8	dual	0x0

7.16.2 GPBDATA

0x50014400	GPBDATA																													
GPIO Port B Data.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	GPBDATA<1024>	Port B data.	3	dual	0x6

7.16.3 GPENA

0x50014800	GPENA																													
GPIO Port Enables.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F1	GPBENA	Enables the Clock-Gate, can be cleared to save power, if none of the GPIO functionality is required	1	rw	0x1
F0	GPAENA	Enables the Clock-Gate, can be cleared to save power, if none of the GPIO functionality is required	1	rw	0x1

7.16.4 GPAP03

0x50014804	GPAP03																													
GPIO Port A Pin 0-3 Control.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	F29	F28	F27	F26	F25	F24	-	-	F21	F20	F19	F18	F17	F16	-	-	F13	F12	F11	F10	F9	F8	-	-	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F29	GPAACTDET[3]	Pin 3 activity interrupt.	1	ro	N/A
F28	GPACLR[3]	Pin 3 interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F27	GPAFE[3]	Pin 3 falling edge enable.	1	rw	0x0
F26	GPARE[3]	Pin 3 rising edge enable.	1	rw	0x0
F25	GPAIE[3]	Pin 3 interrupt enable.	1	rw	0x0
F24	GPADIR[3]	Pin 3 output enable.	1	rw	0x0
F21	GPAACTDET[2]	Pin 2 activity interrupt.	1	ro	N/A
F20	GPACLR[2]	Pin 2 interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F19	GPAFE[2]	Pin 2 falling edge enable.	1	rw	0x0
F18	GPARE[2]	Pin 2 rising edge enable.	1	rw	0x0
F17	GPAIE[2]	Pin 2 interrupt enable.	1	rw	0x0
F16	GPADIR[2]	Pin 2 output enable.	1	rw	0x0
F13	GPAACTDET[1]	Pin 1 activity interrupt.	1	ro	N/A
F12	GPACLR[1]	Pin 1 interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F11	GPAFE[1]	Pin 1 falling edge enable.	1	rw	0x0
F10	GPARE[1]	Pin 1 rising edge enable.	1	rw	0x0
F9	GPAIE[1]	Pin 1 interrupt enable.	1	rw	0x0
F8	GPADIR[1]	Pin 1 output enable.	1	rw	0x0
F5	GPAACTDET[0]	Pin 0 activity interrupt.	1	ro	N/A
F4	GPACLR[0]	Pin 0 interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F3	GPAFE[0]	Pin 0 falling edge enable.	1	rw	0x0
F2	GPARE[0]	Pin 0 rising edge enable.	1	rw	0x0
F1	GPAIE[0]	Pin 0 interrupt enable.	1	rw	0x0
F0	GPADIR[0]	Pin 0 output enable.	1	rw	0x0

7.16.5 GPAP47

0x50014808	GPAP47

GPIO Port A Pin 4-7 Control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	F29	F28	F27	F26	F25	F24	-	-	F21	F20	F19	F18	F17	F16	-	-	F13	F12	F11	F10	F9	F8	-	-	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F29	GPAACTDET[7]	Pin 7 activity interrupt.	1	ro	N/A
F28	GPACLR[7]	Pin 7 interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F27	GPAFE[7]	Pin 7 falling edge enable.	1	rw	0x0
F26	GPARE[7]	Pin 7 rising edge enable.	1	rw	0x0
F25	GPAIE[7]	Pin 7 interrupt enable.	1	rw	0x0
F24	GPADIR[7]	Pin 7 output enable.	1	rw	0x0
F21	GPAACTDET[6]	Pin 6 activity interrupt.	1	ro	N/A
F20	GPACLR[6]	Pin 6 interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F19	GPAFE[6]	Pin 6 falling edge enable.	1	rw	0x0
F18	GPARE[6]	Pin 6 rising edge enable.	1	rw	0x0
F17	GPAIE[6]	Pin 6 interrupt enable.	1	rw	0x0
F16	GPADIR[6]	Pin 6 output enable.	1	rw	0x0
F13	GPAACTDET[5]	Pin 5 activity interrupt.	1	ro	N/A
F12	GPACLR[5]	Pin 5 interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F11	GPAFE[5]	Pin 5 falling edge enable.	1	rw	0x0
F10	GPARE[5]	Pin 5 rising edge enable.	1	rw	0x0
F9	GPAIE[5]	Pin 5 interrupt enable.	1	rw	0x0
F8	GPADIR[5]	Pin 5 output enable.	1	rw	0x0
F5	GPAACTDET[4]	Pin 4 activity interrupt.	1	ro	N/A
F4	GPACLR[4]	Pin 4 interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F3	GPAFE[4]	Pin 4 falling edge enable.	1	rw	0x0
F2	GPARE[4]	Pin 4 rising edge enable.	1	rw	0x0
F1	GPAIE[4]	Pin 4 interrupt enable.	1	rw	0x0
F0	GPADIR[4]	Pin 4 output enable.	1	rw	0x0

7.16.6 GPBP02

0x5001480C	GPBP02

GPIO Port B Pin 0-2 Control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	F21	F20	F19	F18	F17	F16	-	-	F13	F12	F11	F10	F9	F8	-	-	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F21	GPBACTDET[2]	Pin 2 activity interrupt.	1	ro	N/A
F20	GPBCLR[2]	Pin 2 interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F19	GPBFE[2]	Pin 2 falling edge enable.	1	rw	0x0
F18	GPBRE[2]	Pin 2 rising edge enable.	1	rw	0x0
F17	GPBIE[2]	Pin 2 interrupt enable.	1	rw	0x0
F16	GPBDIR[2]	Pin 2 output enable.	1	rw	0x0
F13	GPBACTDET[1]	Pin 1 activity interrupt.	1	ro	N/A

F12	GPBCLR[1]	Pin 1 interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F11	GPBFE[1]	Pin 1 falling edge enable.	1	rw	0x0
F10	GPBRE[1]	Pin 1 rising edge enable.	1	rw	0x0
F9	GPBIE[1]	Pin 1 interrupt enable.	1	rw	0x0
F8	GPBDIR[1]	Pin 1 output enable.	1	rw	0x0
F5	GPBACTDET[0]	Pin 0 activity interrupt.	1	ro	N/A
F4	GPBCLR[0]	Pin 0 interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F3	GPBFE[0]	Pin 0 falling edge enable.	1	rw	0x0
F2	GPBRE[0]	Pin 0 rising edge enable.	1	rw	0x0
F1	GPBIE[0]	Pin 0 interrupt enable.	1	rw	0x0
F0	GPBDIR[0]	Pin 0 output enable.	1	rw	0x0

7.17 PMUAPRE5V

PMUAPRE5V		
Address	**Register**	**Description**
0x50015000	RETAIN0	Retained data 0
0x50015004	CFG_ACCESS	5V domain's configuration regs access
0x50015008	LIN_SLEEP_GF	LINS Glitch Filter Configuration in active mode.
0x5001500C	LIN_WUP	LIN Wakeup Control,
0x50015010	LINS	LIN slave Pin Control.
0x50015018	CTRL	PMU Debug Control.
0x5001501C	BOR	BOR configuration
0x50015020	BORDEGLITCH	BOR Deglitch.
0x50015024	CLK_CTRL	Clock controls for 5V(always on) domain.
0x50015028	DFT	DFT

7.17.1 RETAIN0

0x50015000 **RETAIN0**

Retained data 0.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	RETAIN0	Firmware scratch register 0. Only reset at power-on (e.g contents retained in Hibernate mode and retained despite any hard or soft resets)	8	rw	0x0

7.17.2 CFG_ACCESS

0x50015004 **CFG_ACCESS**

5V domain's configuration regs access.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F4	F0			

#	Field Name	Field Description	Width	Access	Reset
F31	CFG_LOCK	Set Only bit. Write 1 to this bit to lock CFG_CODE bits.	1	rw	0x0
F4	CFG_ACCESS_ENABLED	A status flag that is set when 5V domain's configuration regs access is enabled	1	ro	0x0
F0	CFG_ACCESS_KEY	Write the value 0xB to this register to enable 'trim access' (which allows write access to various trim settings and production test options). Write any other value to disable trim access.	4	rw	0x0

7.17.3 LIN_SLEEP_GF

0x50015008	LIN_SLEEP_GF																													
LINS Glitch Filter Configuration in active mode. NOTE:The write operation of this field register takes effect by configuring 'PMUPRE5V_SFRS->CFG.CFG_ACCESS_KEY = 0xB'.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F28				F24				-	-	-	-	-	-	-	F16	F12				F8				-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F12	LINS_SLEEP_GF_THRES1	LINS RXD glitch filter threshold for 0 to 1, detect '1' width of (T_clk_lf*resetvalue = 4us*3 = 12[us]	4	rw	0x0
F8	LINS_SLEEP_GF_THRES0	LINS RXD glitch filter threshold for 1 to 0, detect '0' width of (T_clk_lf*resetvalue = 4us*3 = 12[us]	4	rw	0x1
F0	LINS_RXD_HIGH_RST_ENA	Enable signal that LINs RXD glitch filter at sleep mode is asynchronous reset by high of LINs_RXD.	1	rw	0x0

7.17.4 LIN_WUP

0x5001500C	LIN_WUP																													
LIN Wakeup Control, NOTE:The write operation of this field register takes effect by configuring 'PMUPRE5V_SFRS->CFG.CFG_ACCESS_KEY = 0xB'.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	F27	F26	F24		F18						-	-	-	-	-	-	F11	F10	F8		F2						-	-

#	Field Name	Field Description	Width	Access	Reset
F11	LINS_BUS_IDLE_TO_DOMN	Dominant Bus Idle Timeout. The bit is set by the lin core if LIN is in hardware mode & the bus is stuck at dominant inactivity state for 4s~10s. Any bus transition will clear this bit. LIN Slave's pullup will be disabled when it is set.	1	ro	0x0
F10	LINS_BUS_DOMN_RLS_WUP_ENA	LIN Slave Bus Dominant Release Wakeup Enable. Set to trigger lin wakeup if bus dominant condition is released after BUS_IDLE_TIMEOUT_DOMINANT is detected.	1	rw	0x0
F8	LINS_BUS_INACTIVE	LIN Slave Bus Inactivity Time. NOTE: When the chip uses the LINs bus idle detection in pre5v domain(PMU_SFRS->CTRL.PD1V5_ENA_HIBERNATE=0x0), the write operation of this register takes effect by IOCTRLA_SFRS->LIN.UPDATE	2	rw	0x0
F2	LINS_WUP_DETECT_THRES	LIN Slave Wakeup Detection Threshold. Threshold setting(LF_CLK_PREDIV clock cycls) of lin wakeup signal. For instace, if target threshold is 150us@LF_CLK_PREDIV=250KHz, WUP_DETECT_THRES = 150/(1000/250)-1. NOTE: When the chip uses the LINs wakeup logic in pre5v domain(PMU_SFRS->CTRL.PD1V5_ENA_HIBERNATE=0x0), the write operation of this register takes effect by IOCTRLA_SFRS->LIN.UPDATE	6	rw	0x24

7.17.5 LINS

0x50015010	LINS																													
LIN slave Pin Control. NOTE:The write operation of this field register takes effect by configuring 'PMUPRE5V_SFRS->CFG.CFG_ACCESS_KEY = 0xB'.																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	F24				-	-	-	-	F16				F13			F10			F8		-	F6	F5	F4	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F24	LIN_DBG	LIN DEBUG. one hot code 0001: select lin_tx_s_duty_ibg1up_tp to gpio2 analog channel 0010: select lin_tx_s_slope_ibg1up_tp to gpio2 analog channel 0100: select lin_tx_m_duty_ibg1up_tp to gpio2 analog channel 1000: select lin_tx_m_slope_ibg1up_tp to gpio2 analog channel	4	rw	0x0
F16	LIN_TX_S_SL	LIN Slave TX driver slew rate select. Slew from 40%*Vbat to 60%*Vbat @Vbat=13V,Cbus=1nF. 0000 -> 1110: 1.07V/us ~ 4.71V/us, step is about 0.26V/us 1111: about 10V/us for fast LIN mode	4	rw	0x4
F13	LIN_TX_S_DT	LIN Slave duty cycle adjust. 0x0: duty cycle = 0.488 0x1: duty cycle = 0.492 0x2: duty cycle = 0.494	3	rw	0x5

		0x3: duty cycle = 0.495 0x4: duty cycle = 0.497 0x5: duty cycle = 0.5 0x6: duty cycle = 0.507 0x7: duty cycle = 0.529			
F10	LINS_TX_BIAS_BOOST	LIN Slave IO TX Bias select. Select LIN IO TX Pull Down Current. 0x0: ~61 mA 0x1: ~83 mA 0x2: ~105 mA 0x3: ~126 mA	3	rw	0x4
F8	LINS_RX_BIAS_BOOST	adjust rise delay from LIN_IN to Input of LINS Controller. 0x0: 2.323 us 0x1: 1.344 us 0x2: 0.968 us 0x3: 0.767 us	2	rw	0x0
F6	LINS_PUOFF_TIMEOUT	LINS Pullup Disable in dominant TimeOut condition. Set to disable LINS 30K pullup in case that lin bus is shorted to ground(Bus idle dominant timeout is detected) for saving power. LINS Pullup will be recovered automatically if bus idle dominant timeout is released by any bus activity. Only reset by power-on sequence.	1	rw	0x1
F1	LINS_RXENA	LIN receive enable.	1	rw	0x0
F0	LINS_PU30K_ENA	LIN 30K pullup enable.	1	rw	0x1

7.17.6 CTRL

0x50015018 **CTRL**

PMU Debug Control.
NOTE:The write operation of this field register takes effect by configuring 'PMUPRE5V_SFRS->CFG.CFG_ACCESS_KEY = 0xB'.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	F30	F26				F20						F16				-	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F31	DBG_LOCK	Set Only bit. Set this bit to lock DBG_CODE bits.	1	rw	0x0
F30	DBG_ACCESS_ENABLED	A status flag that is set when debug access is enabled	1	ro	0x0
F26	DBG_ACCESS_KEY	Write the value 0x5 to this register to enable debug options. Write any other value to disable the debug options.	4	rw	0x0
F20	TRIM_BG	Trim the BG core 1.21415V output voltage (1) The voltage range before trimming is 1.16797V ~ 1.26337V. (2) The trim ratio 1/1.4811. (3) The voltage is 1.21455V while TRIM_BG == 0x0. at PMU debug mode	6	rw	0x0
F16	TRIM_BG_V2I	Trim the BG V2I which output the buffered reference voltage.	4	rw	0x0
F14	VDD1V5_LDO_CHOOSE	1.5V LDO Mode selection. NOTE: This register is not used by Analog PMU 0x0: choose Capless LDO 0x1: choose Caps LDO	1	rw	0x0
F13	OVERTEMP_ENA	OverTemp Monitor Enable bit.	1	rw	0x0
F12	DBG_ISO	NOTE:Don't use. Debug Contrl of isolation of domain 1V5 to domain PRE5V at PMU debug mode.	1	rw	0x0
F11	DBG_DISCHARGE_3V3	3V3 LDO Debug Mode: a. Set '0' to test 3V3-LDO function; b. Set '1' to test 3V3-LDO Discharge Circuit.	1	rw	0x0
F10	DBG_DISCHARGE_1V5	1V5 LDO Debug Mode: a. Set '0' to test 1V5-LDO function; b. Set '1' to test 1V5-LDO Discharge Circuit.	1	rw	0x0
F9	DBG_EN_BOR_3V3	Debug Contrl of dis_bor_3v3 at PMU debug mode.	1	rw	0x0
F8	DBG_EN_BOR_1V5	Debug Contrl of dis_bor_1v5 at PMU debug mode.	1	rw	0x0
F7	DBG_EN_LDO_3V3	NOTE:Don't use.Debug Contrl of en_ldo_3v3 at PMU debug mode.	1	rw	0x0
F6	DBG_DIS_LDO_1V5	Debug Contrl of dis_ldo_1v5 at PMU debug mode.(Not Use)	1	rw	0x0
F5	DBG_EN_LP_BOR1V5	Set to enable of low power mode for BOR1V5 at PMU debug mode.	1	rw	0x0
F4	DBG_EN_LP_5V0	Set to enable of low power mode for LDO5V0 at PMU debug mode.	1	rw	0x0
F3	DBG_EN_LP_1V5	Set to enable of low power mode for LDO1V5 at PMU debug mode.	1	rw	0x0

F2	DBG_EN_LP_BG	Set to enable of low power mode for BG_TOP at PMU debug mode.	1	rw	0x0
F1	OPT_EN_LP	Set to enable of low power mode for BG_TOP at Deepsleep Mode.	1	rw	0x1
F0	PD1V5_ENA_HIBERNATE	enable of 1V5 Power Domain at Hibernate mode. set to enable the 1V5 Power Domain at Hibernate mode, this mode is defined as DEEPSLEEP mode.	1	rw	0x0

7.17.7 BOR

0x5001501C **BOR**

BOR configuration.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F15	F14	F13	F12	-	F10	F9	F8	-	F4			-	F0		

#	Field Name	Field Description	Width	Access	Reset
F15	BOR_1V5_FLAG_CLR	BOR 1v5 clear. Set to clear the 1.5V brownout detected flag	1	wo	0x0
F14	BOR_3V3_FLAG_CLR	BOR 3v3 clear. Set to clear the 3.3V brownout detected flag	1	wo	0x0
F13	BOR_1V5_FLAG	BOR 1v5 flag. Set by the hardware when a brownout of the 1.5V supply is detected.	1	ro	0x0
F12	BOR_3V3_FLAG	BOR 3v3 flag. Set by the hardware when a brownout of the 3.3V supply is detected.	1	ro	0x0
F10	BOR_LOCK	Set Only bit. Set this bit to lock BOR_ACTION & S_BOR bits.	1	rw	0x0
F9	BOR_1V5_ACTION	BOR 1v5 action. Defines the consequences of brown-out condition on the 1v5 supply being detected by the hardware. NOTE: The write operation will be locked by BOR_SFRS->BOR_LOCK 0x1: IRQ generated 0x0: Hard reset generated	1	rw	0x0
F8	BOR_3V3_ACTION	BOR 3v3 action. Defines the consequences of brown-out condition on the 3v3 supply being detected by the hardware. NOTE: The write operation will be locked by BOR_SFRS->BOR_LOCK 0x1: IRQ generated 0x0: Hard reset generated	1	rw	0x0
F4	S_BOR_1V5	BOR 1v5 threshold. Select the BOR threshold voltage level for the 1v5 regulator. Following typical value can be used as reference: NOTE: The write operation will be locked by BOR_SFRS->BOR_LOCK 0x0: Vr: 1.135 V, Vf: 1.055 V, 0x1: Vr: 1.165 V, Vf: 1.095 V, 0x2: Vr: 1.215 V, Vf: 1.135 V, 0x3: Vr: 1.255 V, Vf: 1.175 V, 0x4: Vr: 1.305 V, Vf: 1.215 V, 0x5: Vr: 1.355 V, Vf: 1.265 V(default), 0x6: Vr: 1.405 V, Vf: 1.315 V, 0x7: Vr: 1.465 V, Vf: 1.375 V,	3	rw	0x5
F0	S_BOR_3V3	BOR 3v3 threshold. Select the BOR threshold voltage level for the 3v3 regulator, Following typical value can be used as reference: NOTE: The write operation will be locked by BOR_SFRS->BOR_LOCK 0x0: Vr: 2.223 V, Vf: 2.765 V, 0x1: Vr: 2.288 V, Vf: 2.825 V, 0x2: Vr: 2.358 V, Vf: 2.895 V, 0x3: Vr: 2.428 V, Vf: 2.975 V, 0x4: Vr: 2.503 V, Vf: 3.055 V(default), 0x5: Vr: 2.583 V, Vf: 3.135 V, 0x6: Vr: 2.668 V, Vf: 3.225 V, 0x7: Vr: 2.763 V, Vf: 3.315 V,	3	rw	0x4

7.17.8 BORDEGLITCH

0x50015020 **BORDEGLITCH**

BOR Deglitch.
NOTE:The write operation of this field register takes effect by configuring 'PMUPRE5V_SFRS->CFG.CFG_ACCESS_KEY = 0xB'.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F14		F12		-	-	-	F8	F6		F4		-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F14	SEL_BOR3V3_POS_DEGLITCH	select the deglitch width of BOR3V3 posedge. 0x0: 16us Selected	2	rw	0x3

		0x1: 32us Selected 0x2: 64us Selected 0x3: 128us Selected			
F12	SEL_BOR3V3_NEG_DEGLITCH	select the deglitch width of BOR3V3 negedge. 0x0: 16us Selected 0x1: 32us Selected 0x2: 64us Selected 0x3: 128us Selected	2	rw	0x0
F8	ENA_BOR3V3_DEGLITCH	enable of BOR3V3 deglitch.	1	rw	0x0
F6	SEL_BOR1V5_POS_DEGLITCH	select the deglitch width of BOR1V5 posedge. 0x0: 16us Selected 0x1: 32us Selected 0x2: 64us Selected 0x3: 128us Selected	2	rw	0x3
F4	SEL_BOR1V5_NEG_DEGLITCH	select the deglitch width of BOR1V5 negedge. 0x0: 16us Selected 0x1: 32us Selected 0x2: 64us Selected 0x3: 128us Selected	2	rw	0x0
F0	ENA_BOR1V5_DEGLITCH	enable of BOR1V5 deglitch.	1	rw	0x0

7.17.9 CLK_CTRL

0x50015024 **CLK_CTRL**

Clock controls for 5V(always on) domain.
NOTE:The write operation of this field register takes effect by configuring 'PMUPRE5V_SFRS->CFG.CFG_ACCESS_KEY = 0xB'.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	F17	F16	F8								-	-	-	F4	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F17	CLK_HF_RC_STS	Fast oscillator status. Will be high when High Frequency oscillator is enabled	1	ro	0x0
F16	CLK_LF_RC_STS	Slow oscillator status. Will be high when the Low Frequency oscillator is selected	1	ro	0x0
F8	TRIM_LF_RC	LF RC oscillator trim. Following value only used as a reference:(the trim freq is non-linear) 0x0: freq(250k)=141.1Khz 0xa2: freq(250k)=250.0Khz 0xa4: freq(250k)=256.0Khz 0xff: freq(250k)=441.7Khz	8	rw	N/A
F4	EN_HIGH_BW_LF_RC	set to enable to increase internal comparator bandwidth	1	rw	0x0
F0	PMUA_PRE5V_CLKMUX_SEL	5V domain Clock select. Used to switch between the fast and slow 5v domain clocks 0x0: Slow clock 0x1: Fast clock	1	rw	0x0

7.17.10 DFT

0x50015028 **DFT**

DFT.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F11	F10	F9	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F11	DFT_TESTMODE_START	Puts the ASIC into DFT testmode. Once the start bit is set, the I/O configuration will switch from Application mode to DFT Test Mode. The General Purpose I/Os will be configured as a JTAG interface. Once Test Mode is enabled, the ASIC will be boundary terminated and the processor will lose the ability to communicate with any ASIC peripherals. A chip power cycle is required to get out of the DFT test mode. Test Mode Enable state.	1	wo	0x0
F10	DFT_ACCESS_ENABLED	A status flag that is set when DFT access is enabled.	1	ro	0x0
F9	DFT_LOCK	Set Only bit. Write 1 to this bit to lock DFT_CODE config bits.	1	rw	0x0
F0	DFT_CODE	Write the value 0x1C to this register to Unlock 'Scan Test Mode'.	8	wo	0x0

7.18 TIMER0

TIMER0		
Address	**Register**	**Description**
0x50020000	COUNT	Timer Counter Register
0x50020004	CFG	Timer Control Register

7.18.1 COUNT

0x50020000																COUNT															
Timer Counter Register.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	COUNT	Count. Initial counter value. The timer will count from this value to 0xFFFFFFFF and roll over to 0x00000000. At this point it will generate an interrupt if enabled. The interrupt routine is responsible for reloading the value if needed as this timer does not auto-reload the original content.	32	rw	0x0

7.18.2 CFG

0x50020004																CFG															
Timer Control Register.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	ENA	Enable. This bit starts/stops the timer: 1 = Timer Running 0 = Timer Inactive	1	rw	0x0

7.19 TIMER1

TIMER1		
Address	**Register**	**Description**
0x50020008	COUNT	Timer Counter Register
0x5002000C	CFG	Timer Control Register

7.19.1 COUNT

0x50020008																COUNT															
Timer Counter Register.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	COUNT	Count. Initial counter value. The timer will count from this value to 0xFFFFFFFF and roll over to 0x00000000. At this point it will generate an interrupt if enabled. The interrupt routine is responsible for reloading the value if needed as this timer does not auto-reload the original content.	32	rw	0x0

7.19.2 CFG

0x5002000C																CFG															
Timer Control Register.																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	ENA	Enable. This bit starts/stops the timer: 1 = Timer Running 0 = Timer Inactive	1	rw	0x0

7.20 TIMER2

TIMER2		
Address	**Register**	**Description**
0x50020010	COUNT	Timer Counter Register
0x50020014	CFG	Timer Control Register

7.20.1 COUNT

0x50020010	COUNT

Timer Counter Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	COUNT	Count. Initial counter value. The timer will count from this value to 0xFFFFFFFF and roll over to 0x00000000. At this point it will generate an interrupt if enabled. The interrupt routine is responsible for reloading the value if needed as this timer does not auto-reload the original content.	32	rw	0x0

7.20.2 CFG

0x50020014	CFG

Timer Control Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	ENA	Enable. This bit starts/stops the timer: 1 = Timer Running 0 = Timer Inactive	1	rw	0x0

7.21 WDT1

WDT1		
Address	**Register**	**Description**
0x50020018	CFG	Config
0x5002001C	KEY	Key

7.21.1 CFG

0x50020018	CFG

Config.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F3		F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F3	PRESET	Preset. Defines the watchdog timeout period. It means that the WDT internal counter will count from 0 to the prescaler value at the system clock speed and trigger if not cleared. For instance, a system running from a 30MHz Crystal with WDTPRES[1I0] = 10 will trigger the WDT after approximately 0.14 seconds if not cleared properly and in time by the application. 0x0: 2^13 / System Clock 0x1: 2^19 / System Clock	2	rw	0x0

		0x2: 2^22 / System Clock 0x3: 2^32 / System Clock			
F2	RSTFLAG	Reset flag. This flag is set by the system at the initialization if the initialization was caused by a reset triggered by the WDT. The bit can be cleared by the application.	1	rw	0x0
F1	RSTEN	Reset enable. If enabled a WDT time-out will force the microcontroller to reset. This bit can be asserted but it cannot be de-asserted.	1	rw	0x0
F0	ENA	WDT Enable. This bit can be asserted but it cannot be de-asserted. It means that once the WDT is enabled it cannot be turned off until a Reset or Power-On Reset occurs.	1	rw	0x0

7.21.2 KEY

0x5002001C	KEY				
Key. Writing the sequence CLEAR, KEY0, KEY1 to this register will clear (pet) the watchdog - preventing it from timing out and resetting the system.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
F0					
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	KEY	Key. To clear the WDT counting the following words must be written in this order and without any other instruction between then: 0x3C570001 0x007F4AD6	32	rw	0x0

7.22 FLASH

FLASH		
Address	**Register**	**Description**
0x50020020	FLADDR	Destination address for flash write / erase operation
0x50020024	FLWRDT	Flash data to be written
0x50020028	UNLBWR	Flash data unlock register
0x5002002C	BWRSTRT	Flash write start register
0x50020030	UNLSER	Flash sector erase unlock register
0x50020034	SERSTRT	Flash sector erase start register
0x50020040	FLSCTRL	Flash control register
0x50020044	FLSCP	Flash code protection register
0x50020050	FLS_UNLOCK_CTRL_OP	Flash Unlock Control Operation Register
0x50020054	CTRL_OP	Flash Control Operation Register
0x50020058	TRIM	Flash Trim Register

7.22.1 FLADDR

0x50020020	FLADDR				
Destination address for flash write / erase operation.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
- - - - - - - - - - - - - - - F0					
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	ADDR	Target address for write/erase operation. In byte writes, this is the read address of the flash to be written to. In erase modes, it is a read address inside the sector to be erased. This register must be written in the correct sequence or the operation will fail.	17	rw	0xFFFF

7.22.2 FLWRDT

0x50020024	FLWRDT				
Flash data to be written.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
F0					

#	Field Name	Field Description	Width	Access	Reset
F0	DATA	Content to be written into the targeted address. This register must be written in the correct sequence or the operation will fail.	32	rw	0x0

7.22.3 UNLBWR

0x50020028	UNLBWR

Flash data unlock register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	UNLOCK_WRITE	Control register to unlock write. A value of 0x55555555 must be written to this address at the correct point in the write sequence or the operation will fail.	32	rw	0x0

7.22.4 BWRSTRT

0x5002002C	BWRSTRT

Flash write start register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	WRITE_START	Control register to start a write. A value of 0xAAAAAAAA must be written to this address at the correct point in the write sequence or the operation will fail.	32	rw	0x0

7.22.5 UNLSER

0x50020030	UNLSER

Flash sector erase unlock register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	UNLOCK_ERASE	Control register to unlock a sector erase. A value of 0x66666666 must be written to this address at the correct point in the sector erase sequence or the operation will fail.	32	rw	0x0

7.22.6 SERSTRT

0x50020034	SERSTRT

Flash sector erase start register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	ERASE_START	Control register to commit a sector erase. A value of 0x99999999 must be written to this address at the correct point in the sector erase sequence or the operation will fail.	32	rw	0x0

7.22.7 FLSCTRL

0x50020040	FLSCTRL

Flash control register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0	

#	Field Name	Field Description	Width	Access	Reset
F0	CTRL	Number of wait states used in the reading process. Each read from flash memory will take number of cycles equal to 1+RWC to complete.	2	rw	0x1

7.22.8 FLSCP

0x50020044		FLSCP			
Flash code protection register.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
F0					
#	Field Name	Field Description	Width	Access	Reset
F0	CODE_PROT	Code Protection / SerialWire Lockout Control Code protection control register. Write a value of 0xF2E11047 to disable the SerialWire interface. Write 0x00000000 to enable it. This allows the user program to disable the SerialWire interface to prevent unauthorized debug access to the part. NOTE1: This register does not lock the Flash Memory against read/write/erase by the applications program. Instead what it does is to disable all communications with the debug interface, therefore preventing any external attack. The application code is still able to modify the flash content. NOTE2: Upon Power-On Reset or Normal Reset the system disables the communication for a small time interval (8192 clock cycles). If the application needs to be protected it is mandatory to set this register with the appropriate code in the beginning of the initialization process and before the internal hardware enable the debug communication.	32	rw	0x0

7.22.9 FLS_UNLOCK_CTRL_OP

0x50020050		FLS_UNLOCK_CTRL_OP			
Flash Unlock Control Operation Register.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
F0					
#	Field Name	Field Description	Width	Access	Reset
F0	UNLOCK_CTRL_OP	Flash Control Operation Register Unlock value. 0xACDC_1972 needs to be written in this register to unlock the Control Operation Register access. When this register is read, it returns the state of the lock: 0: The Control Operation Register is locked. The Control Operation Register (FLASH_CTRL_OP) cannot be written. 1: The Control Operation Register is unlocked. The Control Operation Register (FLASH_CTRL_OP) can be written. Note: After each write to the FLASH_CTRL_OP register, the state of the lock is cleared and the pattern needs to be written again to allow a new configuration of the register.	32	rw	0x0

7.22.10 CTRL_OP

0x50020054		CTRL_OP			
Flash Control Operation Register.					
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
- F1 F0					
#	Field Name	Field Description	Width	Access	Reset
F1	SIZE	SIZE of the write operation. Refer to data sheet for more information of the use of this field.	2	rw	0x0
F0	CHIP	CHIP bit. This bit is only used during the Erase operation. It allows the system to erase more than one sector. 0: The Erase operation will only erase the sector selected by the FLASH_ADDR register value. 1: The Erase operation will erase the full main array of the flash.	1	rw	0x0

7.22.11 TRIM

0x50020058	TRIM
Flash Trim Register.	
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	

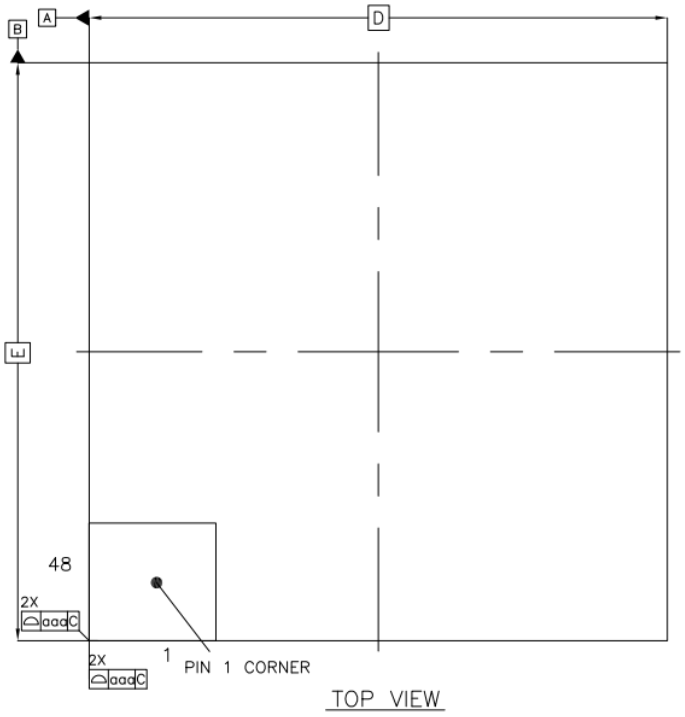
-	-	-	-	-	-	-	-	-	-	-	-	-	-	F17	F16	F0			
#	**Field Name**							**Field Description**									**Width**	**Access**	**Reset**
F17	SLEEPDEEP_CFG							Deep Sleep VDD_IO configuration. This register will be automatically populated with the value stored in the NVR sector 1 (@0001_0000). When set, the system will NOT be reset if VDD_IO is going away during Deep Sleep mode. Otherwise (0), the system is reset if VDD_IO is removed.									1	rw	0x0
F16	SDIO_TIMING_CFG							SDIO interface timing configuration. This register will be automatically populated with the value stored in the NVR sector 1 (@0001_0000). When set, the SDIO/INT signals are captured on the rising edge of CLK. When cleared, these data are captured on the falling edge of CLK									1	rw	0x1
F0	OSC_TRIM							Oscillator Trim Value. This register will be automatically populated with the value stored in the NVR sector 1 (@0001_0000).									16	rw	0x86

Note:

8 Package Information

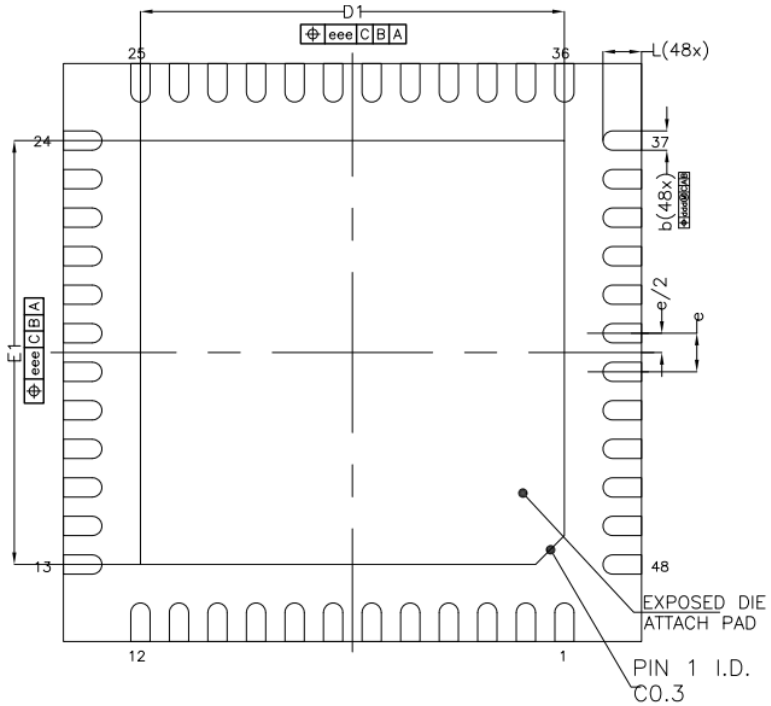
8.1 Package Outline

Package information of iND83213A:

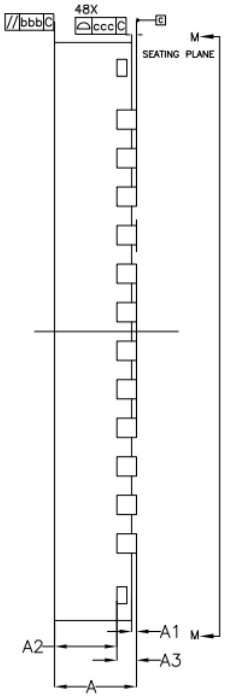


TOP VIEW

DESCRIPTION		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.80	0.85	0.90
STAND OFF		A1	0.00	---	0.05
MOLD THICKNESS		A2	0.60	0.65	0.70
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.14	0.20	0.26
BODY SIZE	X	D	5.90	6.00	6.10
	Y	E	5.90	6.00	6.10
LEAD PITCH		e		0.40 BSC	
EP SIZE	X	D1	4.35	4.40	4.45
	Y	E1	4.35	4.40	4.45
LEAD LENGTH		L	0.30	0.40	0.50
Tolerance of form and position					
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

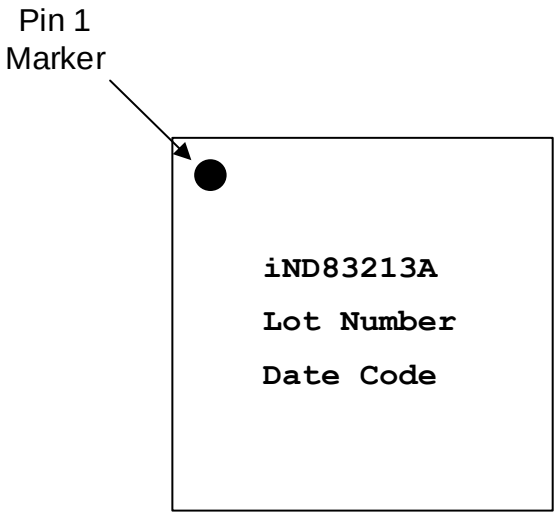


BOTTOM VIEW
VIEW M–M



SIDE VIEW

8.2 Package Branding



Date code: The date code is in format YYWW, where YY are the last two digits of the year, and WW is the week number. The week number calculation is based upon ISO-8601 standard.

9 Ordering Information

Part Number	Package	MSL	Shipping
iND83213A	QFN-48	Level 3	3000pcs/tape & reel

10 Disclaimer

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