# AK2365A

## FM IF Detector with Narrow Band Filter

## 1. Features

The AK2365A includes 2nd-Mixer, AGC+BPF, PLL FM detector, noise squelch, and RSSI circuit. This device can eliminate E to J type ceramic filters, quadrature discriminator, and other external components.

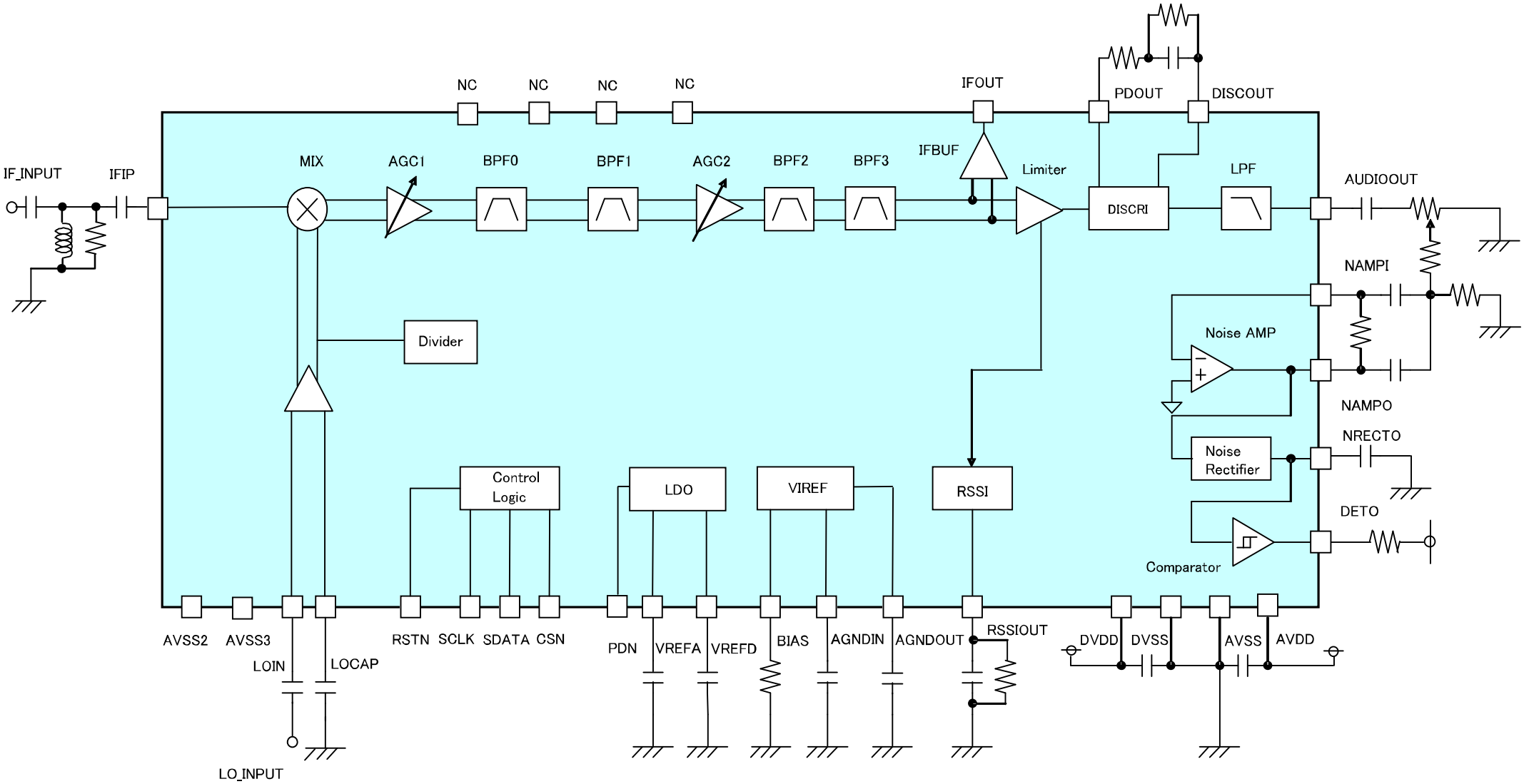
- Low operating voltage: VDD = 2.6 to 5.5 V
- Wide operating temperature: Ta = -40 to 85 °C
- High sensitivity: -102dBm at 12dB SINAD *De-emphasis + BPF
- Built-in PGA and 2nd Mixer
- Local frequency: 45.9MHz, 50.4MHz, 57.6MHz (Triple of 15.3, 16.8 and 19.2MHz)
- Built-in programmable AGC+BPF circuits corresponding to E to J type ceramic filters
- Built-in PLL FM detector
- RSSI function
- Built-in noise squelch circuits
- Low consumption current: 6mA
- Compact plastic packaging: 32-pin QFNJ (4.0 x 4.0 x 0.75mm, 0.4mm pitch)

## 2. Applications

- Narrowband high performance professional digital wireless systems
  (Channel spacing for 6.25kHz,12.5kHz)
- Digital convenience radio systems

# 3. Contents

# 4. Block Diagram



# 5. Circuit Configuration

| Block | Description |
|---|---|
| MIX | 2nd-mixer to convert the input signal down to 450kHz. |
| AGC+BPF | The circuit composed of AGC and BPF, where the desired signal is amplified and spurious components included in the signal from the 2nd-mixer are eliminated. |
| IFBUF | The circuit to output filtered signal by AGC+BPF. |
| Divider | The circuit to divide the signal from LOIN pin. |
| Limiter | The circuit to amplify the signal filtered at the AGC+BPF stage and generate rectangular wave. |
| DISCRI | The demodulator circuit with PLL FM detector, where the audio signal is recovered. |
| LPF | The Low-pass filter to eliminate the noise generated at the DISCRI stage. |
| Noise AMP | The amplifiers to compose the Band-pass filter for noise squelch. |
| Noise Rectifier | The rectification circuit to detect the noise level. |
| Comparator | The circuit to compare the noise level with reference voltage level. |
| RSSI | The circuit to indicate the Received Signal Strength Indicator (RSSI) by generating a DC voltage corresponding to the input level from Limiter. |
| VIREF | The circuit to generate internal reference voltage. |
| LDO | The circuit to supply 1.8V power for some circuits. |
| Control Logic | The control register controls the status of internal condition by serial data that consists of 1 instruction bit, 6 address bits and 8 data bits. |

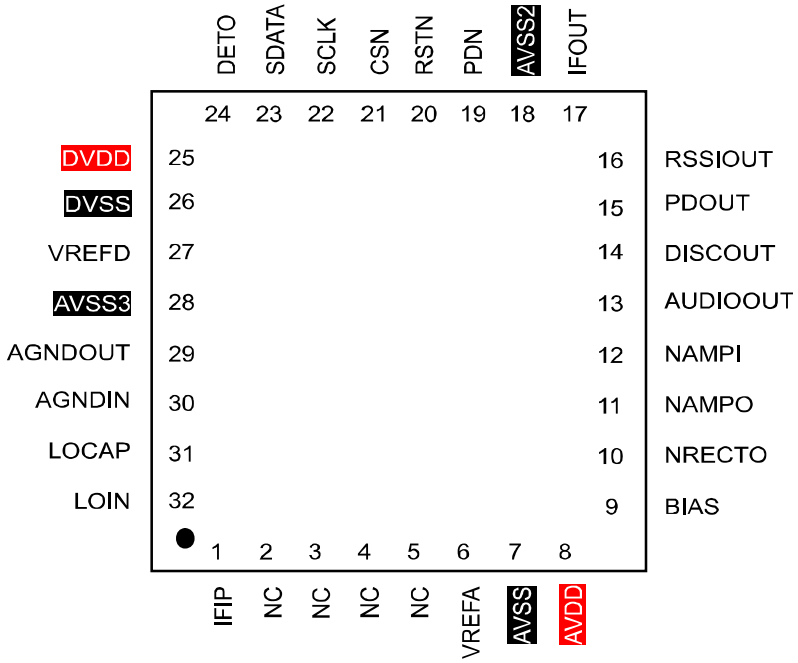
# 6. Pin/Function

| Package | Signal | | | Function |
|---|---|---|---|---|
| Pin No | Name | Type | Conditions at power down | |
| 1 | IFIP | AI | Note 1) | IF signal input pin |
| 2 | NC | AIO | Z | NC pin |
| 3 | NC | AIO | Z | NC pin |
| 4 | NC | AIO | Z | NC pin |
| 5 | NC | AIO | Z | NC pin |
| 6 | VREFA | AO | Low | LDO reference pin<br>Connect the capacitor to stabilize LDO reference voltage. |
| 7 | AVSS | PWR | - | Analog VSS power supply pin |
| 8 | AVDD | PWR | - | Analog VDD power supply pin |
| 9 | BIAS | AO | Z | Output pin to connect bias resistor for reference voltage |
| 10 | NRECTO | AI | Note 2) | Output pin for the rectification circuit |
| 11 | NAMPO | AO | Z | Output pin for noise squelch amplifier |
| 12 | NAMPI | AI | Z | Input pin for noise squelch amplifier |
| 13 | AUDIOOUT | AO | Note 3) | Demodulated audio signal output pin |
| 14 | DISCOUT | AO | Note 4) | Pin2 for Discriminator Low-pass filter |
| 15 | PDOUT | AO | Z | Pin1 for Discriminator Low-pass filter |
| 16 | RSSIOUT | AO | Z | Output pin to connect capacitor for Received Signal Strength Indicator(RSSI) |
| 17 | IFOUT | AO | Note 5) | Output pin for IFBUF |
| 18 | AVSS2 | PWR | - | Analog VSS power supply pin |
| 19 | PDN | DI | Z | Power down pin for LDO |
| 20 | RSTN | DI | Z | Hardware reset pin |
| 21 | CSN | DI | Z | Chip select input pin for serial data |
| 22 | SCLK | DI | Z | Clock input pin for serial data |
| 23 | SDATA | DB | Z | Input and output pin for serial data |
| 24 | DETO | DO | Z | Signal detect output pin |
| 25 | DVDD | PWR | - | Digital VDD power supply pin. |
| 26 | DVSS | PWR | - | Digital VSS power supply pin. |
| 27 | VREFD | AO | Low | LDO reference pin<br>Connect the capacitor to stabilize LDO reference voltage. |
| 28 | AVSS3 | PWR | - | Analog VSS power supply pin |
| 29 | AGNDOUT | AO | Low | Analog ground output pin.<br>Connect the capacitor to stabilize the analog ground level. |
| 30 | AGNDIN | AI | Low | Analog ground input pin.<br>Connect the capacitor to stabilize the analog ground level. |
| 31 | LOCAP | AI | Note 6) | Local signal input pin |
| 32 | LOIN | AI | Note 6) | Local signal input pin |

Note **A**: Analog, **D**: Digital, **PWR**: Power, **I**: Input, **O**: Output, **B**: Bidirectional, **Z**: High-Z, **L**: Low
Note 1) Connecting internally to VSS pin by 50kΩ
Note 2) Connecting internally to VDD pin by 720kΩ
Note 3) Connecting internally to VSS pin by 830kΩ

Note 4) Connecting internally to VSS pin by 50kΩ
Note 5) Connecting internally to VSS pin by 480kΩ
Note 6) Connecting internally to VDD pin by 139kΩ

• Pin Assignment



## 7. Absolute Maximum Ratings

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Power Supply Voltage | AVDD | -0.3 | 6.5 | V |
| | DVDD | -0.3 | 6.5 | V |
| Ground Level | VSS | 0 | 0 | V |
| Input Voltage | $V_{IN}$ analog | -0.3 | AVDD+0.3 | V |
| | $V_{IN}$ digital | -0.3 | DVDD+0.3 | V |
| Input Current (Except power supply pin) | $I_{IN}$ | -10 | +10 | mA |
| Storage Temperature | $T_{stg}$ | -55 | 125 | °C |

Note : All voltages are relative to the VSS pin.

Caution : Exceeding these maximum ratings can result in damage to the device.
Normal operation cannot be guaranteed under this extreme.

## 8. Recommended Operating Conditions

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Operating Temperature | Ta | | -40 | | 85 | °C |
| Power Supply Voltage | AVDD | | 2.6 | 3.0 | 5.5 | V |
| | DVDD | DVDD ≤ AVDD | 2.6 | 3.0 | 5.5 | V |
| Analog Reference Voltage | AGND | AGNDOUT | | 1/2 VREFA | | V |
| Output Load Resistance | $R_{L1}$ | AUDIOOUT, DISCOUNT, NAMPO | 30 | | | kΩ |
| Output Load Capacitance | $C_{L1}$ | AUDIOOUT, DISCOUNT, NAMPO | | | 15 | pF |
| | $C_{L2}$ | IFOUT | | 21 | 26 | pF |

Note : All voltages are relative to the VSS pin.

## 9. Digital DC Characteristics

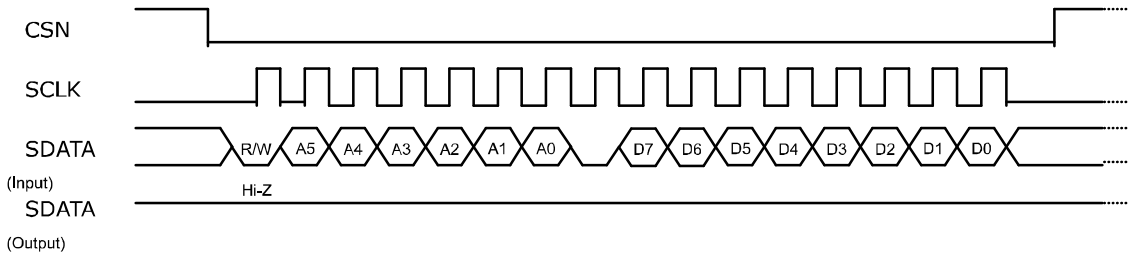
| Parameter | Symbol | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| High level input voltage | $V_{IH}$ | RSTN, SCLK, SDATA, CSN, PDN | 0.8DVDD | | | V |
| Low level input voltage | $V_{IL}$ | RSTN, SCLK, SDATA, CSN, PDN | | | 0.2DVDD | V |
| High level input current | $I_{IH}$ | VIH=DVDD RSTN, SCLK, SDATA, CSN, PDN | | | 10 | uA |
| Low level input current | $I_{IL}$ | VIL=0V RSTN, SCLK, SDATA, CSN, PDN | -10 | | | uA |
| High level output voltage | $V_{OH}$ | IOH=+0.2mA SDATA | DVDD-0.4 | | DVDD | V |
| Low level output voltage | $V_{OL}$ | IOL=-0.4mA SDATA, DETO | 0.0 | | 0.4 | V |

# 10. Digital AC Timing

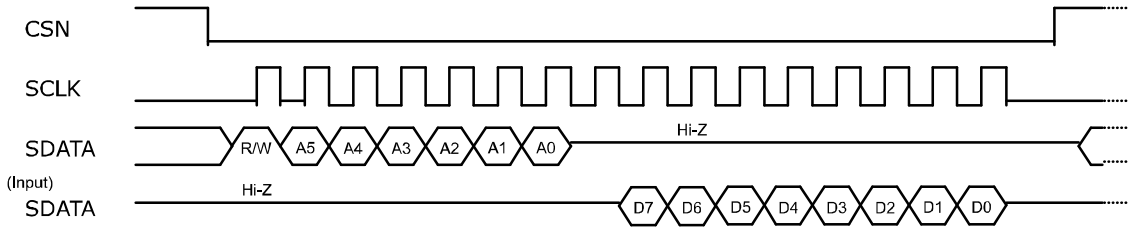
1) Serial Interface Timing

AK2365A is connected to a CPU by three-wired interface through CSN, SCLK and SDATA pins, which can make reading and writing data for control registers.
Serial data named SDATA is consist of 1-bit read and write instruction(R/W), 6-bit address (A5 to A0) and 8-bit data(D7 to D0) in one frame.

Write mode




Read mode




R/W : Instruction bit controls to write data to AK2365A or read back from it. When set to low, AK2365A is in write mode. When set to high, AK2365A is in read mode.

A5 to A0: Register address to be accessed.
D7 to D0: Write or read date to be accessed.

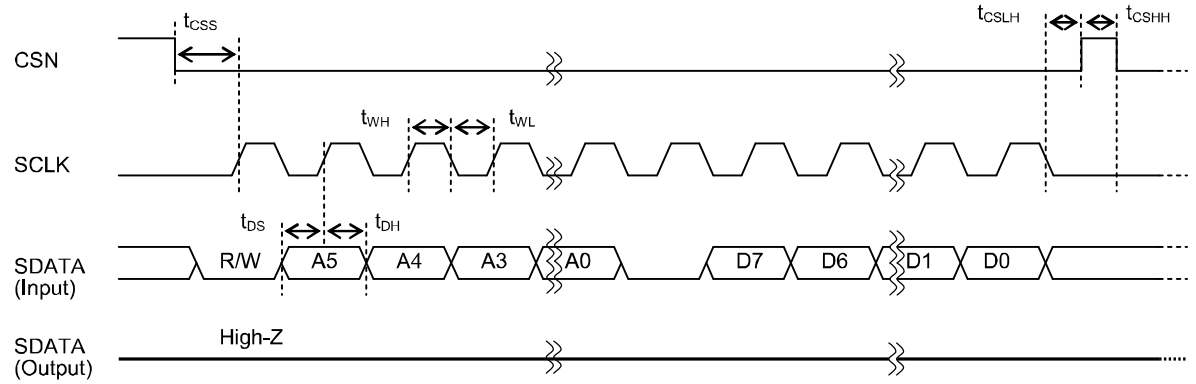
<1> CSN(Chip select) is normally selected high for disable. When CSN is set to low, serial interface becomes active.

<2> In write mode, instruction, address and data input from SDATA pin are synchronized and latched with the rising edge of 16 iterations of SCLK clock. Set to low between address A0 and data D7.Input data is fixed synchronized with the rising edge of 16th clock. Note that if CSN become “H” before 16th clock, setting data becomes invalid. During the period when CSN is set to “L”, consecutive writing is available.

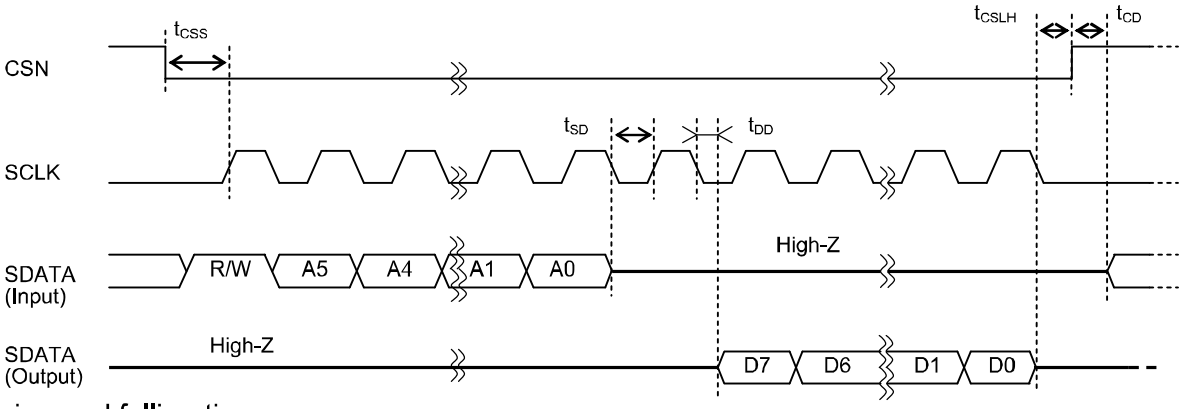
<3> In read mode, instruction and address are synchronized and latched with the rising edge of 7 iterations of SCLK clock. And the register data are output from SDATA pin synchronized with the falling edge of 9 iterations of SCLK clock. The data between address A0 and data D7 is unstable. During the period when data is output, input to SDATA must be “Hi-z”. Set CSN to “H” once reading is completed because consecutive reading is not valid.

2) Detail Timing Chart

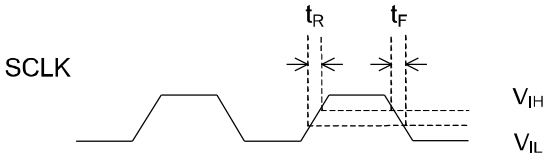
Write mode




Read mode



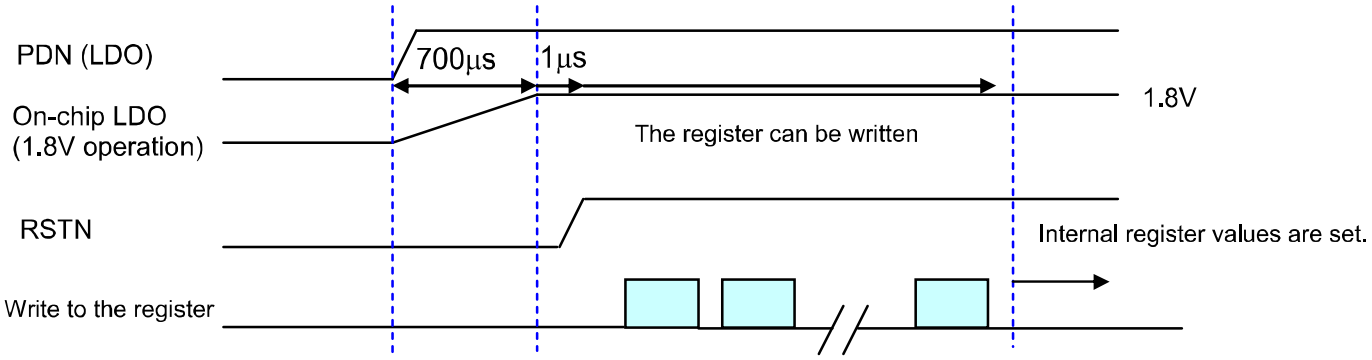

Rising and falling time




| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| CSN setup time | $t_{CSS}$ | | 100 | | | ns |
| SDATA setup time | $t_{DS}$ | | 100 | | | ns |
| SDATA hold time | $t_{DH}$ | | 100 | | | ns |
| SCLK high time | $t_{WH}$ | | 500 | | | ns |
| SCLK low time | $t_{WL}$ | | 500 | | | ns |
| CSN low hold time | $t_{CSLH}$ | | 100 | | | ns |
| CSN high hold time | $t_{CSHH}$ | | 100 | | | ns |
| SDATA Hi-Z setup time | $t_{SD}$ | | 500 | | | ns |
| SCLK to SDATA output delay time | $t_{DD}$ | 20pF load | | | 400 | ns |
| CSN to SDATA input delay time | $t_{CD}$ | 20pF load | 200 | | | ns |
| SCLK rising time | $t_R$ | | | | 250 | ns |
| SCLK falling time | $t_F$ | | | | 250 | ns |

Note) Digital input and output timing is relative to 0.5DVDD of rising signal and falling signal.

## 11. Power-up Sequence

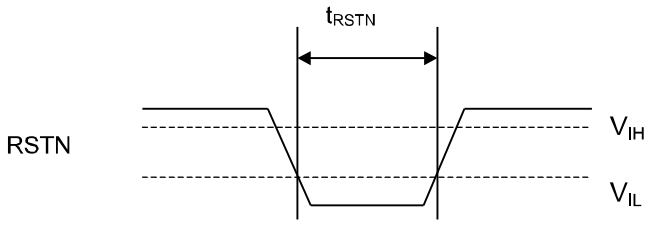



Note) After PDN is set to "High", registers remain undefined. In order to initialize them, RSTN is set to "High"

## 12. System Reset

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| Hardware reset signal input width | $t_{RSTN}$ | RSTN pin | 1 | | | µs | *1) |
| Software reset | | SRST register | | | | | *2) |

*1) After power-on, be sure to perform a hardware reset operation (register initialization). The system is reset by a low pulse input of 1µs (min.) and enters the normal operation state. At this moment, the digital (DI) pins are set as follows: RSTN pin to High, SCLK pin to Low, SDATA pin to Low, CSN pin to Low.




*2) When data 0x04:10101010 is written to the SRST[7:0] register, software reset is performed. This setting initializes the registers and the operation mode is set to mode 2 (Standby 2). After software reset is completed, this register comes to "0".

## 13. Power Consumption

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Power Consumption | IDD0 | Mode 0<br>Power down | | | 0.01 | mA |
| | IDD1 | Mode 1<br>(Prohibited) | | | - | |
| | IDD2 | Mode 2<br>Standby(initial value) | | 0.4 | 0.7 | |
| | IDD3 | Mode 3 | | 1 | 1.6 | |
| | IDD4 | Mode 4<br>Digital Mode 1 with no signal input | | 5.6 | 7.5 | |
| | IDD5 | Mode 5<br>Digital Mode 2 with no signal input | | 6 | 8 | |
| | IDD6 | Mode 6<br>Analog Mode with no signal input | | 6 | 8 | |
| | IDD7 | Mode 7<br>Full Power On with no signal input | | 7 | 9.8 | |

Note 1) Do not use Mode1.

# 14. Analog Characteristics

For the following conditions unless otherwise specified: Mode 6, LOIN=50.4MHz,IFIP=50.85MHz, Δf=±1.5kHz, fmod=1kHz、AGC+BPF=F2, {AGC_OFF}=0, the exposure back pad of the package is connected to VSS, with the external circuit shown in example page 26 to 28.

1) Local

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| Local Frequency | $F_{LO}$ | LOIN | | 45.9<br>50.4<br>57.6 | | MHz | |
| Input amplitude | $V_{LO}$ | LOIN | 0.2 | | 2.0 | $V_{PP}$ | Note 1) |

Note 1) Input from LOIN pin through DC cut

2) 2nd Mixer

| Parameter | Condition | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| Input Impedance | | | 50 | | Ω | Note 2) |
| Input Frequency | | | $F_{LO}$ ±0.45 | | MHz | |
| Voltage Gain | | | 28 | | dB | |

Note 2) Include external matching circuit

3) Discriminator

| Parameter | Condition | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| Demodulation Output Level | Δf=±3.0kHz,fmod=1kHz,<br>LIMITER IN to AUDIOOUT<br>{BAND}=1 | 70 | 100 | 130 | mVrms | |
| | Δf=±1.5kHz,fmod=1kHz,<br>LIMITER IN to AUDIOOUT<br>{BAND}=0 | 70 | 100 | 130 | mVrms | |
| S/N Ratio | Δf=±3.0kHz,fmod=1kHz,<br>Vin=-16dBm<br>LIMITER IN to AUDIOOUT<br>{BAND}=1 | 43 | 50 | | dB | Note 3) |

Note 3) With De-emphasis＋BPF(0.3 to 3kHz)

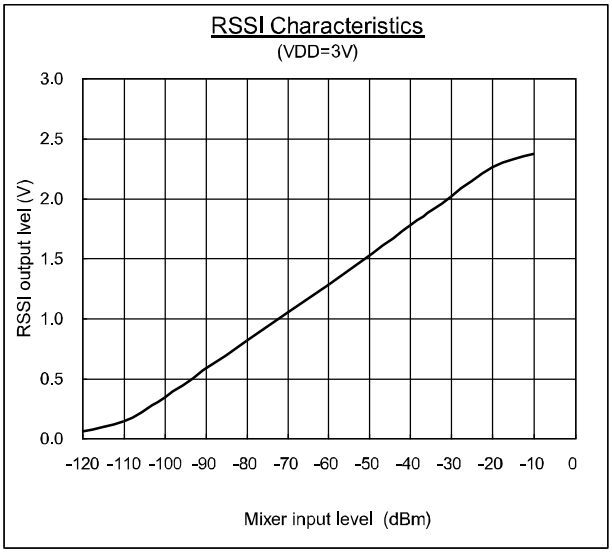
4) RX Overall Characteristics

| Parameter | Condition | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| 12dB SINAD Input Sensitivity | | | -102 | | dBm | Note 4) |
| Total Gain | Mode 5<br>Maximum gain setting for AGC<br>IFIP to IFOUT<br>{IFOG[1:0]}=00 | | 84 | | dB | |
| | Mode 5<br>Minimum gain setting for AGC<br>IFIP to IFOUT<br>{IFOG[1:0]}=00 | | 32 | | dB | |
| C/N ratio | Mode 5, BPF=F3<br>IFIP to IFOUT<br>When in CW, 450kHz, -102dBm<br>Bandwidth: 450kHz ±3kHz<br>{IFOG[1:0]}=00 | | 17 | | | |
| IIP3 | Mode 5<br>Maximum gain setting for AGC<br>IFIP=50.8635MHz&50.876MHz | | -20 | | dBm | |
| Demodulation Output Level | Δf=±3.0kHz,fmod=1kHz,<br>AGC+BPF=F1, {BAND}=1 | 70 | 100 | 130 | mVrms | |
| | Δf=±1.5kHz,fmod=1kHz,<br>AGC+BPF=F2, {BAND}=0 | 70 | 100 | 130 | mVrms | |
| S/N Ratio | Δf=±3.0kHz, fmod=1kHz,<br>AGC+BPF=F1, Vin=-47dBm<br>{BAND}=1 | 40 | 50 | | dB | Note 4) |
| | Δf=±1.5kHz, fmod=1kHz,<br>AGC+BPF=F2, Vin=-47dBm<br>{BAND}=0 | 34 | 44 | | dB | Note 4) |

Note 4) With De-emphasis+BPF(0.3 to 3kHz)

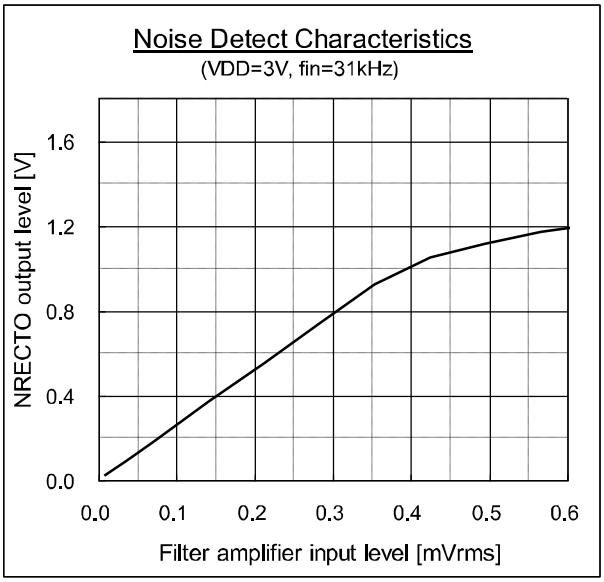
5) RSSI Characteristics

| Parameter | Condition | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| RSSI Output Voltage | IFIP to RSSIOUT {AGC_OFF}=0, IFIP=-100dBm Input | 0.05 | 0.3 | 0.7 | V | |
| | IFIP to RSSIOUT {AGC_OFF}=0, IFIP=-30dBm Input | 1.4 | 2.0 | 2.6 | V | |




6) Noise Squelch Characteristics

| Parameter | Condition | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| Noise Detection Level | NRECTO to DETO Detect High | | 0.5 | 0.7 | V | |
| | NRECTO to DETO Detect Low | 0.3 | 0.4 | | V | |
| Noise Detection Characteristic | NAMPI to NRECTO Input: 31kHz, 0.1mVrms | 0.2 | 0.3 | 0.4 | V | |
| | NAMPI to NRECTO Input: 31kHz, 0.25mVrms | 0.5 | 0.65 | 0.8 | V | |



7) AGC+BPF Characteristics

7.1) F0 (E type)

| Parameter | Condition | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| Attenuation Characteristics (relative to the gain at 450kHz) | 435kHz | | | -50 | dB | |
| | 442.5kHz | -6 | | | dB | |
| | 457.5kHz | -6 | | | dB | |
| | 465kHz | | | -50 | dB | |
| Gain ripple | Within 450±5kHz | | | 3 | dB | |

7.2) F1 (F type)

| Parameter | Condition | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| Attenuation Characteristics (relative to the gain at 450kHz) | 437.5kHz | | | -50 | dB | |
| | 444kHz | -6 | | | dB | |
| | 456kHz | -6 | | | dB | |
| | 462.5kHz | | | -50 | dB | |
| Gain ripple | Within 450±4kHz | | | 3 | dB | |

7.3) F2 (G type)

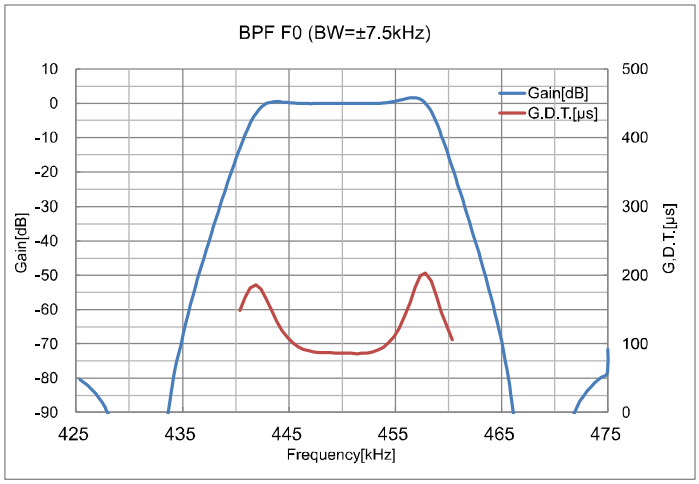
| Parameter | Condition | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| Attenuation Characteristics (relative to the gain at 450kHz) | 439kHz | | | -50 | dB | |
| | 445.5kHz | -6 | | | dB | |
| | 454.5kHz | -6 | | | dB | |
| | 461kHz | | | -50 | dB | |
| Gain ripple | Within 450±3kHz | | | 3 | dB | |

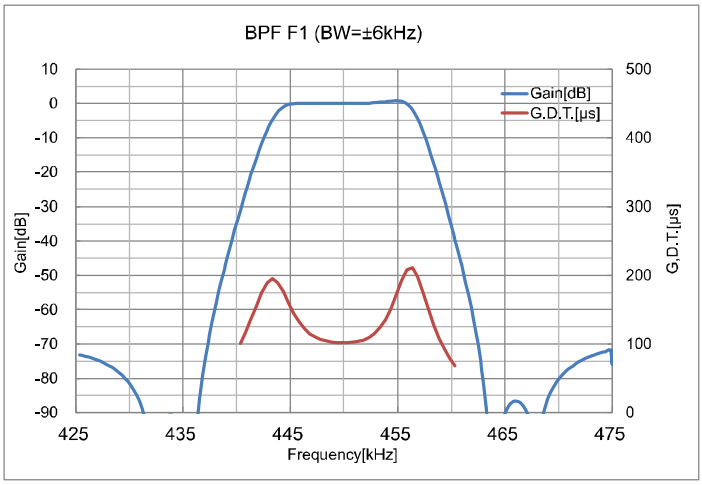
7.4) F3 (H type)

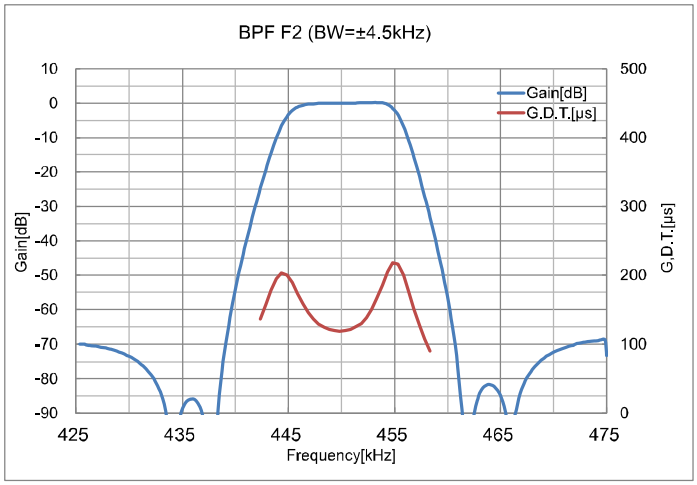
| Parameter | Condition | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| Attenuation Characteristics (relative to the gain at 450kHz) | 441kHz | | | -50 | dB | |
| | 447kHz | -6 | | | dB | |
| | 453kHz | -6 | | | dB | |
| | 459kHz | | | -50 | dB | |
| Gain ripple | Within 450±2kHz | | | 2 | dB | |

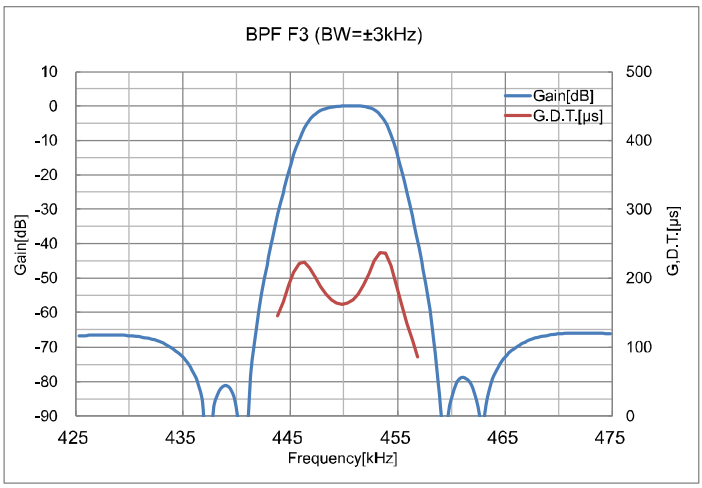
7.5) F4 (J type)

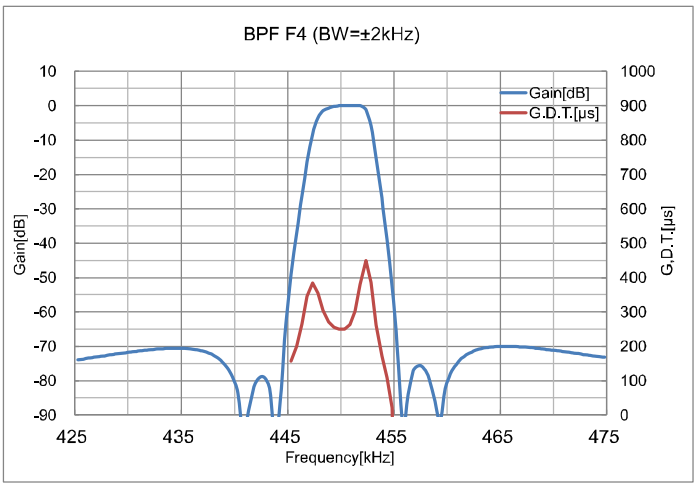
| Parameter | Condition | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| Attenuation Characteristics (relative to the gain at 450kHz) | 443kHz | | | -50 | dB | |
| | 448kHz | -6 | | | dB | |
| | 452kHz | -6 | | | dB | |
| | 457kHz | | | -50 | dB | |
| Gain ripple | Within 450±1.5kHz | | | 2 | dB | |




8) IFBUF Characteristics

| Parameter | Condition | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| Settling time | IFBUF to IFOUT,<br>IFBUF=0.32Vpp/step<br>$C_{L2}$=21pF, {IFOG[1:0]}=00 | | 100 | | ns | |

Note: Convergence time within 1% when 0.32Vpp step signal input to IFBUF pin

# 15. Serial Interface Configuration

1) Register Configuration

| Name | ADRS | D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0(LSB) | W/R |
|---|---|---|---|---|---|---|---|---|---|---|
| Control register 1 | 0x01 | BS[2:0] | | | BAND | BPF_BW[1:0] | | LOFREQ[1:0] | | W/R |
| | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | |
| Control register 2 | 0x02 | Reserved | AGC_ KEEP | AGC_ FAST | Reserved | AGC_TIME[1:0] | | AGC1_ STEP | CAL | W/R |
| | | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | |
| Control register 3 | 0x03 | Reserved | | | | | | IFOG[1:0] | | W/R |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| Software -reset | 0x04 | SRST[7:0] | | | | | | | | W |
| | | — | — | — | — | — | — | — | — | |
| Reserved | 0x05 to 0x0A | Reserved | | | | | | | | — |
| Control register 4 | 0x0B | BPF_BW [2] | AGC_ OFF | AGC1_G[5:0] | | | | | | W/R |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | |
| Control register 5 | 0x0C | Reserved | | | AGC2_G[4:0] | | | | | W/R |
| | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

Note: Do not access the data except specified address above.

2) Description of registers

Address 0x01 (Control Register 1)

| Name | D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0(LSB) |
|---|---|---|---|---|---|---|---|---|
| Control Register 1 | BS[2:0] | | | BAND | BPF_BW[1:0] | | LOFREQ[1:0] | |
| Initial Value | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |

BS[2:0]: Operation mode setting

| PDN pin | BS[2] | BS[1] | BS[0] | Mode name | LDOD | LDOA, AGNDIN | VREF | MIX AGC, BPF, Divider | IFBUF | Limiter, RSSI | DISCRI, Noise Squelch |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | - | - | - | Mode 0 (Power-down) | OFF | OFF | OFF | OFF | OFF | OFF | OFF |
| 1 | 0 | 0 | 1 | Mode 1 (Note1) | ON | OFF | OFF | OFF | OFF | OFF | OFF |
| 1 | 0 | 1 | 0 | Mode 2 (initial value) | ON | ON | OFF | OFF | OFF | OFF | OFF |
| 1 | 0 | 1 | 1 | Mode 3 | ON | ON | ON | OFF | OFF | OFF | OFF |
| 1 | 1 | 0 | 0 | Mode 4 | ON | ON | ON | ON | ON | OFF | OFF |
| 1 | 1 | 0 | 1 | Mode 5 | ON | ON | ON | ON | ON | ON | OFF |
| 1 | 1 | 1 | 0 | Mode 6 | ON | ON | ON | ON | OFF | ON | ON |
| 1 | 1 | 1 | 1 | Mode 7 | ON | ON | ON | ON | ON | ON | ON |

Note1: Do not use Mode1.
Note2: Do not set the combination of the code which is not defined in the table given above.

BAND: Demodulated signal level setting

| BAND | Function |
|---|---|
| 0 | Narrow |
| 1 | Wide |

Note1: When {BAND} register is set to “0”, demodulated signal level at AUDIOOUT pin, when input signal is Δf=±1.5kHz dev, is 100mVrms typ. When {BAND} register is set to “1”, demodulated signal level at AUDIOOUT pin, when input signal is Δf=±3.0kHz dev, is 100mVrms typ.

BPF_BW[1:0]: BPF band width setting

| BPF_BW [2] | BPF_BW [1] | BPF_BW [0] | name | 6dB attenuation | Attenuation band width |
|---|---|---|---|---|---|
| 1 | 0/1 | 0/1 | F0 | ±7.5kHz | ±15kHz |
| 0 | 0 | 0 | F1 | ±6kHz | ±12.5kHz |
| 0 | 0 | 1 | F2 | ±4.5kHz | ±11kHz |
| 0 | 1 | 0 | F3 | ±3kHz | ±9kHz |
| 0 | 1 | 1 | F4 | ±2kHz | ±7kHz |

LOFREQ[1:0]: Local frequency setting

| LOFREQ [1] | LOFREQ [0] | Local frequency |
|---|---|---|
| 0 | 0 | 45.9MHz |
| 0 | 1 | 50.4MHz |
| 1 | 0 | 57.6MHz |

Note: Do no set the combination of the code which is not defined in the table given above.

Address 0x02 (Control Register 2)

| Name | D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0(LSB) |
|---|---|---|---|---|---|---|---|---|
| Control Register 2 | Reserved | AGC_ KEEP | AGC_ FAST | Reserved | AGC_TIME[1:0] | | AGC1_S TEP | CAL |
| Initial Value | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |

AGC_KEEP : The function of AGC1/2 gain keeping

When the AGC function is active, the gain setting of AGC1/2 is kept during AGC_KEEP="1".On the other hand, the gain setting of AGC1/2 is changed by IFIP signal during AGC_KEEP="0".

0: The gain setting of AGC1/2 is changed by IFIP signal. (default)

1: The gain setting of AGC1/2 is kept.

Note: When setting the operation mode 4,5,6,7, AGC_KEEP is available.

AGC_FAST : AGC control switching

0: The time constant of response time is changed by conditions that AGC1/AGC2 output level converges between the upper limit and lower limit(convergence) or not(attack/release).
attack/release : AGC response time is the same as AGC_TIME[1:0]="00".
convergence : AGC response time is set with ACG_TIME[1:0].
This setting provides the fast response time that can be followed the burst signal. (recommended)

1: AGC control is operated with AGC response time described in AGC_TIME[1:0]. (default)

Note : The response speed of AGC must be set to AGC_FAST=0, AGC_TIME[1:0]="11", AGC1_STEP=0. ACS (Adjacent Channel Selectivity) performance is optimized by preventing the periodic operation due to a strong unwanted signal.

AGC_TIME[1:0]: AGC response time setting
This register set response time for AGC1 gain and AGC2 gain to change by 1step.

| AGC_TIME [1] | AGC_TIME [0] | AGC response time [ms] | | | | | |
|---|---|---|---|---|---|---|---|
| | | AGC1_STEP=0 setting | | | AGC1_STEP=1 setting | | |
| | | State A | State B | State C | State A | State B | State C |
| 0 | 0 | 0.56 | 8.50 | 8.50 | 0.38 | 4.35 | 4.35 |
| 0 | 1 | 0.92 | 8.79 | 8.79 | 0.56 | 4.50 | 4.50 |
| 1 | 0 | 1.64 | 9.37 | 9.37 | 0.93 | 4.79 | 4.79 |
| 1 | 1 | 3.08 | 10.52 | 10.52 | 1.66 | 5.38 | 5.38 |

Note 1: Values above indicate response time during AGC gain changes from maximum to minimum or from minimum to maximum.
Note 2: The response speed of AGC must be set to AGC_FAST=0, AGC_TIME[1:0]="11", AGC1_STEP=0. ACS (Adjacent Channel Selectivity) performance is optimized by preventing the periodic operation due to a strong unwanted signal.

State A: AGC1 output level is beyond the upper limit.
State B: AGC1 output level is within the upper limit and AGC2 output level is beyond the upper limit.
State C: AGC2 output level is under the lower limit.

| Data | Function | Operation | | Notes |
|---|---|---|---|---|
| | | 0 | 1 | |
| AGC1_STEP | AGC1 gain switching range setting (Note1) | ±1dB(recommended) | ±2dB | |
| CAL | Discriminator circuit calibration start trigger (Note2) | Invalid | Start | |

Note 1: The response speed of AGC must be set to AGC_FAST=0, AGC_TIME[1:0]="11", AGC1_STEP=0. ACS (Adjacent Channel Selectivity) performance is optimized by preventing the periodic operation due to a strong unwanted signal.
Note 2: calibration is performed synchronized with the rising edge of {CAL}. After calibration is completed, this register is set to "0" automatically. It takes 1.3ms before calibration is completed.
Refer to "calibration procedure" for further information.

Address 0x03 (Control Register 3)

| Name | D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0(LSB) |
|---|---|---|---|---|---|---|---|---|
| Control Register 3 | Reserved | | | | | | IFOG[1:0] | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

IFOG[1:0]: IFBUF Gain setting

| IFOG [1] | IFOG [0] | IFBUF Gain[dB] |
|---|---|---|
| 0 | 0 | 6 |
| 0 | 1 | 9 |
| 1 | 0 | 12 |
| 1 | 1 | 15 |

Address 0x04 (Software Reset)

| Name | D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0(LSB) |
|---|---|---|---|---|---|---|---|---|
| Software-reset | SRST[7:0] | | | | | | | |
| Initial Value | — | — | — | — | — | — | — | — |

When data 0x04:10101010 is written to the SRST[7:0] register, software reset is performed.
Refer to System Reset for further information.

Address 0x0B (Control Register 4)

| Name | D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0(LSB) |
|---|---|---|---|---|---|---|---|---|
| Control Register 4 | BPF_BW [2] | AGC_ OFF | AGC1_G[5:0] | | | | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

| Data | Function | Operation | | Notes |
|---|---|---|---|---|
| | | 0 | 1 | |
| BPF_BW[2] | F0 (±7.5kHz) | OFF | ON | |
| AGC_ OFF | AGC function | Disable (AGC Auto operation) | Enable (AGC manual operation) | |
| AGC1_G[5:0] | AGC1 gain adjustment | 21 to -19dB by 1dB step | | Available only {AGC_OFF}=1 |

| AGC1_G[5] | AGC1_G[4] | AGC1_G[3] | AGC1_G[2] | AGC1_G[1] | AGC1_G[0] | Gain [dB] |
|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 | 1 | 21 |
| 0 | 1 | 0 | 1 | 0 | 0 | 20 |
| 0 | 1 | 0 | 0 | 1 | 1 | 19 |
| 0 | 1 | 0 | 0 | 1 | 0 | 18 |
| 0 | 1 | 0 | 0 | 0 | 1 | 17 |
| 0 | 1 | 0 | 0 | 0 | 0 | 16 |
| 0 | 0 | 1 | 1 | 1 | 1 | 15 |
| 0 | 0 | 1 | 1 | 1 | 0 | 14 |
| 0 | 0 | 1 | 1 | 0 | 1 | 13 |
| 0 | 0 | 1 | 1 | 0 | 0 | 12 |
| 0 | 0 | 1 | 0 | 1 | 1 | 11 |
| 0 | 0 | 1 | 0 | 1 | 0 | 10 |
| 0 | 0 | 1 | 0 | 0 | 1 | 9 |
| 0 | 0 | 1 | 0 | 0 | 0 | 8 |
| 0 | 0 | 0 | 1 | 1 | 1 | 7 |
| 0 | 0 | 0 | 1 | 1 | 0 | 6 |
| 0 | 0 | 0 | 1 | 0 | 1 | 5 |
| 0 | 0 | 0 | 1 | 0 | 0 | 4 |
| 0 | 0 | 0 | 0 | 1 | 1 | 3 |
| 0 | 0 | 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | -1 |
| 1 | 1 | 1 | 1 | 1 | 0 | -2 |
| 1 | 1 | 1 | 1 | 0 | 1 | -3 |
| 1 | 1 | 1 | 1 | 0 | 0 | -4 |
| 1 | 1 | 1 | 0 | 1 | 1 | -5 |
| 1 | 1 | 1 | 0 | 1 | 0 | -6 |
| 1 | 1 | 1 | 0 | 0 | 1 | -7 |
| 1 | 1 | 1 | 0 | 0 | 0 | -8 |
| 1 | 1 | 0 | 1 | 1 | 1 | -9 |
| 1 | 1 | 0 | 1 | 1 | 0 | -10 |
| 1 | 1 | 0 | 1 | 0 | 1 | -11 |
| 1 | 1 | 0 | 1 | 0 | 0 | -12 |
| 1 | 1 | 0 | 0 | 1 | 1 | -13 |
| 1 | 1 | 0 | 0 | 1 | 0 | -14 |
| 1 | 1 | 0 | 0 | 0 | 1 | -15 |
| 1 | 1 | 0 | 0 | 0 | 0 | -16 |
| 1 | 0 | 1 | 1 | 1 | 1 | -17 |
| 1 | 0 | 1 | 1 | 1 | 0 | -18 |
| 1 | 0 | 1 | 1 | 0 | 1 | -19 |

Note: Do not set the combination of the code which is not defined in the table given above.

Address 0x0C (Control Register 5)

| Name | D7(MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0(LSB) |
|---|---|---|---|---|---|---|---|---|
| Control Register 5 | Reserved | | | AGC2_G[4:0] | | | | |
| Initial Value | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Data | Function | Operation | | Notes |
|---|---|---|---|---|
| | | 0 | 1 | |
| AGC2_G[4:0] | AGC2 gain adjustment | 12 to 0dB by 1dB step | | Available only {AGC_OFF}=1 |

| AGC2_G[4] | AGC2_G[3] | AGC2_G[2] | AGC2_G[1] | AGC2_G[0] | Gain [dB] |
|---|---|---|---|---|---|
| 0 | 1 | 1 | 0 | 0 | 12 |
| 0 | 1 | 0 | 1 | 1 | 11 |
| 0 | 1 | 0 | 1 | 0 | 10 |
| 0 | 1 | 0 | 0 | 1 | 9 |
| 0 | 1 | 0 | 0 | 0 | 8 |
| 0 | 0 | 1 | 1 | 1 | 7 |
| 0 | 0 | 1 | 1 | 0 | 6 |
| 0 | 0 | 1 | 0 | 1 | 5 |
| 0 | 0 | 1 | 0 | 0 | 4 |
| 0 | 0 | 0 | 1 | 1 | 3 |
| 0 | 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 |

Note: Do not set the combination of the code which is not defined in the table given above.

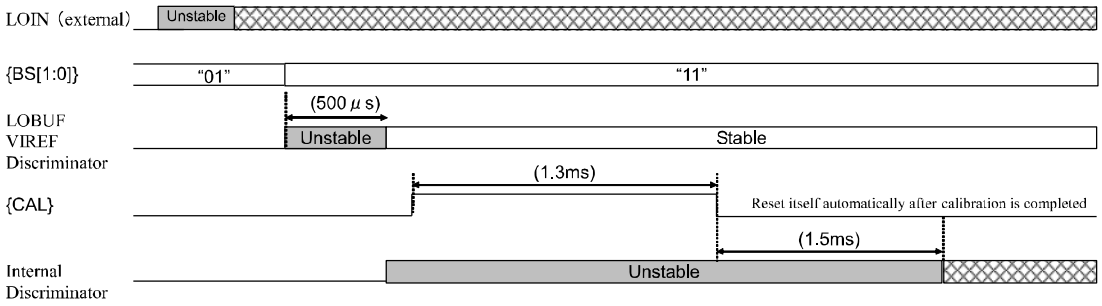
# 16. Calibration Procedure

AK2365A employs a function to calibrate free-running frequency of VCO in Discriminator and demodulated signal level. Before starting RX Operation, calibration is required in order to acquire proper VCO operation range and demodulated signal level.

Following procedure is required before calibration.

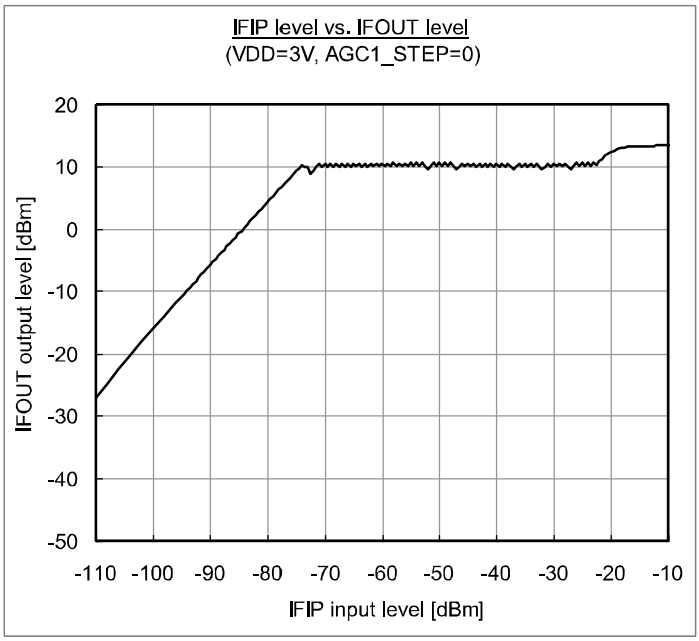
<1> Start up the external TCXO and continuously supply LO signal to AK2365A.
<2> Set “110” to 0x01 {BS[2:0]} and start up all circuits. After this operation, the circuits necessary for calibration (LOBUF, VIREF, Discriminator) will be powered on and calibration can be possible in 500us.
<3> Calibration is begun by setting "1" to address 0x02 {CAL}. When the calibration is executed once, the calibration operation cannot be stopped excluding master reset. Even if "0" is written in {CAL}, the calibration is completely executed.
<4> Calibration data is maintained excluding the time when the master reset is executed or DVDD power supply is down.
<5> It takes 1.5ms for Discriminator to become steady after the calibration is completed.

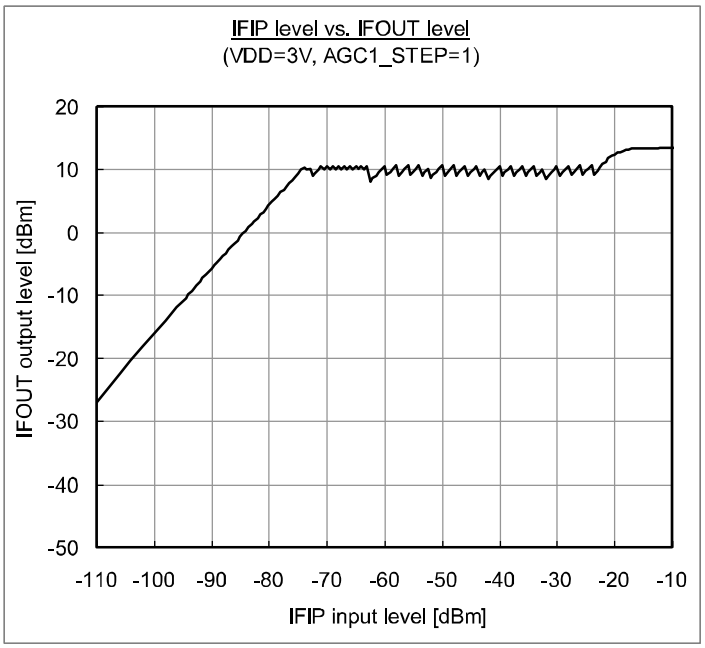
Power-up sequence recommendation



# 17. AGC Operation

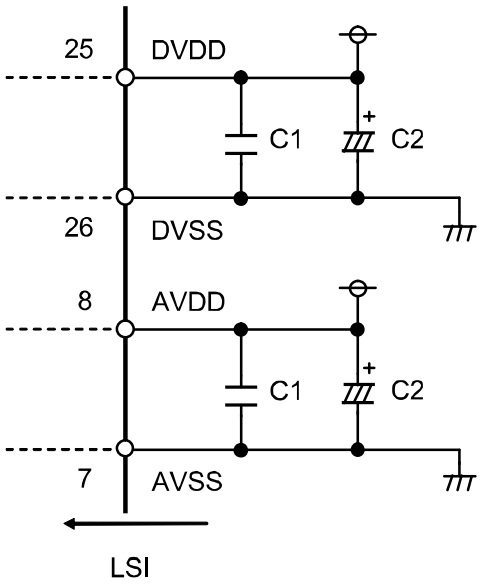
AK2365A has two AGC circuits, AGC1 and AGC2. The signal level from IFIP pin is adjustable automatically by AGC1/2. The following graphs show IFIP input vs. IFOUT output characteristics by setting {AGC1_STEP}=0/1, {IFOG[1:0]}=00, {AGC_OFF}=0. Setting {AGC_OFF}=1 can disable automatic gain adjustable operation and also enable manual gain operation by {AGC1_G[5:0]}, {AGC2_G[4:0]} registers.



## 18. Recommended External Application Circuits

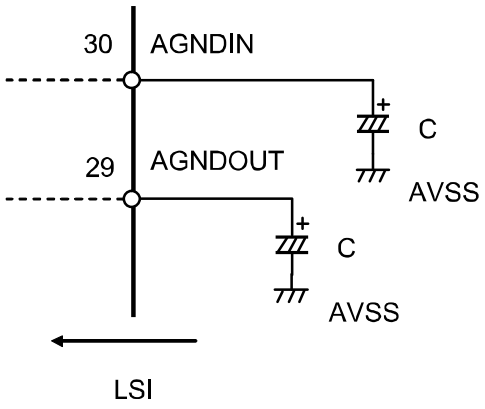
1) Power supply stabilizing capacitors
Connect capacitors between VDD and VSS pins to eliminate ripple and noise included in power supply. For maximum effect, the capacitors should be placed at a shortest distance between the pins.




C1=0.1μF (Ceramic cap)

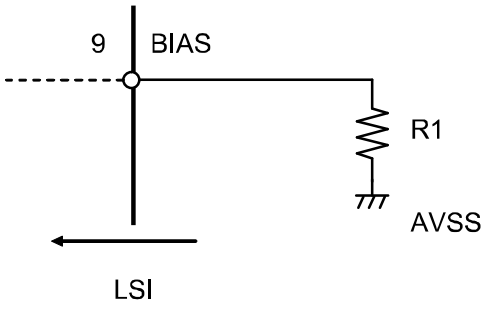
C2=10μF (Electrolytic cap)

2) AGND stabilizing capacitors
It is recommended that capacitors with 1μF or lager be connected between VSS and the AGND and AGNDIN pins to stabilize the AGND signal. The capacitors must be placed as close to the pins as possible.



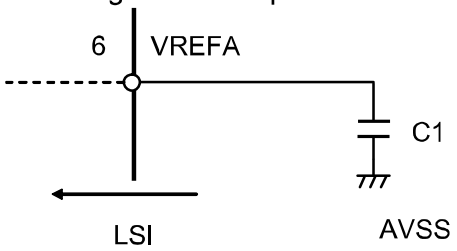

C=1μF (Electrolytic capacitor)

3) BIAS pin



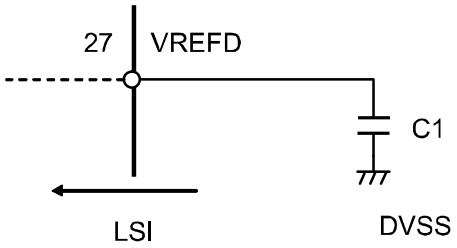

R1=47kΩ±1%

4) VREFA output
It is recommended that capacitors with 220nF or lager be connected between AVSS and VREFA pin to stabilize the VREFA signal. The capacitors must be placed as close to the pins as possible.



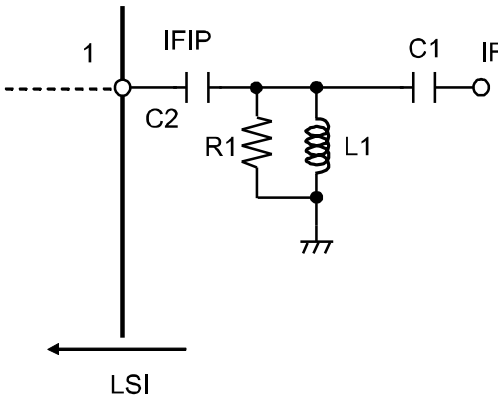

C1=220nF

5) VREFD output
It is recommended that capacitors with 220nF or lager be connected between DVSS and VREFD pin to stabilize the VREFD signal. The capacitors must be placed as close to the pins as possible.



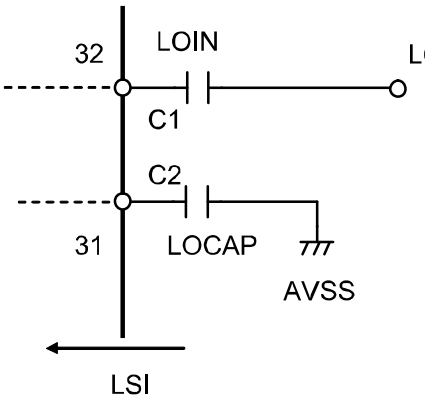

C1=220nF

6) MIX



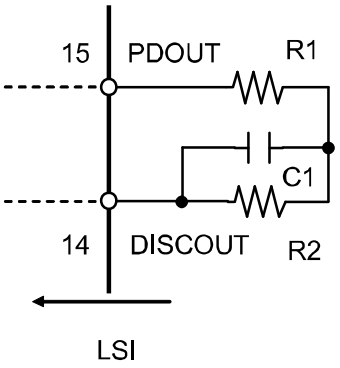

C1=22pF, L1=470nH for 45.9±0.45MHz
C1=18pF, L1=470nH for 50.4±0.45MHz
C1=13pF, L1=470nH for 57.6±0.45MHz
C2=10nF
R1=750Ω

7) LOIN




C1=C2=100pF

8) Discriminator



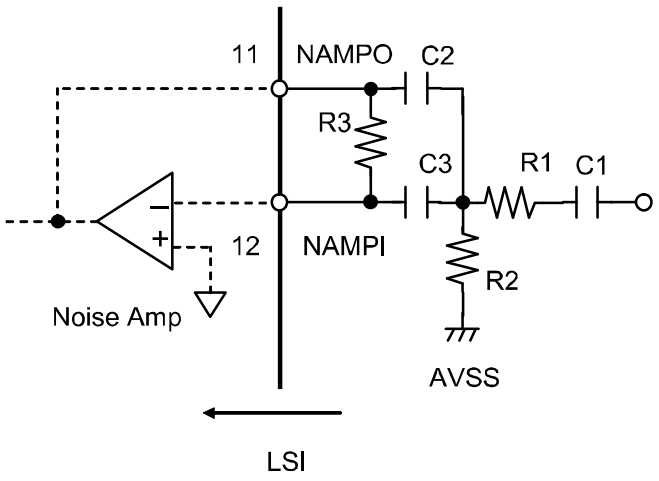

C1=1000pF

R1=220kΩ

R2=1MΩ

9) Noise AMP

The following gives a sample configuration of a BPF when input frequency is 31kHz.
Some parameters can be calculated using following (1) to (3) equations.




C1=0.47uF

C2=C3=220pF

R1=10kΩ

R2=5.6kΩ

R3=150kΩ

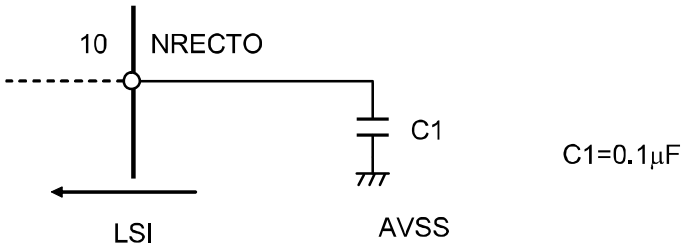
$$(1) \quad f_0 = \frac{1}{2\pi\sqrt{R_3(R_1 // R_2)C_2C_3}}$$

$$(2) \quad G_v = \frac{R_3}{2R_1}$$

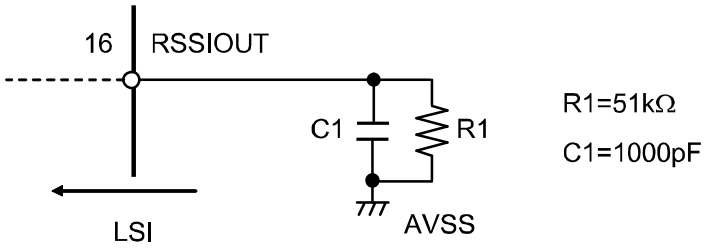
$$(3) \quad Q^2 = \frac{R_3}{4(R_1 // R_2)}$$

10) NECTO pin

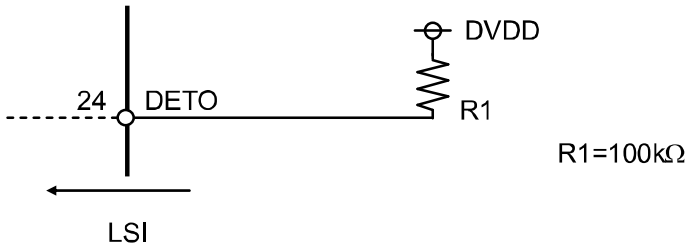
Rise time of noise detection is proportionate to C1=0.1μF and internal resistance 75kΩ




11) RSSIOUT pin

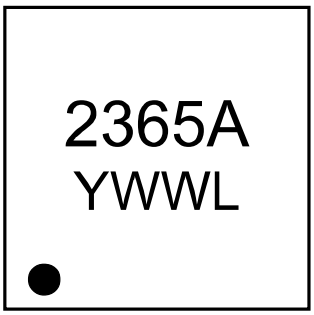



12) DETO



# 19. Packaging

☐ Marking




[Contents of YWWL]

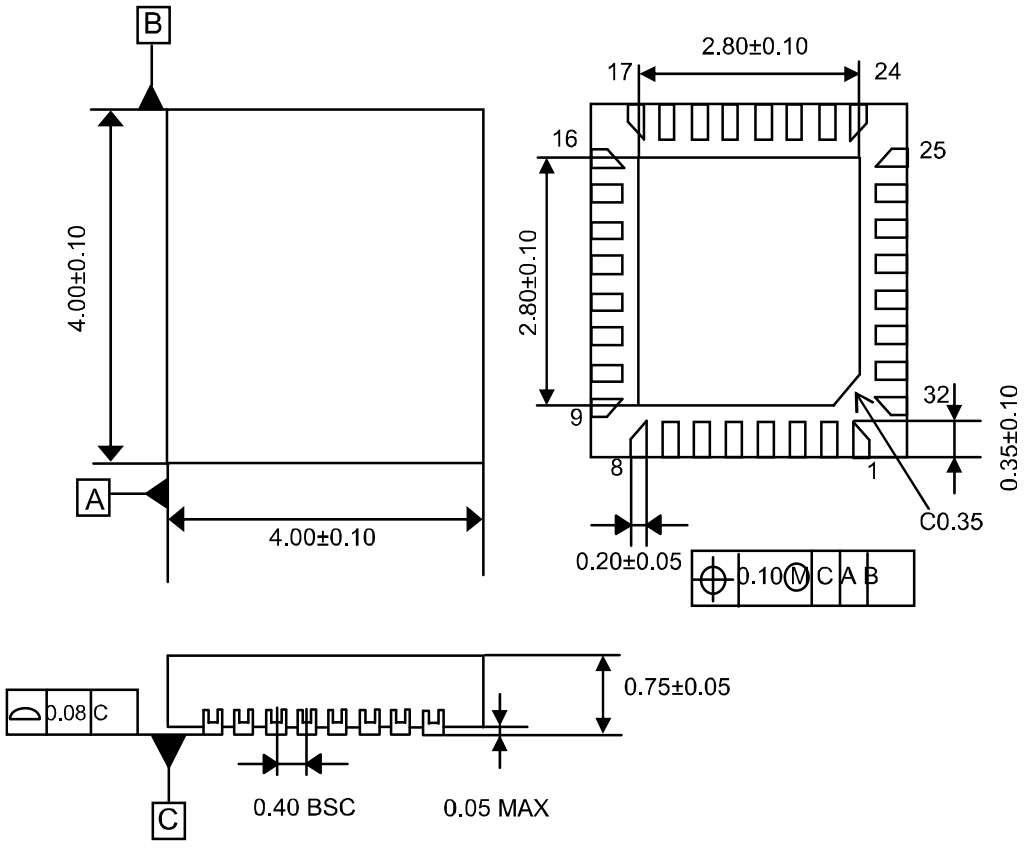
Y: Last digit of calendar year. (Year 2011->1, 2012->2)

WW: Manufacturing week number.

L: Lot identification, given to each product lot which is made in a week.
LOT ID is given in alphabetical order (A, B, C…).

☐ Mechanical Outline

Package: 32pin QFN (4.0 x 4.0 x 0.7mm, 0.4mm pitch)




Note) The exposure pad(Exposed Pad) of the center of the package back is connected to opening or VSS.

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## ●Related Parts

| Part# | Discription | Comments |
|---|---|---|
| Mixer | | |
| AK1220 | 100MHz~900MHz High Linearity Down Conversion Mixer | IIP3:+22dBm |
| AK1222 | 100MHz~900MHz Low Power Down Conversion Mixer | IDD:2.9mA |
| AK1224 | 100MHz~900MHz Low Noise, High Liniarity Down Conversion Mixer | NF:8.5dB, IIP3:+18dBm |
| AK1228 | 10MHz~2GHz Up/Down Conversion Mixer | 3V Supply, NF:8.5dB |
| AK1221 | 0.7GHz~3.5GHz High Linearity Down Conversion Mixer | IIP3:+25dBm |
| AK1223 | 3GHz~8.5GHz High Linearity Down Conversion Mixer | IIP3:+13dB, NF:15dB |
| PLL Synthesizer | | |
| AK1541 | 20MHz~600MHz Low Power Fractional-N Synthesizer | IDD:4.6mA |
| AK1542A | 20MHz~600MHz Low Power Integer-N Synthesizer | IDD:2.2mA |
| AK1543 | 400MHz~1.3GHz Low Power Fractional-N Synthesizer | IDD:5.1mA |
| AK1544 | 400MHz~1.3GHz Low Power Integer-N Synthesizer | IDD:2.8mA |
| AK1590 | 60MHz~1GHz Fractional-N Synthesizer | IDD:2.5mA |
| AK1545 | 0.5GHz~3.5GHz Integer-N Synthesizer | 16-TSSOP |
| AK1546 | 0.5GHz~3GHz Low Phase Noise Integer-N Synthesizer | Normalized C/N:-226dBc/Hz |
| AK1547 | 0.5GHz~4GHz Integer-N Synthesizer | 5V Supply |
| AK1548 | 1GHz~8GHz Low Phase Noise Integer-N Synthesizer | Normalized C/N:-226dBc/Hz |
| IFVGA | | |
| AK1291 | 100~300MHz Analog Signal Control IF VGA w/ RSSI | Dynamic Range:30dB |
| integrated VCO | | |
| AK1572 | 690MHz~4GHz Down Conversion Mixer with Frac.-N PLL and VCO | IIP3:24dBm,<br>-111dBc/Hz@100kHz |
| AK1575 | 690MHz~4GHz Up Conversion Mixer with Frac.-N PLL and VCO | IIP3:24dBm,<br>-111dBc/Hz@100kHz |
| IF Reciever (2nd Mixer + IF BPF + FM Detector) | | |
| AK2364 | Built-in programmable AGC+BPF, FM detector IC | IFBPF:±10kHz ~ ±4.5kHz |
| AK2365A | Built-in programmable AGC+BPF, IFIC | IFBPF:±7.5kHz ~ ±2kHz |
| Analog BB for PMR/LMR | | |
| AK2345C | CTCSS Filter, Encoder, Decoder | 24-VSOP |
| AK2360/<br>AK2360A | Inverted frequency(3.376kHz/3.020kHz) scrambler | 8-SON |
| AK2363 | MSK Modem/DTMF Receiver | 24-QFN |
| AK2346B | 0.3-2.55/3.0kHz Analog audio filter, | 24-VSOP |
| AK2346A | Emphasis, Compandor, scrambler, MSK Modem | 24-QFN |
| AK2347B | 0.3-2.55/3.0kHz Analog audio filter<br>Emphasis, Compandor, scrambler, CTCSS filter | 24-VSOP |
| Function IC | | |
| AK2330 | 8-bit 8ch Electronic Volume | VREF can be selected for each channel |
| AK2331 | 8-bit 4ch Electronic Volume | VREF can be selected for each channel |

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