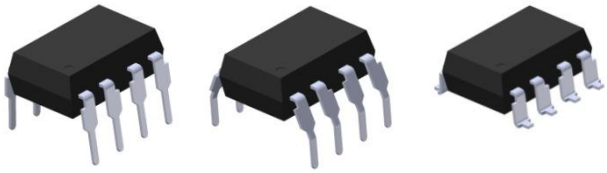
DATASHEET

8 PIN DIP HIGH SPEED LOW INPUT CURRENT LOGIC GATE PHOTOCOUPLER EL220X SERIES



Features

- 1kV/μs min. common mode transient immunity
- Guaranteed performance from -40 to 85℃
- Wide V_{CC} range (4.5V to 20V)
- 5Mbd typical signal rate
- Low input current (1.6mA)
- High isolation voltage between input and output (Viso = 5000 V rms)
- Pb free and RoHS compliant.
- UL 1577 approved (No. 214129)
- VDE approved (No. 40028391)
- SEMKO approved
- NEMKO approved
- DEMKO approved
- FIMKO approved

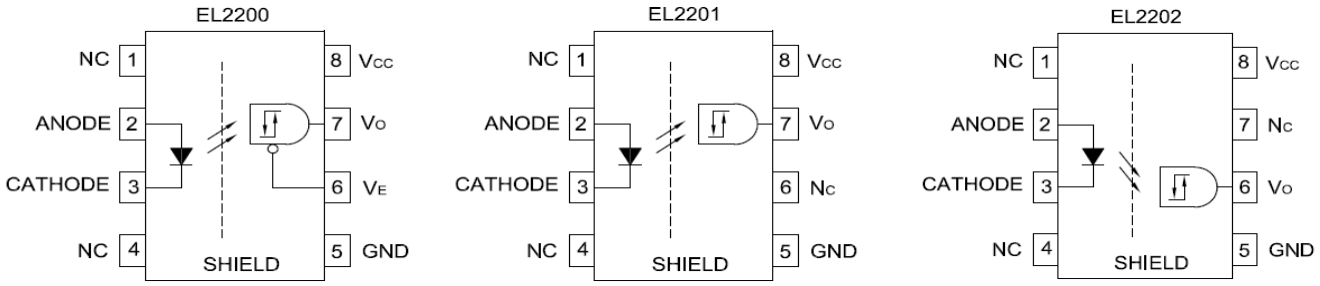
Description

The EL220X are consists of an infrared emitting diode optically coupled to a high speed integrated photo detector logic gate. It is packaged in an 8-pin DIP package and available in SMD options. The detector of EL2200 has a three state output stage and has a detector threshold with hysteresis. The three state output eliminates the need for a pull up resistor and allows for direct drive of data busses. The hysteresis provides differential mode noise immunity and eliminates the potential for output signal chatter.

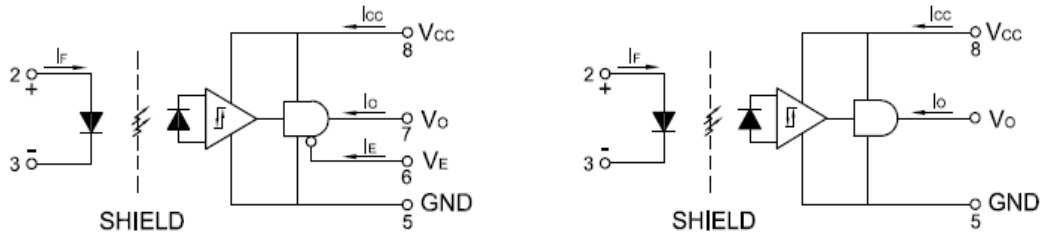
Applications

- Ground Loop Elimination
- LSTTL to LSTTL or CMOS
- Line Receiver, Data Transmission
- Isolated Buss Driver
- Pulse Transformer Replacement
- Microprocessor System Interface
- Computer Peripheral Interface
- High Speed Logic Ground Isolation

Functional Diagram



Schematic



EL2200 EL2201/02

Truth Table

EL2200

Input	Enable	Output
H	H	Z
L	H	Z
H	L	H
L	L	L

EL2201/02

Input	Output
H	H
L	L

Absolute Maximum Ratings (T_A=25℃)

Parameter		Symbol	Rating	Unit
Input	Forward Current	I_F	50	mA
	Reverse Voltage	V_R	5	V
	Three State Enable Voltage	V_E	20	V
Output	Output Current	I_O	25	mA
	Output Voltage	V_O	20	V
	Supply Voltage	V_{CC}	20	V
Total Package Power dissipation(Note 1)		P_T	210	mW
Isolation Voltage (Note 2)		V_{ISO}	5000	V rms
Operating Temperature		T_{OPR}	-40 ~ +85	°C
Storage Temperature		T_{STG}	-55 ~ +125	°C
Soldering Temperature (Note 3)		T_{SOL}	260	°C

Electrical Characteristics (T_A = -40 to 85°C, V_{CC} = 4.5V to 20V, $I_{F(ON)}$ = 1.6mA to 5mA, V_{EH} = 2V to 20V, V_{EL} = 0V to 0.8V, $I_{F(OFF)}$ = 0mA unless otherwise specified) (Note 4)

Input

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Forward Voltage	V_F	-	1.4	1.7	V	I_F = 5mA
Reverse Voltage	V_R	5.0	-	-	V	I_R = 10μA
Temperature Coefficient of Forward Voltage	$\Delta V_F/\Delta T_A$	-	-1.8	-	mV/°C	I_F =10mA
Input Capacitance	C_{IN}	-	60	-	pF	V_F=0, f=1MHz

Output

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition	
High Level Supply Current	I_{CCH}	-	2.3	4.5	mA	V_{CC}=5.5V	I_F=5mA,I_O=Open V_E=Don't care
			3	6		V_{CC}=20V	
Low Level Supply Current	I_{CCL}	-	3.7	6	mA	V_{CC}=5.5V	I_F=0mA,I_O=Open V_E=Don't care
			4.5	7.5		V_{CC}=20V	
High Level Enable Current(EL2200 only)	I_{EL}	-	- 0.1	-0.32	mA	V_E=0.4V	
Low Level Enable Current(EL2200 only)	I_{EH}	-	-	20	μA	V_E=2.7V	
		-	-	100		V_E=5.5V	
		-	0.005	250		V_E=20V	
High Level Enable Voltage(EL2200 only)	V_{EH}	2.0	-	-	V		
Low Level Enable Voltage(EL2200 only)	V_{EL}	-	-	0.8	V		

Transfer Characteristics (T_A = -40 to 85°C, V_{CC} = 4.5V to 20V, $I_{F(ON)}$ = 1.6mA to 5mA, V_{EH} = 2V to 20V, V_{EL} = 0V to 0.8V, $I_{F(OFF)}$ = 0mA unless otherwise specified) (Note 4)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition	
Output Leakage Current	I_{OHH}	-	1.5	100	μA	V_O=5.5V	V_{CC}=4.5V, I_F=5mA
			2	500		V_O=20V	
Low Level Output Current	V_{OL}	-	0.33	0.5	V	V_{CC} = 4.5V, I_F=0mA, V_E=0.4V, I_{OL}=6.4mA	
Input Threshold Current	I_{FT}	-	-	1.6	mA	V_{CC} = 4.5V, V_O = 0.5V, V_E = 0.4V, I_{OL} = 6.4mA	
Logic High Output Voltage	V_{OH}	2.4	V_{CC}-1.8	-	V	I_{OH} = -2.6mA	
High Impedance State Output Current (EL2200 only)	I_{OZL}	-	-	-20	μA	V_O = 0.4V, I_F = 5mA, V_{EN} = 2V	
	I_{OZH}	-	-	20	μA	V_O = 2.4V	I_F = 5mA, V_{EN} = 2V
		-	-	100		V_O = 5.5V	
		-	-	500		V_O = 20V	
Logic Low Short Circuit Output Current	I_{OSL}	25	-	-	mA	V_O = V_{CC} = 5.5V	I_F = 0mA (Note 5)
		40	-	-		V_O = V_{CC} = 20V	
Logic High Short Circuit Output Current	I_{OSH}	-10	-	-	mA	V_{CC} = 5.5V	I_F = 5mA, V_O = GND (Note 5)
		-25	-	-		V_{CC} = 20V	
Input Current Hysteresis	I_{HYS}	-	0.03	-	mA	V_{CC} = 4.5V	

Switching Characteristics (T_A = -40 to 85°C, V_{CC} = 4.5V to 20V, $I_{F(ON)}$ = 1.6mA to 5mA, $I_{F(OFF)}$ = 0mA unless otherwise specified) (Note 4)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition	
Propagation Delay Time to Output High Level	T_{PLH}	-	100	300	ns	(Note 6&8) , Fig. 11	
Propagation Delay Time to Output Low Level	T_{PHL}	-	105	300	ns	(Note 7&8), Fig. 11	
Output Rise Time	t_r	-	45	-	ns	(Note 9) , Fig. 11	
Output Fall Time	t_f	-	10	-	ns	(Note 10) , Fig. 11	
Enable Propagation Delay Time to Output High Level (EL2200 only)	t_{PZH}	-	20	-	ns	Fig. 12	
Enable Propagation Delay Time to Output Low Level (EL2200 only)	t_{PZL}	-	25	-	ns	Fig. 12	
Disable Propagation Delay Time to Output High Level (EL2200 only)	t_{PHZ}	-	130	-	ns	Fig. 12	
Disable Propagation Delay Time to Output Low Level (EL2200 only)	t_{PLZ}	-	35	-	ns	Fig. 12	
Common Mode Transient Immunity at Output High	CM_H	1000	-	-	V/µS	I_F=5mA V_{OH}(Min.)=2V (Note 11)	$\|V_{CM}\|$=50V V_{CC}=5V T_A = 25°C (Fig. 13)
Common Mode Transient Immunity at Output Low	CM_L	1000	-	-	V/µS	I_F=0mA V_{OL}(Max.)=2V (Note 12)	

Typical Electro-Optical Characteristics Curves

Figure 1. Input Forward Current vs. Forward Voltage

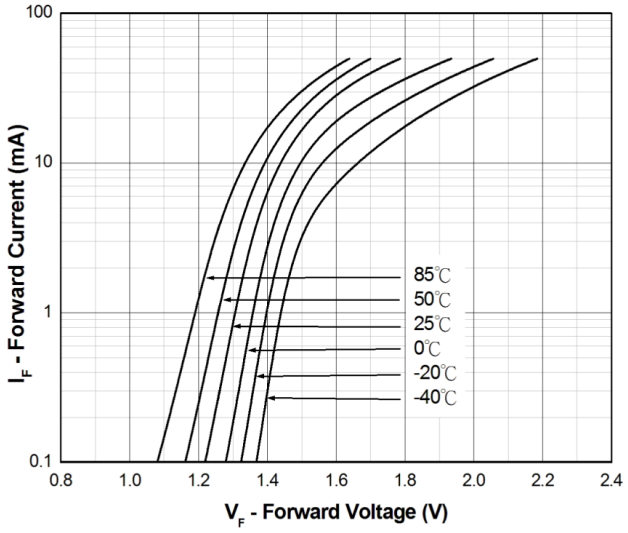


Figure 2. Output Voltage vs. Input Forward Current

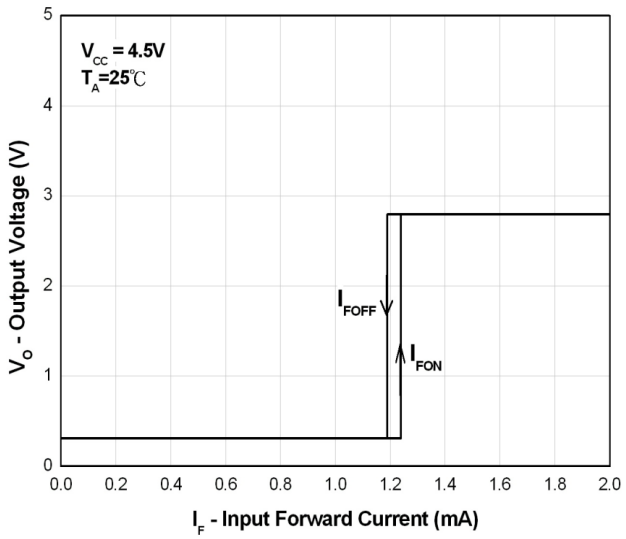


Figure 3. Input Threshold Current vs. Ambient Temperature

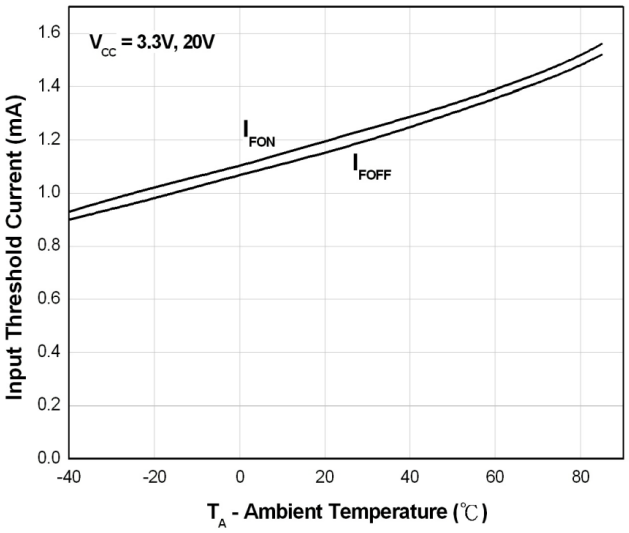


Figure 4. Logic Low Output Voltage vs. Ambient Temperature

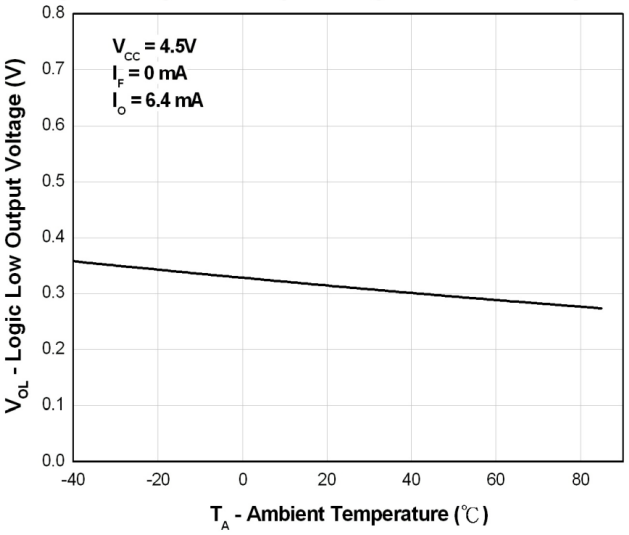


Figure 5. Logic High Output Voltage vs. Supply Voltage

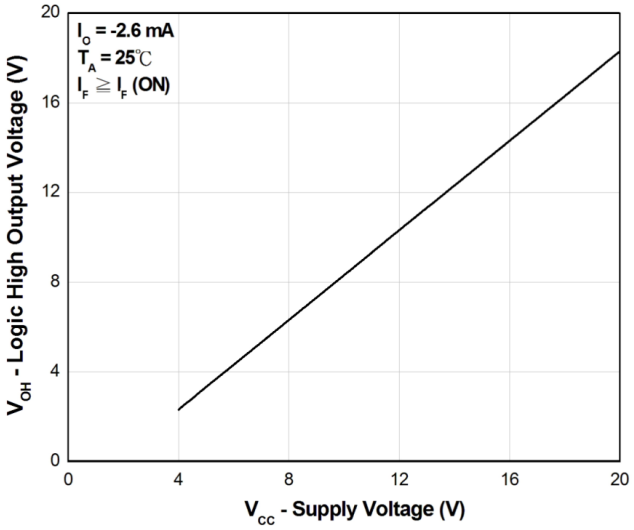


Figure 6. Logic High Output Current vs. Ambient Temperature

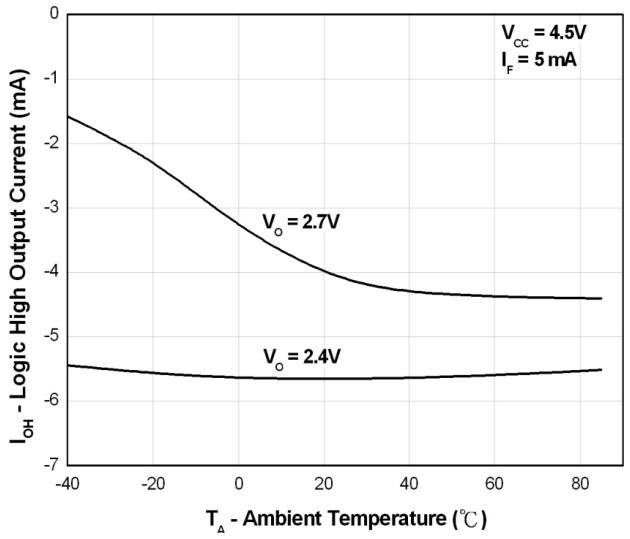


Figure 7. Propagation Delay vs. Ambient Temperature

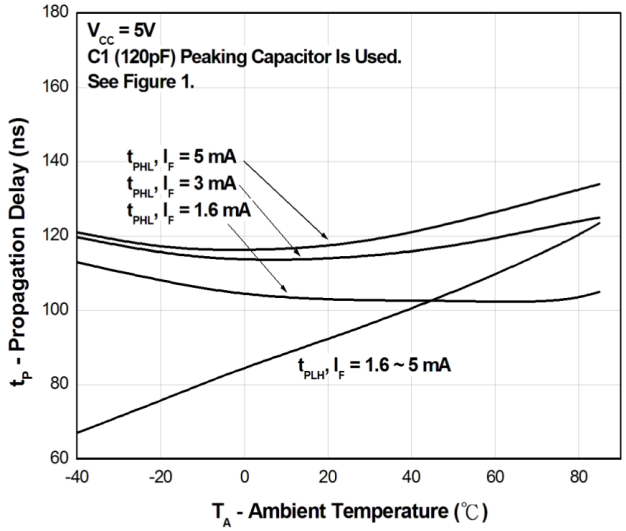


Figure 8. Typical Logic Low Enable Propagation Delay vs.Temperature.

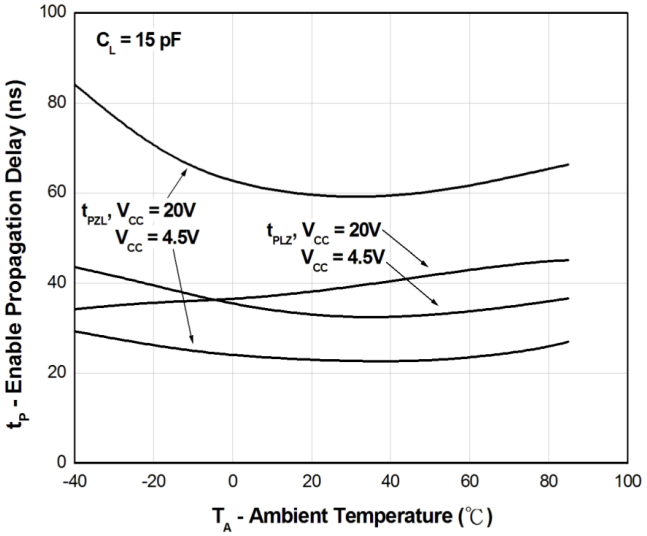


Figure 9. Typical Logic Low Enable Propagation Delay vs. Temperature.

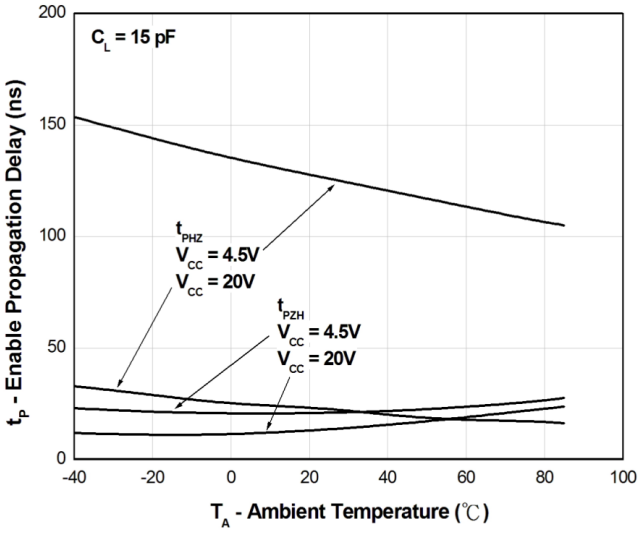
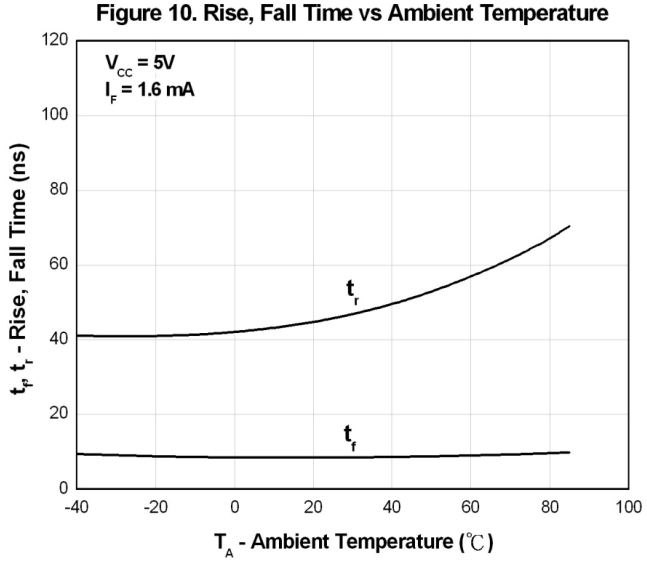
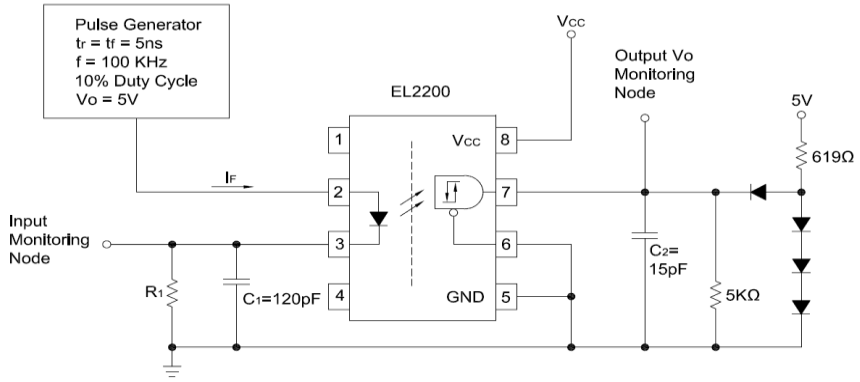


Figure 10. Rise, Fall Time vs Ambient Temperature





The Probe and Jig Capacitances are Included in C_1 and C_2
All Diodes are 1N916 and 1N3064.

R_1	2.25KΩ	1.2KΩ	720Ω
$I_{F(ON)}$	1mA	3mA	5mA

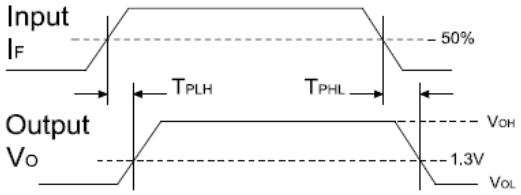


Fig. 11 Test Circuit and Waveforms for t_{PLH}, t_{PHL}, t_r, and t_f (Note 13)

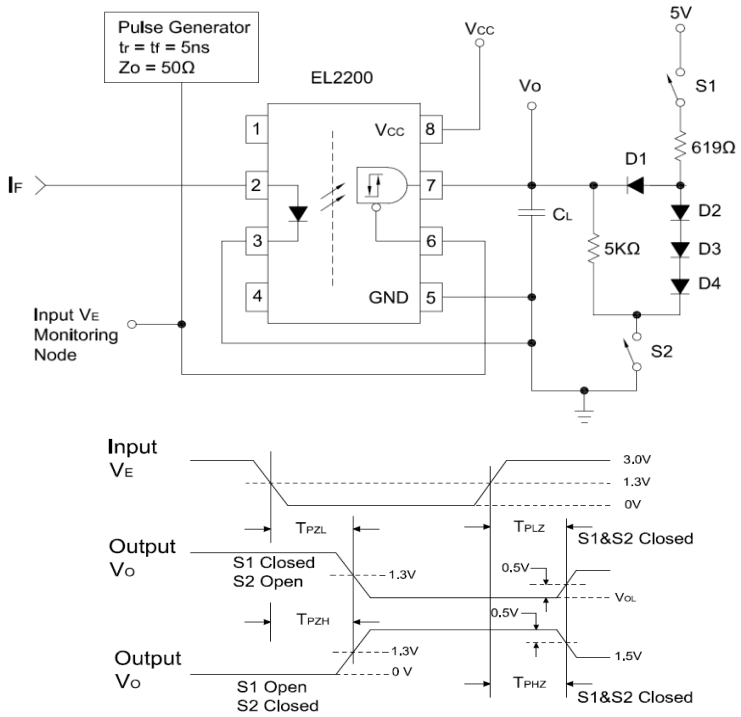


Fig. 12 Test Circuit and Waveform for t_{PHZ} and t_{PLZ}, t_{PLZ} and t_{PZL}

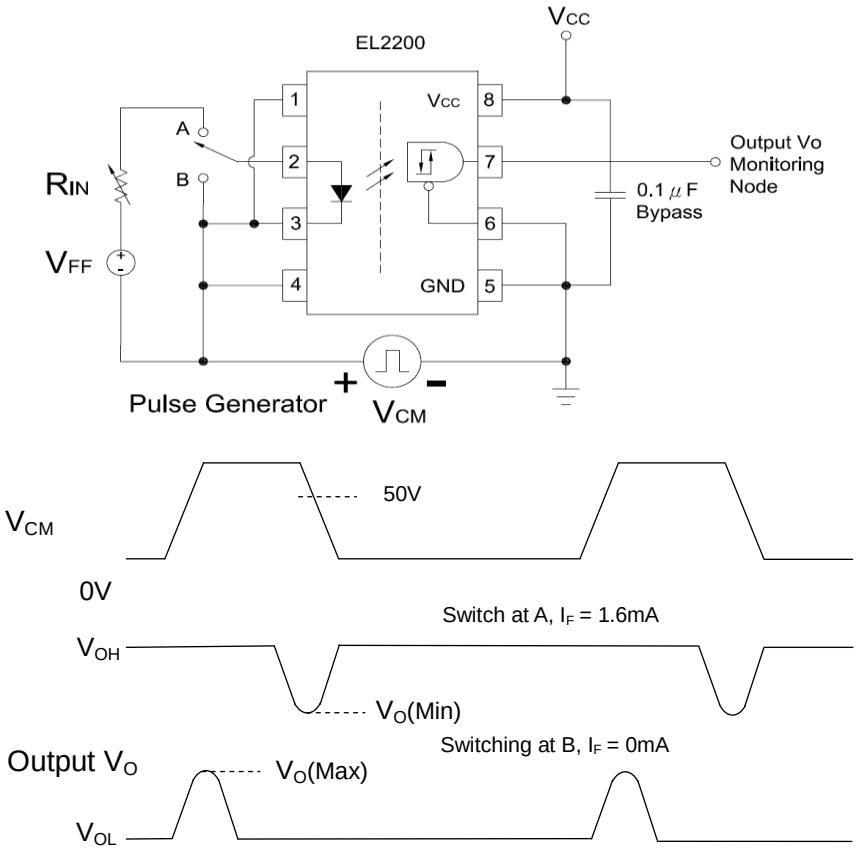


Fig. 13 Test Circuit Common Mode Transient Immunity (Note 13)

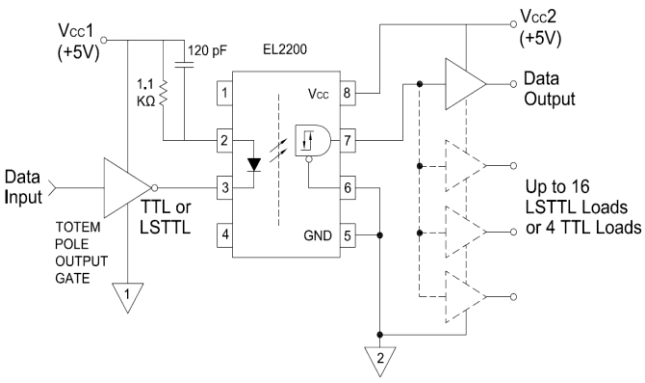


Fig. 14 Recommended LSTTL to LSTTL Circuit. (Note 13)

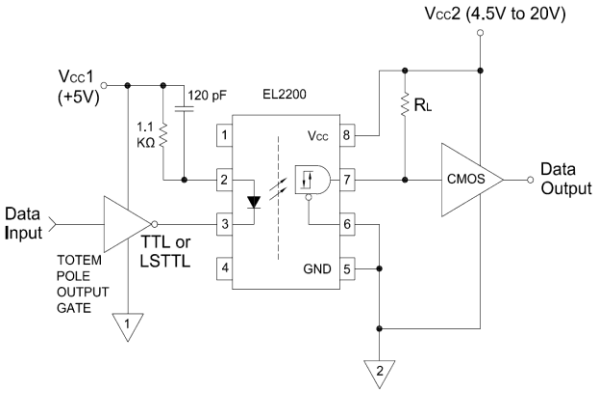


Fig. 15 LSTTL to CMOS Interface Circuit. (Note 13)

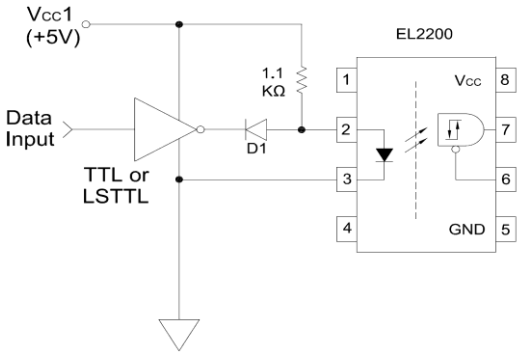


Fig. 16 Recommended LED Drive Circuit.

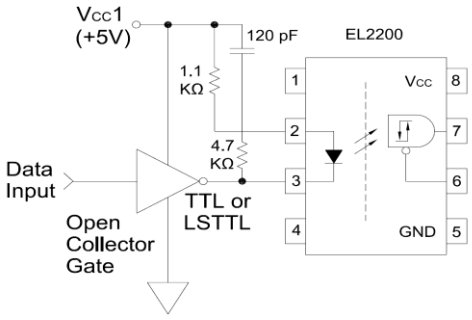


Fig. 17 Series LED Drive With Open Collector Gate. (4.7KΩ Resister Shunts I_{OH} from the LED)

Note

1. Derate total package power dissipation, PT, linearly above 70°C free air temperature at a rate of 4.5 mW/°C.
2. AC for 1 minute, R.H.= 40 ~ 60% R.H. In this test, pins 1, 2, 3 & 4 are shorted together, and pins 5, 6, 7 & 8 are shorted together.
3. For 10 seconds.
4. The VCC supply must be bypassed by a 0.1μF capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package V_{CC} and GND pins.
5. Duration of output short circuit time should not exceed 10 ms.
6. t_{PLH} – Propagation delay is measured from the 50% level on the LOW to HIGH transition of the input current pulse to the 1.3 V level on the LOW to HIGH transition of the output voltage pulse.
7. t_{PHL} – Propagation delay is measured from the 50% level on the HIGH to LOW transition of the input current pulse to the 1.3 V level on the HIGH to LOW transition of the output voltage pulse.
8. When the peaking capacitor is omitted, propagation delay times may increase by 100 ns.
9. t_r – Rise time is measured from the 10% to the 90% levels on the LOW to HIGH transition of the output pulse.
10. t_f – Fall time is measured from the 90% to the 10% levels on the HIGH to LOW transition of the output pulse.
11. CM_H – The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the HIGH state (i.e., V_{OUT} > 2.0V).
12. CM_L – The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the LOW output state (i.e., V_{OUT} < 0.8V).
13. For testing EL2201/02 the enable pin must be floating.

Order Information

Part Number

EL2200Y(Z)-V
EL2201Y(Z)-V
EL2202Y(Z)-V

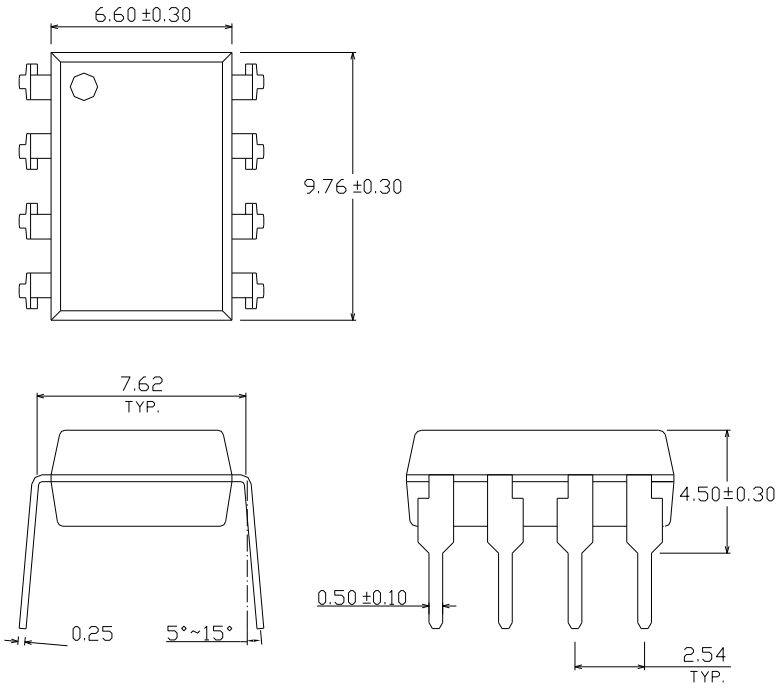
Note

Y = Lead form option (S, S1, M or none)
Z = Tape and reel option (TA, TB or none).
V = VDE (optional)

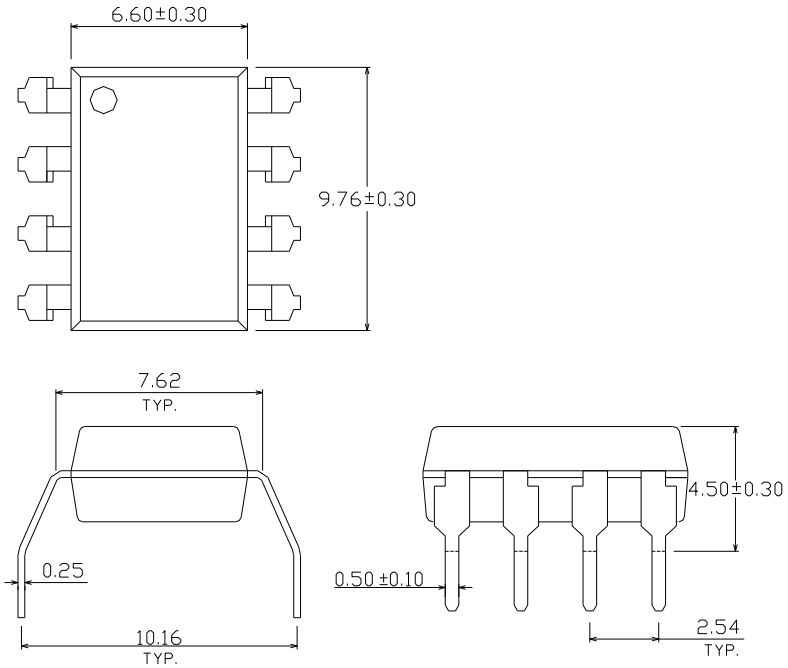
Option	Description	Packing quantity
None	Standard DIP-8	45 units per tube
M	Wide lead bend (0.4 inch spacing)	45 units per tube
S (TA)	Surface mount lead form + TA tape & reel option	1000 units per reel
S (TB)	Surface mount lead form + TB tape & reel option	1000 units per reel
S1 (TA)	Surface mount lead form (low profile) + TA tape & reel option	1000 units per reel
S1 (TB)	Surface mount lead form (low profile) + TB tape & reel option	1000 units per reel

Package Dimension
(Dimensions in mm)

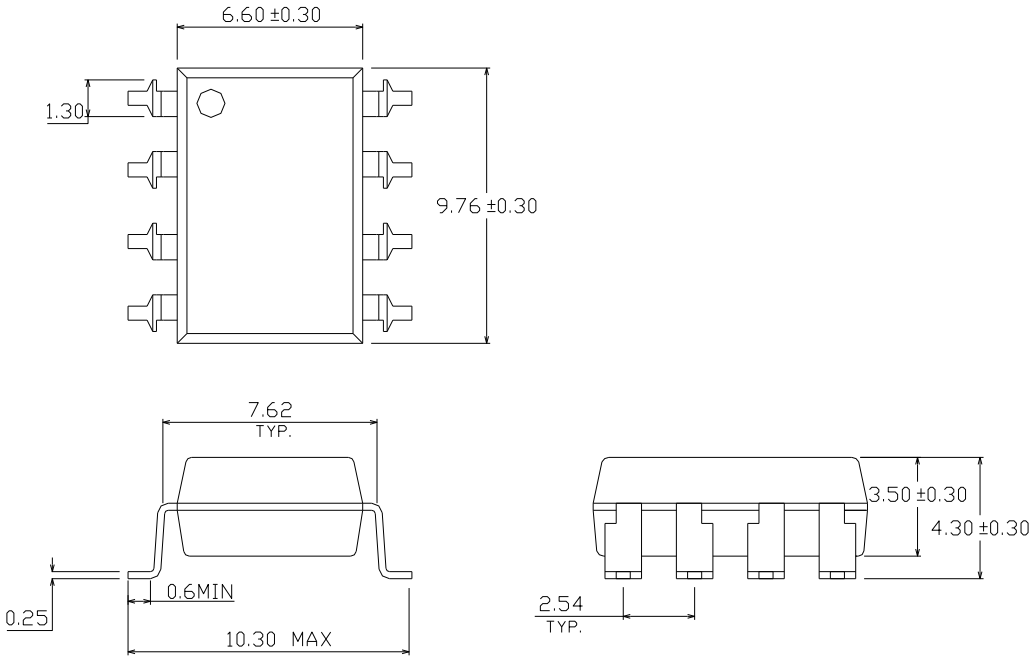
Standard DIP Type



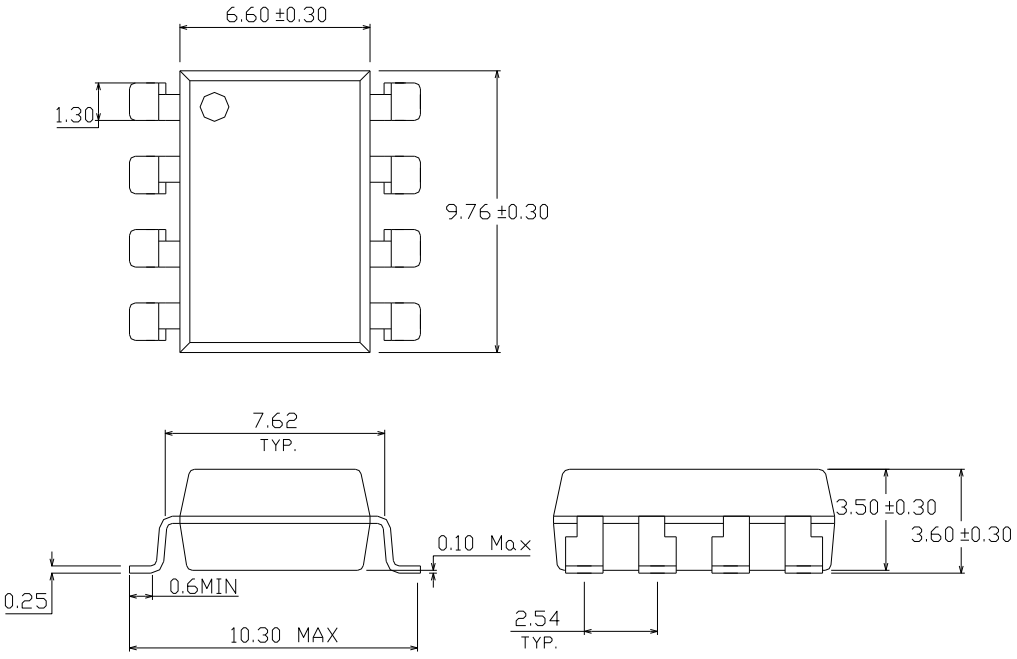
Option M Type



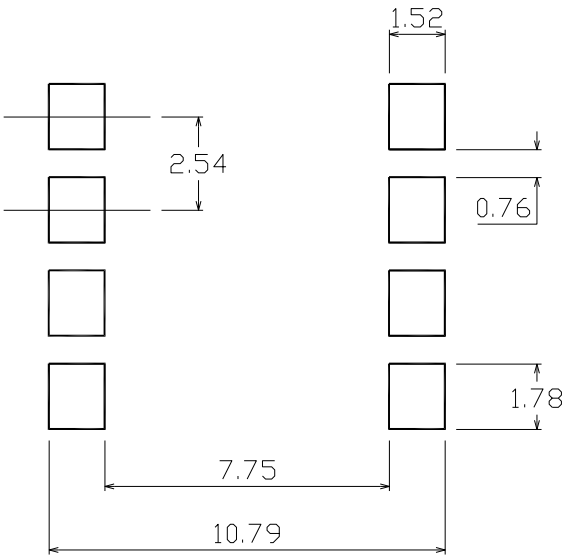
Option S Type



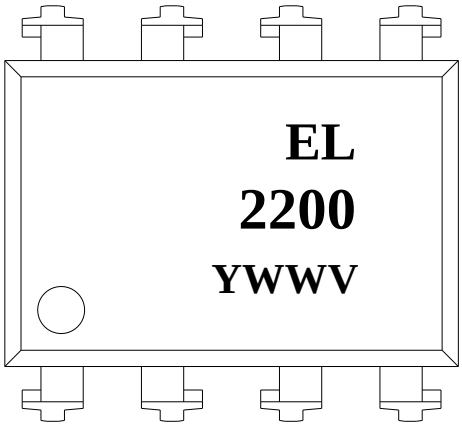
Option S1 Type



Recommended Pad Layout for Surface Mount Leadform



Device Marking

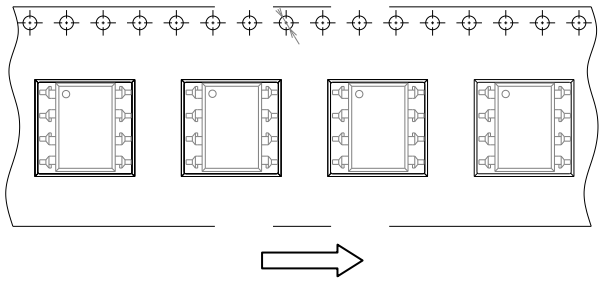


Notes

EL	denotes EVERLIGHT
2200	denotes Device Number
Y	denotes 1 digit Year code
WW	denotes 2 digit Week code
V	denotes VDE (optional)

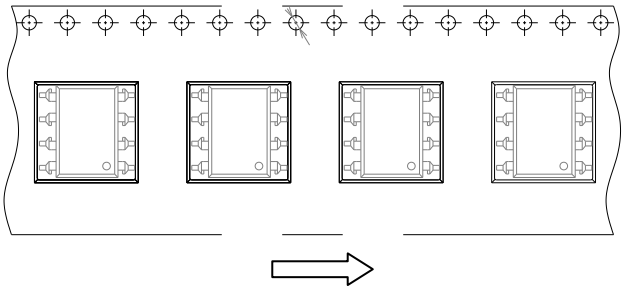
Tape & Reel Packing Specifications

Option TA



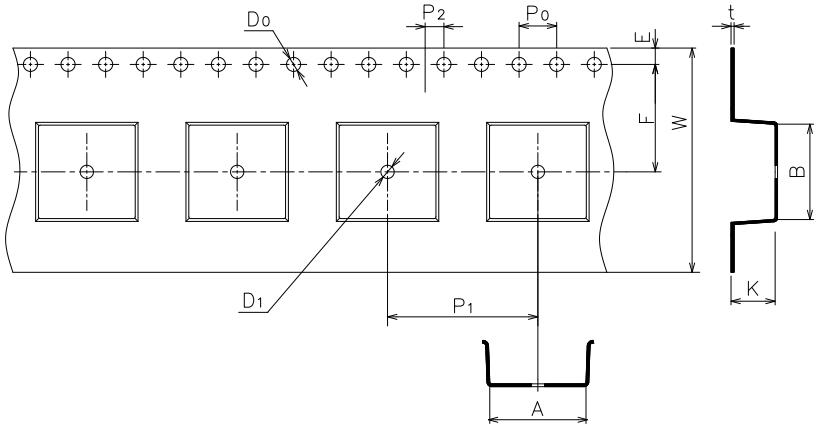
Direction of feed from reel

Option TB



Direction of feed from reel

Tape Dimension

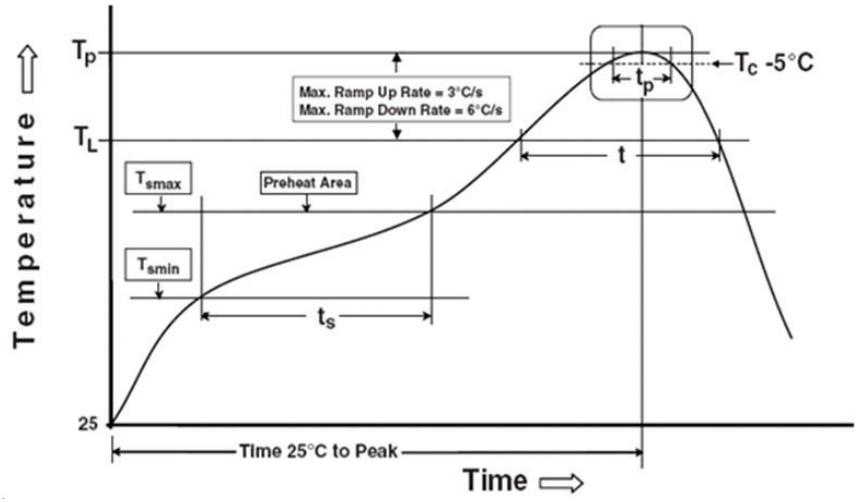


Dimension No.	A	B	Do	D1	E	F
Dimension(mm)	10.4±0.1	10.0±0.1	1.5+0.1/-0	1.5±0.25/-0	1.75±0.1	7.5±0.1
Dimension No.	**Po**	**P1**	**P2**	**t**	**W**	**K**
Dimension(mm)	4.0±0.1	12.0±0.1	2.0±0.05	0.4±0.05	16.0±0.3/	4.5±0.1

Precautions for Use

1. Soldering Condition

1.1 (A) Maximum Body Case Temperature Profile for evaluation of Reflow Profile



Note: Reference: IPC/JEDEC J-STD-020D

Preheat	
Temperature min (T_{smin})	150 °C
Temperature max (T_{smax})	200°C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max
Other	
Liquidus Temperature (T_L)	217 °C
Time above Liquidus Temperature (t_L)	60-100 sec
Peak Temperature (T_P)	260°C
Time within 5 °C of Actual Peak Temperature: T_P - 5°C	30 s
Ramp- Down Rate from Peak Temperature	6°C /second max.
Time 25°C to peak temperature	8 minutes max.
Reflow times	3 times

DISCLAIMER

1. Above specification may be changed without notice. EVERLIGHT will reserve authority on material change for above specification.
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