

Embedded Multi-Media Card

(*e*•MMC™ 5.1)

EMMC04G-CT32-01G10

v1.6

Kingston Digital Inc.

Product Features

- Packaged managed NAND flash memory with *e*•MMC™ 5.1 interface
- Backward compatible with all prior *e*•MMC™ specification revisions
- 153-ball JEDEC FBGA RoHS Compliant package
- Operating voltage range:
 - VCCQ = 1.8 V/3.3 V
 - VCC = 3.3 V
- Operating Temperature -25C to +85C
- Storage Temperature -40C to +85C
- Compliant with *e*•MMC™ 5.1 JEDEC Standard Number JESD84-B51

e•MMC™ Specific Feature Support

- High-speed *e*•MMC™ protocol
- Variable clock frequencies of 0-200MHz
- Ten-wire bus interface (clock, 1 bit command, 8 bit data bus) with an optional hardware reset
- Supports three different data bus widths: 1 bit(default), 4 bits, 8 bits
- Bus Modes:
 - Single data transfer rate: up to 52MB/s (using 8 parallel data lines at 52MHz)
 - Dual data rate mode (DDR-104) : up to 104MB/s @ 52MHz
 - High speed, single data rate mode (HS-200) : up to 200MB/s @ 200MHz
 - High speed, dual data rate mode (HS-400) : up to 400MB/s @ 200MHz
- Supports alternate boot operation mode to provide a simple boot sequence method
 - Supports SLEEP/AWAKE (CMD5)
 - Host initiated explicit sleep mode for power saving
- Enhanced write protection with permanent and partial protection options
- Multiple user data partition with enhanced attribute for increased reliability
- Error free memory access
 - Cyclic Redundancy Code (CRC) for reliable command and data communication
 - Internal error correction code (ECC) for improved data storage integrity
 - Internal enhanced data management algorithm
 - Data protection for sudden power failure during program operations
- Security
 - Secure bad block erase commands
 - Enhanced write protection with permanent and partial protection options
- Power off notification for sleep
- Field firmware update (FFU)
- Production state awareness
- Device health report
- Command queuing
- Enhanced strobe
- Cache flushing report
- Cache barrier

- Background operation control & High Priority Interrupt (HPI)
- RPMB throughput improvement
- Secure write protection
- Pre EOL information
- Optimal size
- Endurance of 3,000 Program-erase cycles

Product Description

Kingston's e•MMC™ products conform to the JEDEC e•MMC™ 5.1 standard. These devices are an ideal universal storage solution for many commercial and industrial applications. In a single integrated packaged device, e•MMC™ combines multi-level cell (MLC) NAND flash memory with an onboard e•MMC™ controller, providing an industry standard interface to the host system. The integrated e•MMC™ controller directly manages NAND flash media which relieves the host processor of these tasks, including flash media error control, wear-leveling, NAND flash management and performance optimization. Future revision to the JEDEC e•MMC™ standard will always maintain backward compatibility. The industry standard interface to the host processor ensures compatibility across future NAND flash generations as well, easing product sustainment throughout the product life cycle.

Configurations

Kingston's e•MMC™ products support a variety of configurations that allow the e•MMC™ device to be tailored to your specific application needs. The most popular configurations described below are each offered under standard part numbers.

Standard MLC – By default the e•MMC™ device is configured with the NAND flash in a standard MLC mode. This configuration provides reasonable performance and reliability for many applications.

Pseudo Single Level Cell (pSLC) – The MLC NAND flash in the Kingston e•MMC™ device can be configured to further improve device endurance, data retention, reliability and performance over the standard MLC configuration. This is done by converting the NAND MLC cells to a pseudo single level cell (SLC) configuration. In this configuration, along with the performance and reliability gains, the device capacity is reduced by 50%. This one-time configuration is achieved by setting the e•MMC™ enhanced attribute for the hardware partition.

Enhanced Reliable Write – When not configured as pSLC, MLC NAND flash stores 2 bits of information in 4 energy levels per NAND flash cell. Since these paired bits are organized in different NAND pages, there is a possibility that a power failure while programming a page could corrupt a paired page that was already programmed. For the Kingston e•MMC™, this condition is rare and the possibility is further reduced due to the device's built-in data protection with on-board error correction code (ECC) bits. With *reliable write* set, the onboard e•MMC™ controller will back-up any paired pages to ensure that there is no data loss during sudden power failure. This configuration can result in a write performance penalty of up to 20% over the standard MLC configuration.

Kingston e•MMC™ can be ordered preconfigured with the option of *reliable write* or *pSLC* at no additional cost. Standard MLC devices can also be one-time configured in-field by following the procedures outlined in the JEDEC e•MMC™ specification. The JEDEC e•MMC™ specification allows for many additional configurations such as up to 4 additional general purpose (GPn) hardware partitions each with the option to support pSLC and *reliable write*. Additionally, Kingston provides a content loading service that can streamline your product assembly while reducing production costs. For more information, contact your Kingston representative.

Kingston e•MMC™ devices are fully compliant with the JEDEC Standard Specification No. JESD84-B51. This datasheet provides technical specifications for Kingston's family of e•MMC™ devices. Refer to the JEDEC e•MMC™ standard for specific information related to e•MMC™ device function and operation. See: <http://www.jedec.org/sites/default/files/docs/JESD84-B51.pdf>

Part Numbering

Figure 1 – Part Number Format

| | | | | | |
|-------------|------------|----------|-------------|----------|--------------|
| EMMC | 04G | - | CT32 | - | 01G10 |
| A | B | | C | | D |

Part Number Fields

A: Product Family : **EMMC**

B: Device Capacity : Available capacities of 4GB

C: Hardware Revision and Configuration

D: Device Firmware Revision and Configuration

Table 1 - Device Summary

| Product Part Number | NAND Density | Package | Operating voltage |
|--------------------------------|-------------------------|----------------|---|
| EMMC04G-CT32-01G10 | 4GB | FBGA153 | V _{CC} =3.3V, V _{CCQ} =1.8V/3.3V |

Device Performance

Table 2 below provides sequential read and write speeds for all capacities. Performance numbers can vary under different operating conditions. Values are given at HS400 bus mode. Contact your Kingston Representative for performance numbers using other bus modes.

Table 2 - Sequential Read / Write Performance

| Product | Transfer Rate (MB/s) | |
|--------------------|----------------------|------------------|
| | Sequential Read | Sequential Write |
| EMMC04G-CT32-01G10 | 250 | 50 |

Power Consumption

Device current consumption for various device configurations is defined in the power class fields of the EXT_CSD register. Power consumption values are summarized in Table 3 below.

Table 3 - Device Power Consumption

| Product | Read (mA) | | Write (mA) | | Standby (mA) |
|--|-------------|----------|-------------|------------|--------------|
| | VCCQ = 1.8V | VCC=3.3V | VCCQ = 1.8V | VCC = 3.3V | |
| EMMC04G-CT32-01G10 | 76.32 | 74.43 | 32.00 | 33.88 | 0.08 |
| Note: Measurement operating conditions were conducted at HS400 bus mode, VCC = 3.3V \pm 5%, VCCQ = 1.8V \pm 5%. Standby current measured at 8-bit bus, VCC = 3.3V \pm 5%, with clock idle. | | | | | |

Device and Partition Capacity

The device NAND flash capacity is divided across two boot partitions (2048 KB each), a Replay Protected Memory Block (RPMB) partition (512 KB), and the main user storage area. Four additional general purpose storage partitions can be created from the user partition. These partitions can be factory preconfigured or configured in-field by following the procedure outlined in section 6.2 of the JEDEC eMMC™ specification JESD84-B51. A small portion of the NAND storage capacity is used for the storage of the onboard controller firmware and mapping tables. Additionally, several NAND blocks are held in reserve to boost performance and extend the life of the eMMC™ device. Table 4 identifies the specific capacity of each partition. This information is reported in the device EXT_CSD register. The contents of this register are also listed in the Appendix.

Table 4 - Partition Capacity

| Part Number | Partition | | | |
|--------------------|-----------------|---------|---------|--------|
| | User | Boot 1 | Boot 2 | RPMB |
| EMMC04G-CT32-01G10 | 3,827,957,760 B | 2048 KB | 2048 KB | 512 KB |

Table 5 - eMMC™ Operating Voltage

| Parameter | Symbol | Min | Nom | Max | Unit |
|--|---------------------------------|-----|-----|------|------|
| Supply voltage (NAND) | V _{CC} | 2.7 | 3.3 | 3.6 | V |
| Supply voltage (I/O) | V _{CCQ} ⁽¹⁾ | 2.7 | 3.3 | 3.6 | V |
| | | 1.7 | 1.8 | 1.95 | V |
| Supply power-up for 3.3V | t _{PRUH} | | | 35 | ms |
| Supply power-up for 1.8V | t _{PRUL} | | | 25 | ms |
| Note 1 : V _{CCQ} (I/O) 3.3 volt range is not supported while operating in HS200 & HS400 modes | | | | | |

e•MMC™ Bus Modes

Kingston e•MMC™ devices support all bus modes defined in the JEDEC e•MMC™ 5.1 specification. These modes are summarized in Table 6 below.

Table 6 - e•MMC™ Bus Modes

| Mode | Data Rate | IO Voltage | Bus Width | CLK Frequency | Maximum Data Bus Throughput |
|----------------|-----------|-------------|-----------|---------------|-----------------------------|
| Legacy MMC | Single | 3.3V / 1.8V | 1, 4, 8 | 0 – 26 MHz | 26 MB/s |
| High Speed SDR | Single | 3.3V / 1.8V | 4, 8 | 0 – 52 MHz | 52 MB/s |
| High Speed DDR | Dual | 3.3V / 1.8V | 4, 8 | 0 – 52 MHz | 104 MB/s |
| HS200 | Single | 1.8V | 4, 8 | 0 – 200 MHz | 200 MB/s |
| HS400 | Dual | 1.8V | 8 | 0 – 200 MHz | 400 MB/s |

Signal Description

Table 7 - e•MMC™ Signals

| Name | Type | Description |
|---|-----------|--|
| CLK | I | Clock: Each cycle of this signal directs a one bit transfer on the command and either a one bit (1x) or a two bits transfer (2x) on all the data lines. The frequency may vary between zero and the maximum clock frequency. |
| DAT[7:0] | I/O/PP | Data: These are bidirectional data channels. The DAT signals operate in push-pull mode. These bidirectional signals are driven by either the e•MMC™ device or the host controller. By default, after power up or reset, only DAT0 is used for data transfer. A wider data bus can be configured for data transfer, using either DAT0-DAT3 or DAT0-DAT7, by the e•MMC™ host controller. The e•MMC™ device includes internal pull-ups for data lines DAT1-DAT7. Immediately after entering the 4-bit mode, the device disconnects the internal pull ups of lines DAT1, DAT2, and DAT3. Correspondingly, immediately after entering to the 8-bit mode, the device disconnects the internal pull-ups of lines DAT1–DAT7. |
| CMD | I/O/PP/OD | Command: This signal is a bidirectional command channel used for device initialization and transfer of commands. The CMD signal has two operation modes: open-drain for initialization mode, and push-pull for fast command transfer. Commands are sent from the e•MMC™ host controller to the e•MMC™ device and responses are sent from the device to the host. |
| DS | O | This signal is generated by the device and used for output in HS400 mode. The frequency of this signal follows the frequency of CLK. For data output each cycle of this signal directs two bits transfer(2x) on the data - one bit for positive edge and the other bit for negative edge. For CRC status response output and CMD response output (enabled only HS400 enhanced strobe mode), the CRC status and CMD Response are latched on the positive edge only, and don't care on the negative edge. |
| RST_n | I | Hardware Reset: By default, hardware reset is disabled and must be enabled in the EXT_CSD register if used. Otherwise, it can be left un-connected. |
| RFU | - | Reserved for future use: These pins are not internally connected. Leave floating |
| NC | - | Not Connected: These pins are not internally connected. Signals can be routed through these balls to ease printed circuit board design. See Kingston's Design Guidelines for further details. |
| VSF | - | Vendor Specific Function: These pins are not internally connected |
| Vddi | - | Internal Voltage Node: Note that this is not a power supply input. This pin provides access to the output of an internal voltage regulator to allow for the connection of an external Creg capacitor. See Kingston's Design Guidelines for further details. |
| Vcc | S | Supply voltage for core |
| Note: I=Input; O=Output; PP=Push-Pull; OD=Open_Drain; NC=Not Connected(or logical high); S=Power Supply | | |

Signal Description Continued

Table 8 - e•MMC™ Signals Continued

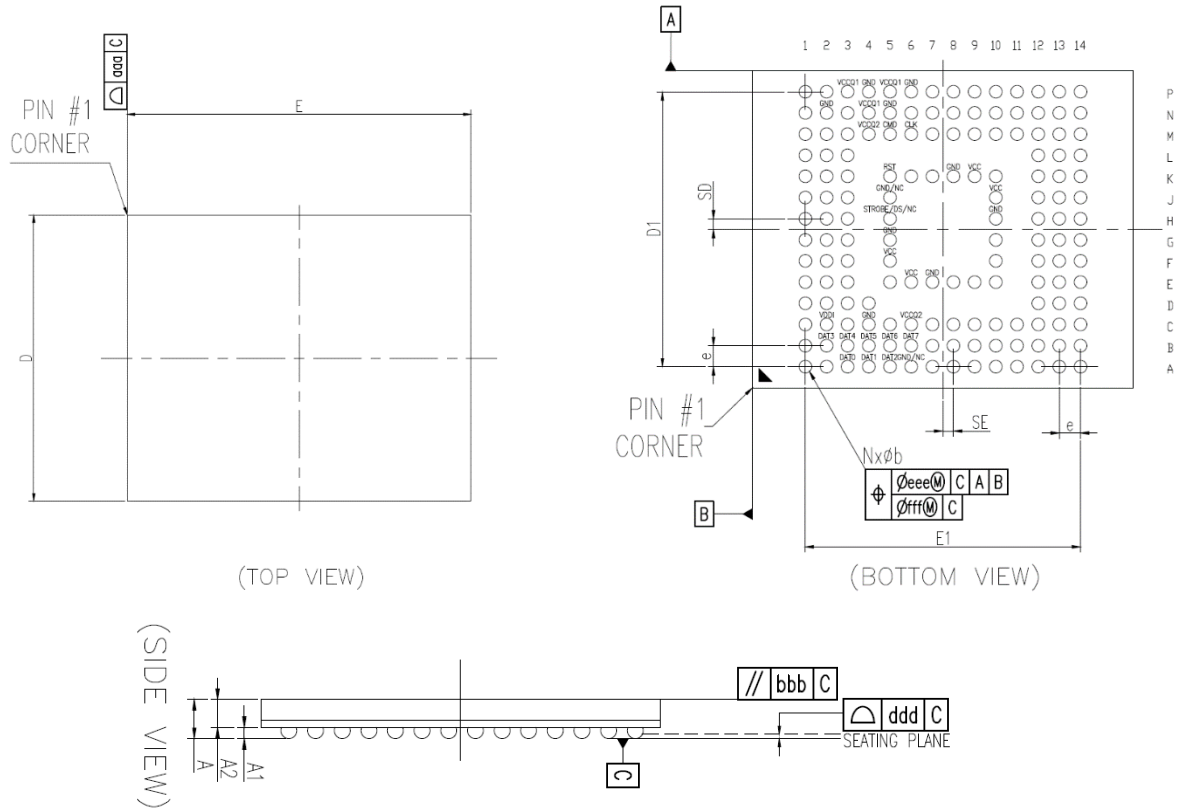
| Name | Type | Description |
|---|------|------------------------|
| Vccq | S | Supply voltage for I/O |
| Vss | S | Supply ground for core |
| Vssq | S | Supply ground for I/O |
| Note: I=Input; O=Output; PP=Push-Pull; OD=Open_Drain; NC=Not Connected(or logical high); S=Power Supply | | |

Design Guidelines

Design guidelines are outlined in a separate document. Contact your Kingston Representative for more information.

Package Dimensions

Figure 2 – Package Dimensions



| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|--------|-------------------|-----------|-------------|-------------------|-----------|--------------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.62 | 0.73 | 0.80 | 0.024 | 0.029 | 0.031 |
| A1 | 0.15 | 0.21 | 0.26 | 0.006 | 0.008 | 0.010 |
| A2 | 0.46 | 0.52 | 0.60 | 0.018 | 0.020 | 0.024 |
| b | 0.25 | 0.30 | 0.35 | 0.010 | 0.012 | 0.014 |
| E | 8.90 | 9.00 | 9.10 | 0.350 | 0.354 | 0.358 |
| D | 7.40 | 7.50 | 7.60 | 0.291 | 0.295 | 0.299 |
| e | 0.50 BSC. | | | 0.020 BSC. | | |
| JEDEC | MO-276(REF.) / MM | | | | | |
| aaa | 0.15 | | | | | |
| bbb | 0.20 | | | | | |
| ddd | 0.08 | | | | | |
| eee | 0.15 | | | | | |
| fff | 0.05 | | | | | |
| N | SE (mm) | SD (mm) | E1 (mm) | | D1 (mm) | |
| 153L | 0.25 BSC. | 0.25 BSC. | 6.50 BSC. | | 6.50 BSC. | |

Ball Assignment (153 ball)

Table 9 – Ball Assignment, Top View (HS400)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | | |
|---|----|------|------|------|-------|------|-----|-----|-----|-----|-----|----|----|----|----|---|
| A | NC | NC | DAT0 | DAT1 | DAT2 | Vss | RFU | NC | NC | NC | NC | NC | NC | NC | A | |
| B | NC | DAT3 | DAT4 | DAT5 | DAT6 | DAT7 | NC | NC | NC | NC | NC | NC | NC | NC | B | |
| C | NC | Vddi | NC | Vssq | NC | Vccq | NC | NC | NC | NC | NC | NC | NC | NC | C | |
| D | NC | NC | NC | NC | | | | | | | | NC | NC | NC | D | |
| E | NC | NC | NC | | RFU | Vcc | Vss | VSF | VSF | VSF | | | | NC | E | |
| F | NC | NC | NC | | Vcc | | | | | | VSF | | | | NC | F |
| G | NC | NC | RFU | | Vss | | | | | | VSF | | | | NC | G |
| H | NC | NC | NC | | DS | | | | | | Vss | | | | NC | H |
| J | NC | NC | NC | | Vss | | | | | | Vcc | | | | NC | J |
| K | NC | NC | NC | | RST_n | RFU | RFU | Vss | Vcc | VSF | | | | NC | K | |
| L | NC | NC | NC | | | | | | | | NC | NC | NC | L | | |
| M | NC | NC | NC | Vccq | CMD | CLK | NC | NC | NC | NC | NC | NC | NC | NC | M | |
| N | NC | Vssq | NC | Vccq | Vssq | NC | NC | NC | NC | NC | NC | NC | NC | NC | N | |
| P | NC | NC | Vccq | Vssq | Vccq | Vssq | RFU | NC | NC | RFU | NC | NC | NC | NC | P | |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | | |

Note: VSF, RFU and NC balls are not electrically connected. RFU balls may be defined with functionality by the Joint Electron Device Engineering Council (JEDEC) in future revisions of the e•MMC™ standard. Please refer to Kingston's design guidelines for more info.

Device Marking

Figure 4 - EMMC Package Marking



Line 1: Kingston logo

Line 2: 240xxxx-xxx.xxxx-x: Internal control number

Line 3: YYWW: Date code (YY– Last 2 digital of year, WW- Work week)

PPPPPPPPPPPP Internal control number (within 12 digits)

Line 4: Part Number: xxxxxx-xxxxxxx

Line 5: xxxxxxxxxxxx: Internal control number (within 12 digits)

Line 6: Country of Origin (CoO): TAIWAN *or* CHINA

Card Identification Register (CID)

The Card Identification (CID) register is a 128-bit register that contains device identification information used during the *e*•MMC™ protocol device identification phase. Refer to JEDEC Standard Specification No.JESD84-B51 for details.

| Field | Bits | Value |
|----------|-----------|------------------------|
| MID | [127:120] | 0x70 |
| reserved | [119:114] | 0x00 |
| CBX | [113:112] | 0x01 |
| OID | [111:104] | 0x00 |
| PNM | [103:56] | CT3204 |
| PRV | [55:48] | 0x01 |
| PSN | [47:16] | Random |
| MDT | [15:8] | month, year |
| CRC | [7:1] | Follows JEDEC Standard |
| reserved | [0:0] | 0x01 |

Card Specific Data Register [CSD]

The Card-Specific Data (CSD) register provides information on how to access the contents stored in eMMC™. The CSD registers are used to define the error correction type, maximum data access time, data transfer speed, data format...etc. For details, refer to section 7.3 of the JEDEC Standard Specification No.JESD84-B51.

| Field | Bits | Value |
|--------------------|-----------|------------------|
| CSD_Structure | [127:126] | 0x03 (V2.0) |
| SPEC_VER | [125:122] | 0x04 (V4.0~4.2) |
| reserved | [121:120] | 0x00 |
| TAAC | [119:112] | 0x4F (40ms) |
| NSAC | [111:104] | 0x01 |
| TRAN_SPEED | [103:96] | 0x32 (26Mbit/s) |
| CCC | [95:84] | 0x8F5 |
| READ_BL_LEN | [83:80] | 0x09 (512 Bytes) |
| READ_BL_PARTIAL | [79:79] | 0x00 |
| WRITE_BLK_MISALIGN | [78:78] | 0x00 |
| READ_BLK_MISALIGN | [77:77] | 0x00 |
| DSR_IMP | [76:76] | 0x00 |
| reserved | [75:74] | 0x00 |
| C_SIZE | [73:62] | 0xFFF |
| VDD_R_CURR_MIN | [61:59] | 0x07 (100mA) |
| VDD_R_CURR_MAX | [58:56] | 0x07 (200mA) |
| VDD_W_CURR_MIN | [55:53] | 0x07 (100mA) |
| VDD_W_CURR_MAX | [52:50] | 0x07 (200mA) |
| C_SIZE_MULT | [49:47] | 0x07 (512 Bytes) |
| ERASE_GRP_SIZE | [46:42] | 0x17 |
| ERASE_GRP_MULT | [41:37] | 0x1F |
| WP_GRP_SIZE | [36:32] | 0x0F |
| WP_GRP_ENABLE | [31:31] | 0x01 |
| DEFAULT_ECC | [30:29] | 0x00 |
| R2W_FACTOR | [28:26] | 0x02 |
| WRITE_BL_LEN | [25:22] | 0x09 (512 Bytes) |
| WRITE_BL_PARTIAL | [21:21] | 0x00 |
| reserved | [20:17] | 0x00 |
| CONTENT_PROT_APP | [16:16] | 0x00 |
| FILE_FORMAT_GRP | [15:15] | 0x00 |
| COPY | [14:14] | 0x00 |
| PERM_WRITE_PROTECT | [13:13] | 0x00 |
| TMP_WRITE_PROTECT | [12:12] | 0x00 |
| FILE_FORMAT | [11:10] | 0x00 |

| Field | Bits | Value |
|----------|---------|-----------------------|
| ECC | [9:8] | 0x00 |
| CRC | [7:1] | Follow JEDEC Standard |
| reserved | [0:0] | 0x01 |

Extended Card Specific Data Register [EXT_CSD]

The Extended CSD register defines the Device properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines the Device capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the Device is working in. These modes can be changed by the host by means of the SWITCH command. For details, refer to section 7.4 of the JEDEC Standard Specification No.JESD84-B51.

| Field | Byte | Value |
|---|-----------|-------|
| Reserved | [511:506] | 0 |
| EXT_SECURITY_ERR | [505:505] | 0x00 |
| S_CMD_SET | [504:504] | 0x01 |
| HPI_FEATURES | [503:503] | 0x01 |
| BKOPS_SUPPORT | [502:502] | 0x01 |
| MAX_PACKED_READS | [501:501] | 0x3C |
| MAX_PACKED_WRITES | [500:500] | 0x20 |
| DATA_TAG_SUPPORT | [499:499] | 0x01 |
| TAG_UNIT_SIZE | [498:498] | 0x03 |
| TAG_RES_SIZE | [497:497] | 0x00 |
| CONTEXT_CAPABILITIES | [496:496] | 0x05 |
| LARGE_UNIT_SIZE_M1 | [495:495] | 0x0B |
| EXT_SUPPORT | [494:494] | 0x03 |
| SUPPORTED_MODES | [493:493] | 0x01 |
| FFU_FEATURES | [492:492] | 0x00 |
| OPERATION_CODE_TIMEOUT | [491:491] | 0x00 |
| FFU_ARG | [490:487] | 65535 |
| BARRIER_SUPPORT | [486:486] | 0x01 |
| Reserved | [485:309] | 0 |
| CMDQ_SUPPORT | [308:308] | 0x01 |
| CMDQ_DEPTH | [307:307] | 0x0F |
| Reserved | [306:306] | 0x00 |
| NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED | [305:302] | 0 |
| VENDOR_PROPRIETARY_HEALTH_REPORT | [301:270] | 0 |
| DEVICE_LIFE_TIME_EST_TYP_B | [269:269] | 0x01 |
| DEVICE_LIFE_TIME_EST_TYP_A | [268:268] | 0x01 |
| PRE_EOL_INFO | [267:267] | 0x01 |
| OPTIMAL_READ_SIZE | [266:266] | 0x01 |
| OPTIMAL_WRITE_SIZE | [265:265] | 0x04 |
| OPTIMAL_TRIM_UNIT_SIZE | [264:264] | 0x01 |
| DEVICE_VERSION | [263:262] | 0 |
| FIRMWARE_VERSION | [261:254] | 0x01 |
| PWR_CL_DDR_200_360 | [253:253] | 0x00 |

| Field | Byte | Value |
|------------------------------------|-----------|---------|
| CACHE_SIZE | [252:249] | 512 |
| GENERIC_CMD6_TIME | [248:248] | 0x19 |
| POWER_OFF_LONG_TIME | [247:247] | 0x03 |
| BKOPS_STATUS | [246:246] | 0x00 |
| CORRECTLY_PRG_SECTORS_NUM | [245:242] | 0 |
| INI_TIMEOUT_AP | [241:241] | 0x64 |
| CACHE_FLUSH_POLICY | [240:240] | 0x01 |
| PWR_CL_DDR_52_360 | [239:239] | 0x00 |
| PWR_CL_DDR_52_195 | [238:238] | 0x00 |
| PWR_CL_200_195 | [237:237] | 0x00 |
| PWR_CL_200_130 | [236:236] | 0x00 |
| MIN_PERF_DDR_W_8_52 | [235:235] | 0x00 |
| MIN_PERF_DDR_R_8_52 | [234:234] | 0x00 |
| Reserved | [233:233] | 0x00 |
| TRIM_MULT | [232:232] | 0x05 |
| SEC_FEATURE_SUPPORT | [231:231] | 0x55 |
| SEC_ERASE_MULT | [230:230] | 0x1E |
| SEC_TRIM_MULT | [229:229] | 0x1E |
| BOOT_INFO | [228:228] | 0x07 |
| Reserved | [227:227] | 0x00 |
| BOOT_SIZE_MULT | [226:226] | 0x10 |
| ACC_SIZE | [225:225] | 0x06 |
| HC_ERASE_GRP_SIZE | [224:224] | 0x01 |
| ERASE_TIMEOUT_MULT | [223:223] | 0x05 |
| REL_WR_SEC_C | [222:222] | 0x01 |
| HC_WP_GRP_SIZE | [221:221] | 0x10 |
| S_C_VCC | [220:220] | 0x08 |
| S_C_VCCQ | [219:219] | 0x08 |
| PRODUCTION_STATE_AWARENESS_TIMEOUT | [218:218] | 0x14 |
| S_A_TIMEOUT | [217:217] | 0x13 |
| SLEEP_NOTIFICATION_TIME | [216:216] | 0x0F |
| SEC_COUNT | [215:212] | 7476480 |
| SECURE_WP_INFO | [211:211] | 0x01 |
| MIN_PERF_W_8_52 | [210:210] | 0x08 |
| MIN_PERF_R_8_52 | [209:209] | 0x08 |
| MIN_PERF_W_8_26_4_52 | [208:208] | 0x08 |
| MIN_PERF_R_8_26_4_52 | [207:207] | 0x08 |
| MIN_PERF_W_4_26 | [206:206] | 0x08 |
| MIN_PERF_R_4_26 | [205:205] | 0x08 |
| Reserved | [204:204] | 0x00 |
| PWR_CL_26_360 | [203:203] | 0x00 |

| Field | Byte | Value |
|-----------------------|-----------|-------|
| PWR_CL_52_360 | [202:202] | 0x00 |
| PWR_CL_26_195 | [201:201] | 0x00 |
| PWR_CL_52_195 | [200:200] | 0x00 |
| PARTITION_SWITCH_TIME | [199:199] | 0x03 |
| OUT_OF_INTERRUPT_TIME | [198:198] | 0x08 |
| DRIVER_STRENGTH | [197:197] | 0x1F |
| DEVICE_TYPE | [196:196] | 0x57 |
| Reserved | [195:195] | 0x00 |
| CSD_STRUCTURE | [194:194] | 0x02 |
| Reserved | [193:193] | 0x00 |
| EXT_CSD_REV | [192:192] | 0x08 |
| CMD_SET | [191:191] | 0x00 |
| Reserved | [190:190] | 0x00 |
| CMD_SET_REV | [189:189] | 0x00 |
| Reserved | [188:188] | 0x00 |
| POWER_CLASS | [187:187] | 0x00 |
| Reserved | [186:186] | 0x00 |
| HS_TIMING | [185:185] | 0x01 |
| STROBE_SUPPORT | [184:184] | 0x01 |
| BUS_WIDTH | [183:183] | 0x02 |
| Reserved | [182:182] | 0x00 |
| ERASED_MEM_CONT | [181:181] | 0x00 |
| Reserved | [180:180] | 0x00 |
| PARTITION_CONFIG | [179:179] | 0x00 |
| BOOT_CONFIG_PROT | [178:178] | 0x00 |
| BOOT_BUS_CONDITIONS | [177:177] | 0x00 |
| Reserved | [176:176] | 0x00 |
| ERASE_GROUP_DEF | [175:175] | 0x00 |
| BOOT_WP_STATUS | [174:174] | 0x00 |
| BOOT_WP | [173:173] | 0x00 |
| Reserved | [172:172] | 0x00 |
| USER_WP | [171:171] | 0x00 |
| Reserved | [170:170] | 0x00 |
| FW_CONFIG | [169:169] | 0x00 |
| RPMB_SIZE_MULT | [168:168] | 0x04 |
| WR_REL_SET | [167:167] | 0x1F |
| WR_REL_PARAM | [166:166] | 0x15 |
| SANITIZE_START | [165:165] | 0x00 |
| BKOPS_START | [164:164] | 0x00 |
| BKOPS_EN | [163:163] | 0x00 |
| RST_n_FUNCTION | [162:162] | 0x00 |

| Field | Byte | Value |
|-----------------------------|-----------|---------|
| HPI_MGMT | [161:161] | 0x00 |
| PARTITIONING_SUPPORT | [160:160] | 0x07 |
| MAX_ENH_SIZE_MULT | [159:157] | 228 |
| PARTITIONS_ATTRIBUTE | [156:156] | 0x00 |
| PARTITION_SETTING_COMPLETED | [155:155] | 0x00 |
| GP_SIZE_MULT_4 | [154:152] | 0 |
| GP_SIZE_MULT_3 | [151:149] | 0 |
| GP_SIZE_MULT_2 | [148:146] | 0 |
| GP_SIZE_MULT_1 | [145:143] | 0 |
| ENH_SIZE_MULT | [142:140] | 0 |
| ENH_START_ADDR | [139:136] | 0 |
| Reserved | [135:135] | 0x00 |
| SEC_BAD_BLK_MGMNT | [134:134] | 0x00 |
| PRODUCTION_STATE_AWARENESS | [133:133] | 0x00 |
| TCASE_SUPPORT | [132:132] | 0x00 |
| PERIODIC_WAKEUP | [131:131] | 0x00 |
| PROGRAM_CID_CSD_DDR_SUPPORT | [130:130] | 0x01 |
| Reserved | [129:128] | 0 |
| VENDOR_SPECIFIC_FIELD | [127:67] | 1049600 |
| ERROR_CODE | [66:65] | 0 |
| ERROR_TYPE | [64:64] | 0x00 |
| NATIVE_SECTOR_SIZE | [63:63] | 0x00 |
| USE_NATIVE_SECTOR | [62:62] | 0x00 |
| DATA_SECTOR_SIZE | [61:61] | 0x00 |
| INI_TIMEOUT_EMU | [60:60] | 0x00 |
| CLASS_6_CTRL | [59:59] | 0x00 |
| DYNCAP_NEEDED | [58:58] | 0x00 |
| EXCEPTION_EVENTS_CTRL | [57:56] | 0 |
| EXCEPTION_EVENTS_STATUS | [55:54] | 0 |
| EXT_PARTITIONS_ATTRIBUTE | [53:52] | 0 |
| CONTEXT_CONF | [51:37] | 0 |
| PACKED_COMMAND_STATUS | [36:36] | 0x00 |
| PACKED_FAILURE_INDEX | [35:35] | 0x00 |
| POWER_OFF_NOTIFICATION | [34:34] | 0x00 |
| CACHE_CTRL | [33:33] | 0x00 |
| FLUSH_CACHE | [32:32] | 0x00 |
| BARRIER_CTRL | [31:31] | 0x00 |
| MODE_CONFIG | [30:30] | 0x00 |
| MODE_OPERATION_CODES | [29:29] | 0x00 |
| Reserved | [28:27] | 0 |
| FFU_STATUS | [26:26] | 0x00 |

| Field | Byte | Value |
|------------------------------------|-----------|---------|
| PRE_LOADING_DATA_SIZE | [25:22] | 0 |
| MAX_PRE_LOADING_DATA_SIZE | [21:18] | 3674880 |
| PRODUCT_STATE_AWARENESS_ENABLEMENT | [17:17] | 0x01 |
| SECURE_REMOVAL_TYPE | [16:16] | 0x09 |
| CMDQ_MODE_EN | [15:15] | 0x00 |
| Reserved | [14:0] | 0 |

History

| Revision | History | Date |
|----------|---|-----------|
| v1.0 | Initial Release | 07 / 2023 |
| v1.1 | Updated Package Dimension Size | 07 / 2023 |
| v1.2 | Updated bookmark naming | 11 / 2023 |
| v1.3 | Updated operating temperature | 04 / 2024 |
| v1.4 | Updated power/performance numbers | 05 / 2024 |
| v1.5 | Updated package drawing | 06 / 2024 |
| v1.6 | Updated Top/Bottom View Drawing, Dimensions Table | 10 / 2024 |

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