Technical Specification

PIM 4820 series Power Interface Module Input 36-75 V, Output up to 16.5-20 A / 960-1080 W	28701-EN/LZT146443 Rev G November 2017

Key Features

- Industry standard low profile Quarter-brick
  57.9 x 36.8 x 13.7 mm (2.28 x 1.45 x 0.539 in)
- Up to 960 W at 48 Vin & 1080 W at 54 Vin
- High efficiency, typ. 99.2% at 600 W
- Monitoring via PMBus
- Surge pulse durability acc to IEC & ANSI standards
- 2250 Vdc input to output isolation
- 15 W/ 5 A adjustable management power output
- Functional isolation according to IEC/EN/UL 60950-1
- MTBF 1.2 Mh

General Characteristics

- Dual power feeds input
- Input transient suppression
- Input current monitoring
- Input under voltage shutdown and Power good
- Over temperature protection
- Output voltage and current protection
- A/B Feed loss alarm
- Inrush protection and hot swap functionality
- Hold-up charge and management
- ORing MOSFET short circuit alarm
- Highly automated manufacturing ensures quality
- ISO 9001/14001 certified supplier

Safety Approvals

Design for Environment

Meets requirements in high-temperature lead-free soldering processes.

Contents

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Technical Specification

PIM 4820 series Power Interface Module Input 36-75 V, Output up to 16.5-20 A / 960-1080 W	28701-EN/LZT146443 Rev G November 2017
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Ordering Information

Product program	Output
PIM 4820B	16.5 - 20 A / 0.85 - 7 V, 5 A

Product number and Packaging

PIM 4820B $n_1n_2n_3n_4$					
Options	n_1	n_2	n_3	n_4	n_5
Mounting	o				
Communication interface		o			
Baseplate			o		
Lead length				o	
Delivery package information					o

Options	Description	
n_1	P	Through hole
n_2	D	PMBus interface
n_3	HS	Baseplate
n_4		5.33 mm*
	LA	3.69 mm
	LB	4.57 mm
n_5		Soft tray *

Example a through-hole mounted, PMBus interface, standard pin product with tray packaging would be PIM 4820B PD.

* Standard variant (i.e. no option selected).

General Information

Reliability

The failure rate (λ) and mean time between failures (MTBF= $1/\lambda$) is calculated at max output power and an operating ambient temperature (T_A) of +40°C. Flex Power Modules uses Telcordia SR-332 Issue 2 Method 1 to calculate the mean steady-state failure rate and standard deviation (σ).

Telcordia SR-332 Issue 2 also provides techniques to estimate the upper confidence levels of failure rates based on the mean and standard deviation.

Mean steady-state failure rate,	Std. deviation, σ
846 nFailures/h	59 nFailures/h

MTBF (mean value) for the PIM series = 1.18 Mh.
MTBF at 90% confidence level = 1.08 Mh

Compatibility with RoHS requirements

The products are compatible with the relevant clauses and requirements of the RoHS directive 2011/65/EU and have a maximum concentration value of 0.1% by weight in homogeneous materials for lead, mercury, hexavalent chromium, PBB and PBDE and of 0.01% by weight in homogeneous materials for cadmium.

Exemptions in the RoHS directive utilized in Flex Power Modules products are found in the Statement of Compliance document.

Flex Power Modules fulfills and will continuously fulfill all its obligations under regulation (EC) No 1907/2006 concerning the registration, evaluation, authorization and restriction of chemicals (REACH) as they enter into force and is through product materials declarations preparing for the obligations to communicate information on substances in the products.

Quality Statement

The products are designed and manufactured in an industrial environment where quality systems and methods like ISO 9000, Six Sigma, and SPC are intensively in use to boost the continuous improvements strategy. Infant mortality or early failures in the products are screened out and they are subjected to an ATE-based final test. Conservative design rules, design reviews and product qualifications, plus the high competence of an engaged work force, contribute to the high quality of the products.

Warranty

Warranty period and conditions are defined in Flex Power Modules General Terms and Conditions of Sale.

Limitation of Liability

Flex Power Modules does not make any other warranties, expressed or implied including any warranty of merchantability or fitness for a particular purpose (including, but not limited to, use in life support applications, where malfunctions of product can cause injury to a person's health or life).

Safety Specification

General information

Flex Power Modules DC/DC converters and DC/DC regulators are designed in accordance with safety standards IEC/EN/UL 60950-1 *Safety of Information Technology Equipment*.

IEC/EN/UL 60950-1 contains requirements to prevent injury or damage due to the following hazards:

- Electrical shock
- Energy hazards
- Fire
- Mechanical and heat hazards
- Radiation hazards
- Chemical hazards

On-board DC/DC converters and DC/DC regulators are defined as component power supplies. As components they cannot fully comply with the provisions of any safety requirements without “conditions of acceptability”. Clearance between conductors and between conductive parts of the component power supply and conductors on the board in the final product must meet the applicable safety requirements. Certain conditions of acceptability apply for component power supplies with limited stand-off (see Mechanical Information and Safety Certificate for further information). It is the responsibility of the installer to ensure that the final product housing these components complies with the requirements of all applicable safety standards and regulations for the final product.

Component power supplies for general use should comply with the requirements in IEC/EN/UL 60950-1 *Safety of Information Technology Equipment.* Product related standards, e.g. IEEE 802.3af *Power over Ethernet*, and ETS-300132-2 *Power interface at the input to telecom equipment, operated by direct current (dc)* are based on IEC/EN/UL 60950-1 with regards to safety.

Flex Power Modules DC/DC converters, Power interface modules and DC/DC regulators are UL 60950-1 recognized and certified in accordance with EN 60950-1. The flammability rating for all construction parts of the products meet requirements for V-0 class material according to IEC 60695-11-10, *Fire hazard testing, test flames* – 50 W horizontal and vertical flame test methods.

Isolated DC/DC converters & Power interface modules

The product may provide basic or functional insulation between input and output according to IEC/EN/UL 60950-1 (see Safety Certificate), different conditions shall be met if the output of a basic or a functional insulated product shall be considered as safety extra low voltage (SELV).

For basic insulated products (see Safety Certificate) the output is considered as safety extra low voltage (SELV) if
For basic insulated products (see Safety Certificate) the
output is considered as safety extra low voltage (SELV) if one of the following conditions is met:

- The input source provides supplementary or double or reinforced insulation from the AC mains according to IEC/EN/UL 60950-1.
- The input source provides functional or basic insulation from the AC mains and the product’s output is reliably connected to protective earth according to IEC/EN/UL 60950-1.

For functional insulated products (see Safety Certificate) the output is considered as safety extra low voltage (SELV) if one of the following conditions is met:

- The input source provides double or reinforced insulation from the AC mains according to IEC/EN/UL 60950-1.
- The input source provides basic or supplementary insulation from the AC mains and the product’s output is reliably connected to protective earth according to IEC/EN/UL 60950-1.
- The input source is reliably connected to protective earth and provides basic or supplementary insulation according to IEC/EN/UL 60950-1 and the maximum input source voltage is 60 Vdc.

Galvanic isolation between input and output is verified in an electric strength test and the isolation voltage (V_{iso}) meets the voltage strength requirement for basic insulation according to IEC/EN/UL 60950-1.

It is recommended to use a slow blow fuse at the input of each DC/DC converter. If an input filter is used in the circuit the fuse should be placed in front of the input filter. In the rare event of a component problem that imposes a short circuit on the input source, this fuse will provide the following functions:

- Isolate the fault from the input power source so as not to affect the operation of other parts of the system
- Protect the distribution wiring from excessive current and power loss thus preventing hazardous overheating

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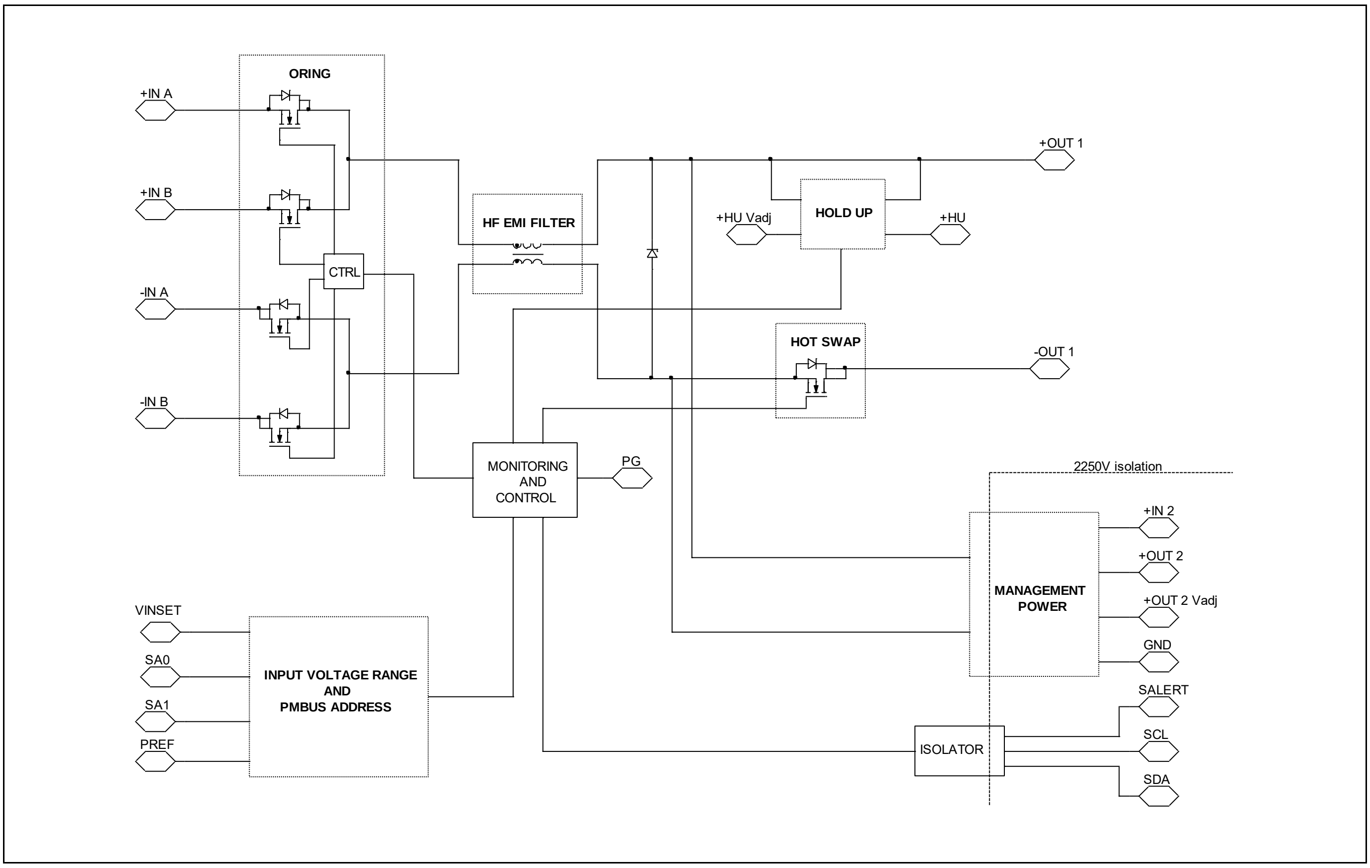
Absolute Maximum Ratings

Characteristics		min	typ	max	Unit
T_{P1}	Operating Temperature (see Thermal Consideration section)	-40		+110	°C
T_S	Storage temperature	-55		+100	°C
V_I	Input voltage	-60		80	V
V_I	Input voltage, reverse polarity			60	V
V_I	Input voltage transient ANSI T1.315-2001 (R2006)			100	V
V_I	Common mode surge pulses (1.2/50 µs) IEC 61000-4-5			1000	V
V_{ISO}	Isolation voltage			2250	V
V_{HU}	Hold-up capacitor voltage			100	V
C_{HU}	Hold-up capacitor capacitance			6600	µF
V_{VINSET}	Input voltage range setting	-0.3		3.6	V
V_{SA0}, V_{SA1}	PMBus address pin-strap	-0.3		3.6	V
V_{PG}	Power good, open collector voltage			120	V
I_{PG}	Power good, sink current			8	mA
V_{SCL}	PMBus clock	-0.5		7	V
V_{SDA}	PMBus data	-0.5		7	V
V_{SALERT}	PMBus alert, open collector voltage	-7		70	V
I_{SALERT}	PMBus alert, sink current			50	mA
V_{IN2}	Management power external supply voltage	-60		16	V

Stress in excess of Absolute Maximum Ratings may cause permanent damage. Absolute Maximum Ratings, sometimes referred to as no destruction limits, are normally tested with one parameter at a time exceeding the limits in the Electrical Specification. If exposed to stress above these limits, function and performance may degrade in an unspecified manner.

Fundamental Circuit Diagram



Functional Description

PIM 4820B PD

Unless otherwise specified under conditions values are given at I_{O1} = 16.5 A, no external supply, P_{O2} = 15 W and output 2 unadjusted (V_{O2} = 5.05 V). Minimum and maximum values given at T_{P1} = -30 to 90 ºC, V_I = 36 to 75 V and typical values given at: T_{P1} = +25 °C, V_I = 53 V.

Characteristics		Comments	min	typ	max	Unit
PMBus monitoring accuracy						
READ_VIN	ORed input voltage	Converted from PMBus format	-2	±0.5	2	% of full scale
		Scale	0		108	V
READ_IIN	ORed input current, See Note 1.	Converted from PMBus format	-1	±0.3	1	% of full scale
		Scale	0		32	A
READ_TEMPERATURE_1	P1 temperature	Converted from PMBus format	-5	±3	5	ºC
Fault Protection Characteristics						
UVLO, input under voltage lockout	Delay			1	40	ms
OVP, input over voltage protection	Fault response time			90		ms
OCP, over current protection	Fault response time, see Note 2			0.7/1.5		ms
OTP, over temperature protection	OTP_FAULT_LIMIT			120		°C
	OTP_ALERT_LIMIT			110		°C
	Hysteresis			10		°C
	Fault response time				1	s

Note 1: With output 2 loaded the min/max error is ±2.5%.

Note 2: The lesser of the two values is valid during the following conditions: 1) At start up prior to PG assertion. 2) Within a period of ($t_{HU\ block}$ + $t_{HU\ EN}$) after an HU dump event.

Command			Read	Format
Registers				
MFR_SPECIFIC_00	Status register	Read byte	Initial state: 00h	bit field
MFR_SPECIFIC_01	Fault register	Read/Write byte	Initial state: 00h	bit field
MFR_SPECIFIC_02	Alert register	Read/Write byte	Initial state: 80h	bit field
MFR_SPECIFIC_04	Control register	Read/Write byte	Initial state: 00h	bit field
Status command				
STATUS_BYTE	Only CML bit used (communication fault only)	Read word PMBus spec. 1.2 17.1	Initial state: 00h	bit field
PMBus revision				
PMBUS_REVISION	PMBus revision	Read byte PMBus spec. 1.2 22.1	Example: 1.2	bit field

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Functional Description (Continued) — PIM 4820B PD

Unless otherwise specified under conditions values are given at I_{O1} = 16.5 A, no external supply, P_{O2} = 15 W and output 2 unadjusted (V_{O2} = 5.05 V). Minimum and maximum values given at T_{P1} = -30 to 90 °C, V_I = 36 to 75 V and typical values given at: T_{P1} = +25 °C, V_I = 53 V.

Characteristics		Conditions	Read	Unit
Manufacturer's information				
MFR_ID	Manufacturer's ID	Read block, format: 8 byte	ERICSSON	ASCII
MFR_MODEL	Manufacturer's type designation	Read block, format: 18 byte	Example: PIM4820BPD	ASCII
MFR_REVISION	Product's revision	Read block, format: 3 byte	Example: R1A	ASCII
MFR_DATE	Date of manufacture	Read block, format: YYMMDD	Example: 120425	ASCII

Logic Input/Output Characteristics		min	typ	max	Unit
Logic Input/Output Characteristics					
PMBus frequency	Note 3	10		400	kHz
Logic input low (V_{IL})	SCL, SDA			0.96	V
Logic input high (V_{IH})	SCL, SDA	2.38			V
Logic output low (V_{OL})	SCL, SDA			0.4	V
Logic output high (V_{OH})	SCL, SDA	3.16			V
Logic output high (V_{OH})	SALERT	3.16			V
Logic output low (V_{OL})	PG (sink current 8 mA)			1	V
	SALERT (sink current 0.3 mA)			0.4	V
Logic Delay time PG ($t_{PG\ delay}$)	PG, see note 4	0		100	ms
Logic output low to high (V_{OL} - V_{OH})	SALERT rise time			100	µs
Logic output high to low (V_{OH} - V_{OL})	SALERT fall time			10	µs
Setup time, SMBus		460			ns
Hold time, SMBus		210			ns
Bus free time T (BUF)	Note 5	2			ms

Note 3: Do not use PEC when running PMBus at frequencies above 100 kHz.

Note 4: Delay between output 1 reach 90 % of V_{OI} and PG asserted, see "Operating Information" section entitled "Start-up procedure"

Note 5: It is recommended that a PMBus master reads back written data for verification i.e. do not rely on the ACK/NACK bit since this bit is as susceptible to errors as any other bit. However, under very rare operating conditions, it is possible to get intermittent read back failures. It is therefore recommended to implement error handling in the master that also deals with those situations.

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Main Unit (Output 1), 36-75 V, 16.5 A, Electrical Specification — PIM 4820B PD

Unless otherwise specified under conditions values are given at I_{O1} = 16.5 A, no external supply, P_{O2} = 15 W and output 2 unadjusted (V_{O2} = 5.05 V). Minimum and maximum values given at T_{P1} = -30 to 90 °C, V_I = 36 to 75 V and typical values given at: T_{P1} = +25 °C, V_I = 53 V.

Characteristics		Conditions	min	typ	max	Unit
V_I	Input voltage range	See Note 6	36	53	75	V
$V_{I\,off}$	Turn-off threshold voltage, decreasing feed A and B voltage	Input voltage range 3, see Note 6	41	42		V
$V_{I\,on}$	Turn-on threshold voltage, Increasing feed A or B voltage			44.2	45	
V_{OVP}	OVP turn-off threshold voltage, Increasing feed A or B voltage			65		
$V_{I\,FEED\,ALARM\,on}$	Feed Alarm turn-on threshold voltage, decreasing feed A or B voltage			33.9		
$V_{I\,FEED\,ALARM\,off}$	Feed Alarm turn-on threshold voltage, increasing feed A or B voltage			35.9		
$V_{I\,off}$	Turn-off threshold voltage, decreasing feed A and B voltage	Input voltage range 2, see Note 6	37.5	38.5		V
$V_{I\,on}$	Turn-on threshold voltage, Increasing feed A or B voltage			43.7	44.2	
V_{OVP}	OVP turn-off threshold voltage, Increasing feed A or B voltage			77		
$V_{I\,FEED\,ALARM\,on}$	Feed Alarm turn-on threshold voltage, decreasing feed A or B voltage			33.5		
$V_{I\,FEED\,ALARM\,off}$	Feed Alarm turn-on threshold voltage, increasing feed A or B voltage			35.5		
$V_{I\,off}$	Turn-off threshold voltage, decreasing feed A and B voltage	Input voltage range 1, see Note 6	37.5	38.5		V
$V_{I\,on}$	Turn-on threshold voltage, Increasing feed A or B voltage			43.5	44	
V_{OVP}	OVP turn-off threshold voltage, Increasing feed A or B voltage			80		
$V_{I\,FEED\,ALARM\,on}$	Feed Alarm turn-on threshold voltage, decreasing feed A or B voltage			33.5		
$V_{I\,FEED\,ALARM\,off}$	Feed Alarm turn-on threshold voltage, increasing feed A or B voltage			35.5		
$V_{I\,off}$	Turn-off threshold voltage, decreasing feed A and B voltage	Input voltage range 0, see Note 6	32	33		V
$V_{I\,on}$	Turn-on threshold voltage, Increasing feed A or B voltage			38.2	39	
V_{OVP}	OVP turn-off threshold voltage, Increasing feed A or B voltage			80		
$V_{I\,FEED\,ALARM\,on}$	Feed Alarm turn-on threshold voltage, decreasing feed A or B voltage			29		
$V_{I\,FEED\,ALARM\,off}$	Feed Alarm turn-on threshold voltage, increasing feed A or B voltage			31		
C_I	Internal input capacitance			0.1		μF
η	Efficiency	V_I = 53 V, P_{O1} = 800 W, I_{O2} = 0 A		99.2		%
		V_I = 53 V, P_{O1} = 600 W, I_{O2} = 0 A		99.2		
		I_{O1} = 16.5 A, I_{O2} = 0 A	98.6	99.2		
P_d	Power Dissipation	I_{O1} = 16.5 A, no external management power supply, P_{O2} = 15 W		9.4	13.1	W
P_{li}	Input idling power	V_I = 53 V, I_{O1} = I_{O2} = 0 A		2		W
P_{UVLO}	Input standby power	V_I < turn off input voltage			1.6	W
t_r	Ramp-up time (from 10−90 % of V_{Oi})	V_I = 53 V, I_{O1} = I_{O2} = 0 A, C_{O1} = 220 μF		0.6		ms
t_s	Start-up time (from V_I connection to 90 % of V_{Oi})			370		ms
$t_{restart}$	Restart time (from Vo1 disabled to Vo1 enabled), see Note 7.			550		ms

I_{O1}	Output current	See Note 8	0		16.5	A
		See Notes 8 and 9	0		20	
I_{lim}	Output current limit threshold (OCP)	T_{P1} < max $T_{P1,}$ see Note 10 and Note 11.	22.5	23.5	25	A
I_{sc}	Short circuit current	T_{P1} = 25 ºC, see Note 12		0.5		A
C_{O1}	Recommended Capacitive Load	See Note 13	100		470	µF
I_{PK}	Inrush current transient	0-0.1 ms			40	A
		0.1-3.0 ms			0.1	

Note 6: See “Operating Information” section entitled “Input voltage range setting”

Note 7: Output 1 restarted by setting the CONTROL_VO1_RESTART bit.

Note 8: No load before power good, see "Operating Information" section entitled “Start-up procedure”

Note 9: See "Operating Information" section entitled "Increased output 1 maximum current to 20 A"

Note 10: The FET check function will regularly generate a short current transient on the feeding line which may lower the I_{lim} 1.5-2 A

Note 11: At operation where V_I <$V_{HU\ trig}$ the unit generates a short current transient on the feeding line which may lower the I_{lim} 1.0-2 A

Note 12: RMS current, hiccup at short circuit

Note 13: See "Operating Information" section entitled “Hold-up Event Voltage”

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Technical Specification

PIM 4820 series Power Interface Module Input 36-75 V, Output up to 16.5-20 A / 960-1080 W	28701-EN/LZT146443 Rev G November 2017 © Flex

Hold-up, Electrical Specification

PIM 4820B PD

Unless otherwise specified under conditions values are given at I_{O1} = 16.5 A, no external supply, P_{O2} = 15 W and output 2 unadjusted (V_{O2} = 5.05 V). Minimum and maximum values given at T_{P1} = -30 to 90 °C, V_I = 36 to 75 V and typical values given at: T_{P1} = +25 °C, V_I = 53 V.

Characteristics		Conditions	min	typ	max	Unit
C_{HU}	Hold-up capacitance	See Note 14, Note 15 and Note 16.			6600	µF
f_{HU}	Hold-up generator switching frequency			500		kHz
V_{HU}	Hold-up capacitor voltage adjust range		40		95	V
	Hold-up capacitor voltage regulation		-5		5	
t_{HU}	Hold-up time, see Note 17	C_{HU} = 1000 µF, P_{O1} = 800 W, V_{HU} = 75 V, input voltage range 0		2		ms
$t_{HU\ EN}$	Hold-up enable time, see Note 18			40		
$t_{HU\ block}$	Hold-up block time, see Note 19			2		s
$V_{HU\ trig}$	Hold-up trig level, decreasing feed A and B voltage	Input voltage range 3, see Note 20	43	44	45	V
		Input voltage range 2, see Note 20	42.5	43.5	44.5	
		Input voltage range 1, see Note 20	42.5	43.5	44.5	
		Input voltage range 0, see Note 20	37	38	39	

Note 14: See “Operating Information” section entitled “Hold-up Capacitor Safety Discharge”

Note 15: See “Operating Information” section entitled “Hold-up SOA”

Note 16: See Operation information” section entitled “Hold-up Capacitor Safety Discharge”

Note 17: Time elapsed between output 1 reaches the hold-up threshold voltage prior to and after the hold-up event

Note 18: The time limit for a hold-up event

Note 19: Time elapsed between a hold-up event until a second hold-up events can occur

Note 20: See “Operating Information” section entitled “Input voltage range setting”

Management Power (Output 2), 5.05 V, 15 W / 5 A, Electrical Specification

Unless otherwise specified under conditions values are given at I_{O1} = 16.5 A, no external supply, P_{O2} = 15 W and output 2 unadjusted (V_{O2} = 5.05 V). Minimum and maximum values given at T_{P1} = -30 to 90 °C, V_I = 36 to 75 V and typical values given at: T_{P1} = +25 °C, V_I = 53 V.

Characteristics		Conditions	min	typ	max	Unit
V_I	Input voltage range		36	53	75	V
$V_{I\ off}$	Turn-off threshold voltage, Decreasing feed A and B voltage			25		V
$V_{I\ on}$	Turn-on threshold voltage, Increasing feed A or B voltage			31		
V_{IN2}	External supply voltage	See Note 21	5	12	14.4	V
η	Efficiency	no external supply, I_{O1} = 0 A, I_{O2} = 3 A, unadjusted voltage, see Note 22		78		%
		V_{IN2} = 12 V, I_{O1} = 0 A, I_{O2} = 3 A, unadjusted voltage, see Note 23		91		
		V_{IN2} = 12 V, I_{O1} = 0 A, I_{O2} = 5 A, unadjusted voltage, see Note 23		90		
P_d	Power Dissipation	no external supply, I_{O1} = 0 A, I_{O2} = 3 A, unadjusted voltage, see Note 22		4.2		W
		V_{IN2} = 12 V, I_{O1} = 0 A, I_{O2} = 3 A, unadjusted voltage, see Note 23		1.5		
		V_{IN2} = 12 V, I_{O1} = 0 A, I_{O2} = 5 A, unadjusted voltage, see Note 23		2.6		

Management Power (Output 2), 5.05 V, 15 W / 5 A, Electrical Specification (Continued) PIM 4820B PD

Unless otherwise specified under conditions values are given at I_{O1} = 16.5 A, no external supply, P_{O2} = 15 W and output 2 unadjusted (V_{O2} = 5.05 V). Minimum and maximum values given at T_{P1} = -30 to 90 °C, V_I = 36 to 75 V and typical values given at: T_{P1} = +25 °C, V_I = 53 V.

Characteristics		Conditions	min	typ	max	Unit
V_O	Output voltage tolerance band	unadjusted voltage, no external supply, P_{O2} = 0 to 15 W or V_{IN2} = 6 to 14.4 V, I_{O2} = 0 to 5 A	4.9	5.05	5.2	V
	Output voltage adjust range	See Note 24	0.85		7.0	
	Line regulation	unadjusted voltage, I_{O2} = 3 A		1		mV
	Load regulation	unadjusted voltage, V_I = 53 V, no external supply, I_{O2} = 0...3 A		4		
		unadjusted voltage, V_I = 53 V, V_{IN2} = 12 V, I_{O2} = 0...5 A		8		
V_{tr}	Load transient, voltage deviation	V_I = 53 V, no external supply, Load step I_{O2} = 0.75-2.25-0.75 A, di/dt = 1 A/µs, unadjusted voltage		±210		mV
		V_I = 53 V, V_{IN2} = 12 V, Load step I_{O2} = 1.25-3.75-1.25 A, di/dt = 1 A/µs, unadjusted voltage		±320		
t_{tr}	Load transient, recovery time	V_I = 53 V, no external supply, Load step I_{O2} = 0.75-2.25-0.75 A, di/dt = 1 A/µs, unadjusted voltage		23		µs
		V_I = 53 V, V_{IN2} = 12 V, Load step I_{O2} = 1.25-3.75-1.25 A, di/dt = 1 A/µs, unadjusted voltage		27		
t_r	Ramp-up time (from 10-90 % of V_{Oi})			3		ms
t_s	Start-up time (from V_I connection to 90 % of V_{Oi})			6		ms
P_O	Output power	Continuous output power, no external supply	0		15	W
I_O	Output current	Continuous output current, with external supply, see Note 21	0		5	A
		Peak output current, with external supply, see Note 21			7	
I_{lim}	Current limit threshold	T_{P1} < max T_{P1}, unadjusted voltage, no external supply		3.6	4.5	A
		T_{P1} < max T_{P1}, V_{IN2} = 12 V		10	11.5	
I_{sc}	Short circuit current	T_{P1} = 25 °C, see Note 25		10	12.5	A
C_{O2}	Recommended Capacitive Load		100			µF
V_{Oac}	Output ripple & noise	See ripple & noise section		60		mV_{p-p}
f_s	Switching frequency	First stage		510		kHz
		Second stage		480		

Note 21: External supply shall be 1.5 V greater than adjusted voltage for loads exceeding 15 W, see "Operating Information" section entitled "Management power, external power supply"

Note 22: Idling losses in main unit is included

Note 23: Idling losses in main unit is not included

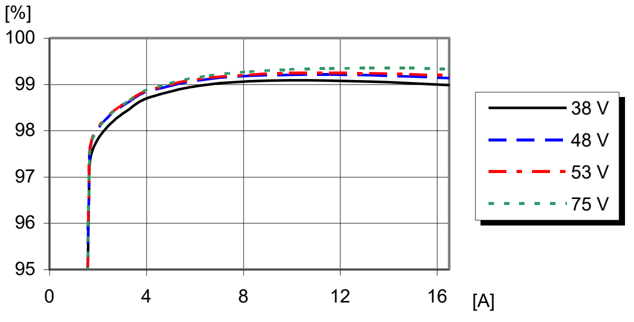
Note 24: See "Operating Information" section entitled "Management power, output voltage adjust"

Note 25: Operates in constant current mode at over current

Main Unit (Output 1), 36-75 V, 16.5 A, Typical Characteristics

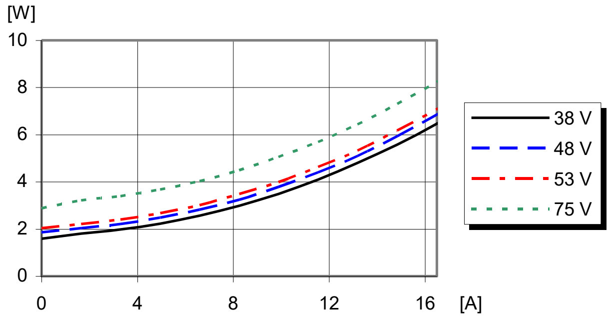
PIM 4820B PD

Efficiency



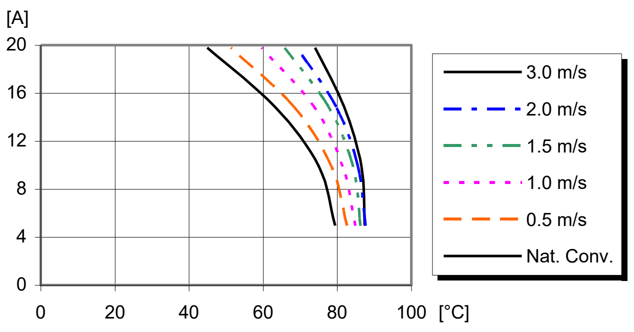
Efficiency vs. load current and input voltage at T_{P1} = +25 °C
I_{O2} = 0 A

Power Dissipation



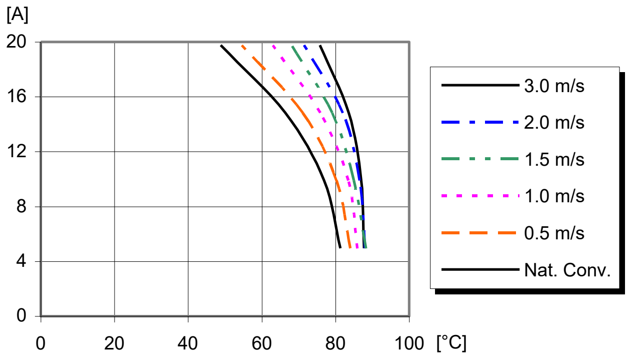
Dissipated power vs. load current and input voltage at
T_{P1} = +25 °C, I_{O2} = 0 A

Output Current Derating, no external supply



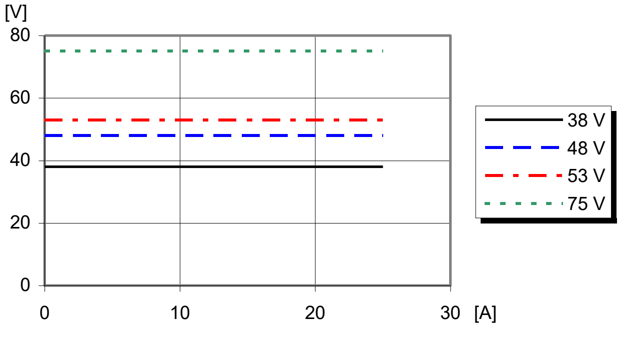
Available load current vs. ambient air temperature and airflow at
V_I = 53 V, no external supply, I_{O2} = 1.5 A, unadjusted output 2 voltage (V_{O2} = 5.05 V).
Maximum output 1 current is 16.5 A but under some conditions higher loads are allowed
See Increased output 1 maximum current and Thermal Consideration sections.

Output Current Derating, external 12 V supply



Available load current vs. ambient air temperature and airflow at
V_I = 53 V, V_{IN2} = 12 V, I_{O2} = 2.5 A, unadjusted output 2 voltage (V_{O2} = 5.05 V).
Maximum output 1 current is 16.5 A but under some conditions higher loads are allowed
See Increased output 1 maximum current and Thermal Consideration sections.

Current Limit Characteristic



Output voltage vs. load current at I_{O1} > max I_{O1} , T_{P1} = +25 °C
I_{O2} = 0 A
Output 1 enters hiccup mode at current limit.

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Technical Specification

PIM 4820 series Power Interface Module Input 36-75 V, Output up to 16.5-20 A / 960-1080 W	28701-EN/LZT146443 Rev G November 2017
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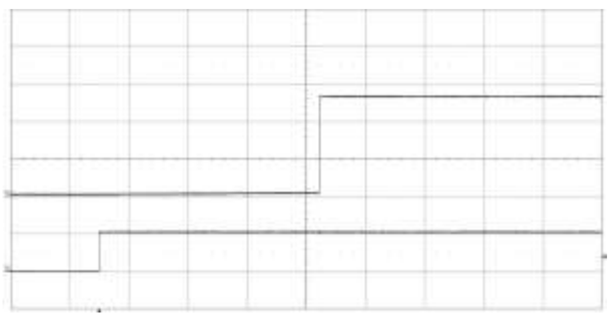
Main Unit (Output 1), 36-75 V, 16.5 A, Typical Characteristics **PIM 4820B PD**

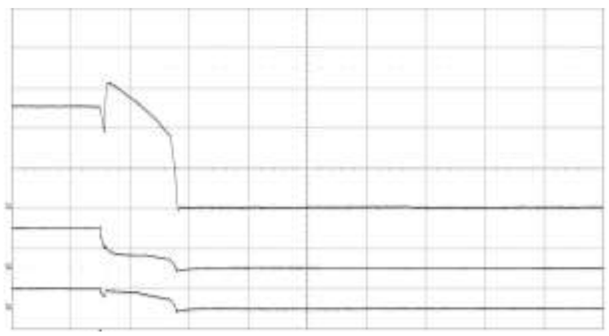
Start-up



Start-up enabled by connecting V_I at: hold-up capacitance = 1000 µF, hold-up voltage = 75 V, T_{P1} = +25 °C, output 1 capacitance = 220 µF, I_{O1} = I_{O2} = 0 A

Top trace: output 1 voltage (20 V/div.)
Bottom trace: input voltage (50 V/div.)
Time scale: (100 ms/div.)

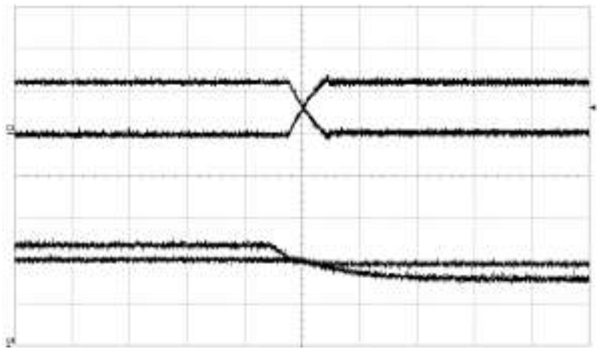
Hold-up performance



Output voltage at loss of input power at: hold-up capacitance = 1000 µF, hold-up voltage = 75 V, T_{P1} = +25 °C, output 1 capacitance = 220 µF, P_{O1} = 875 W, I_{O2} = 0 A

Top trace: output 1 voltage (20 V/div.)
Middle trace: input A voltage (50 V/div.)
Bottom trace: input B voltage (50 V/div.)
Time scale: (2 ms/div.)

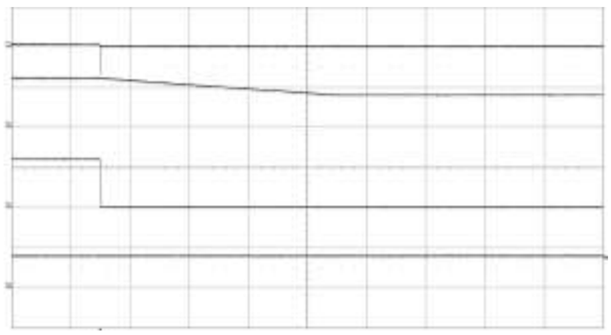
ORing – feed switch



ORing at:
T_{P1} = +25 °C, V_{IA} = 54-52 V, V_{IB} = 53 V, I_{O1} = 6 A electronic load, I_{O2} = 0 A.

Top trace: input A current (5 A/div.).
Second trace: input B current (5 A/div.).
Third trace: input A voltage (2 V/div.).
Bottom trace: input B voltage (2 V/div.).
Time scale: (0.1 s/div.).

ORing – short circuit of the feed with highest voltage

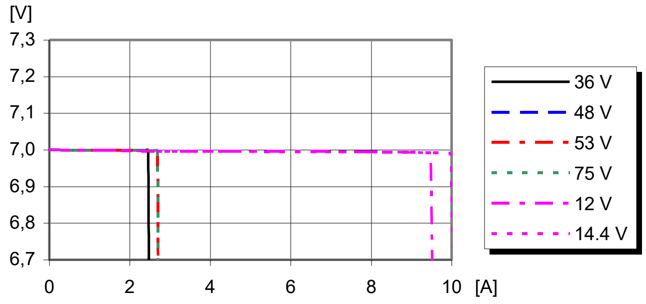


ORing functionality at:
T_{P1} = +25 °C, V_{IA} = 60 V (before short circuit), V_{IB} = 40 V, output 1 load = 10 kΩ, I_{O2} = 0 A.

Top trace: input A current (1 A/div.)
Second trace: output 1 voltage (50 V/div.)
Third trace: input A voltage (50 V/div.)
Bottom trace: input B voltage (50 V/div.)
Time scale: (10 ms/div.)

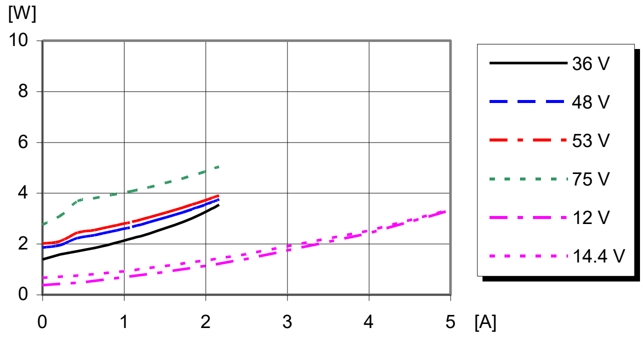
Management Power (Output 2), 5.05 V, 15 W / 5 A, Typical Characteristics — PIM 4820B PD

Output Characteristics, output voltage adjusted to 7.0 V



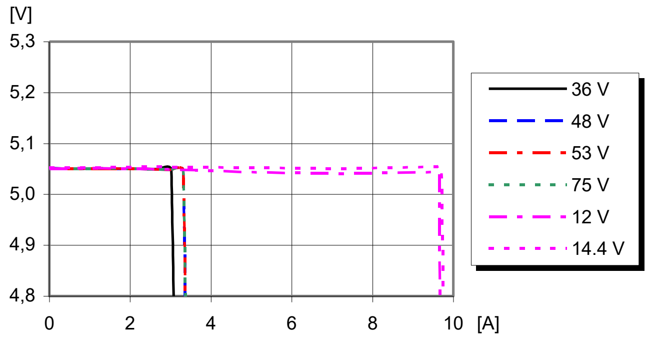
Output 2 voltage vs. load 2 current at:
T_{P1} = +25 °C. I_{O1} = 0 A, V_I = 53 V when external voltage is supplied,
max continuous P_{O2} = 15 W without external supply,
max continuous I_{O2} = 5 A and max peak I_{O2} = 7 A with external supply

Power Dissipation, output voltage adjusted to 7.0 V



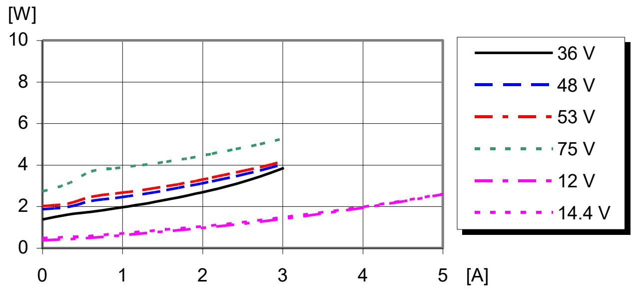
Output 2 voltage vs. load 2 current at:
T_{P1} = +25 °C. I_{O1} = 0 A, V_I = 53 V when external voltage is supplied, no losses in main unit included for the curves when external voltage is supplied,
max continuous P_{O2} = 15 W without external supply,
max continuous I_{O2} = 5 A and max peak I_{O2} = 7 A with external supply

Output Characteristics, unadjusted output voltage



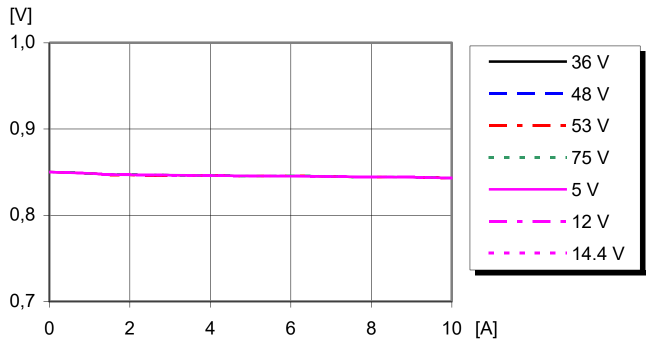
Output 2 voltage vs. load 2 current at:
T_{P1} = +25 °C. I_{O1} = 0 A, V_I = 53 V when external voltage is supplied,
max continuous P_{O2} = 15 W without external supply,
max continuous I_{O2} = 5 A and max peak I_{O2} = 7 A with external supply

Power Dissipation, unadjusted output voltage



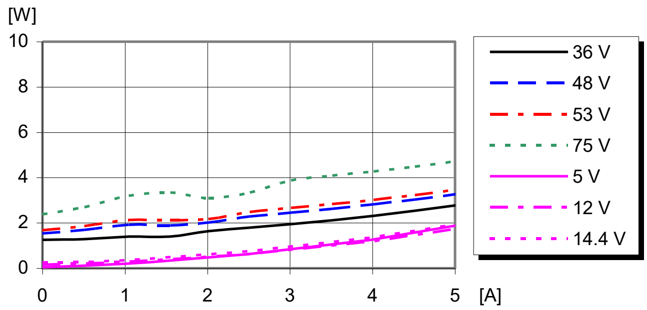
Output 2 voltage vs. load 2 current at:
T_{P1} = +25 °C. I_{O1} = 0 A, V_I = 53 V when external voltage is supplied, no losses in main unit included for the curves when external voltage is supplied,
max continuous P_{O2} = 15 W without external supply,
max continuous I_{O2} = 5 A and max peak I_{O2} = 7 A with external supply

Output Characteristics, output voltage adjusted to 0.85 V



Output 2 voltage vs. load 2 current at:
T_{P1} = +25 °C. I_{O1} = 0 A, V_I = 53 V when external voltage is supplied,
max continuous P_{O2} = 15 W without external supply,
max continuous I_{O2} = 5 A and max peak I_{O2} = 7 A with external supply

Power Dissipation, output voltage adjusted to 0.85 V



Output 2 voltage vs. load 2 current at:
T_{P1} = +25 °C. I_{O1} = 0 A, V_I = 53 V when external voltage is supplied, no losses in main unit included for the curves when external voltage is supplied,
max continuous P_{O2} = 15 W without external supply,
max continuous I_{O2} = 5 A and max peak I_{O2} = 7 A with external supply

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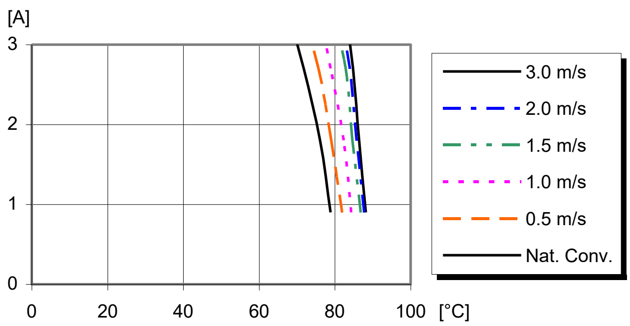
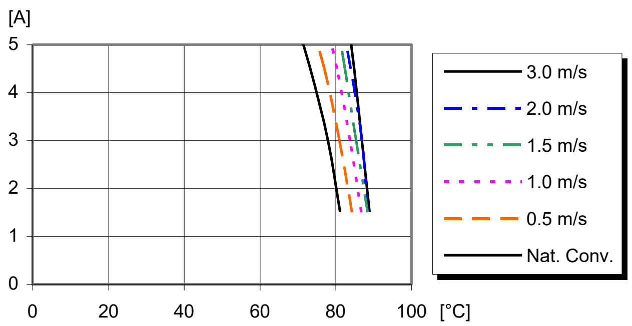
Management Power (Output 2), 5.05 V, 15 W / 5 A, Typical Characteristics — PIM 4820B PD

Output Current Derating, no external supply



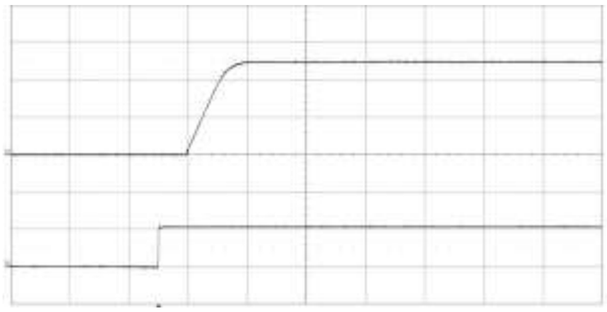
Available load current vs. ambient air temperature and airflow at V_I = 53 V, no external supply, I_{O1} = 8.25 A, unadjusted output 2 voltage (V_{O2} = 5.05 V).
See Thermal Consideration section.

Output Current Derating, external 12 V supply



Available load current vs. ambient air temperature and airflow at V_I = 53 V, V_{IN2} = 12 V, I_{O1} = 8.25 A, unadjusted output 2 voltage (V_{O2} = 5.05 V).
See Thermal Consideration section.

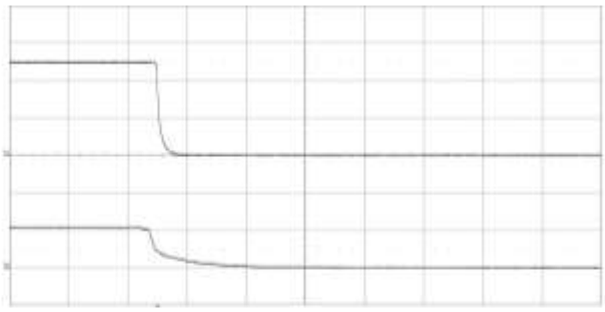
Start-up



Start-up enabled by connecting V_I at:
T_{P1} = +25 °C, V_I = 53 V, I_{O1} = 0 A,
I_{O2} = 3.0 A resistive load, unadjusted output 2 voltage (V_{O2} = 5.05 V), no hold-up capacitance, no output 1 capacitance.

Top trace: output 2 voltage (2 V/div.)
Bottom trace: input voltage (50 V/div.)
Time scale: (5 ms/div.)

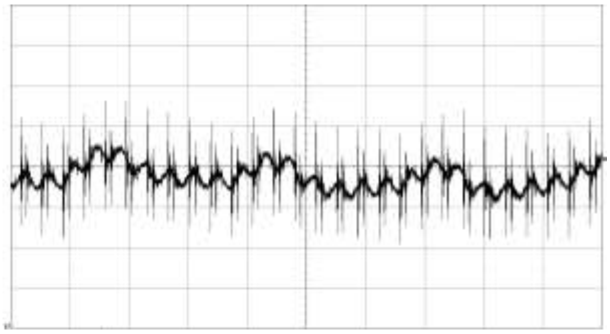
Shut-down



Shut-down enabled by disconnecting V_I at:
T_{P1} = +25 °C, V_I = 53 V, I_{O1} = 0 A,
I_{O2} = 3.0 A, resistive load, unadjusted output 2 voltage (V_{O2} = 5.05 V), no hold-up capacitance, no output 1 capacitance.

Top trace: output 2 voltage (2 V/div.)
Bottom trace: input voltage (50 V/div.)
Time scale: (2 ms/div.)

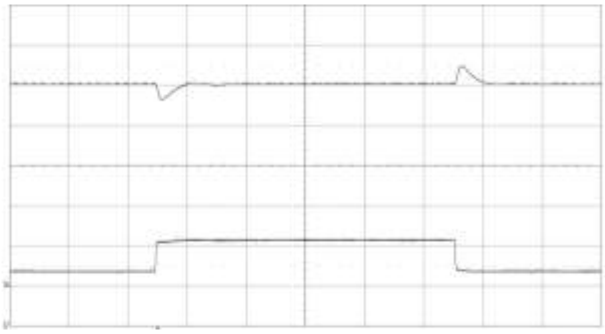
Output 2 Ripple & Noise



Output voltage ripple at:
T_{P1} = +25 °C, V_I = 53 V,
I_{O1} = 0 A, I_{O2} = 3.0 A, resistive load, unadjusted output 2 voltage (V_{O2} = 5.05 V).

Output 2 voltage (20 mV/div.).
Time scale: (5 µs/div.).

Output Load Transient Response



Output voltage response to load current step-change, output 2 (0.75-2.25-0.75 A) at:
T_{P1} = +25 °C, V_I = 53 V I_{O1} = 0 A,
unadjusted output 2 voltage (V_{O2} = 5.05 V).

Top trace: output 2 voltage (0.5 V/div.)
Bottom trace: output 2 current (2 A/div.)
Time scale: (0.1 ms/div.)

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Technical Specification

PIM 4820 series Power Interface Module Input 36-75 V, Output up to 16.5-20 A / 960-1080 W	28701-EN/LZT146443 Rev G November 2017
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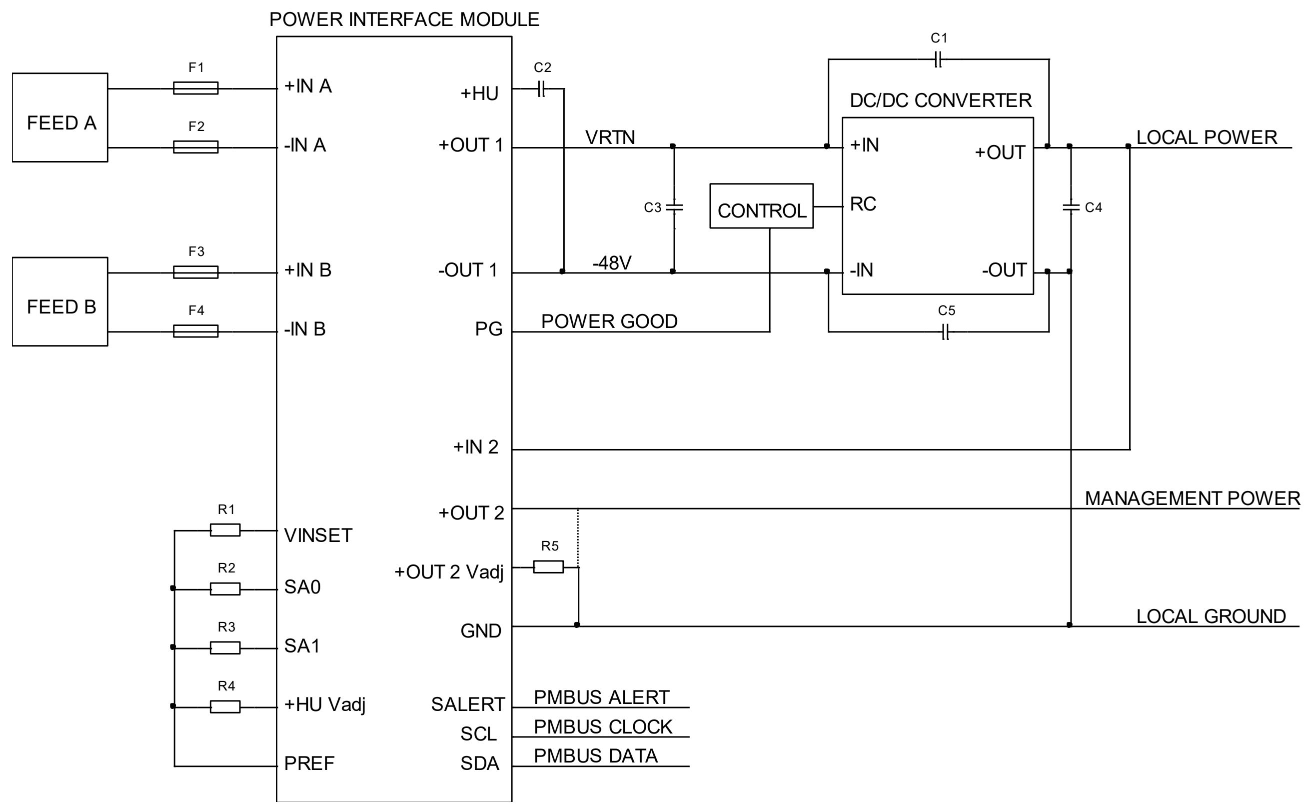
Typical Application Circuit



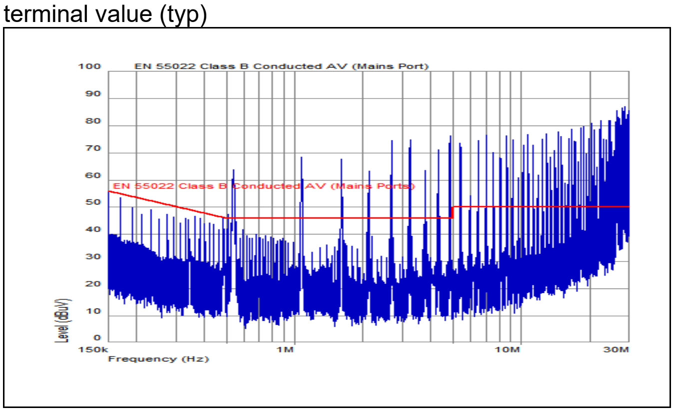
External components
C1 = EMI suppression capacitor
C2 = hold-up capacitor, C_{HU}
C3 = DC/DC converter input capacitor, C_{O1} (see technical specification for the DC/DC converter)
C4 = DC/DC converter output capacitor (see technical specification for the DC/DC converter)
C5 = EMI suppression capacitor
F1 = fuse (recommended >25 A)
F2 = fuse (recommended >25 A)
F3 = fuse (recommended >25 A)
F4 = fuse (recommended >25 A)
R1 = input voltage range pin-strap resistor, R_{VINSET} (see Input Voltage Range Setting section)
R2 = PMBus address pin-strap resistor, R_{SA0} (see PMBus Addressing section)
R3 = PMBus address pin-strap resistor, R_{SA1} (see PMBus Addressing section)
R4 = hold-up voltage adjust resistor, $R_{+HU\ Vadj}$ (see Hold-up Capacitor Charge section)
R5 = management power voltage adjust resistor, $R_{+OUT\ 2\ Vadj}$ (see Management power, output voltage adjust section)

PIM 4820 series Power Interface Module Input 36-75 V, Output up to 16.5-20 A / 960-1080 W	28701-EN/LZT146443 Rev G November 2017 © Flex

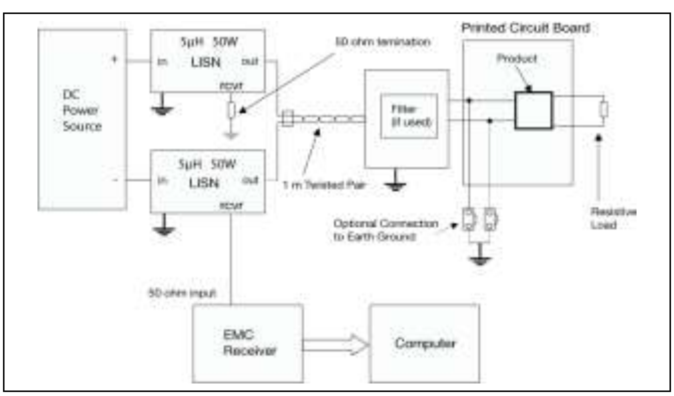
EMC Specification

Conducted EMI measured according to EN 55022, CISPR 22 and FCC part 15J (see test set-up). See Design Note 009 for further information. The management power first stage typical fundamental switching frequency is 510 kHz and the second stage typical fundamental switching frequency is 480 kHz. PIM 4820B PD suppresses only high frequency conducted EMI from the downstream DC/DC converter. In order to suppress noise further additional filters have to be placed in feed A and B. Follow the downstream DC/DC converter supplier guidelines for design of such filters.

Conducted EMI, Management power (Output 2), Input terminal value (typ)

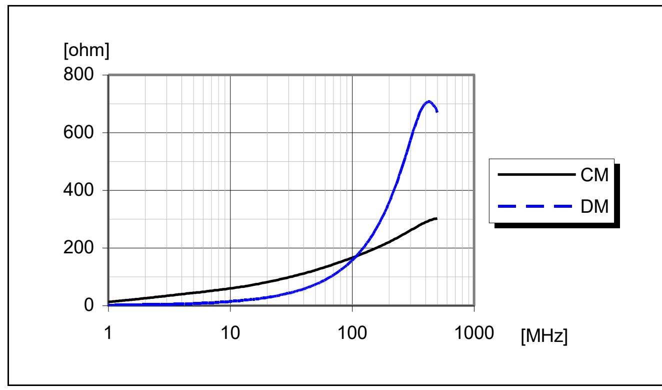


EMI without filter, without external supply, without downstream DC/DC converter



Test set-up

High frequency conducted EMI suppression (Output 1 and Output 2)



Common mode (CM) and differential mode (DM) impedance versus frequency

Layout Recommendations

The radiated EMI performance of the product will depend on the PWB layout and ground layer design. It is also important to consider the stand-off of the product. If a ground layer is used, it should be connected to the output of the product and the equipment ground or chassis.
A ground layer will increase the stray capacitance in the PWB and improve the high frequency EMC performance.

The pin-strap resistors, R_{VINSET} and R_{SA0}/R_{SA1} and the voltage adjust resistors for hold-up and output 2 should be placed as close to the product as possible to minimize loops that may pick up noise.
Avoid current carrying planes under the pin-strap and the voltage adjust resistors and the PMBus signals.

Operating information

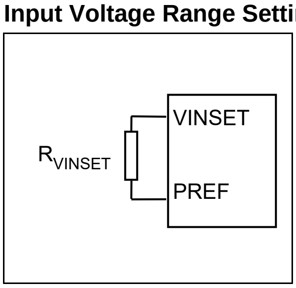
Power Management Overview

This product is equipped with a PMBus interface. The product incorporates a range of readable and configurable power management features that are simple to implement with a minimum of external components. Additionally, the product includes protection features that continuously safeguard the load from damage due to unexpected system faults. A fault is also shown as an alert on the SALERT pin. The following product parameters can continuously be monitored by a host: ORed input voltage, ORed input current and internal junction temperature.

Input Voltage

The input voltage range 36 to 75 Vdc meets the requirements of the European Telecom Standard ETS 300 132-2 for normal input voltage range in -48 and -60 Vdc systems, -40.5 to -57.0 V and –50.0 to -72 V respectively.
At input voltages exceeding 75 V, the power loss will be higher than at normal input voltage and T_{P1} must be limited to absolute max +110 °C. The absolute maximum continuous input voltage is 80 Vdc.

Input Voltage Range Setting



Using an external Pin-strap resistor, R_{VINSET}, the input voltage range can be set in the four different ranges shown in the table below. (The setting affects input turn on, input turn off, OVP and hold-up trig levels). The resistor should be connected between the VINSET pin and the PREF pin.

The following table shows recommended resistor values for R_{VINSET}. Maximum 1% tolerance resistors are required.

Range	R_{VINSET}	Turn-on	Turn-off	Feed ALARM on	Feed ALARM off	OVP
3	100 kΩ	44.2 V	42 V	33.9 V	35.9V	65 V
2	39 kΩ	43.7 V	38.5 V	33.5 V	35.5 V	77 V
1	12 kΩ	43.5 V	38.5 V	33.5 V	35.5 V	80 V
0	closed	38.2 V	33 V	29 V	31 V	80 V

A/B Feed ORing

Eight MOSFETs (four ORing controls) provide ORing of the input feeds. If a short is detected on one of the feeds a control circuit will detect reverse current and quickly turn the MOSFETs off. This feature also protects the product against reverse polarity up to 60 V. If a fuse blow is desired in case of reverse polarity place TVS diodes between negative and positive branch in both feeds. At high load operation the MOSFETs are operated at a low $R_{DS(on)}$ condition.

ORing MOSFET short circuit check

All input feed ORing FETs are monitored. Short circuited ORing FETs in the supplying feeds will be detected and reported through the product PMBus interface. The “FET Check” function periodically and briefly, turns off either both high side or both low side ORing FETs. During the off state, the “FET Check” function detects the forward voltage (V_f) through the ORing FET. The “FET Check” function requires a minimum load of 2 A on Output 1 to detect short; no FET Check faults will be reported if load < 2A.

Hot Swap Functionality

The hot swap function is designed to control the inrush current to the downstream DC/DC converter. The level and duration of the inrush current complies with the PICMG 3.0 ATCA base specification Inrush transient specifications.
Note: The hot swap circuit limits the main unit output current during start up. Hence, output 1 cannot be loaded before its external filter capacitor has been charged (power good pin (PG) is asserted)

Hold-up Capacitor Charge

An internal DC/DC converter charges the hold-up capacitor to a voltage of 40 to 95 V. The charge level is set by an external resistor. If no resistor is connected to the +HU Vadj the V_{HU} voltage defaults to ~50V.

Resistor connected between +HU Vadj and PREF for hold-up voltages from 50 to 95 V:

$$R_{+HU\,Vadj} = \frac{500}{V_{HU} - 50} - 10 \quad [k\Omega]$$

where V_{HU} is the hold-up voltage.

Resistor connected between +HU Vadj and +HU for hold-up voltages from 40 to 50 V:

$$R_{+HU\,Vadj} = \frac{400 \times V_{HU} - 500}{50 - V_{HU}} - 10 \quad [k\Omega]$$

where V_{HU} is the hold-up voltage.

The hold-up capacitor will be connected to the power train and provide energy to the system whenever the voltage on both A and B feeds has dropped below the hold-up trig level. When the voltage level on one or either feeds has returned to the input turn on voltage the hold-up capacitor will go off line and be recharged. The hold-up capacitance is calculated by the following formula:

$$C_{HU} \geq \frac{2.6 \times P \times t_{HU}}{V_{HU}^2 - V_{HU\,trig}^2} \quad [mF]$$

where P is the power of the downstream DC/DC converter, t_{HU} is the hold-up time (ms), V_{HU} is the hold-up voltage and $V_{HU\,trig}$ is the hold-up trig level which normally is selected to be at or above the input turn off voltage for the downstream DC/DC converter. Conditions for best formula accuracy: $V_{HU} \geq 75$ V, $C_{HU} \geq C_{O1}$, 1 ms $\leq t_{HU} <$ 10 ms.

If no hold-up is used (pin 16 and 18), these pins can be left open.

Hold-up Capacitor Safety Discharge

When input A and input B are disconnected the hold-up and output capacitors will be discharged to less than 60 V within 1 s, conditions:

- C_{HU} is selected to be equal or less than the calculated value when using formula in section "Hold-up Event Voltage" and using variables VRTN = 75 V and $V_{HU\,trig}$ = 38.5 V.
- C_{HU} must not exceed 3.3 mF.

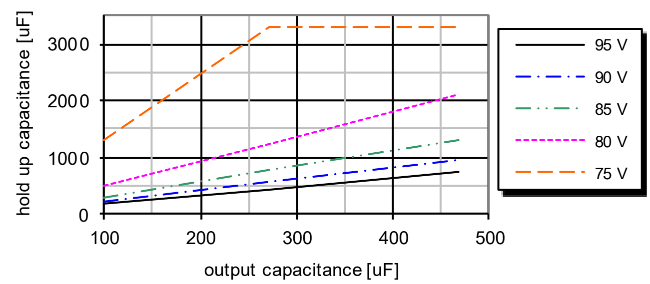
If larger C_{HU} is used a bleeder has to be added to output 1 to ensure discharge of the hold-up and output capacitors to a voltage below 60 V within 1 s.

Hold-up Event Voltage

The resulting voltage across the output capacitor at a hold-up event depends on the selected hold-up voltage and the relation between hold-up- and output 1 capacitance. Maximum allowed hold-up capacitance can be calculated using the following formula:

$$C_{HU} = \frac{(C_{O1} + 10) \times (VRTN - V_{HU\,trig})}{V_{HU} - VRTN} \quad [\mu F]$$

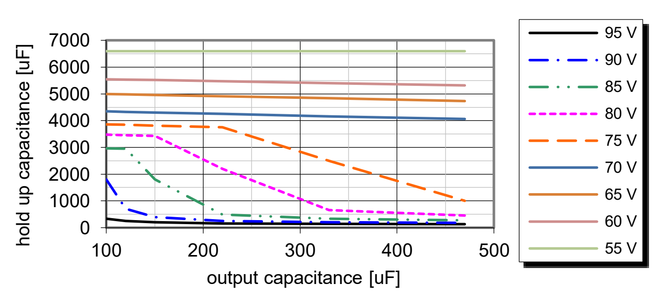
where C_{HU} is the hold-up capacitance, C_{O1} is the output 1 capacitance (μF), VRTN is the max input voltage for the downstream DC/DC converter, $V_{HU\,trig}$ is the hold-up trig level and V_{HU} is the hold-up voltage. Make sure that the resulting voltage is lower than maximum specified input voltage for the downstream DC/DC converter.



The chart shows output 1 and hold-up capacitances at different hold-up voltages for maximum 72 V peak input voltage to the downstream DC/DC converter.

Hold-up SOA

Apart from the constraints upon C_{HU} set by section above and/or safety discharge section, the C_{HU} must be selected using below SOA chart and/or table.



The chart above and the table below shows max allowed Hold-Up capacitor value as function of the output 1 capacitor C_{O1} value and the Hold-Up voltage V_{HU}.

V_{HU} [V]								
C_{O1} [µF]	60	65	70	75	80	85	90	95
100	5550	4990	4350	3850	3470	2970	1800	330
120	5540	4980	4330	3840	3440	2950	700	250
150	5520	4960	4310	3810	3420	1800	400	200
220	5470	4900	4250	3750	2200	490	250	160
330	5403	4830	4160	2500	660	330	200	140
470	5320	4730	4060	660	450	280	180	130

Start-up Procedure

The product follows a specific internal start-up procedure after power is applied to input A or input B:

1. Management power (Output 2) is available
2. Status of the PMBus address and input voltage range pin-straps are checked and values associated with the settings are loaded.
3. When input A or input B reaches the turn on voltage level set by the input voltage range pin-strap, the Hot swap circuit is enabled and the hold-up generator starts to charge the hold-up capacitor.
4. The Hot Swap controller charges C_{O1} for a defined time with a defined maximum current throughout or with a maximum power loss over the Hot Swap FET. If C_{O1} cannot be charged such as V_{O1} equals V_I within the defined time the module shuts down the Hot Swap FET. See OCP fault response time.
5. The module waits a time equal to 100 times the OCP fault response time ~70 ms before attempting to charge C_{O1} as described in “item” 4 above again.

   The module makes three attempts to charge C_{O1}. If they fail the module pauses for about 2 seconds before attempting a new start sequence as described above.
6. If C_{O1} can be charged until V_{O1} equals V_I within the OCP fault response time period the unit asserts the PG signal after a delay.

   The delay between C_{O1} is charged to V_I and until PG is asserted will be about 100 times the time the module needed to limit the current through, or power loss over, the Hot Swap FET during charging of C_{O1}.

   Hence the charging time of C_{O1}, V_{O1} voltage waveform and the PG assertion delay will be dependent on VI and C_{O1}. The PG assertion delay will in its extremes vary between 0 and 100 ms.

   At high V_I voltages and large C_{01} the V_{O1} will be a staircase shaped waveform.

Once this procedure is completed the product is ready to be loaded and accept commands via the PMBus interface, which will overwrite any default values used during the start-up procedure. Please note that an additional time may be needed in order to fully charge the hold-up capacitor, depending on capacitance and hold-up voltage.

Shut Down Procedure

The product follows a specific internal shut down procedure after power is removed from input A and input B. At moderate slew rates on V_I the following response will occur.

1) When V_{O1} reaches the V_{HU} trig level the module tries to restore the V_{O1} level by triggering a hold-up discharge. When operating in conditions where V_{O1} is at or is lower than the V_{HU} trig level the modules continuously and cyclically trigger hold-up dump discharges onto V_{O1}.

   If used and configured properly the ALERT signal is asserted and latched when the V_{O1} reaches the $V_{HU\ trig}$ threshold.

2) If V_I falls below the $V_{I\ off}$ threshold and not returns above $V_{I\ on}$ threshold within 40 ms the module shuts down the V_{O1}, de-asserts the PG signal and enables the safety discharge of C_{HU} and C_{O1}.

   or

   If both feeds are detected to be below FEED alarm on threshold for longer than 40 ms the module shuts down the V_{O1}, de-asserts the PG signal and enables the safety discharge of C_{HU} and C_{O1}.

3) When V_I reaches below the $V_{I\ off}$ level for the V_{O2} the V_{O2} shuts down. (If an auxiliary supply is connected, this supply behavior will determine how V_{O2} behaves).

Power Good

The power good (PG) pin indicates that output 1 is ready to be loaded. V_{O1} must not be loaded prior to that the PG is asserted. An open collector turns on (sinks current) when the output 1 voltage is enabled and is equal to the voltage present on input A or input B. See sections describing the start up and shut down procedure above. PG is referenced to –OUT1.

Management power (Output 2)

The product provides an isolated DC output referred to GND. The voltage is adjustable and it is available as soon as the input voltage level is within the input voltage range. The output is short circuit protected.

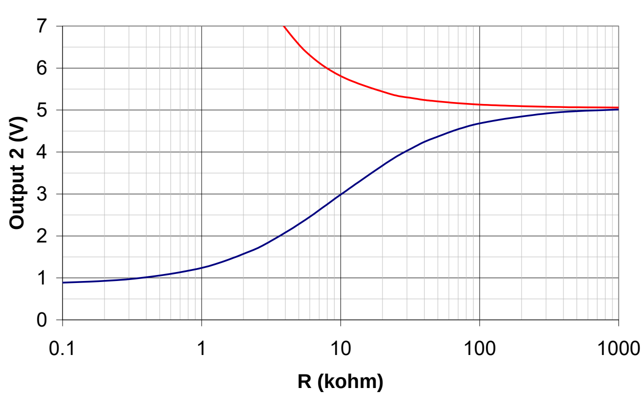
Management power (Output 2), output voltage adjust

Management power output voltage can be adjusted between 0.85 V and 7.0 V.
For management power output voltages greater than 5.05 V and up to 7.0 V a resistor is connected between +OUT 2 Vadj and GND, the resistance can be calculated using the following formula:

$$R_{+OUT\ 2Vadj} = \frac{8.2 - 0.1 \times V_{O2}}{V_{O2} - 5.05} \quad [k\Omega]$$

For management power output voltages less than 5.05 V and down to 0.85 V a resistor is connected between +OUT 2 Vadj and +OUT 2, the resistance can be calculated using the following formula:

$$R_{+OUT\ 2Vadj} = \frac{9.6 \times V_{O2} - 8.1}{5.05 - V_{O2}} \quad [k\Omega]$$



Management power (Output 2), external power supply

With an external power supply (Input 2) management power can be continuously loaded with 5 A and handle peak loads up to 7 A.
The external power supply voltage has to be 1.5 V greater than the management power output voltage in order to deliver the correct management power output voltage for loads exceeding 15 W. The power dissipation for loads up to 15 W will decrease if the external power supply voltage is 12 V or greater.

Management power (Output 2), Pre-Bias Startup Capability

Pre-bias startup often occurs in complex digital systems when current from another power source is fed back through a dual-supply logic component, such as FPGAs or ASICs. The PIM 4820B PD management power incorporates synchronous rectifiers, but will not sink current during startup, or turn off, or whenever a fault shuts down the product in a pre-bias condition.

Input Transient Over Voltage Protection

The product incorporates a transient voltage protector which will protect the product and the downstream DC/DC converter against over voltage transients exceeding 80 V. The transient voltage protector is rated for 1.5 kW peak pulse power with a breakdown voltage of 83 V. The product also handles transients of up to 100 V for 10 µs.

Over Voltage Protection (OVP)

The main unit (Output 1) of the product includes over voltage limiting circuitry for protection of the load. The OVP can be set in four different levels, see Input voltage range setting section.

Over Temperature Protection (OTP)

The main unit (Output 1) of the product is protected from thermal overload by a temperature calibrated micro controller. When T_{P1} as defined in thermal consideration section exceeds 110 °C an OT flag is asserted in the PMBus accessible STATUS and FAULT registers and when T_{P1} exceeds 120 °C the product will shut down. The product will make continuous attempts to start up (non-latching mode) and resume normal operation automatically when the temperature has dropped > 10 °C below the temperature threshold. In an over temperature situation the management power is still available.

Over Current Protection (OCP)

Both the main unit (Output 1) and the management power (Output 2) of the product include current limiting circuitry for protection at continuous overload.

The main unit (Output 1) will abruptly be interrupted if the output overcurrent- or an internal component overpower thresholds are exceeded for a time longer than the stated fault response time.

The management power (Output 2) output voltage will decrease towards zero for output currents in excess of max output current. The product will resume normal operation after removal of the overload. The load distribution should be designed for the maximum output short circuit current specified.

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Increased output 1 maximum current to 20 A

Maximum continuous current is chosen to 16.5 A in order to ensure sufficient headroom for current transients (between 16.5 A and the current limit trig point). Such transients could be the result of a sudden change in input voltage due to a feed switch for instance. However, under benign circumstances maximum continuous current could be increased to 20 A.

Following conditions have to be met for continuous 20 A operation:

- possible input voltage step less than 5 V

or all the following constraints

- possible input voltage step less than 20 V
- the slew rate of an input voltage step shall not exceed 1 V/µs
- the hold-up voltage shall be at least as high as the maximum input voltage
- the hold-up capacitor shall be chosen to give at least 1 ms hold-up time

Thermal Consideration

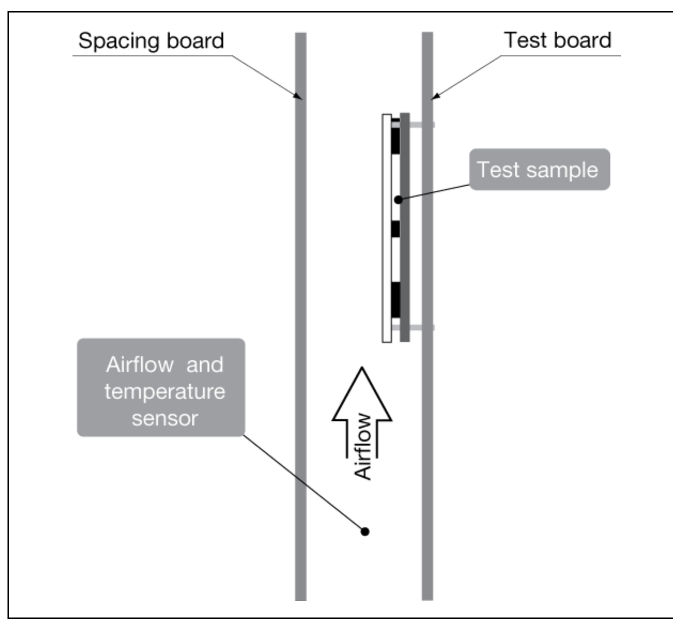
General

The products are designed to operate in different thermal environments and sufficient cooling must be provided to ensure reliable operation.

For products mounted on a PCB without a heat sink attached, cooling is achieved mainly by conduction, from the pins to the host board, and convection, which is dependent on the airflow across the product. Increased airflow enhances the cooling of the product. The Output Current Derating graphs found in the Output section provides the available output current vs. ambient air temperature and air velocity at V_I = 53 V with and without external 12 V management power supply.

A guard band of 5 °C is applied to the maximum recorded component temperatures when calculating output current derating curves.

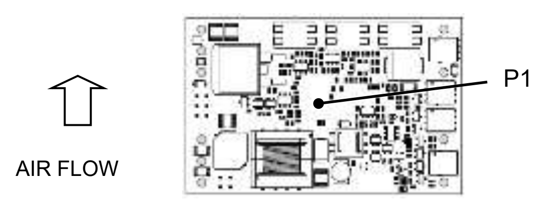
The product is tested on a 254 x 254 mm, 35 µm (1 oz), 16-layer test board mounted vertically in a wind tunnel with a cross-section of 608 x 203 mm.



Definition of product operating temperature

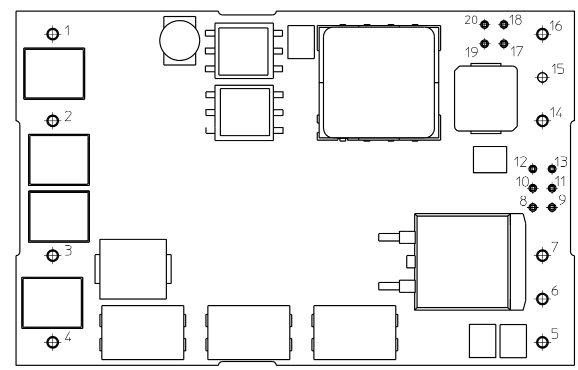
The product operating temperature is used to monitor the temperature of the product, and proper thermal conditions can be verified by measuring the temperature at position P1 (the temperature can be monitored by PMBus). The temperature shall not exceed the maximum temperature in the table below. Temperatures above maximum T_{P1}, is not allowed and may cause permanent damage.

Position	Description	Max Temp.
P1	Printed wiring board	T_{P1} = 105 ºC



Temperature position and air flow direction.

Connections



Pin layout, top view (component placement for illustration only).

Pin	Designation	Function
1	+IN A	Input A, positive feed
2	+IN B	Input B, positive feed
3	-IN A	Input A, negative feed
4	-IN B	Input B, negative feed
5	+OUT 1	Main unit, positive output
6	-OUT 1	Main unit, negative output
7	+HU	Hold-up capacitor bank, positive side
8	+HU Vadj	Hold-up, voltage adjust
9	PG	Power good
10	SA1	PMBus address pin-strap 1
11	SA0	PMBus address pin-strap 0
12	PREF	Pin-strap reference
13	VINSET	Input voltage range
14	+IN 2	External management power supply
15	+OUT 2	Management power, positive output
16	GND	Management power, negative output
17	SALERT	PMBus alert
18	SCL	PMBus clock
19	SDA	PMBus data
20	+OUT 2 Vadj	Management power, voltage adjust

PMBus Interface

This product provides a PMBus digital interface that enables the user to monitor the input and output 1 voltages, input current and device temperature. The product can be used with any standard two-wire I^2C or SMBus host device. In addition, the module is compatible with PMBus version 1.2 and includes an SALERT line to help mitigate bandwidth limitations related to continuous fault monitoring. The product supports bus clock frequencies from 10 to 400 kHz. The PMBus signals, SCL, SDA and SALERT have internal 47 kΩ pull-up resistors to 3.3 V (referred to GND). External pull-up resistors may be added to the PMBus. Note that the SALERT signal driver capability is lower than the PMBus compatible SDA and SCL signal drive capabilities.

Monitoring via PMBus

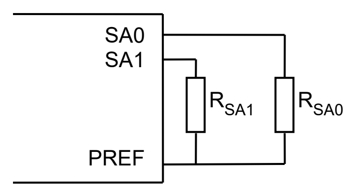
It is possible to monitor a variety of different parameters and status/fault flags through the PMBus interface. Status and fault conditions can be monitored using the SALERT pin, which will be asserted when a number of pre-configured fault or warning conditions occur. It is also possible to continuously monitor one or more of the below parameters:

Monitored parameters
- ORed input voltage
- ORed input current
- Internal junction temperature

Monitored status/fault flags
- Over temperature
- ORed input over current
- Feed A under voltage
- Feed B under voltage
- ORed input over voltage
- ORed input under voltage
- ORing MOSFET short circuit
- Output 1 under voltage

PMBus Addressing

The PMBus address should be configured with resistors connected between the SA0/SA1 pins and the PREF pin, as shown in the figure below. Recommended resistor values for hard-wiring PMBus addresses are shown in the table. 1% tolerance resistors are required.



Schematic of connection of address resistor.

SA0 index	R_{SA0}	SA1 index	R_{SA1}
7	open	7	open
6	120 kΩ	6	120 kΩ
5	56 kΩ	5	56 kΩ
4	27 kΩ	4	27 kΩ
3	18 kΩ	3	18 kΩ
2	10 kΩ	2	10 kΩ
1	4.7 kΩ	1	4.7 kΩ
0	closed	0	closed

The PMBus address follows the equation below:

Eq. 8

$$\text{PMBus address (decimal)} = 8 \times (\text{SA1 index}) + (\text{SA0 index})$$

Note: PMBus address = 127d for closed R_{SA0} and R_{SA1}

The user can theoretically configure up to 64 unique PMBus addresses. The user shall also be aware of further limitations of the address space as stated in the SMBus Specification.

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Technical Specification

PIM 4820 series Power Interface Module Input 36-75 V, Output up to 16.5-20 A / 960-1080 W	28701-EN/LZT146443 Rev G November 2017 © Flex

PMBus Commands

The product is PMBus compliant. The following table lists the implemented PMBus commands. For more detailed information see PMBus Power System Management Protocol Specification; Part I – General Requirements, Transport and Electrical Interface and PMBus Power System Management Protocol; Part II – Command Language.

Designation	Cmd	Impl
PMBUS_OPERATION	01h	Yes
CLEAR_FAULTS	03h	Yes
PMBUS_COEFFICIENTS	30h	Yes
STATUS_BYTE	78h	Yes
READ_VIN (DIRECT)	88h	Yes
READ_IIN (DIRECT)	89h	Yes
READ_TEMPERATURE_1 (DIRECT)	8Dh	Yes
PMBUS_REVISION	98h	Yes
MFR_ID	99h	Yes
MFR_MODEL	9Ah	Yes
MFR_REVISION	9Bh	Yes
MFR_LOCATION	9Ch	Yes
MFR_DATE	9Dh	Yes
MFR_SERIAL	9Eh	Yes
MFR_READ_STATUS	D0h	Yes
MFR_RW_FAULT	D1h	Yes
MFR_RW_ALERT	D2h	Yes
MFR_RW_CONTROL	D4h	Yes

Notes:
Cmd is short for Command.
Impl is short for Implemented.
RW is short for Read Write access
CLEAR_FAULTS only supports clearing of the CML bit.
STATUS_BYTE only supports reading of the CML bit.
DIRECT, value is represented in PMBus DIRECT format. The coefficients are obtained using the PMBUS_COEFFICENTC cmd; see PMBus specification rev. 1.2 chapters 7.2 and 14.1.

PMBus STATUS, FAULT and ALERT registers

Basically the flag within the STATUS register is only asserted when a fault or certain status is present.
The FAULT register latches any assertion of flags in the STATUS register.
The ALERT register is used to mask which of the flags in the FAULT register that generates an assertion of the PMBus SALERT signal.

The SALERT signal is only activated when any of the flags, selected by the ALERT register, is asserted in the FAULT register. By clearing the FAULT register flag(s) the SALERT signal assertion can be cleared.

The SALERT signal will remain activated until all of the flags, selected by the ALERT register, are cleared in the FAULT register.

MFR_READ_STATUS (STATUS register)

A read only register that display any current status/faults.

Designation	Bit
STATUS_FLAG_OV	0
STATUS_FLAG_UV	1
STATUS_FLAG_OC	2
STATUS_FLAG_FBUV	3
STATUS_FLAG_FAUV	4
STATUS_FLAG_FET	5
STATUS_FLAG_OT	6
STATUS_FLAG_HU_EVENT	7

MFR_RW_FAULT (FAULT register)

A read/write register that latch the status/fault flags asserted in the STATUS register. Flags are cleared by writing a one “1” to the corresponding flag.

Designation	Bit
FAULT_FLAG_OV	0
FAULT_FLAG_UV	1
FAULT_FLAG_OC	2
FAULT_FLAG_FBUV	3
FAULT_FLAG_FAUV	4
FAULT_FLAG_FET	5
FAULT_FLAG_OT	6
FAULT_FLAG_HU_EVENT	7

MFR_RW_ALERT (ALERT register)

A Read/Write register that selects which of the status/fault flag in the FAULT register that will cause the SALERT signal to be asserted. Writing a one “1” to the flag will activate SALERT assertion when the corresponding flag is asserted in the FAULT register. A Write to the ALERT register will clear the SALERT signal.

Designation	Bit
ALERT_FLAG_OV	0
ALERT_FLAG_UV	1
ALERT_FLAG_OC	2
ALERT_FLAG_FBUV	3
ALERT_FLAG_FAUV	4
ALERT_FLAG_FET	5

ALERT_FLAG_OT	6
ALERT_FLAG_HU_EVENT	7

STATUS/FAULT/ALERT flag description

Designation	Function
FLAG_OV	Asserted when an Over Voltage (OV) is present on the ORed input voltage node. The Over Voltage Protection (OVP) is activated and disables output 1. The OVP threshold is dependent on the input voltage range setting.
FLAG_UV	Asserted when an Under Voltage (UV) is present on the ORed input voltage node. The Under Voltage Lock Out (UVLO) is activated and disables output 1. The UVLO threshold is dependent on the input voltage range setting.
FLAG_OC	Asserted when an Over Current (OC) and/or an Over Power (OP) condition is sensed on the ORed input voltage node.
FLAG_FBUV	Asserted when the input voltage on FEED A is reaching the ALARM_ON threshold or is below the ALARM_OFF threshold. The thresholds are dependent on the input voltage range setting.
FLAG_FAUV	Asserted when the input voltage on FEED A is reaching the ALARM_ON threshold or is below the ALARM_OFF threshold. The thresholds are dependent on the input voltage range setting.
FLAG_FET	Asserted when one or more of the ORing FETs are determined to be shorted (requires a current greater than approximately 2 A through the FET).
FLAG_OT	Asserted when the temperature sensor reaches 110°C. The Over Temperature Protection (OTP) is activated at 120°C and disables output 1.
FLAG_HU_EVENT	Asserted when the output 1 voltage reach the Hold-up (HU) activation voltage threshold. The HU threshold is dependent on the input voltage range setting.

PMBus CONTROL register

The bits within the CONTROL register control the behavior and/or operation of the PIM.

MFR_READ_CONTROL (CONTROL register)

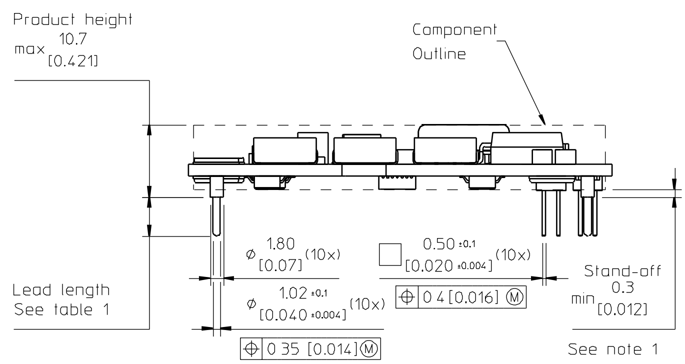
A read/write register for-control of the behavior and/or operation of the PIM.

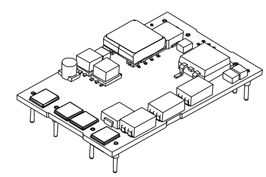
Designation	Bit
Reserved	0
Reserved	1
Reserved	2
Reserved	3
Reserved	4
CONTROL_VO1_DISABLE	5
CONTROL_VO1_RESTART	6
Reserved	7

CONTROL description

Designation	Function
VO1_DISABLE	Controls the output 1 (OUT 1). ´1´ Disable output, ‘0’ Enable output. Be careful when using this function. When the OUT1 is switched off all devices powered from this rail will be switched off. Some devices may clamp the digital bus when off. In such case the PIM cannot be switched on again via the bus. Only power cycling will then work. The situation may be overcome by partitioning off parts of the bus. Flex strongly recommends to partition off any BMR 453, 454, 456, 457 by means of a multiplexer or similar if the OUT1 of the PIM is going to be switched on and off via the digital bus.
VO1_RESTART	Forces the PIM to shut down the output 1 (OUT1), for a predefined time, before it automatically tries to restart the output. The bit is automatically cleared when modules tries to restart the output. ´1´ Force restart, ‘0’ Restart Enable.

Mechanical Information





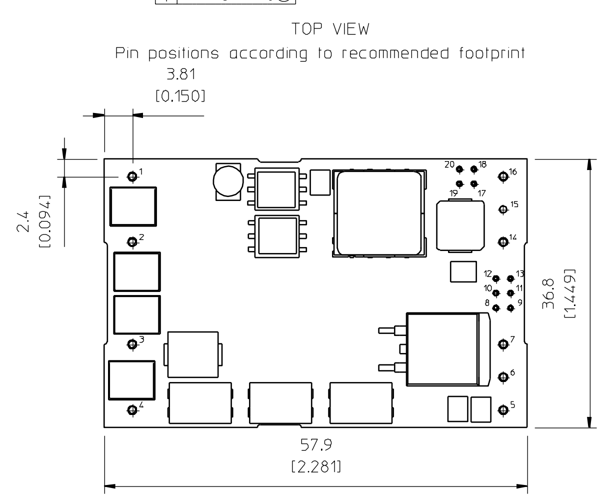
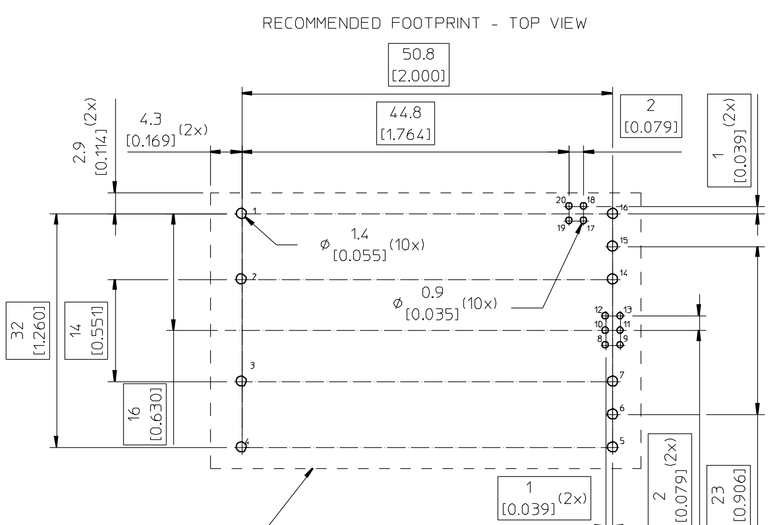


Table 1

Pin option	Lead Length
Standard	5.33 [0.210]
LA	3.69 [0.145]
LB	4.57 [0.180]
LC	2.79 [0.110]



Pins:
1-7, 14-16
Material: Copper alloy
Plating: 10µm Matte Tin over 4µm Nickel
8-13; 17-20
Material: CuSn4
Plating: min0,1 µm Gold over 2 µm Nickel

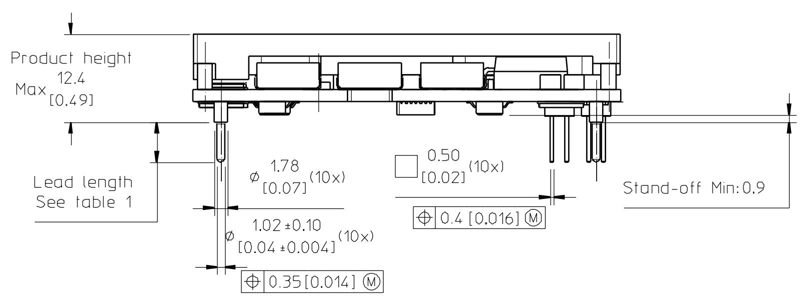
Notes
1- Stand off to none conductive components
min 0.3 [0.012]
Stand off to conductive components
min 0.9 [0.035]
For details see safety section page 3.

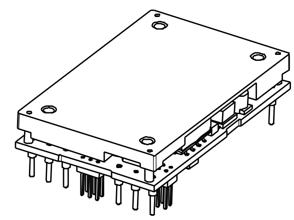
Recommended keep out area for user components

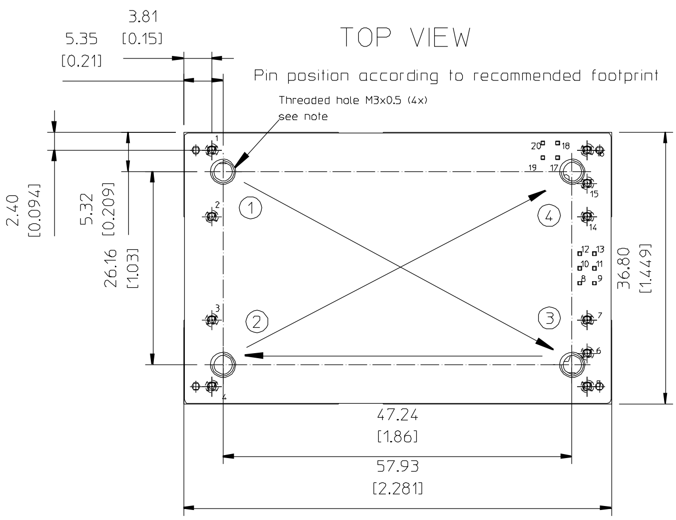
The standoff in combination with insulating material ensures that requirements as per IEC/EN/UL60950 are met and 2250 V isolation maintained even if open vias or traces are present under the power module.

Weight: typical 24.5 g
All dimensions in mm [inch].
Tolerances unless specified
x.x mm ±0.50 mm [0.02], x.xx mm ±0.25 mm [0.01]
(not applied on footprint or typical values)

Mechanical Information - Hole Mount, Baseplate Version







Case
Material: Aluminum
- For screw attachement apply mouting Torque of max 0.44Nm [3.9 lbf in]
  Too much stress will be applied to pins if using torque over max recommendaton, the internal connection might be weakened.
- M3 screw must not protrude more than 2.5mm [0.1] into the baseplate
- Recommended M3 screw mounting sequence 1->3->2->4
- Avoid leaving corner area empty when apply thermal pad, which might lead to baseplate warpage during screw mounting process

Pins:
1-7; 14-16
Material: Copper alloy
Plating: 10μm Au over 4μm Nickel
8-13; 17-20
Material: Copper alloy
Plating: min 0.1 μm Gold over 2 μm Nickel

RECOMMENDED FOOTPRINT - TOP VIEW

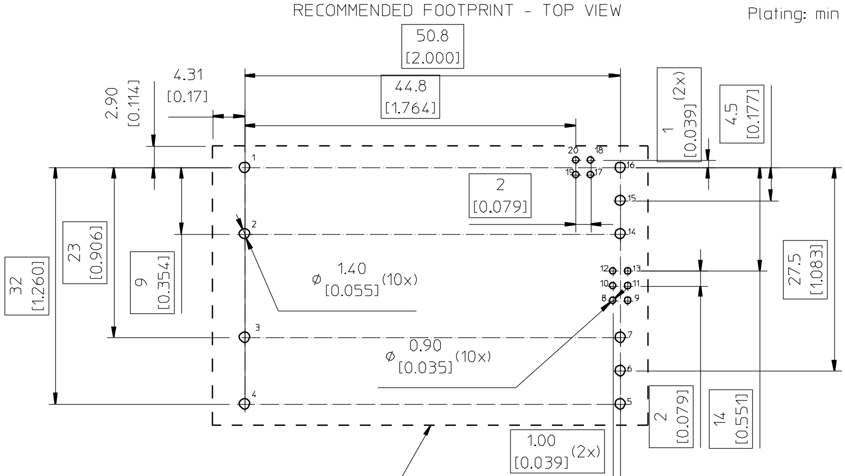


Table 1

Pin option	Lead Length
Standard	5.33 [0.210]
LA	3.69 [0.145]
LB	4.57 [0.180]
LC	2.79 [0.110]

Recommended keep out area for user components
The standoff in combination with insulating material ensures that requirements as per IEC/EN/UL60950 are met and 2250 V isolation maintained even if open vias or traces are present under the power module.

Weight: typical 49 g
All dimensions in mm [inch].
Tolerances unless specified
x.x mm ±0.50 mm [0.02], x.xx mm ±0.25 mm [0.01]
(not applied on footprint or typical values)

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Soldering Information - Hole Mounting

The hole mounted product is intended for plated through hole mounting by wave or manual soldering. The pin temperature is specified to maximum to 270°C for maximum 10 seconds.

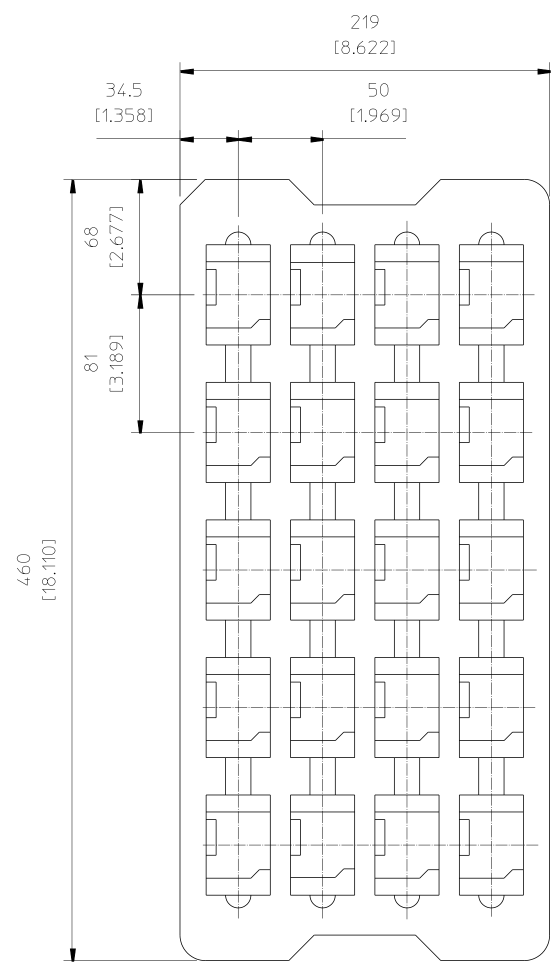
A maximum preheat rate of 4°C/s and maximum preheat temperature of 150°C is suggested. When soldering by hand, care should be taken to avoid direct contact between the hot soldering iron tip and the pins for more than a few seconds in order to prevent overheating.

A no-clean flux is recommended to avoid entrapment of cleaning fluids in cavities inside the product or between the product and the host board. The cleaning residues may affect long time reliability and isolation voltage.

Delivery Package Information

The products are delivered in antistatic trays.

Tray Specifications	
Material	Antistatic PE Foam
Surface resistance	10^5 < Ohm/square < 10^{12}
Bakeability	The trays are not bakeable
Tray thickness	24.00 mm [0.945 inch]
Box capacity	20 products (1 full trays/box)
Tray weight	Open Frame version- 43 g empty, 533 g full tray Baseplate version- 43 g empty, 1023g full tray



Product Qualification Specification

Characteristics			
External visual inspection	IPC-A-610		
Change of temperature (Temperature cycling)	IEC 60068-2-14 Na	Temperature range Number of cycles Dwell/transfer time	-40 to 100°C 1000 15 min/0-1 min
Cold (in operation)	IEC 60068-2-1 Ad	Temperature T_A Duration	-45°C 72 h
Damp heat	IEC 60068-2-67 Cy	Temperature Humidity Duration	85°C 85 % RH 1000 hours
Dry heat	IEC 60068-2-2 Bd	Temperature Duration	125°C 1000 h
Electrostatic discharge susceptibility	IEC 61340-3-1, JESD 22-A114 IEC 61340-3-2, JESD 22-A115	Human body model (HBM) Machine Model (MM)	Class 2, 2000 V Class 3, 200 V
Immersion in cleaning solvents	IEC 60068-2-45 XA, method 2	Water Glycol ether Isopropyl alcohol	55°C 35°C 35°C
Mechanical shock	IEC 60068-2-27 Ea	Peak acceleration Duration	100 g 6 ms
Moisture reflow sensitivity [1]	J-STD-020C	Level 1 (SnPb-eutectic) Level 3 (Pb Free)	225°C 260°C
Operational life test	MIL-STD-202G, method 108A	Duration	1000 h
Resistance to soldering heat [2]	IEC 60068-2-20 Tb, method 1A	Solder temperature Duration	270°C 10-13 s
Robustness of terminations	IEC 60068-2-21 Test Ua1 IEC 60068-2-21 Test Ue1	Through hole mount products Surface mount products	All leads All leads
Solderability	IEC 60068-2-58 test Td [1] IEC 60068-2-20 test Ta [2]	Preconditioning Temperature, SnPb Eutectic Temperature, Pb-free Preconditioning Temperature, SnPb Eutectic Temperature, Pb-free	150°C dry bake 16 h 215°C 235°C Steam ageing 235°C 245°C
Vibration, broad band random	IEC 60068-2-64 Fh, method 1	Frequency Spectral density Duration	10 to 500 Hz 0.07 g^2/Hz 10 min in each direction

Notes
[1] Only for products intended for reflow soldering (surface mount products)
[2] Only for products intended for wave soldering (plated through hole products)