1T 8051

8-bit Microcontroller

NuMicro® Family
MS51 Series
MS51DA9AE
MS51BA9AE
Datasheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

www.nuvoton.com

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1 GENERAL DESCRIPTION

The MS51 is an embedded flash type, 8-bit high performance 1T 8051-based microcontroller. The instruction set is fully compatible with the standard 80C51 and performance enhanced.

The MS51 8K Bytes of main Flash called APROM, in which the contents of User Code resides. The MS51 Flash supports In-Application-Programming (IAP) function, which enables on-chip firmware updates. IAP also makes it possible to configure any block of User Code array to be used as non-volatile data storage, which is written by IAP and read by IAP or MOVC instruction, this function means whole 8K Bytes area all can be use as Data Flash through IAP command. MS51 support an function of configurationable Flash from APROM called LDROM, in which the Boot Code normally resides for carrying out In-System-Programming (ISP). The LDROM size is configurable with a maximum of 4K Bytes by CONFIG define. There is an additional include special 128 bytes security protection memory (SPROM) to enhance the security and protection of customer application. To facilitate programming and verification, the Flash allows to be programmed and read electronically by parallel Writer or In-Circuit-Programming (ICP). Once the code is confirmed, user can lock the code for security.

The MS51 provides rich peripherals including 256 Bytes of SRAM, 1K Bytes of auxiliary RAM (XRAM), Up to 12 general purpose I/O, two 16-bit Timers/Counters 0/1, one 16-bit Timer2 with three-channel input capture module, one Watchdog Timer (WDT), one Self Wake-up Timer (WKT), one 16-bit auto-reload Timer3 for general purpose or baud rate generator, two UARTs with frame error detection and automatic address recognition, one SPI, one I^2C, five enhanced PWM output channels, eight-channel shared pin interrupt for all I/O, and one 12-bit ADC. The peripherals are equipped with 18 sources with 4-level-priority interrupts capability.

The MS51 is equipped with three clock sources and supports switching on-the-fly via software. The three clock sources include external clock input, 10 kHz internal oscillator, and one 16 MHz internal precise oscillator that is factory trimmed to ±1% at room temperature. The MS51 provides additional power monitoring detection such as power-on reset and 4-level brown-out detection, which stabilizes the power-on/off sequence for a high reliability system design.

The MS51 microcontroller operation consumes a very low power with two economic power modes to reduce power consumption — Idle and Power-down mode, which are software selectable. Idle mode turns off the CPU clock but allows continuing peripheral operation. Power-down mode stops the whole system clock for minimum power consumption. The system clock of the MS51 can also be slowed down by software clock divider, which allows for a flexibility between execution performance and power consumption.

With high performance CPU core and rich well-designed peripherals, the MS51 benefits to meet a general purpose, home appliances, or motor control system accomplishment.

2 FEATURES

Core and System	
8051	• Fully static design 8-bit high performance 1T 8051-based CMOS microcontroller. • Instruction set fully compatible with MCS-51. • 4-priority-level interrupts capability. • Dual Data Pointers (DPTRs).
Power On Reset (POR)	• POR with 1.15V threshold voltage level
Brown-out Detector (BOD)	• 4-level selection, with brown-out interrupt and reset option. (4.4V / 3.7V / 2.7V / 2.2V)
Low Voltage Reset (LVR)	• LVR with 2.0V threshold voltage level
Security	• 96-bit Unique ID (UID) • 128-bit Unique Customer ID (UCID) • 128-bytes security protection memory SPROM
Memories	
Flash	• 8 KBytes of APROM for User Code. • 4/3/2/1 Kbytes of Flash for loader (LDROM) configure from APROM for In-System-Programmable (ISP) • Flash Memory accumulated with pages of 128 Bytes from APROM by In-Application-Programmable (IAP) means whole APROM can be use as Data Flash • An additional 128 bytes security protection memory SPROM • Code lock for security by CONFIG
SRAM	• 256 Bytes on-chip RAM. • Additional 1 KBytes on-chip auxiliary RAM (XRAM) accessed by MOVX instruction.
Clocks	
Internal Clock Source	• Default 16 MHz high-speed internal oscillator (HIRC) trimmed to ±1% (accuracy at 25 °C, 3.3 V). • Selectable 24 MHz high-speed internal oscillator (HIRC). • 10 kHz low-speed internal oscillator (LIRC) calibrating to ±1% by software from high-speed internal oscillator
Timers	

16-bit Timer	• Two 16-bit Timers/Counters 0 and 1 compatible with standard 8051. • One 16-bit Timer2 with three-channel input capture module and 9 input pin can be selected. • One 16-bit auto-reload Timer3, which can be the baud rate clock source of UART0 and UART1.
Watchdog	• 6-bit free running up counter for WDT time-out interval. • Selectable time-out interval is 6.40 ms ~ 1.638s since WDT_CLK = 10 kHz (LIRC). • Able to wake up from Power-down or Idle mode • Interrupt or reset selectable on watchdog time-out
Wake-up Timer	• 16-bit free running up counter for time-out interval. • Clock sources from LIRC • Able self Wake-up wake up from Power-down or Idle mode, and auto reload count value. • Supports Interrupt
PWM	• Up To 5 channel output pins can be selected • Supports maximum clock source frequency up to 24 MHz • Supports independent mode for PWM output • Supports complementary mode for up to 2 complementary paired PWM output channels • Dead-time insertion with 8-bit resolution • Supports 16-bit resolution PWM counter • Supports mask function and tri-state enable for each PWM pin • Supports brake function • Supports trigger ADC on the following events
Analog Interfaces	
Analog-to-Digital Converter (ADC)	• Analog input voltage range: 0 ~ AV_{DD}. • 12-bit resolution and 10-bit accuracy is guaranteed. • Up to 7 single-end analog input channels • 1 internal channels, they are band-gap voltage (VBG). • Up to 500 ksps sampling rate. • Software Write 1 to ADCS bit. • External pin (STADC) trigger • PWM trigger.
Communication Interfaces	
UART	• Supports up to 2 UARTs: UART0 & UART1

	• Full-duplex asynchronous communications • Programmable 9th bit. • UART0_TXD and UART0_RXD pins exchangeable via software.
I²C	• 1 set of I²C devices • Master/Slave mode • Bidirectional data transfer between masters and slaves • Multi-master bus (no central master) • 7-bit addressing mode • Standard mode (100 kbps) and Fast mode (400 kbps). • Supports 8-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows • Supports hold time programmable
SPI	• 1 set of SPI devices • Supports Master or Slave mode operation • Supports MSB first or LSB first transfer sequence • slave mode up to 12 MHz
GPIO	• Four I/O modes: – Quasi-bidirectional mode – Push-Pull Output mode – Open-Drain Output mode – Input only with high impendence mode • Schmitt trigger input / TTL mode selectable. • Each I/O pin configured as interrupt source with edge/level trigger setting • Standard interrupt pins $\overline{INT0}$ and $\overline{INT1}$. • Supports high drive and high sink current I/O • I/O pin internal pull-up or pull-down resistor enabled in input mode. • Maximum I/O Speed is 24 MHz • Each GPIO enabling the pin interrupt function will also enable the wake-up function
ESD & EFT	
ESD	• HBM pass 8 kV
EFT	• > ± 4.4 kV
Latch-up	• 150 mA pass

3 PARTS INFORMATION

3.1 Package Type

	MSOP10	TSSOP14	TSSOP20	QFN20	TSSOP28	LQFP32	QFN33
Part No.	MS51BA9AE	MS51DA9AE	MS51FB9AE MS51FC0AE	MS51XB9AE MS51XB9BE MS51XC0BE	MS51EC0AE	MS51PC0AE	MS51TC0AE

3.2 MS51 Series Selection Guide

Part Number	Flash (KB)	SRAM (KB)	ISP ROM (KB) [1]	I/O	Timer/	PWM	Connectivity				ADC(12-Bit)	Package
							ISO 7816 -3 [2]	UART	SPI	I²C		
MS51BA9AE	8	1	4	8	4	5	-	2	-	1	5-ch	MSOP10
MS51DA9AE	8	1	4	12	4	5	-	2	1	1	7-ch	TSSOP14
MS51XB9AE	16	1	4	18	4	6	-	2	1	1	8-ch	QFN20 [3]
MS51XB9BE	16	1	4	18	4	6	-	2	1	1	8-ch	QFN20 [3]
MS51FB9AE	16	1	4	18	4	6	-	2	1	1	8-ch	TSSOP20
MS51FC0AE	32	2	4	18	4	8	2	2	1	1	10-ch	TSSOP20
MS51XC0BE	32	2	4	18	4	8	2	2	1	1	10-ch	QFN20
MS51EC0AE	32	2	4	26	4	10	3	2	1	1	15-ch	TSSOP28
MS51PC0AE	32	2	4	30	4	12	3	2	2	1	15-ch	LQFP32
MS51TC0AE	32	2	4	30	4	12	3	2	2	1	15-ch	QFN33

Note:

1. ISP ROM programmable 1K/2K/3K/4KB Flash for user program loader (LDROM) share from ARPOM.
2. ISO 7816-3 configurable as UART2.
3. Detailed package information please refer to Chapter 7
4. This TRM only for 8KB flash size part number product

Table 3.2-1 MS51 Series Selection Table

3.3 MS51 Series Selection Code

MS	51	F	B	9	A	E
Core	**Line**	**Package**	**Flash**	**SRAM**	**Reserve**	**Temperature**
1T 8051 Industry	51: Base	B: MSOP10 (3x3 mm) D: TSSOP14 (4.4x5.0 mm) E: TSSOP28 (4.4x9.7 mm) F: TSSOP20 (4.4x6.5 mm) I: SOP8 (4x5mm) O: SOP20 (300 mil) P: LQFP32 (7x7 mm) T: QFN33 (4x4 mm) U: SOP28 (300 mil) X: QFN20 (3x3mm)	A: 8 KB B: 16 KB C: 32 KB	0: 2 KB 1: 4 KB 2: 8/12 KB 3: 16 KB 6: 32 KB 8: 64 KB 9: 1 KB A: 96 KB		E:-40 ~ 105° C

Table 3.3-1 MS51 Series Selection Code

4 PIN CONFIGURATION

Users can find pin configuaration informations by using NuTool - PinConfigure. The NuTool - PinConfigure contains all Nuvoton NuMicro® Family chip series with all part number, and helps users configure GPIO multi-function correctly and handily.

4.1 MS51 8KB Series Multi Function Pin Diagram

4.1.1 TSSOP 14-pin Package Pin Diagram

Corresponding Part Number: MS51DA9AE

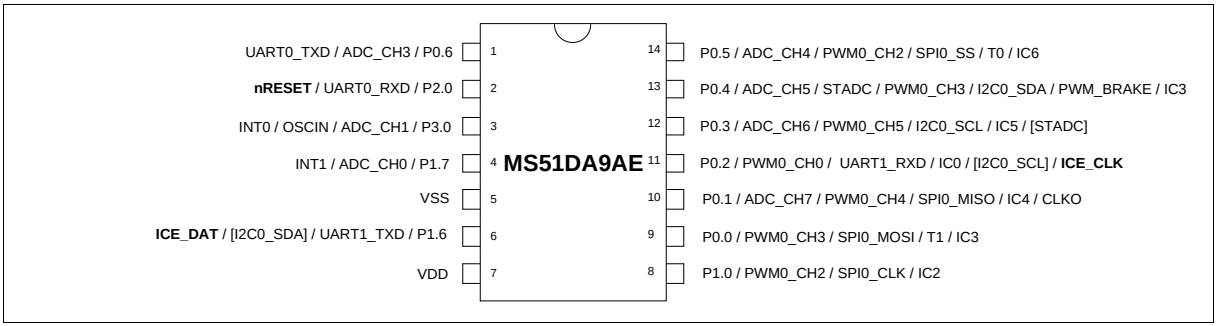


Figure 4.1-1 Pin Assignment of TSSOP-14 Package

4.1.2 MSOP 10-pin Package Pin Diagram

Corresponding Part Number: MS51BA9AE

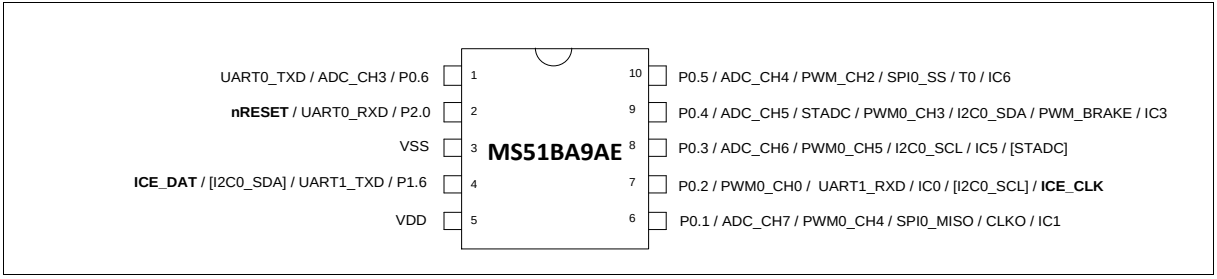


Figure 4.1-2 Pin Assignment of MSOP-10 Package

4.2 MS51 8KB Series Pin Description

Pin Number		Symbol	Multi-Function Description[1]
MS51DA9AE	MS51BA9AE		
7	5	**VDD**	Supply voltage VDD for operation.
5	3	**VSS**	Ground potential.
9	-	**P0.0**	Port 0 bit 0.
		PWM0_CH3	PWM output channel 3.
		SPI0_MOSI	SPI master output/slave input.
		IC3	Input capture channel 3.
		T1	External count input to Timer/Counter 1 or its toggle output.
10	6	**P0.1**	Port 0 bit 1.
		ADC_CH7	ADC input channel 7
		PWM0_CH4	PWM output channel 4.
		SPI0_MISO	SPI master input/slave output.
		IC4	Input capture channel 4.
		CLKO	Clock output
11	7	**P0.2**	Port 0 bit 2.
		ICE_CLK	ICP clock input.
		PWM0_CH0	PWM0 channel 0
		UART1_RXD[2]	Serial port 1 receive input.
		IC0	Input Capture channel 0
		[I2C0_SCL]	I^2C clock.
12	8	**P0.3**	Port 0 bit 3.
		ADC_CH6	ADC input channel 6
		PWM0_CH5	PWM output channel
		I2C0_SCL	I^2C0 clock pin
		IC5	Input capture channel 5.
		[STADC]	External start ADC trigger
13	9	**P0.4**	Port 0 bit 4.
		ADC_CH5	ADC input channel 5.
		PWM0_CH3	PWM output channel 3.
		PWM0_BRAKE	PWM0 Fault Brake input.
		I2C0_SDA	I^2C0 data pin
		IC3	Input capture channel 3.
		STADC	External start ADC trigger
14	10	**P0.5**	Port 0 bit 5.
		ADC_CH4	ADC input channel 4
		PWM0_CH2	PWM output channel 2.
		SPI0_SS	SPI0 slave select input.
		IC6	Input capture channel 6.
		T0	External count input to Timer/Counter 0 or its toggle output.
1	1	**P0.6**	Port 0 bit 6.
		ADC_CH3	ADC input channel 3.
		UART0_TXD	Serial port 0 transmit data output.
8	-	**P1.0**	Port 1 bit 0.
		PWM0_CH2	PWM output channel 2.
		SPI0_CLK	SPI clock.
		IC2	Input capture channel 2.
6	4	**P1.6**	Port 1 bit 6.
		ICE_DAT	ICP / ICE data input or output.
		UART1_TXD[2]	Serial port 1 transmit data output.

Pin Number		Symbol	Multi-Function Description[1]
MS51DA9AE	MS51BA9AE		
		[I2C0_SDA]	I2C data.
4	-	**P1.7**	Port 1 bit 7.
		ADC_CH0	ADC input channel 0.
		INT1	External interrupt 1 input.
2	2	**P2.0**	Port 2 bit 0 input pin available when RPD (CONFIG0.2) is programmed as 0.
		nRESET	nRESET pin is a Schmitt trigger input pin for hardware device reset. A low on this pin resets the device. nRESETpin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND.
		UART0_RXD	Serial port 0 receive input.
3	-	**P3.0**	Port 3 bit 0 available when the internal oscillator is used as the system clock.
		ADC_CH1	ADC input channel 1.
		INT0	External interrupt 0 input.
		OSCIN	If the ECLK mode is enabled, Xin is the external clock input pin.

Note:

1. All I/O pins can be configured as a interrupt pin. This feature is not listed in multi-function description.
2. UART0_TXD and UART0_RXD pins are software exchangeable by UART0PX (AUXR1.2).
3. [I2C] alternate function remapping option. I^2C pins is software switched by I2CPX (I2CON.0).
4. [STADC] alternate function remapping option. STADC pin is software switched by STADCPX(ADCCON1.6).
5. PIOx register decides which pins are PWM or GPIO.
6. UART1_TXD and UART1_RXD pins are software exchangeable by UART1PX (AUXR1.1).

Table 4.2-1 MS51 8KB Series Pin Description

5 BLOCK DIAGRAM

5.1 MS51 8KB Series BLOCK DIAGRAM

Figure 5.1-1 shows the MS51 functional block diagram and gives the outline of the device. User can find all the peripheral functions of the device in the diagram.

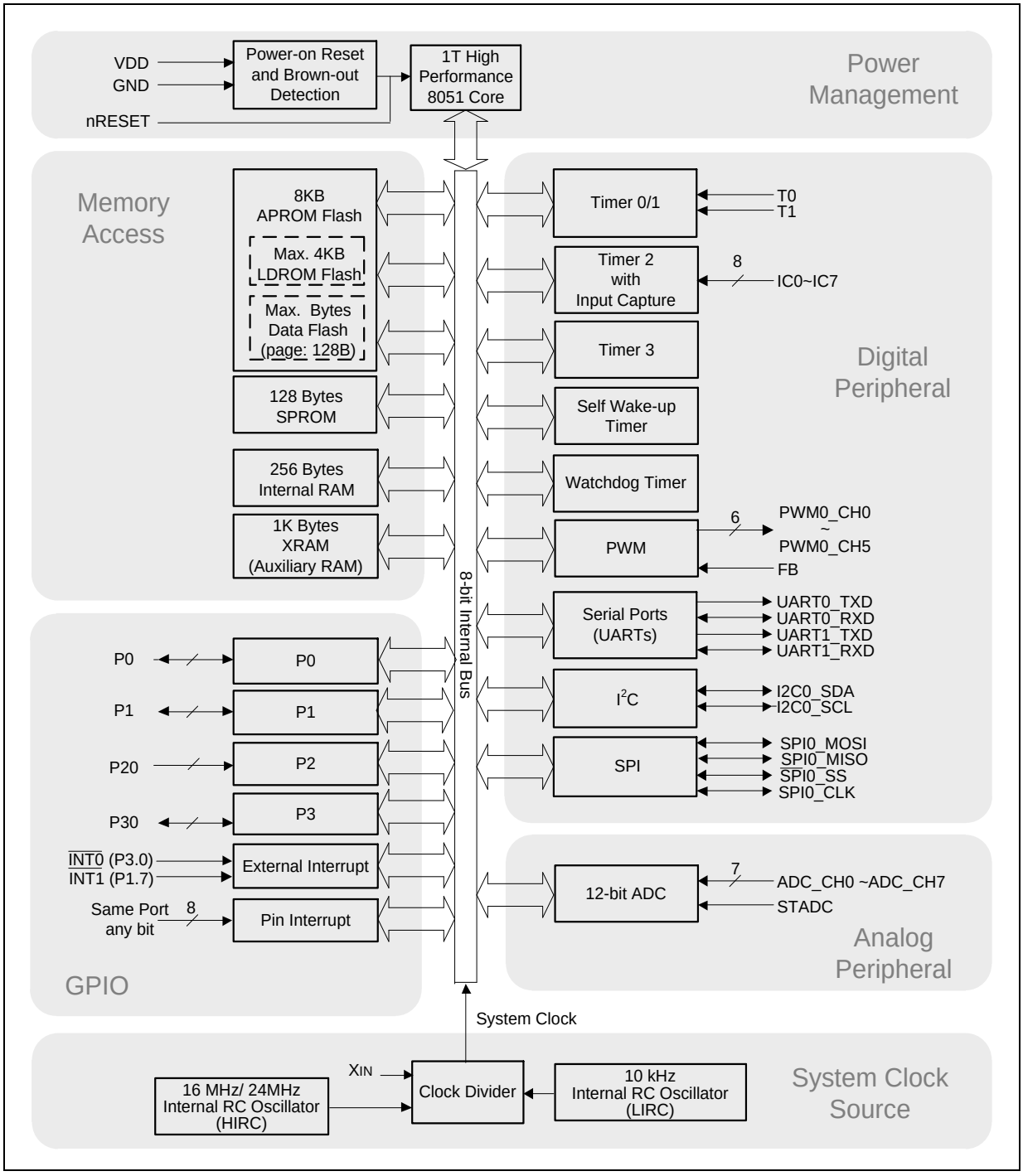


Figure 5.1-1 Functional Block Diagram

6 FUNCTION DESCRIPTION

6.1 Memory Organization

A standard 80C51 based microcontroller divides the memory into two different sections, Program Memory and Data Memory. The Program Memory is used to store the instruction codes, whereas the Data Memory is used to store data or variations during the program execution.

The Data Memory occupies a separate address space from Program Memory. In MS51, there are 256 Bytes of internal scratch-pad RAM. For many applications those need more internal RAM, the MS51 provides another on-chip 1K Bytes of RAM, which is called XRAM, accessed by MOVX instruction.

The whole embedded flash, functioning as Program Memory, is divided into three blocks: Application ROM (APROM) normally for User Code, Loader ROM (LDROM) normally for Boot Code, and CONFIG bytes for hardware initialization. Actually, APROM and LDROM function in the same way but have different size. Each block is accumulated page by page and the page size is 128 Bytes. The flash control unit supports Erase, Program, and Read modes. The external writer tools though specific I/O pins, In-Application-Programming (IAP), or In-System-Programming (ISP) can both perform these modes.

6.2 Config Bytes

The MS51 has several hardware configuration bytes, called CONFIG, those are used to configure the hardware options such as the security bits, system clock source, and so on. These hardware options can be re-configured through the parallel Writer, In-Circuit-Programming (ICP), or In-Application-Programming (IAP). Several functions, which are defined by certain CONFIG bits are also available to be re-configured by SFR. Therefore, there is a need to load such CONFIG bits into respective SFR bits. Such loading will occur after resets. These SFR bits can be continuously controlled via user's software.

CONFIG0

7	6	5	4	3	2	1	0
CBS	-	OCDPWM	OCDEN	-	RPD	LOCK	-
R/W	-	R/W	R/W	-	R/W	R/W	-

Factory default value: 1111 1111b

Bit	Name	Description
7	CBS	CONFIG boot select This bit defines from which block that MCU re-boots after resets except software reset. 1 = MCU will re-boot from APROM after resets except software reset. 0 = MCU will re-boot from LDROM after resets except software reset.
5	OCDPWM	PWM output state under OCD halt This bit decides the output state of PWM when OCD halts CPU. 1 = Tri-state pins those are used as PWM outputs. 0 = PWM continues. Note that this bit is valid only when the corresponding PIO bit of PWM channel is set as 1.
4	OCDEN	OCD enable 1 = OCD Disabled. 0 = OCD Enabled. **Note:** If MCU run in OCD debug mode and OCDEN = 0, hard fault reset will be disabled and only Hard F flag be asserted.
2	RPD	Reset pin disable 1 = The reset function of P2.0/Nrst pin Enabled. P2.0/Nrst functions as the external reset pin. 0 = The reset function of P2.0/Nrst pin Disabled. P2.0/Nrst functions as an input-only pin P2.0.
1	LOCK	Chip lock enable 1 = Chip is unlocked. Flash Memory is not locked. Their contents can be read out through a parallel Writer/ICP programmer. 0 = Chip is locked. Whole Flash Memory is locked. Their contents read through a parallel Writer or ICP programmer will be all blank (FFH). Programming to Flash Memory is invalid. Note that CONFIG bytes are always unlocked and can be read. Hence, once the chip is locked, the CONFIG bytes cannot be erased or programmed individually. The only way to disable chip lock is execute “whole chip erase”. However, all data within the Flash Memory and CONFIG bits will be erased when this procedure is executed. If the chip is locked, it does not alter the IAP function.

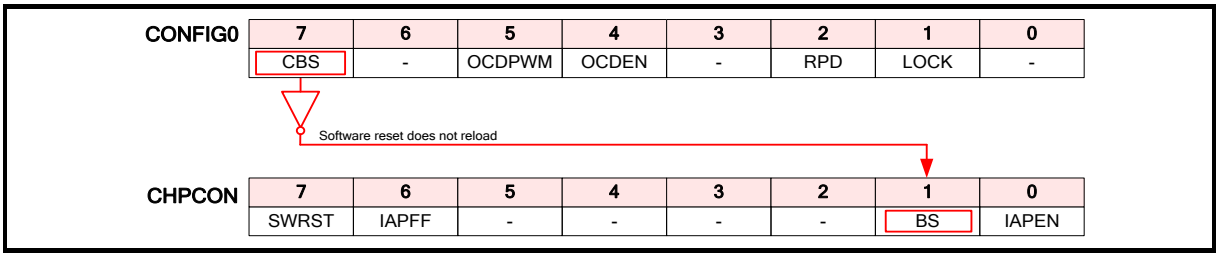


Figure 6.2-1 CONFIG0 Any Reset Reloading

CONFIG1

7	6	5	4	3	2	1	0
-	-	-	-	-	LDSIZE[2:0]		
-	-	-	-	-	R/W		

Factory default value: 1111 1111b

Bit	Name	Description
2:0	LDSIZE[2:0]	LDROM size select 111 = No LDROM. APROM is 16 Kbytes. 110 = LDROM is 1 Kbytes. APROM is 7 Kbytes. 101 = LDROM is 2 Kbytes. APROM is 6 Kbytes. 100 = LDROM is 3 Kbytes. APROM is 5 Kbytes. 0xx = LDROM is 4 Kbytes. APROM is 4 Kbytes.

CONFIG2

7	6	5	4	3	2	1	0
CBODEN	CBOV[2:0]			BOIAP	CBORST	-	-
R/W	R/W			R/W	R/W	-	-

Factory default value: 1111 1111b

Bit	Name	Description
7	CBODEN	CONFIG brown-out detect enable 1 = Brown-out detection circuit on. 0 = Brown-out detection circuit off.
5:4	CBOV[1:0]	CONFIG brown-out voltage select 11 = V_{BOD} is 2.2V. 10 = V_{BOD} is 2.7V. 01 = V_{BOD} is 3.7V. 00 = V_{BOD} is 4.4V.
3	BOIAP	Brown-out inhibiting IAP This bit decides whether IAP erasing or programming is inhibited by brown-out status. This bit is valid only when brown-out detection is enabled. 1 = IAP erasing or programming is inhibited if V_{DD} is lower than V_{BOD}. 0 = IAP erasing or programming is allowed under any workable V_{DD}.
2	CBORST	CONFIG brown-out reset enable This bit decides whether a brown-out reset is caused by a power drop below V_{BOD}. 1 = Brown-out reset Enabled. 0 = Brown-out reset Disabled.

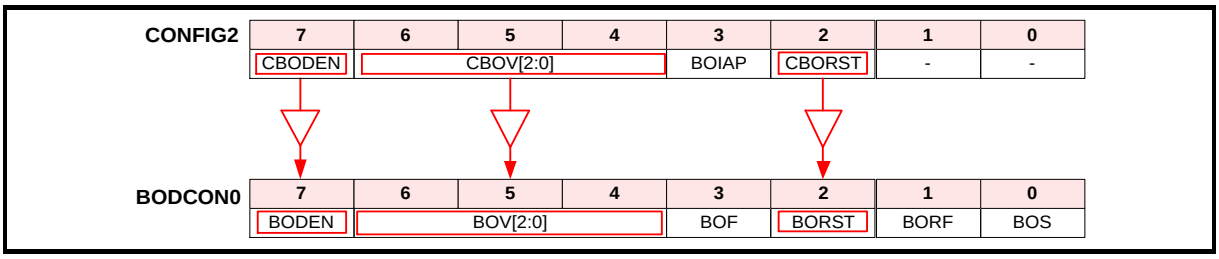


Figure 6.2-2 CONFIG2 Power-On Reset Reloading

CONFIG4

7	6	5	4	3	2	1	0
WDTEN[3:0]				-	-	-	-
R/W				-	-	-	-

Factory default value: 1111 1111b

Bit	Name	Description
7:4	WDTEN[3:0]	WDT enable This field configures the WDT behavior after MCU execution. 1111 = WDT is Disabled. WDT can be used as a general purpose timer via software control. 0101 = WDT is Enabled as a time-out reset timer and it stops running during Idle or Power-down mode. Others = WDT is Enabled as a time-out reset timer and it keeps running during Idle or Power-down mode.
3:0	-	Reserved

6.3 System Manager

6.3.1 Clock System

The MS51 has a wide variety of clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. The MS51 provides three options of the system clock sources including internal oscillator, or external clock from XIN pin via software. The MS51 is embedded with two internal oscillators: one 10 kHz low-speed and one 16 MHz high-speed, which is factory trimmed to ±2% under all conditions. A clock divider CKDIV is also available on MS51 for adjustment of the flexibility between power consumption and operating performance.

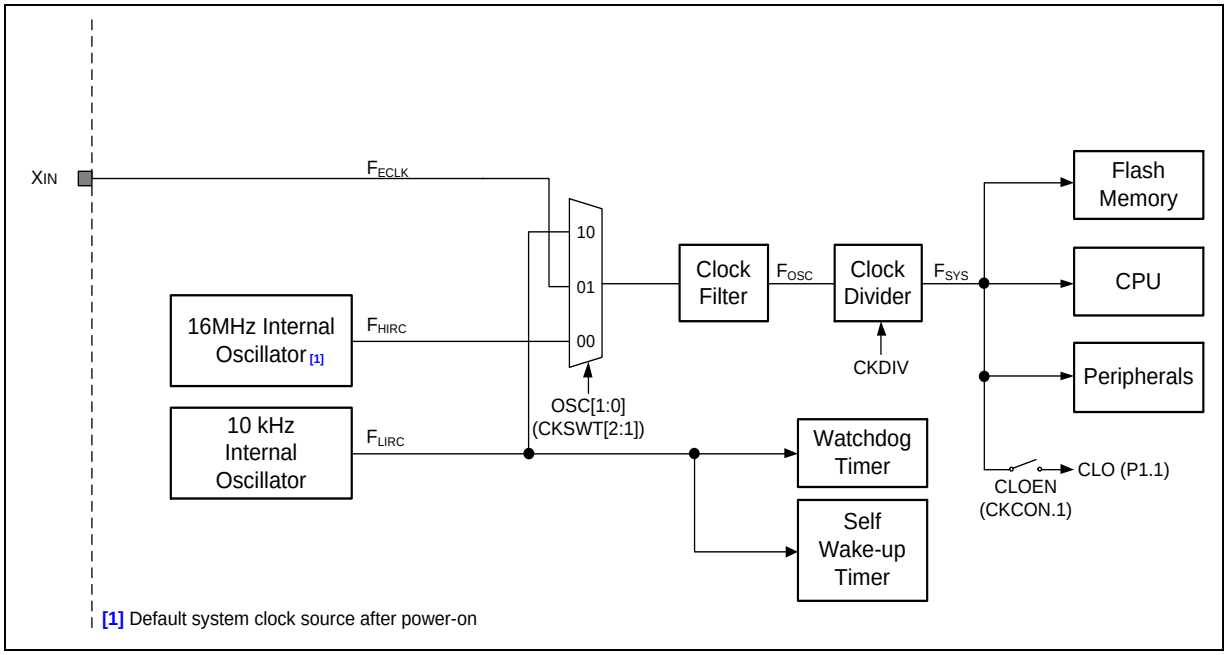


Figure 6.3-1 Clock System Block Diagram

6.4 Flash Memory Control

6.4.1 In-Application-Programming (IAP)

Unlike RAM's real-time operation, to update flash data often takes long time. Furthermore, it is a quite complex timing procedure to erase, program, or read flash data. The MS51 carried out the flash operation with convenient mechanism to help user re-programming the flash content by In-Application-Programming (IAP). IAP is an in-circuit electrical erasure and programming method through software.

After IAP enabling by setting IAPEN (CHPCON.0 with TA protected) and setting the enable bit in IAPUEN that allows the target block to be updated, user can easily fill the 16-bit target address in IAPAH and IAPAL, data in IAPFD, and command in IAPCN. Then the IAP is ready to begin by setting a triggering bit IAPGO (IAPTRG.0). Note that IAPTRG is also TA protected. At this moment, the CPU holds the Program Counter and the built-in IAP automation takes over to control the internal charge-pump for high voltage and the detail signal timing. The erase and program time is internally controlled disregard of the operating voltage and frequency. Nominally, a page-erase time is 5 ms and a byte-program time is 23.5 μs. After IAP action completed, the Program Counter continues to run the following instructions. The IAPGO bit will be automatically cleared. An IAP failure flag, IAPFF (CHPCON.6), can be check whether the previous IAP operation was successful or not. Through this progress, user can easily erase, program, and verify the Flash Memory by just taking care of pure software.

6.4.2 In-Circuit-Programming (ICP)

The Flash Memory can be programmed by "In-Circuit-Programming" (ICP). If the product is just under development or the end product needs firmware updating in the hand of an end customer, the hardware programming mode will make repeated programming difficult and inconvenient. ICP method makes it easy and possible without removing the microcontroller from the system. ICP mode also allows customers to manufacture circuit boards with un-programmed devices. Programming can be done after the assembly process allowing the device to be programmed with the most recent firmware or a customized firmware.

There are three signal pins, nRESET, ICPDA, and ICPCK, involved in ICP function. nRESET is used to enter or exit ICP mode. ICPDA is the data input and output pin. ICPCK is the clock input pin, which synchronizes the data shifted in to or out from MCU under programming. User should leave these three pins plus VDD and GND pins on the circuit board to make ICP possible.

Nuvoton provides ICP tool for MS51, which enables user to easily perform ICP through Nuvoton ICP programmer. The ICP programmer developed by Nuvoton has been optimized according to the electric characteristics of MCU. It also satisfies the stability and efficiency during production progress. For more details, please visit Nuvoton 8-bit Microcontroller website: Nuvoton 80C51 Microcontroller Technical Support.

6.4.3 On-Chip-Debugger (OCD)

The MS51 is embedded in an on-chip-debugger (OCD) providing developers with a low cost method for debugging user code, which is available on each package. The OCD gives debug capability of complete program flow control with eight hardware address breakpoints, single step, free running, and non-intrusive commands for memory access. The OCD system does not occupy any locations in the memory map and does not share any on-chip peripherals.

6.5 General Purpose I/O (GPIO)

6.5.1 GPIO Mode

The MS51 has a maximum of 43 general purpose I/O pins which 40 bit-addressable general I/O pins grouped as 5 ports, P0 to P4, and 7 general I/O pins grouped as P5. Each port has its port control register (Px register). The writing and reading of a port control register have different meanings. A write to port control register sets the port output latch logic value, whereas a read gets the port pin logic state. These four modes are quasi-bidirectional (standard 8051 port structure), push-pull, input-only, and open-drain modes. Each port spends two special function registers PxM1 and PxM2 to select the I/O mode of port Px. The list below illustrates how to select the I/O mode of Px.n. Note that the default configuration of is input-only (high-impedance) after any reset.

PnM1.X[1]	PnM2.X[1]	I/O Type
0	0	Quasi-bidirectional
0	1	Push-pull
1	0	Input-only (high-impedance)
1	1	Open-drain
NOTE1: N = 0~5, x = 0~7		

Table 6.5-1 Configuration for Different I/O Modes

All I/O pins can be selected as TTL level inputs or Schmitt triggered inputs by selecting corresponding bit in PxS register. Schmitt triggered input has better glitch suppression capability. All I/O pins also have bit-controllable, slew rate select ability via software. The control registers are PxSR. By default, the slew rate is slow. If user would like to increase the I/O output speed, setting the corresponding bit in PxSR, the slew rate is selected in a faster level.

For example:

```
    P0M1 |= 0x40;
    P0M2 &= 0xBF;           //Set P0.6 as input only mode
```

6.6 Timer

6.6.1 Timer/Counter 0 And 1

Timer/Counter 0 and 1 on MS51 are two 16-bit Timers/Counters. Each of them has two 8-bit registers those form the 16-bit counting register. For Timer/Counter 0 they are TH0, the upper 8-bit register, and TL0, the lower 8-bit register. Similarly Timer/Counter 1 has two 8-bit registers, TH1 and TL1. TCON and TMOD can configure modes of Timer/Counter 0 and 1.

The Timer or Counter function is selected by the C/$\overline{T}$ bit in TMOD. Each Timer/Counter has its own selection bit. TMOD.2 selects the function for Timer/Counter 0 and TMOD.6 selects the function for Timer/Counter 1

When configured as a “Timer”, the timer counts the system clock cycles. The timer clock is 1/12 of the system clock (F_{SYS}) for standard 8051 capability or direct the system clock for enhancement, which is selected by T0M (CKCON.3) bit for Timer 0 and T1M (CKCON.4) bit for Timer 1. In the “Counter” mode, the countering register increases on the falling edge of the external input pin T0. If the sampled value is high in one clock cycle and low in the next, a valid 1-to-0 transition is recognized on T0 or T1 pin.

The Timers 0 and 1 can be configured to automatically to toggle output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. This function is enabled by control bits T0OE and T1OE in the CKCON register, and apply to Timer 0 and Timer 1 respectively. The port outputs will be logic 1 prior to the first timer overflow when this mode is turned on. In order for this mode to function, the C/$\overline{T}$ bit should be cleared selecting the system clock as the clock source for the timer.

Note that the TH0 (TH1) and TL0 (TL1) are accessed separately. It is strongly recommended that in mode 0 or 1, user should stop Timer temporally by clearing TR0 (TR1) bit before reading from or writing to TH0 (TH1) and TL0 (TL1). The free-running reading or writing may cause unpredictable result.

6.6.2 Timer2 and Input Capture

Timer 2 is a 16-bit up counter cascaded with TH2, the upper 8 bits register, and TL2, the lower 8 bit register. Equipped with RCMP2H and RCMP2L, Timer 2 can operate under compare mode and auto-reload mode selected by CM/$\overline{RL2}$ (T2CON.0). An 3-channel input capture module makes Timer 2 detect and measure the width or period of input pulses. The results of 3 input captures are stores in C0H and C0L, C1H and C1L, C2H and C2L individually. The clock source of Timer 2 is from the system clock pre-scaled by a clock divider with 8 different scales for wide field application. The clock is enabled when TR2 (T2CON.2) is 1, and disabled when TR2 is 0. The following registers are related to Timer 2 function.

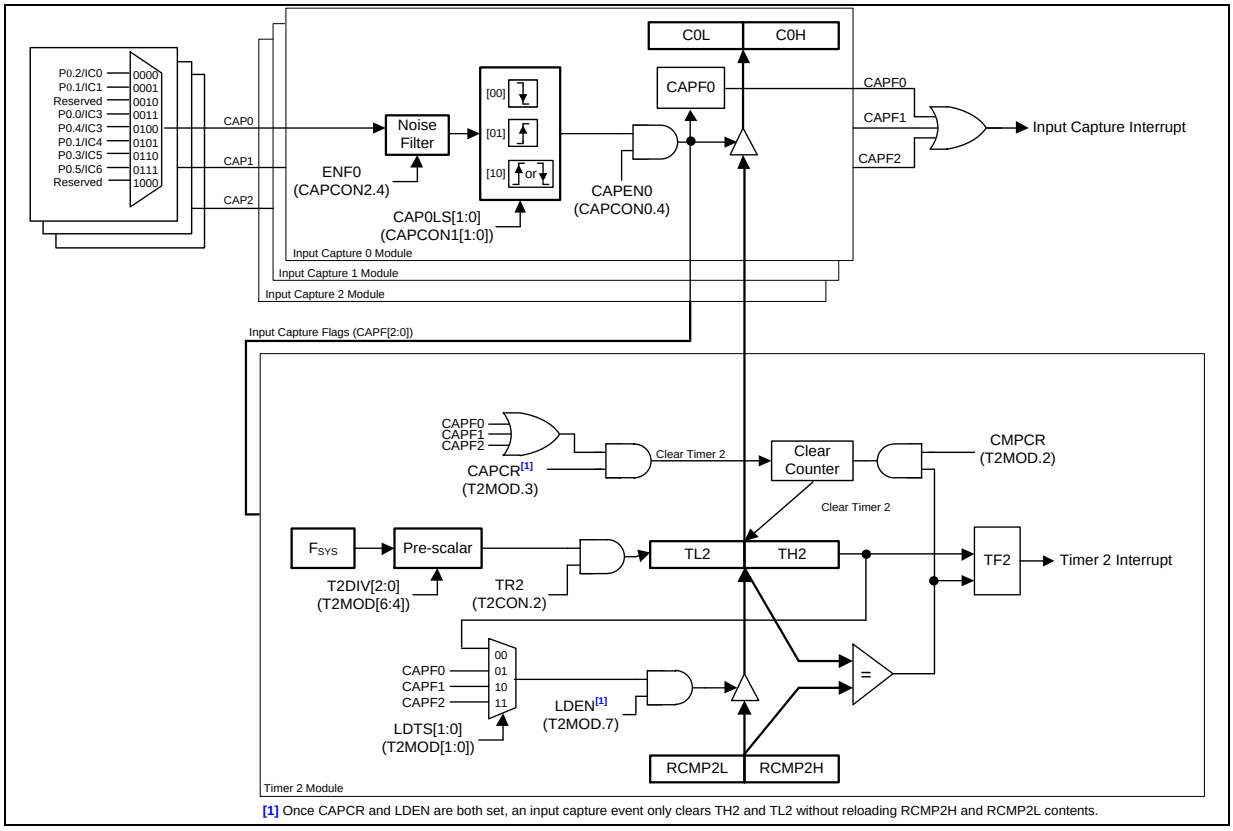


Figure 6.6-1 Timer 2 Full Function Block Diagram

6.6.3 Timer3

Timer 3 is implemented simply as a 16-bit auto-reload, up-counting timer. The user can select the pre-scale with T3PS[2:0] (T3CON[2:0]) and fill the reload value into RH3 and RL3 registers to determine its overflow rate. User then can set TR3 (T3CON.3) to start counting. When the counter rolls over FFFFH, TF3 (T3CON.4) is set as 1 and a reload is generated and causes the contents of the RH3 and RL3 registers to be reloaded into the internal 16-bit counter. If ET3 (EIE1.1) is set as 1, Timer 3 interrupt service routine will be served. TF3 is auto-cleared by hardware after entering its interrupt service routine.

Timer 3 can also be the baud rate clock source of both UARTs. For details, please see Section 錯誤! 找不到參照來源。"錯誤! 找不到參照來源。".

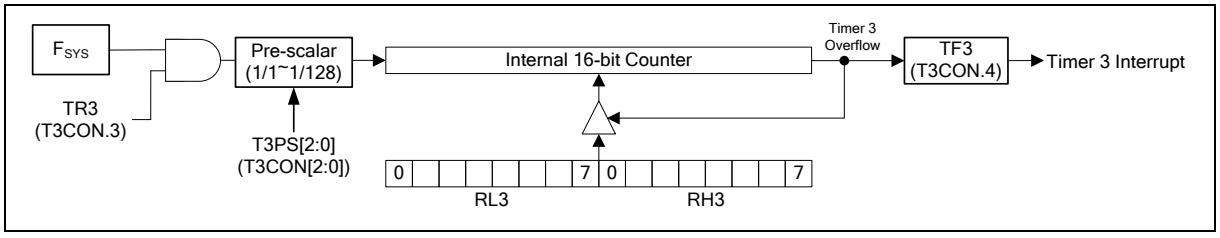


Figure 6.6-2 Timer 3 Block Diagram

6.7 Watchdog Timer (WDT)

The MS51 provides one Watchdog Timer (WDT). It can be configured as a time-out reset timer to reset whole device. Once the device runs in an abnormal status or hangs up by outward interference, a WDT reset recover the system. It provides a system monitor, which improves the reliability of the system. Therefore, WDT is especially useful for system that is susceptible to noise, power glitches, or electrostatic discharge. The WDT also can be configured as a general purpose timer, of which the periodic interrupt serves as an event timer or a durational system supervisor in a monitoring system, which is able to operate during Idle or Power-down mode. WDTEN[3:0] (CONFIG4[7:4]) initialize the WDT to operate as a time-out reset timer or a general purpose timer.

The WDT is implemented with a set of divider that divides the low-speed internal oscillator clock nominal 10kHz. The divider output is selectable and determines the time-out interval. When the time-out interval is fulfilled, it will wake the system up from Idle or Power-down mode and an interrupt event will occur if WDT interrupt is enabled. If WDT is initialized as a time-out reset timer, a system reset will occur after a period of delay if without any software action.

The Watchdog time-out interval is determined by the formula $\frac{1}{F_{LIRC} \times clock\,divider\,scalar} \times 64$, where F_{LIRC} is the frequency of internal 10 kHz oscillator. The following table shows an example of the Watchdog time-out interval with different pre-scales.

WDPS.2	WDPS.1	WDPS.0	Clock Divider Scale	WDT Time-Out Timing[1]
0	0	0	1/1	6.40 ms
0	0	1	1/4	25.60 ms
0	1	0	1/8	51.20 ms
0	1	1	1/16	102.40 ms
1	0	0	1/32	204.80 ms
1	0	1	1/64	409.60 ms
1	1	0	1/128	819.20 ms
1	1	1	1/256	1.638 s
Note: This is an approximate value since the deviation of LIRC.				

Table 6.7-1 Watchdog Timer-out Interval Under Different Pre-scalars

Since the limitation of the maxima vaule of WDT timer delay. To up MS51 from idle mode or power down mode suggest use WKT function see Chapter 6.8 Self Wake-Up Timer (WKT).

6.8 Self Wake-Up Timer (WKT)

The MS51 has a dedicated Self Wake-up Timer (WKT), which serves for a periodic wake-up timer in low power mode or for general purpose timer. WKT remains counting in Idle or Power-down mode. When WKT is being used as a wake-up timer, a start of WKT can occur just prior to entering a power management mode. WKT has one clock source, internal 10 kHz. Note that the system clock frequency must be twice over WKT clock. If WKT starts counting, the selected clock source will remain active once the device enters Idle or Power-down mode. Note that the selected clock source of WKT will not automatically enabled along with WKT configuration. User should manually enable the selected clock source and waiting for stability to ensure a proper operation.

The WKT is implemented simply as a 8-bit auto-reload, up-counting timer with pre-scale 1/1 to 1/2048 selected by WKPS[2:0] (WKCON[2:0]). User fills the reload value into RWK register to determine its overflow rate. The WKTR (WKCON.3) can be set to start counting. When the counter rolls over FFH, WKTF (WKCON.4) is set as 1 and a reload is generated and causes the contents of the RWK register to be reloaded into the internal 8-bit counter. If EWKT (EIE1.2) is set as 1, WKT interrupt service routine will be served.

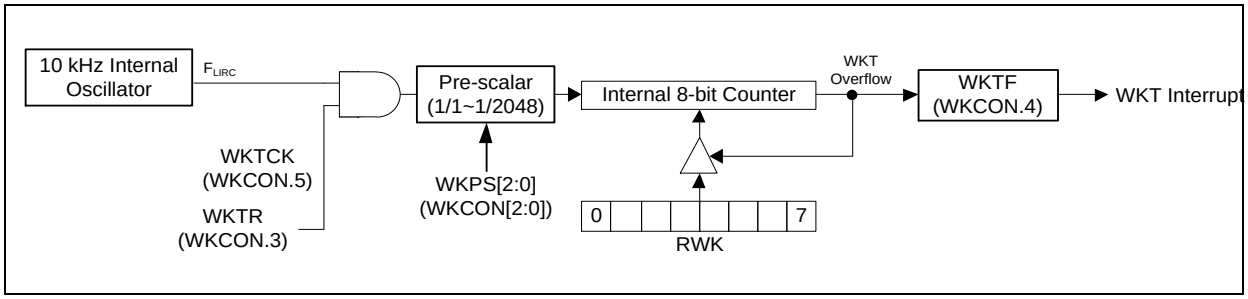


Figure 6.8-1 Self Wake-Up Timer Block Diagram

6.9 Pulse Width Modulated (PWM)

The PWM (Pulse Width Modulation) signal is a useful control solution in wide application field. It can used on motor driving, fan control, backlight brightness tuning, LED light dimming, or simulating as a simple digital to analog converter output through a low pass filter circuit.

The MS51 PWM is especially designed for motor control by providing three pairs, maximum 16-bit resolution of PWM output with programmable period and duty. The architecture makes user easy to drive the one-phase or three-phase brushless DC motor (BLDC), or three-phase AC induction motor. Each of six PWM can be configured as one of independent mode, complementary mode, or synchronous mode. If the complementary mode is used, a programmable dead-time insertion is available to protect MOS turn-on simultaneously. The PWM waveform can be edge-aligned or center-aligned with variable interrupt points.

6.10 Serial Port (UART0 & UART1)

The MS51 includes two enhanced full duplex serial ports enhanced with automatic address recognition and framing error detection. As control bits of these two serial ports are implemented the same. Generally speaking, in the following contents, there will not be any reference to serial port 1, but only to serial port 0.

Each serial port supports one synchronous communication mode, Mode 0, and three modes of full duplex UART (Universal Asynchronous Receiver and Transmitter), Mode 1, 2, and 3. This means it can transmit and receive simultaneously. The serial port is also receiving-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the register. The receiving and transmitting registers are both accessed at SBUF. Writing to SBUF loads the transmitting register, and reading SBUF accesses a physically separate receiving register. There are four operation modes in serial port. In all four modes, transmission initiates by any instruction that uses SBUF as a destination register.

6.11 Inter-Integrated Circuit (I^2C)

The MS51 provides two Inter-Integrated Circuit (I^2C) bus to serves as an serial interface between the microcontrollers and the I^2C devices such as EEPROM, LCD module, temperature sensor, and so on. The I^2C bus used two wires design (a serial data line I2C0_SDA and a serial clock line I2C0_SCL) to transfer information between devices.

The I^2C bus uses bi-directional data transfer between masters and slaves. There is no central master and the multi-master system is allowed by arbitration between simultaneously transmitting masters. The serial clock synchronization allows devices with different bit rates to communicate via one serial bus. The I^2C bus supports four transfer modes including master transmitter, master receiver, slave receiver, and slave transmitter. The I^2C interface only supports 7-bit addressing mode. A special mode General Call is also available. The I^2C can meet both standard (up to 100kbps) and fast (up to 400k bps) speeds.

For a bi-directional transfer operation, the I2C0_SDA and I2C0_SCL pins should be open-drain pads. This implements a wired-AND function, which is essential to the operation of the interface. A low level on a I^2C bus line is generated when one or more I^2C devices output a “0”. A high level is generated when all I^2C devices output “1”, allowing the pull-up resistors to pull the line high. In MS51, user should set output latches of I2C0_SCL and I2C0_SDA. As logic 1 before enabling the I^2C function by setting I2CEN.

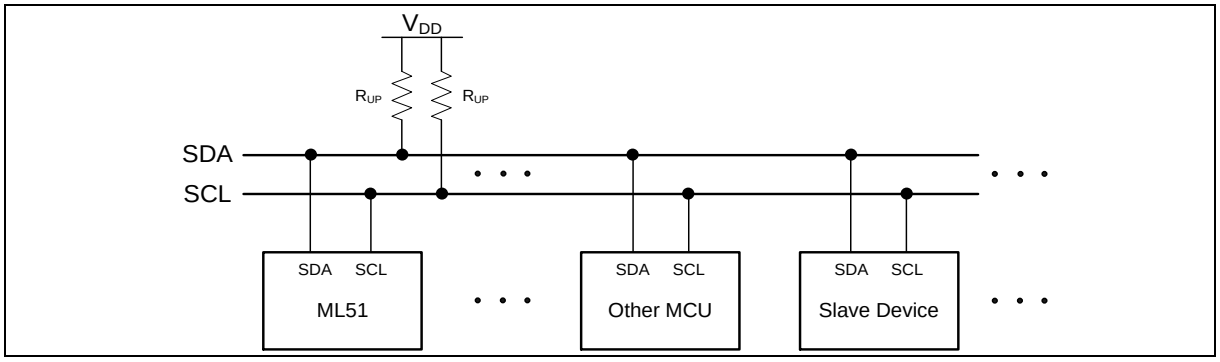


Figure 6.11-1 I^2C Bus Interconnection

The I^2C is considered free when both lines are high. Meanwhile, any device, which can operate as a master can occupy the bus and generate one transfer after generating a START condition. The bus now is considered busy before the transfer ends by sending a STOP condition. The master generates all of the serial clock pulses and the START and STOP condition. However if there is no START condition on the bus, all devices serve as not addressed slave. The hardware looks for its own slave address or a General Call address. (The General Call address detection may be enabled or disabled by GC (I2CnADDRx.0).) If the matched address is received, an interrupt is requested.

Every transaction on the I^2C bus is 9 bits long, consisting of 8 data bits (MSB first) and a single acknowledge bit. The number of bytes per transfer (defined as the time between a valid START and STOP condition) is unrestricted but each byte has to be followed by an acknowledge bit. The master device generates 8 clock pulse to send the 8-bit data. After the 8^{th} falling edge of the I2C0_SCL line, the device outputting data on the I2C0_SDA changes that pin to an input and reads in an acknowledge value on the 9^{th} clock pulse. After 9^{th} clock pulse, the data receiving device can hold I2C0_SCL line stretched low if next receiving is not prepared ready. It forces the next byte transaction suspended. The data transaction continues when the receiver releases the I2C0_SCL line.

6.12 Serial Peripheral Interface (SPI)

The MS51 provides two Serial Peripheral Interface (SPI) block to support high-speed serial communication. SPI is a full-duplex, high-speed, synchronous communication bus between microcontrollers or other peripheral devices such as serial EEPROM, LCD driver, or D/A converter. It provides either Master or Slave mode, high-speed rate up to $F_{SYS}/4$, transfer complete and write collision flag. For a multi-master system, SPI supports Master Mode Fault to protect a multi-master conflict.

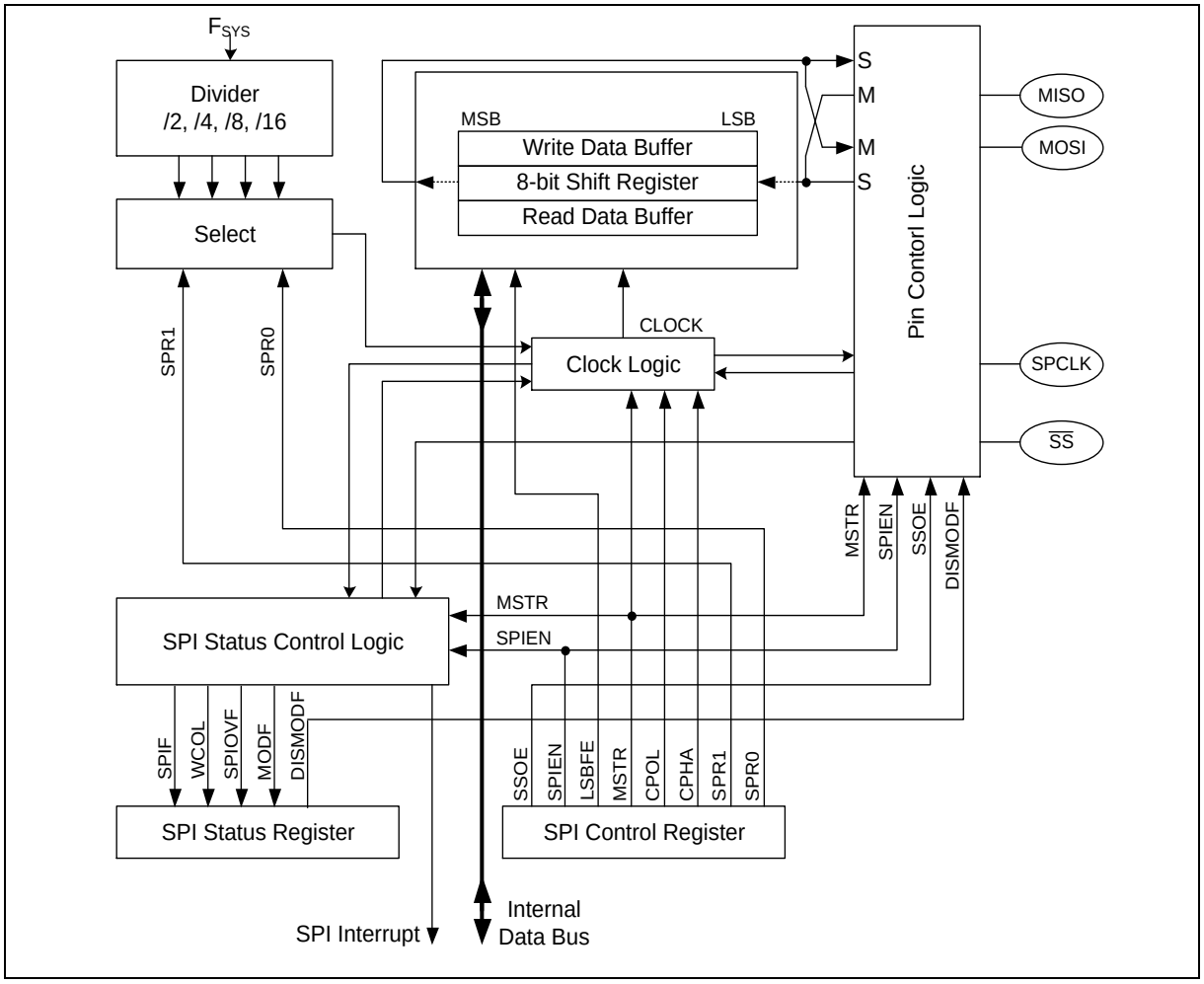


Figure 6.12-1 SPI Block Diagram

6.13 12-Bit Analog-To-Digital Converter (ADC)

The MS51 is embedded with a 12-bit SAR ADC. The ADC (analog-to-digital converter) allows conversion of an analog input signal to a 12-bit binary representation of that signal. The MS51 is selected as 8-channel inputs in single end mode. The internal band-gap voltage also can be the internal ADC input. The analog input, multiplexed into one sample and hold circuit, charges a sample and hold capacitor. The output of the sample and hold capacitor is the input into the converter. The converter then generates a digital result of this analog level via successive approximation and stores the result in the result registers. The ADC controller also supports DMA (direct memory access) function for ADC continuous conversion and storage result data into XRAM no need special enable PDMA module.

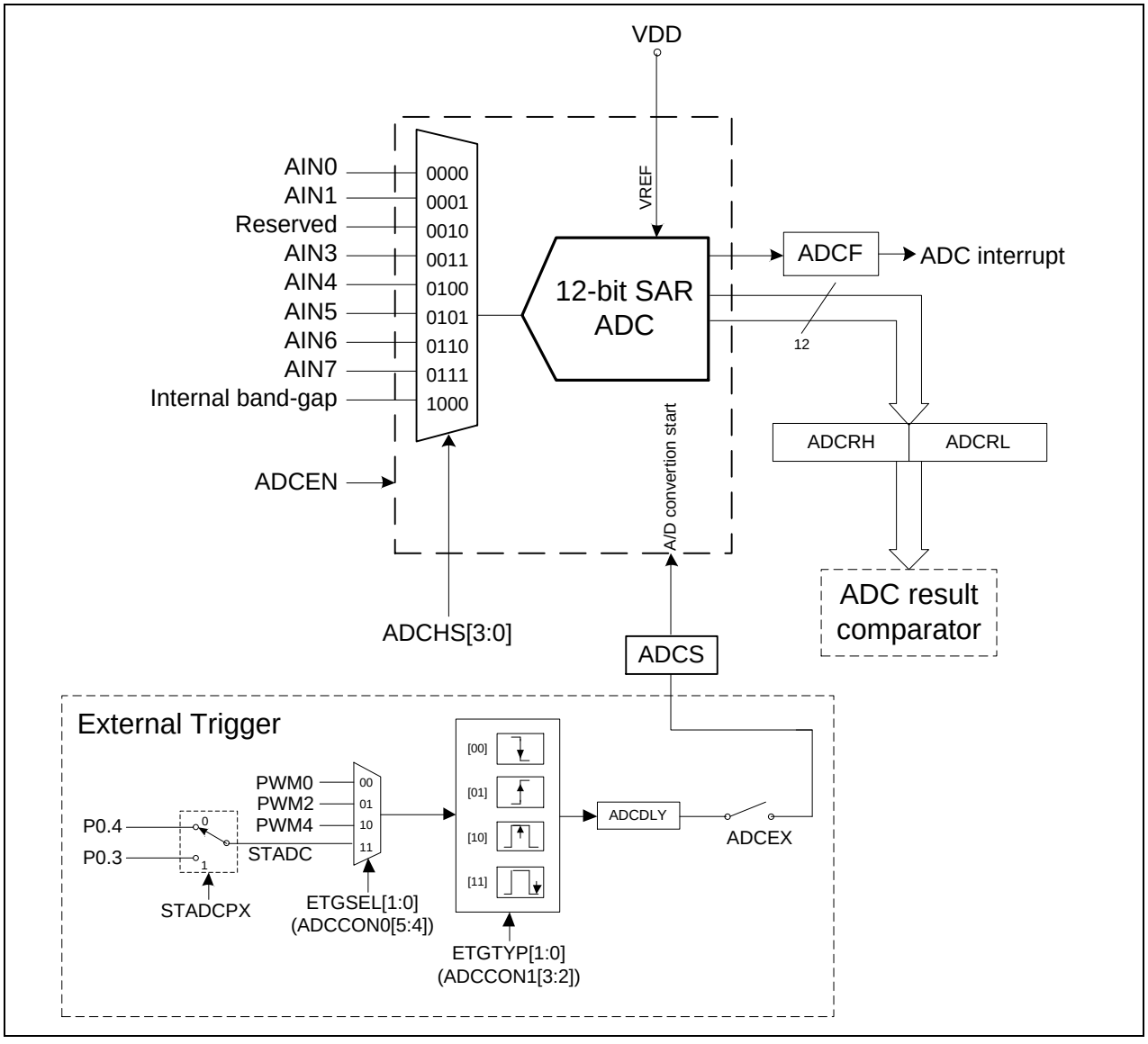


Figure 6.13-112-bit ADC Block Diagram

7 APPLICATION CIRCUIT

7.1 Power Supply Scheme

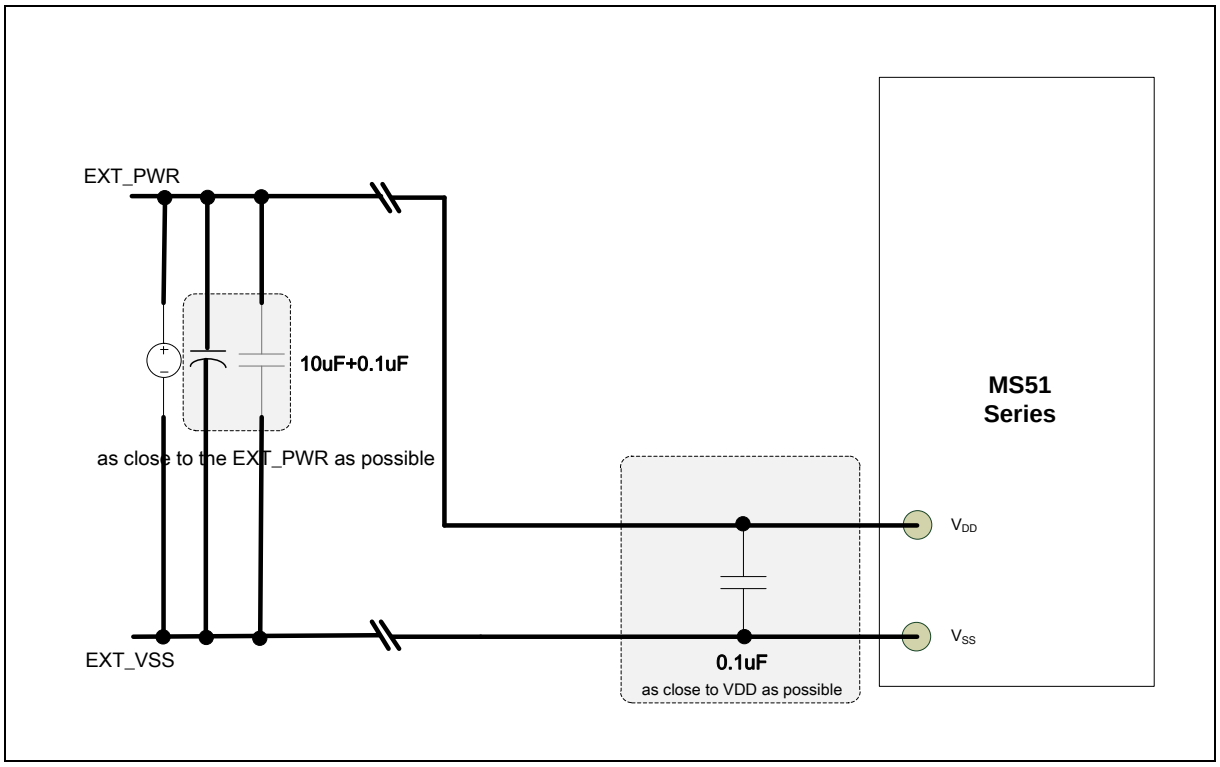


Figure 7.1-1 Numara® MS51 Power Supply Circuit

7.2 Peripheral Application Scheme

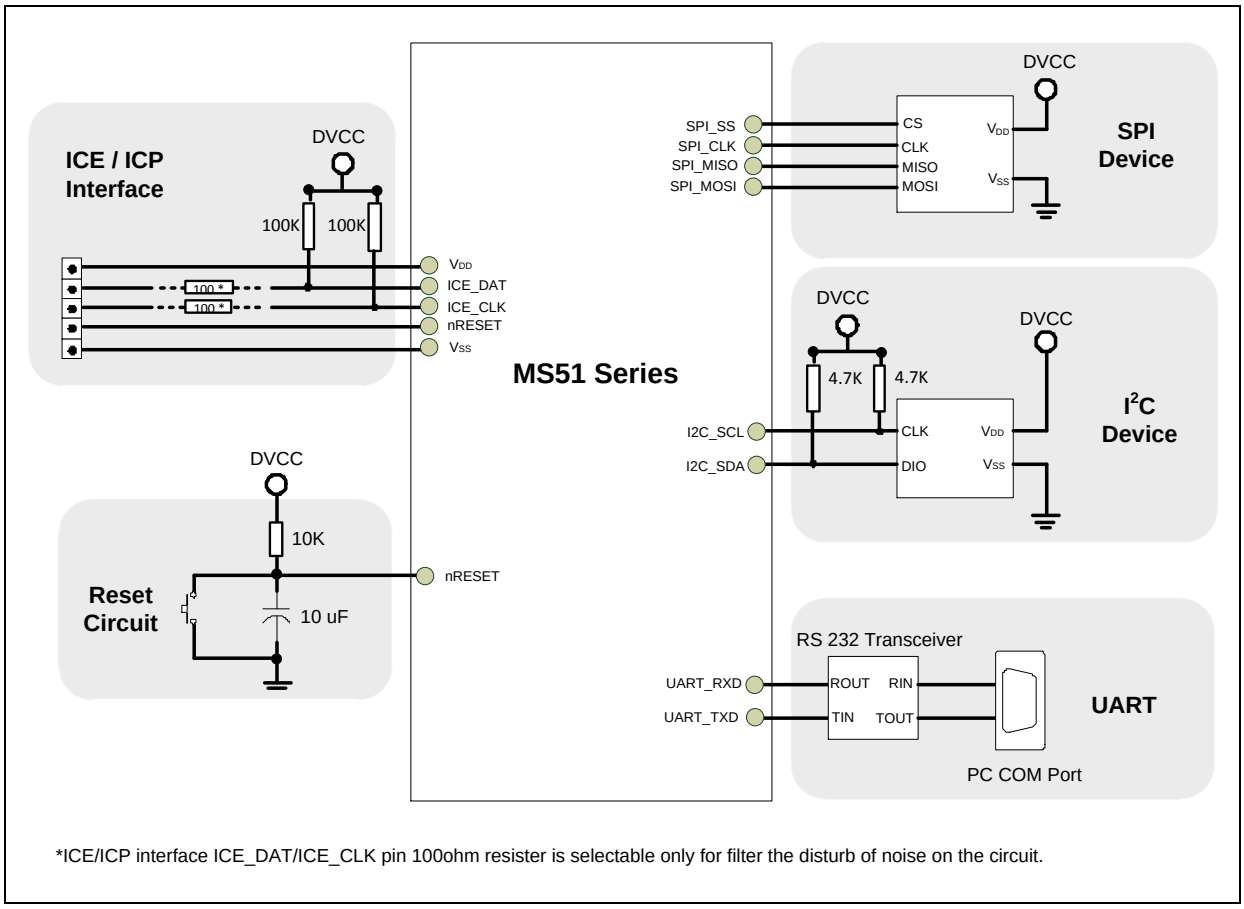


Figure 7.2-1 NuMicro® MS51 Peripheral Interface Circuit

8 ELECTRICAL CHARACTERISTICS

8.1 General Operating Conditions

(V_{DD}-V_{SS} = 2.4 ~ 5.5V, T_A = 25°C, Fsys = 16 MHz unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
V_{DD}	Operation voltage	2.4	-	5.5	V	
AV_{DD}[*1]	Analog operation voltage	V_{DD}				
V_{BG}	Band-gap voltage[2]	1.17	1.22	1.30		T_A = 25 °C
		1.14		1.33		T_A = -40°C ~105 °C,

Note:

1. It is recommended to power V_{DD} and AV_{DD} from the same source. A maximum difference of 0.3V between V_{DD} and AV_{DD} can be tolerated during power-on and power-off operation .
2. Based on characterization, tested in production.

Table 8.1-1 General operating conditions

8.2 DC Electrical Characteristics

8.2.1 Supply Current Characteristics

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in below condition and table to inform test characterization result.

- All GPIO pins are in push pull mode and output high.
- The maximum values are obtained for V_{DD} = 2.4V ~ 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.
- $V_{DD} = AV_{DD}$
- When the peripherals clock base is the system clock Fsys.
- Program run “while (1);” in Flash.

Symbol	Conditions	Fsys	Typ [6]	Max[6][7]			Unit
			T_A = 25 °C	T_A = -40 °C	T_A = 25 °C	T_A = 105 °C	
I_{DD_RUN}	Normal run mode, executed from Flash, all peripherals disable	24 MHz(HIRC)[1] @5.5V	3.6	4.2	4.6	4.8	mA
		24 MHz(HIRC)[1] @3.3V	3.2				
		24 MHz(HIRC)[1] @2.4V	2.9				
		16 MHz (HIRC) [1] @5.5V	3.3	3.4	3.9	4.6	
		16 MHz (HIRC) [1] @3.3V	3.1				
		16 MHz (HIRC) [1] @2.4V	2.8				
		10 kHz (LIRC)[2]	0.30	0.32	0.46	2.33	

Notes:

1. This value base on HIRC enable, LIRC enable
2. This value base on HIRC disable, LIRC enable
3. LVR17 enabled, POR enable and BOD enable.
4. Based on characterization, not tested in production unless otherwise specified.

Table 8.2-1 Current Consumption In Normal Run Mode

Symbol	Conditions	Fsys	Typ [3]	Max[3][4]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_IDLE}	Idle mode, executed from Flash, all peripherals disable	24 MHz(HIRC)[1] @5.5V	2.8	2.9	3.2	3.8	mA
		24 MHz(HIRC)[1] @3.3V	2.4				
		24 MHz(HIRC)[1] @2.4V	2.2				
		16 MHz (HIRC)[1] @5.5V	2.2	2.5	2.6	3.2	
		16 MHz (HIRC)[1] @3.3V	1.9				
		16 MHz (HIRC)[1] @2.4V	1.8				
		10 kHz (LIRC)[2]	0.3	0.5	0.9	2.3	

Notes:
1. This value base on HIRC enable, LIRC enable
2. This value base on HIRC disable, LIRC enable
3. LVR17 enabled, POR enable and BOD enable.
4. Based on characterization, not tested in production unless otherwise specified.

Table 8.2-2 Current Consumption In Idle Mode

Symbol	Test Conditions	Typ[1]	Max[2]			Unit
		T_A = 25 °C	T_A = -40 °C	T_A = 25 °C	T_A = 105 °C	
I_{DD_PD}	Power down mode, all peripherals disable@5.5V	6.5	6.2	9	55	µA
	Power down mode, all peripherals disable@3.3V	6				
	Power down mode, all peripherals disable@2.4V	5.8				
	Power down mode, LVR enable all other peripherals disable	7.5	6.7	10[3]	57	
	Power down mode, LVR enable BOD enable all other peripherals disable	180	165	197	292	

Notes:
1. AV_{DD} = V_{DD} = 3.3V unless otherwise specified, LVR17 disabled, POR disabled and BOD disabled.
2. Based on characterization, not tested in production unless otherwise specified.
3. Based on characterization, tested in production.

Table 8.2-3 Chip Current Consumption In Power Down Mode

8.2.2 Wakeup Time from Low-Power Modes

Symbol	Parameter		Typ	Max	Unit
t_{WU_IDLE}[1]	Wakeup from IDLE mode		5	6	cycles
t_{WU_NPD}[2][3]	Wakeup from Power down mode	Fsys = HIRC @16MHz	-	30	µs
		Fsys = HIRC @ 24MHz		30	µs

Notes:

1. Measured on a wakeup phase with a 16 MHz HIRC oscillator.
2. Based on test during characterization, not tested in production.
3. The wakeup times are measured from the wakeup event to the point in which the application code reads the first.

Table 8.2-4 Low-Power Mode Wakeup Timings

8.2.3 I/O DC Characteristics

8.2.3.1 PIN Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input low voltage (I/O with TTL input)	V_{SS}-0.3	-	0.2V_{DD}-0.1	V	
V_{IL1}	Input low voltage	0	-	0.3*V_{DD}	V	
V_{IH}	Input high voltage	0.2V_{DD}+0.9	-	V_{DD}+0.3	V	
V_{IH1}	Input high voltage (I/O with Schmitt trigger input and Xin)	0.7*V_{DD}	-	V_{DD}	V	
V_{HY}[*1]	Hysteresis voltage of schmitt input	-	0.2*V_{DD}	-	V	
I_{LK}[*2]	Input leakage current	-1		1	µA	V_{SS} < V_{IN} < V_{DD}, Open-drain or input only mode
		-1		1		V_{DD} < V_{IN} < 5.5 V, Open-drain or input only mode

Notes:

1. Guaranteed by characterization result, not tested in production.
2. Leakage could be higher than the maximum value, if abnormal injection happens.
3. To sustain a voltage higher than V_{DD} +0.3 V, the internal pull-up resistors must be disabled. Leakage could be higher than the maximum value, if positive current is injected on adjacent pins

Table 8.2-5 I/O Input Characteristics

8.2.3.2 I/O Output Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{SR}[1] [2]	Source current for quasi-bidirectional mode and high level	-7.4	-	-7.5	μA	V_{DD} = 5.5 V V_{IN} =(V_{DD}-0.4) V
		-7.3	-	-7.5	μA	V_{DD} = 3.3 V V_{IN} =(V_{DD}-0.4) V
		-7.3	-	-7.5	μA	V_{DD} = 2.4 V V_{IN} =(V_{DD}-0.4) V
		-57.2	-	-58.3	μA	V_{DD} = 5.5 V V_{IN} = 2.4 V
	Source current for push-pull mode and high level	-9	-	-9.6	mA	V_{DD} = 5.5 V V_{IN} =(V_{DD}-0.4) V
		-6	-	-6.6	mA	V_{DD} = 3.3 V V_{IN} =(V_{DD}-0.4) V
		-4.2	-	-4.9	mA	V_{DD} = 2.7 V V_{IN} =(V_{DD}-0.4) V
		-18	-	-20	mA	V_{DD} = 5.5 V V_{IN} = 2.4 V
I_{SK}[1] [2]	Sink current for push-pull mode and low level	18	-	20	mA	V_{DD} = 5.5 V V_{IN} = 0.4 V
		16	-	18	mA	V_{DD} = 3.3 V V_{IN} = 0.4 V
		9.7	-	11	mA	V_{DD} = 2.4 V V_{IN} = 0.4 V
C_{IO}[1]	I/O pin capacitance	-	5	-	pF	

Notes:

1. Guaranteed by characterization result, not tested in production.
2. The I_{SR} and I_{SK} must always respect the abslute maximum current and the sum of I/O, CPU and peripheral must not exceed ΣI_{DD} and ΣI_{SS}.

Table 8.2-6 I/O Output Characteristics

8.2.3.3 nRESET Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{ILR}	Negative going threshold, nRESET	-	-	0.3*V_{DD}	V	
V_{IHR}	Positive going threshold, nRESET	0.7*V_{DD}	-	-	V	
R_{RST}[1]	Internal nRESET pull up resistor	45	-	60	KΩ	V_{DD} = 5.5 V
		45	-	65		V_{DD} = 2.4 V
t_{FR}[1]	nRESET input response time	-	1.5	-	µs	Normal run and Idle mode
		10	-	25		Power down mode

Notes:

1. Guaranteed by characterization result, not tested in production.
2. It is recommended to add a 10 kΩ and 10uF capacitor at nRESET pin to keep reset signal stable.

Table 8.2-7 nRESET Input Characteristics

8.3 AC Electrical Characteristics

8.3.1 Internal High Speed 16MHz RC Oscillator (HIRC)

8.3.1.1 Internal High Speed 16MHz RC Oscillator

The 16 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	2.4	-	5.5	V	
F_{HRC}	Oscillator frequnecy	-	16[1]	-	MHz	T_A = 25 °C, V_{DD} = 3.3
	Frequency drift over temperarure and volatge	-1[3]	-	1[3]	%	T_A = 25 °C, V_{DD} = 3.3V
		-2[4]	-	2[4]	%	T_A = -20°C ~ +105 °C, V_{DD} = 2.4 ~ 5.5V
		-4[4]		4[4]	%	T_A = -40°C ~ -20 °C, V_{DD} = 2.4 ~ 5.5V
I_{HRC}[2]	Operating current	-	490	550	µA	
T_S[3]	Stable time	-	3	5	µs	T_A = -40°C ~ +105 °C, V_{DD} = 2.4 ~ 5.5V

Notes:

1. Default setting value for the product
2. Based on reload value.
3. Based on characterization, tested in production.
4. Guaranteed by characterization result, not tested in production.
5. Guaranteed by design.

Table 8.3-1 16 MHz Internal High Speed RC Oscillator(HIRC) Characteristics

8.3.1.2 Internal High Speed 24MHz RC Oscillator

The 24 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	2.4	-	5.5	V	
F_{HRC}	Oscillator frequnecy	-	24[1]	-	MHz	T_A = 25 °C, V_{DD} = 3.3
	Frequency drift over temperarure and volatge	-1[3]	-	1[3]	%	T_A = 25 °C, V_{DD} = 3.3V
		-2[4]	-	2[4]	%	T_A = -20°C ~ +85 °C, V_{DD} = 2.4 ~ 5.5V
		-4[4]		4[4]	%	T_A = -40°C ~ +105 °C, V_{DD} = 2.4 ~ 5.5V
I_{HRC}[2]	Operating current	-	490	550	µA	
T_S[3]	Stable time	-	3	5	µs	T_A = -40°C ~ +105 °C, V_{DD} = 2.4 ~ 5.5V

Notes:

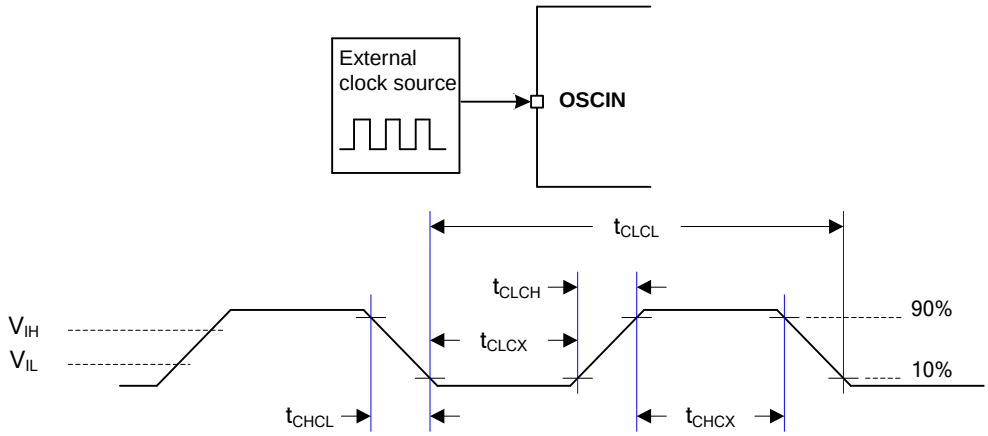
1. Default setting value for the product
2. Based on reload value.
3. Based on characterization, tested in production.
4. Guaranteed by characterization result, not tested in production.
5. Guaranteed by design.

Table 8.3-2 24 MHz Internal High Speed RC Oscillator(HIRC) characteristics

8.3.2 External 4~24 MHz High Speed Clock Input Signal Characteristics

For clock input mode the ECLK mode is enabled, OSCIN is the external clock input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{HXT_ext}	External user clock source frequency	4	-	24	MHz	
t_{CHCX}	Clock high time	8	-	-	ns	
t_{CLCX}	Clock low time	8	-	-	ns	
t_{CLCH}	Clock rise time	-	-	10	ns	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	10	ns	High (90%) to low level (10%) fall time
Du_{E_HXT}	Duty cycle	40	-	60	%	
V_{IH}	Input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	
V_{IL}	Input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	



Notes:

1. Guaranteed by characterization, not tested in production.

Table 8.3-3 External 4~24 MHz High Speed Clock Input Signal

Internal 10 kHz Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	2.4	-	5.5	V	
F_{LRC}	Oscillator frequnecy	-	10	-	kHz	
	Frequency drift over temperarure and volatge	-10[1]	-	10[1]	%	T_A = 25 °C, V_{DD} = 5V
		-35[2]	-	35[2]	%	T_A=-40~105°C Without software calibration
I_{LRC}[3]	Operating current	-	0.85	1	μA	V_{DD} = 3.3V
T_S	Stable time	-	500	-	μs	T_A=-40~105°C

Notes:

1. Guaranteed by characterization, tested in production.
2. Guaranteed by characterization, not tested in production.
3. Guaranteed by design.

Table 8.3-4 10 kHz Internal Low Speed RC Oscillator(LIRC) Characteristics

8.3.4 I/O AC Characteristics

Symbol	Parameter	Typ.	Max[*1].	Unit	Test Conditions[*2]
$t_{f(IO)out}$	Normal mode [4] output high (90%) to low level (10%) falling time	4.6	5.1	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		2.9	3.3		C_L = 10 pF, V_{DD} >= 5.5 V
		6.6	8		C_L = 30 pF, V_{DD} >= 3.3 V
		4.3	5		C_L = 10 pF, V_{DD} >= 3.3 V
		8.5	12.5		C_L = 30 pF, V_{DD} >= 2.4 V
		8.0	10.7		C_L = 10 pF, V_{DD} >= 2.4 V
$t_{f(IO)out}$	High slew rate mode [5] output high (90%) to low level (10%) falling time	4.0	4.3	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		2.1	2.5		C_L = 10 pF, V_{DD} >= 5.5 V
		4.9	5.8		C_L = 30 pF, V_{DD} >= 3.3 V
		3.0	3.7		C_L = 10 pF, V_{DD} >= 3.3 V
		9.5	13.8		C_L = 30 pF, V_{DD} >= 2.4 V
		5.4	7.4		C_L = 10 pF, V_{DD} >= 2.4 V
$t_{r(IO)out}$	Normal mode [4] output low (10%) to high level (90%) rising time	5.6	6.1	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		3.4	3.7		C_L = 10 pF, V_{DD} >= 5.5 V
		8.1	9.4		C_L = 30 pF, V_{DD} >= 3.3 V
		5.1	5.8		C_L = 10 pF, V_{DD} >= 3.3 V
		15.1	20.3		C_L = 30 pF, V_{DD} >= 2.4 V
		9.6	12.4		C_L = 10 pF, V_{DD} >= 2.4 V
$t_{r(IO)out}$	High slew rate mode [5] output low (10%) to high level (90%) rising time	4.8	5.2	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		2.1	2.5		C_L = 10 pF, V_{DD} >= 5.5 V
		6.4	7.4		C_L = 30 pF, V_{DD} >= 3.3 V
		3.0	3.7		C_L = 10 pF, V_{DD} >= 3.3 V
		12.7	16.9		C_L = 30 pF, V_{DD} >= 2.4 V
		5.4	7.4		C_L = 10 pF, V_{DD} >= 2.4 V
$f_{max(IO)out}$ [*3]	I/O maximum frequency	24	24	MHz	C_L = 30 pF, V_{DD} >= 2.4 V
					C_L = 10 pF, V_{DD} >= 2.4 V

Notes:

1. Guaranteed by characterization result, not tested in production.
2. C_L is a external capacitive load to simulate PCB and device loading.
3. The maximum frequency is defined by $f_{max} = \frac{2}{3 \times (t_f + t_r)}$.
4. PxSR.n bit value = 0, Normal output slew rate
5. PxSR.n bit value = 1, high speed output slew rate

Table 8.3-5 I/O AC Characteristics

8.4 Analog Characteristics

8.4.1 Reset and Power Control Block Characteristics

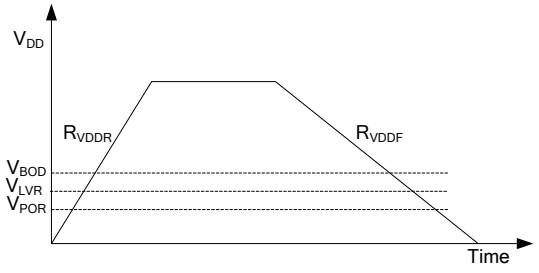
The parameters in below table are derived from tests performed under ambient temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{POR}[*1]	POR operating current	10		20	μA	AV_{DD} = 5.5V
I_{LVR}[*1]	LVR operating current	0.5	-	1		AV_{DD} = 5.5V
I_{BOD}[*1]	BOD operating current	-	0.5	2.9		AV_{DD} = 5.5V
V_{POR}	POR reset voltage	1	1.15	1.3	V	-
V_{LVR}	LVR reset voltage	1.7	2.0	2.4		-
V_{BOD}	BOD brown-out detect voltage	4.25	4.4	4.55		BOV[1:0] = [0,0]
		3.55	3.7	3.85		BOV[1:0] = [0,1]
		2.60	2.7	2.80		BOV[1:0] = [1,0]
		2.10	2.2	2.35		BOV[1:0] = [1,1]
T_{LVR_SU}[*1]	LVR startup time	60	-	80	μs	-
T_{LVR_RE}[1]	LVR respond time	0.4	-	4		Fsys = HIRC@16MHz
		180	-	350		Fsys = LIRC
T_{BOD_SU}[1]	BOD startup time	180	-	320		Fsys = HIRC@16MHz
T_{BOD_RE}[1]	BOD respond time	2.5	-	5		Fsys = HIRC@16MHz

Notes:

1. Guaranteed by characterization, not tested in production.
2. Design for specified applcaiton.

Table 8.4-1 Reset And Power Control Unit



BODFLT (BODCON1.1)	BOD Operation Mode	System Clock Source	Minimum Brown-out Detect Pulse Width
0	Normal mode (LPBOD[1:0] = [0,0])	Any clock source	Typ. 1μs
	Low power mode 1 (LPBOD[1:0] = [0,1])	Any clock source	16 ($1/F_{LIRC}$)
	Low power mode 2 (LPBOD[1:0] = [1,0])	Any clock source	64 ($1/F_{LIRC}$)
	Low power mode 3 (LPBOD[1:0] = [1,1])	Any clock source	256 ($1/F_{LIRC}$)
1	Normal mode (LPBOD[1:0] = [0,0])	HIRC/ECLK	Normal operation: 32 ($1/F_{SYS}$) Idle mode: 32 ($1/F_{SYS}$) Power-down mode: 2 ($1/F_{LIRC}$)
		LIRC	2 ($1/F_{LIRC}$)
	Low power mode 1 (LPBOD[1:0] = [0,1])	Any clock source	18 ($1/F_{LIRC}$)
	Low power mode 2 (LPBOD[1:0] = [1,0])	Any clock source	66 ($1/F_{LIRC}$)
	Low power mode 3 (LPBOD[1:0] = [1,1])	Any clock source	258 ($1/F_{LIRC}$)

Table 8.4-2 Minimum Brown-Out Detect Pulse Width

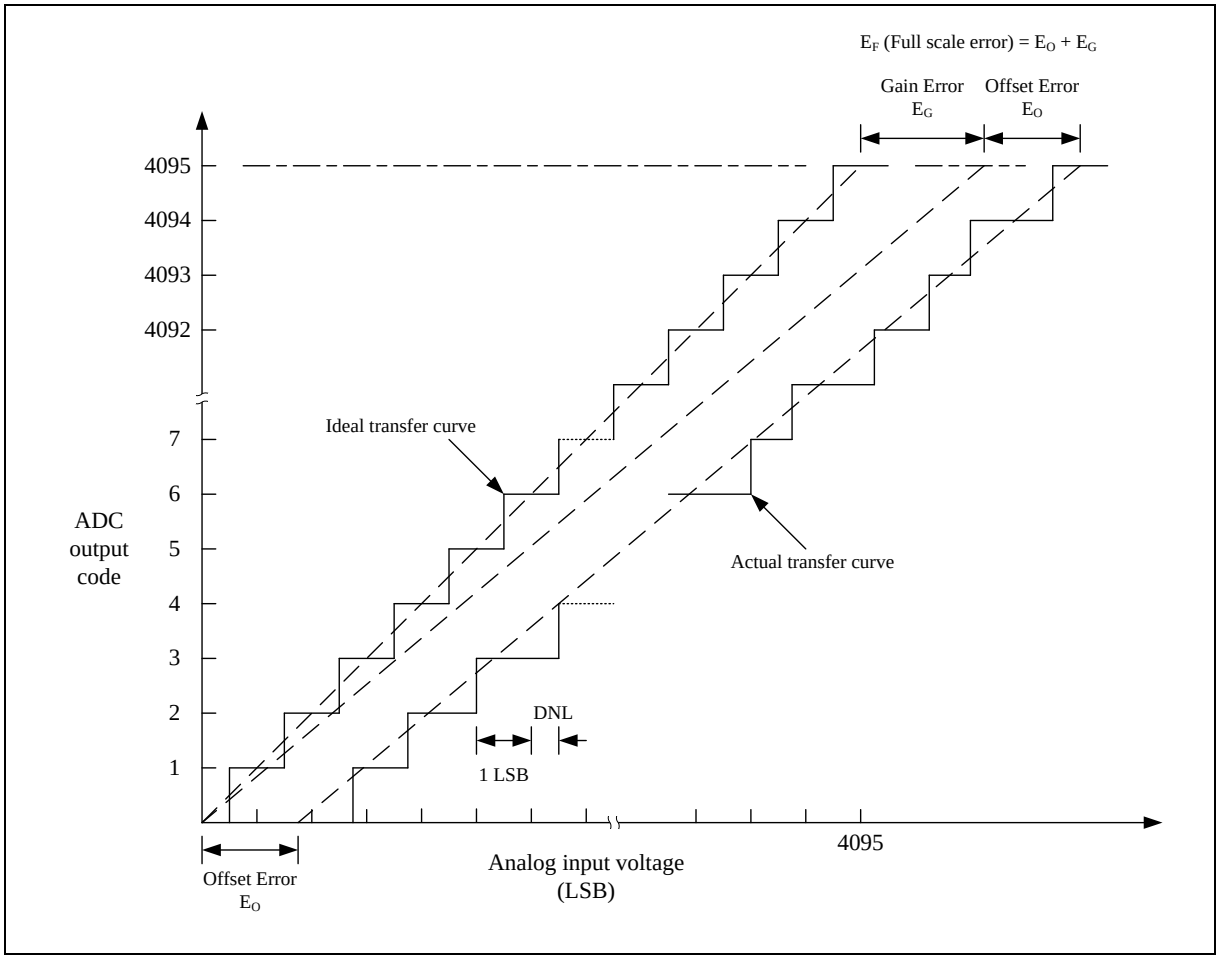
8.4.2 12-bit SAR ADC

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
AV_{DD}	Analog operating voltage	2.7	-	5.5	V	$AV_{DD} = V_{DD}$
V_{REF}	Reference voltage	2.7	-	AV_{DD}	V	$V_{REF} = AV_{DD}$
V_{IN}	ADC channel input voltage	0	-	V_{REF}	V	
I_{ADC}[*1]	Operating current (AV_{DD} + V_{REF} current)	-	-	418	μA	$AV_{DD} = V_{DD} = V_{REF} = 5.5$ V F_{ADC} = 500 kHz $T_{CONV} = 17 * T_{ADC}$
N_R	Resolution	12			Bit	
F_{ADC}[1]	ADC conversion rate	-	-	500	kHz	$F_{ADC} = 1/T_{ADC}$ $T_{ADC} = T_{SMP} + T_{CONV}$
T_{SMP}	Sampling Time [2]	0.375	-	2.12	μs	Fsys = 16MHz;
		0.417	-	1.54	μs	Fsys = 24MHz; For Min. ADCAQT = 1 [3]
T_{CONV}	Conversion time	-	-	1.625	μs	
T_{EN}	Enable to ready time	20	-	-	μs	
INL[*1]	Integral Non-Linearity Error	-3	-	+3	LSB	$V_{REF} = AV_{DD} = V_{DD}$
DNL[*1]	Differential Non-Linearity Error	-2	-	+4	LSB	$V_{REF} = AV_{DD} = V_{DD}$
E_G[*1]	Gain error	-3.5	-	+0.4	LSB	$V_{REF} = AV_{DD} = V_{DD}$
E_O[*1]$_T$	Offset error	-2	-	+2.8	LSB	$V_{REF} = AV_{DD} = V_{DD}$
E_A[*1]	Absolute Error	-7		+7	LSB	$V_{REF} = AV_{DD} = V_{DD}$

Notes:

1. ~~1.~~ Guaranteed by characterization result, not tested in production.
2. ADC sampling time =. $\frac{4 * ADCAQT + 6}{F_{ADCAQT}}$, F_{ADCAQT} is defined in ADCDIV (ADCCON2[3:1]). As default $F_{ADCAQT} = F_{SYS}$ (ADCDIV=0),
3. Since the minima sampling time must over 370ns that means when F_{ADCAQT} = 24MHz, ADCAQT should be defined as 1 at least. This value is defined by software.

Table 8.4-3 ADC Characteristics



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

8.5 Flash DC Electrical Characteristics

The devices are shipped to customers with the Flash memory erased.

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[1]	Supply voltage	1.62	1.8	1.98	V	T_A = 25℃
T_{ERASE}	Page erase time	-	5	-	ms	
T_{PROG}	Program time	-	10	-	μs	
I_{DD1}	Read current	-	4	-	mA	
I_{DD2}	Program current	-	4	-	mA	
I_{DD3}	Erase current	-	12	-	mA	
N_{ENDUR}	Endurance	100,000	-		cycles[2]	T_J = -40℃~125℃
T_{RET}	Data retention	50	-	-	year	100 kcycle[3] T_A = 55℃
		25	-	-	year	100 kcycle[3] T_A = 85℃
		10	-	-	year	100 kcycle[3] T_A = 105℃

Notes:
1. V_{FLA} is source from chip internal LDO output voltage.
2. Number of program/erase cycles.
3. Guaranteed by design.

Table 8.5-1 Flash Memory Characteristics

8.6 Absolute Maximum Ratings

Voltage Stesses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

8.6.1 Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}[*1]	DC power supply	-0.3	6.5	V
ΔV_{DD}	Variations between different power pins	-	50	mV
$\|V_{DD} - AV_{DD}\|$	Allowed voltage difference for V_{DD} and AV_{DD}	-	50	mV
ΔV_{SS}	Variations between different ground pins	-	50	mV
$\|V_{SS} - AV_{SS}\|$	Allowed voltage difference for V_{SS} and AV_{SS}	-	50	mV
V_{IN}	Input voltage on I/O	V_{SS}-0.3	5.5	V

Notes:

1. All main power (V_{DD}, AV_{DD}) and ground (V_{SS}, AV_{SS}) pins must be connected to the external power supply.

Table 8.6-1 Voltage Characteristics

8.6.2 Current Characteristics

Symbol	Description	Min	Max	Unit
ΣI_{DD}[*1]	Maximum current into V_{DD}	-	150	mA
ΣI_{SS}	Maximum current out of V_{SS}	-	150	
I_{IO}	Maximum current sunk by a I/O Pin	-	22	
	Maximum current sourced by a I/O Pin	-	10	
	Maximum current sunk by total I/O Pins[*2]	-	100	
	Maximum current sourced by total I/O Pins[*2]	-	100	

Note:

1. Maximum allowable current is a function of device maximum power dissipation.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. A positive injection is caused by V_{IN}>A_{VDD} and a negative injection is caused by V_{IN}<V_{SS}. $I_{INJ(PIN)}$ must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

Table 8.6-2 Current Characteristics

8.6.3 Thermal Characteristics

The average junction temperature can be calculated by using the following equation:

$T_J = T_A + (P_D \times \theta_{JA})$

- T_A = ambient temperature (℃)
- θ_{JA} = thermal resistance junction-ambient (℃/Watt)
- P_D = sum of internal and I/O power dissipation

Symbol	Description	Min	Typ	Max	Unit
T_A	Operating ambient temperature	-40	-	105	℃
T_J	Operating junction temperature	-40	-	125	
T_{ST}	Storage temperature	-65	-	150	
θ_{JA}[*1]	Thermal resistance junction-ambient 8-pin SOP (4x5 mm)	-	120	-	℃/Watt
	Thermal resistance junction-ambient 10-pin MSOP (3x3 mm)	-	160	-	
	Thermal resistance junction-ambient 14-pin TSSOP (4.4x5 mm)	-	100	-	

Note:

1. Determined according to JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions

Table 8.6-3 Thermal Characteristics

8.6.4 EMC Characteristics

8.6.4.1 Electrostatic discharge (ESD)

For the Nuvoton MCU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

8.6.4.2 Static latchup

Two complementary static tests are required on six parts to assess the latchup

performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

8.6.4.3 Electrical fast transients (EFT)

In some application circuit compoment will produce fast and narrow high-frequency trasnients bursts of narrow high-frequency transients on the power distribution system..

- Inductive loads:
  - Relays, switch contactors
  - Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International ElectrotechnicalCommission (IEC).

Symbol	Description	Min	Typ	Max	Unit
V_{HBM}[*1]	Electrostatic discharge,human body mode	-8000	-	+8000	V
V_{CDM}[*2]	Electrostatic discharge,charge device model	-1000	-	+1000	
LU[*3]	Pin current for latch-up[*3]	-400	-	+400	mA
V_{EFT}[*4] [*5]	Fast transient voltage burst	-4.4	-	+4.4	kV

Notes:

1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.
3. Determined according to JEDEC EIA/JESD78 standard.
4. Determinded according to IEC 61000-4-4 Electrical fast transient/burst immunity test.
5. The performace cretia class is 4A.

Table 8.6-4 EMC Characteristics

8.6.5 Package Moisture Sensitivity(MSL)

The MSL rating of an IC determines its floor life before the board mounting once its dry bag has been opened. All Nuvoton surface mount chips have a moisture level classification. The information is also displayed on the bag packing.

Pacakge	MSL
8-pin SOP (4.0 x 5.0 x 1.75 mm) [1]	MSL 3
10-pin MSOP (3.0 x 3.0 x 0.85 mm) [1]	MSL 3
14-pin TSSOP (4.4 x 5.0 x 0.9 mm) [1]	MSL 3
Note: 1. Determined according to IPC/JEDEC J-STD-020	

Table 8.6-5 Package Moisture Sensitivity(MSL)

8.6.6 Soldering Profile

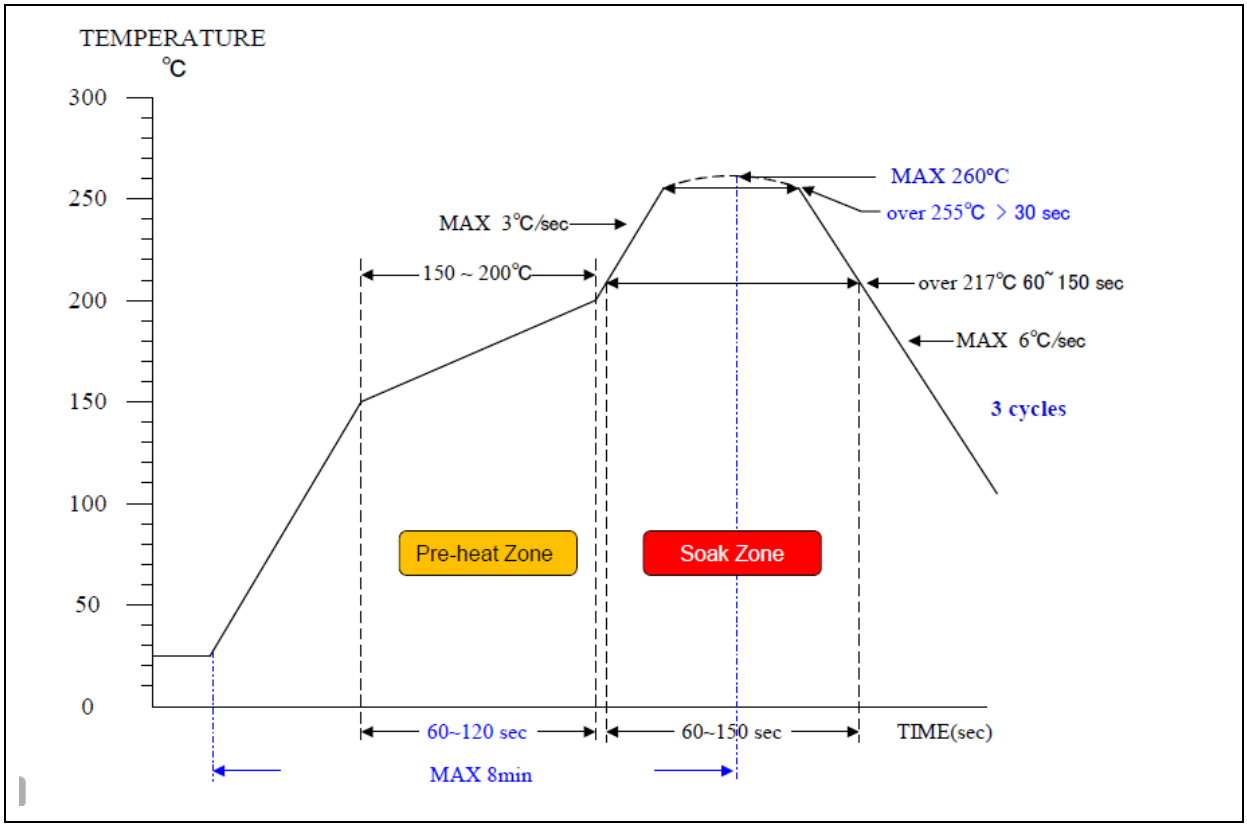


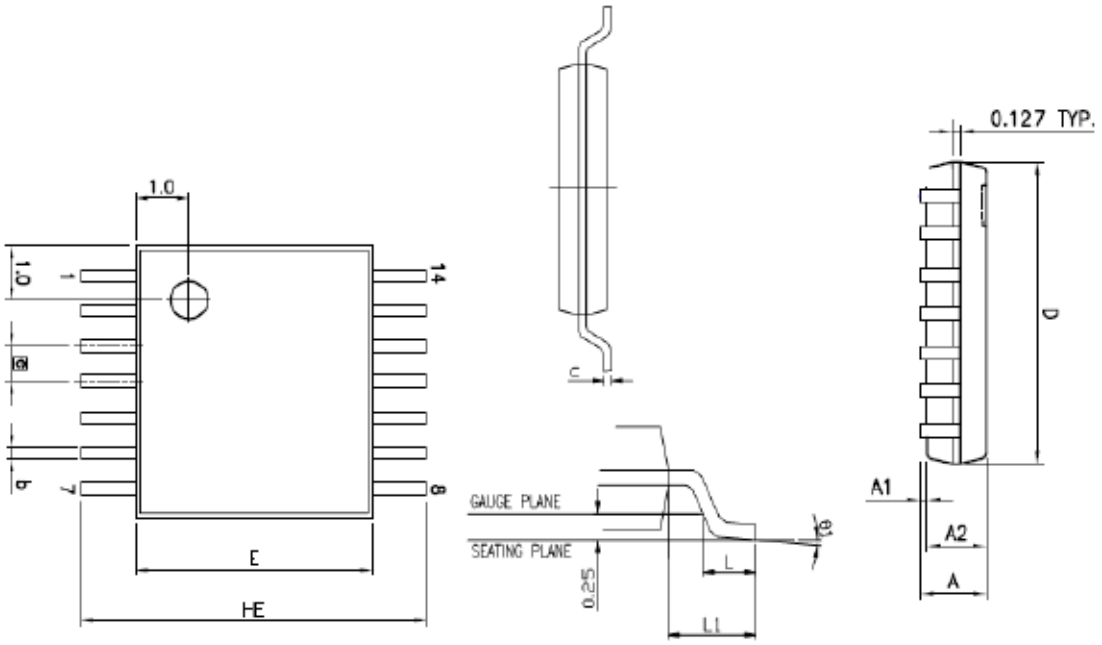
Figure 8.6-1 Soldering profile from J-STD-020C

Porfile Feature	Pb Free Package
Average ramp-up rate (217℃ to peak)	3℃/sec. max
Preheat temperature 150℃ ~200℃	60 sec. to 120 sec.
Temperature maintained above 217℃	60 sec. to 150 sec.
Time with 5℃ of actual peak temperature	> 30 sec.
Peak temperature range	260℃
Ramp-down rate	6℃/sec ax.
Time 25℃ to peak temperature	8 min. max
Note: 1. Determined according to J-STD-020C	

Table 8.6-6 Soldering Profile

9 PACKAGE DIMENSIONS

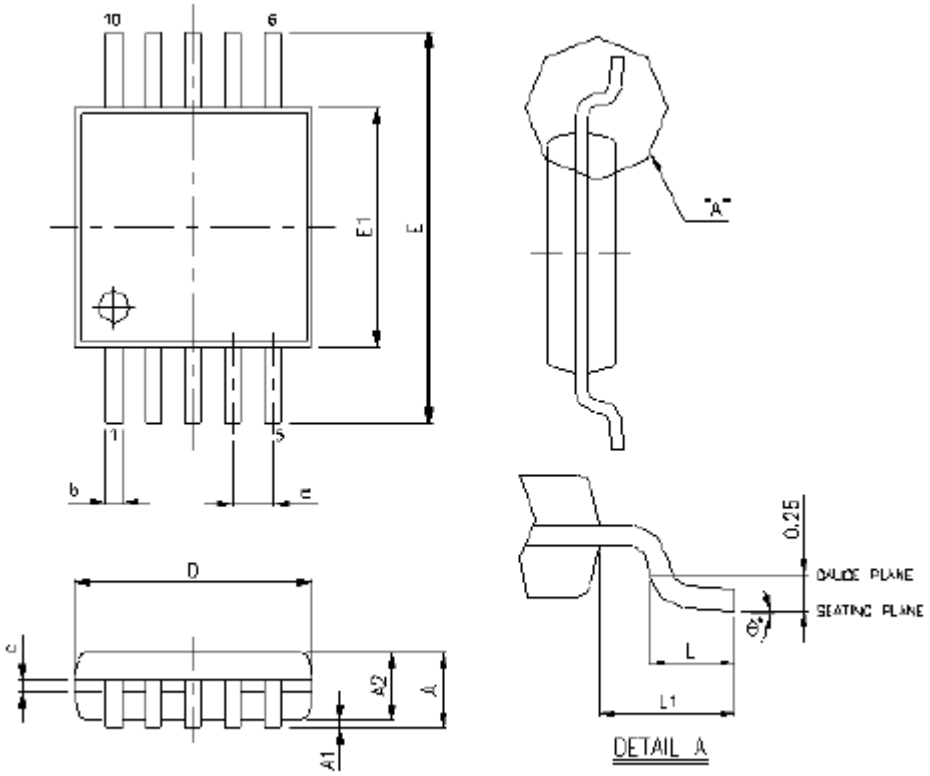
9.1 TSSOP 14-pin (4.4 x 5.5 x 1.2 mm)



CONTROLLING DIMENSION: MILLMETERS						
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	---	---	1.20	---	---	0.043
A1	0.05	---	0.15	0.02	---	0.006
A2	0.80	0.90	1.05	0.031	0.035	0.041
L	0.50	0.60	0.75	0.020	0.024	0.030
HE	6.40 BSC.			0.252 BSC.		
E	4.30	4.40	4.50	0.169	0.173	0.177
D	4.90	5.00	5.10	0.193	0.197	0.201
b	0.19	---	0.30	0.007	---	0.012
c	0.09	---	0.20	0.004	---	0.008
L1	1.0 REF.			0.039 REF.		
e	0.65 BSC.			0.026 BSC.		
θ1	0	---	8	0	---	8

Figure 9.1-1 TSSOP-14 Package Dimension

9.2 MSOP 10-pin (3.0 x 3.0 x 1.1 mm)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.10
A1	0.00	–	0.15
A2	0.75	0.85	0.95
b	0.17	–	0.27
c	0.08	–	0.23
D	3.00 BSC		
E	4.90 BSC		
E1	3.00 BSC		
e	0.50 BSC		
L	0.40	0.60	0.80
L1	0.95 REF		
θ°	0	–	8

UNIT : MM

Figure 9.2-1 MSOP -10 Package Dimension

10 ABBREVIATIONS

10.1 Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
BOD	Brown-out Detection
GPIO	General-Purpose Input/Output
Fsys	Frequency of system clock
HIRC	12 MHz Internal High Speed RC Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIRC	10 kHz internal low speed RC oscillator (LIRC)
LVR	Low Voltage $eset
PDMA	Peripheral Direct Memory Access
POR	Power On Reset
PWM	Pulse Width Modulation
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
WKT	Wakeup Timer
WDT	Watchdog Timer

Table 10.1-1 List of Abbreviations

11 REVISION HISTORY

Date	Revision	Description	
2019.8.12	1.00	Initial release.	
2019.9.3	1.01	Section 4.1.2	Modified pin name of MSOP10 pin diagram.
		Section 7.3	Removed HIRC and LIRC Deviation Figure.
		Section 7.6.5	Modified package name in the Package Moisture Sensitivity table.
2019.10.7	1.02	Section 8.3.1	Modified Frequency drift over temperature and voltage range.
		Section 8.4.1	Modified BOD brown-out detect voltage maximum value to 2.35.
2019.12.17	1.03	Section8.6.4	Modified V_{EFT} value to 4.4kV
		Section8.6.2	Modified Maximum current into V_{DD} and out of Vss value to 150mA.

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Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

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