Revision History

256M (16M x 16) Low Power SDRAM AS4C16M16MSB 54ball FBGA PACKAGE

Revision	Details	Date
Rev 1.0	Initial Release	Mar. 2023

1. GENERAL DESCRIPTION

The AS4C16M16MSB is high-performance CMOS Dynamic RAMs (DRAM) organized as 16M x 16. Synchronous design allows precise cycle control with the use of system clock and I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst lengths and programmable latencies allow the same device to be useful for a variety of high bandwidth and high-performance memory system applications.

2. FEATURES

- Power supply
  VDD/VDDQ = 1.7~1.95V
- Data width: x16
- Clock rate: 166MHz
- Partial Array Self-Refresh(PASR)
- Auto Temperature Compensated Self-Refresh(ATCSR)
- Power Down Mode
- Deep Power Down Mode (DPD Mode)
- Programmable output buffer driver strength
- Four internal banks for concurrent operation
- Clock Stop capability during idle periods
- Auto Pre-charge option for each burst access
- Burst Read Single-bit write operation.
- CAS Latency: 2 and 3
- Burst Length: 1,2,4,8 and Full Page
- Burst Type: Sequential or Interleave
- 64ms Refresh period
- Interface: LVCMOS
- Operating Temperature Range
  Industrial (-40℃ to + 85 ℃)

Table Ⅰ.Ordering Information

Product part No	Org	Temperature	Max Clock (MHz)	Package
AS4C16M16MSB-6BIN	**16M x 16**	**Industrial -40°C to 85°C**	**166**	**54-ball FBGA**

Table Ⅱ.Key Specifications

AS4C16M16MSB-6BIN		-6
tCK(3)	Clock Cycle time(min.)	6ns
tAC(3)	Access time from CLK (max.)	5.5ns
tRAS	Row Active time(min.)	42 ns
tRC	Row Cycle time(min.)	60ns

3. PIN DESCRIPTION

54-Ball FPBGA Assignment (8mm x 8mm)

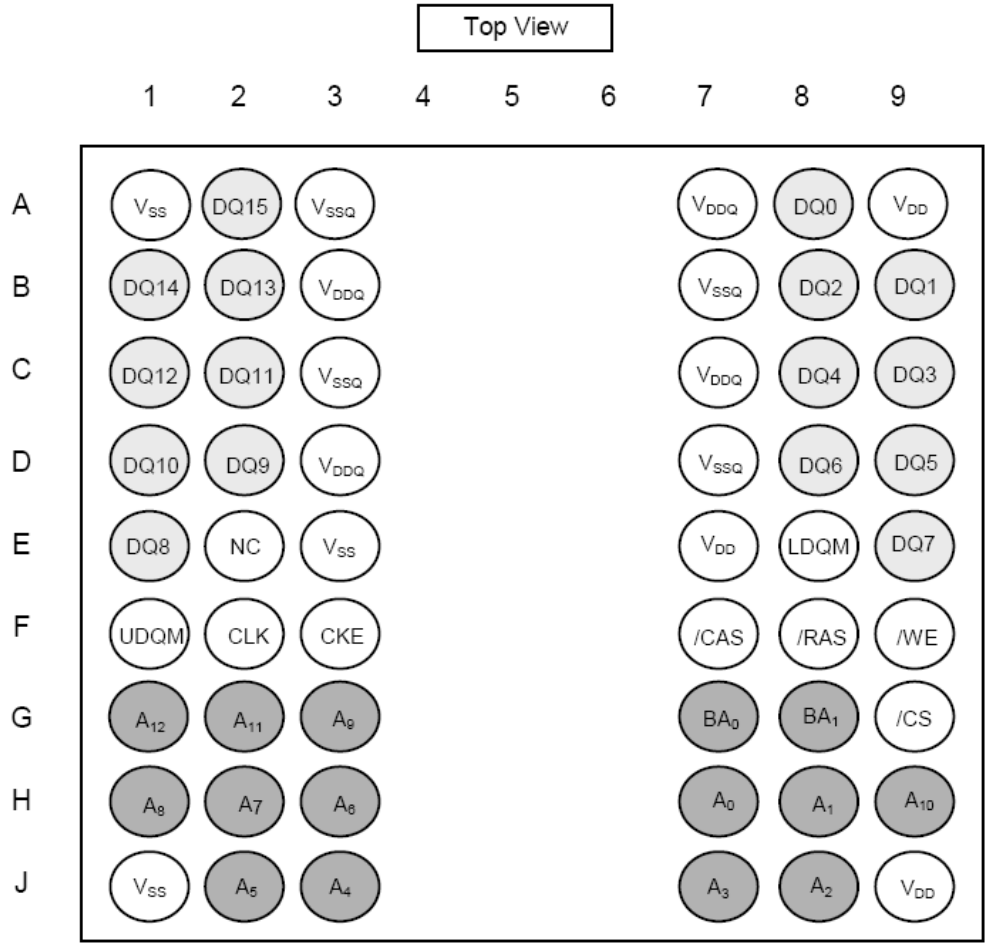


Figure 1 — PIN DESCRIPTION

3.1 Signal Descriptions

SIGNAL NAME	TYPE	DESCRIPTION
CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
CKE	Input	Clock Enable : CKE activates(HIGH) and deactivates(LOW) the CLK signal. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation(all banks idle), ACTIVE POWER-DOWN(row ACTIVE in any bank), DEEP POWER-DOWN (all banks idle), or CLOCK SUSPEND operation(burst/access in progress). CKE is synchronous except after the device enters power down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
/CS	Input	Chip Select: /CS enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when /CS is registered HIGH. /CS provides for external bank selection on systems with multiple banks. /CS is considered part of the command code.
/RAS,/CAS,/WE	Input	Command Inputs: /RAS, /CAS and /WE (along with /CS) define the command being entered.
LDQM,UDQM	Input	Input Data Mask: DQM is an input mask signal for write data. Input data is masked when DQM is sampled HIGH along with that input data during a WRITE access. DQM is sampled on both edges of DQS. Although DQM pins are input-only, the DQM loading matches the DQ and DQS loading. For x16 devices, LDQM corresponds to the data on DQ0-DQ7, UDQM corresponds to the data on DQ8-DQ15.
BA0,BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
A [n : 0]	Input	Address Inputs: provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ / WRITE commands, to select one location out of the memory array in the respective bank. The address inputs also provide the opcode during a MODE REGISTER SET command.
DQ0-DQ15	I/O	Data Bus: Input / Output
NC	-	No Connect: No internal electrical connection is present
VDDQ	Supply	I/O Power Supply
VSSQ	Supply	I/O Ground
VDD	Supply	Power Supply
VSS	Supply	Ground

Table 1 — Signal Descriptions

3.2 SDRAM Addressing Table

Density		256Mb
Number of banks		4
Bank address pins		BA0,BA1
Auto precharge pin		A10/AP
X16	**Row addresses**	A0-A12
	Column addresses	A0-A8
	tREFI(μs)	7.8

Table 2 — Addressing Table

4. BLOCK DIAGRAM

4.1 Block Diagram

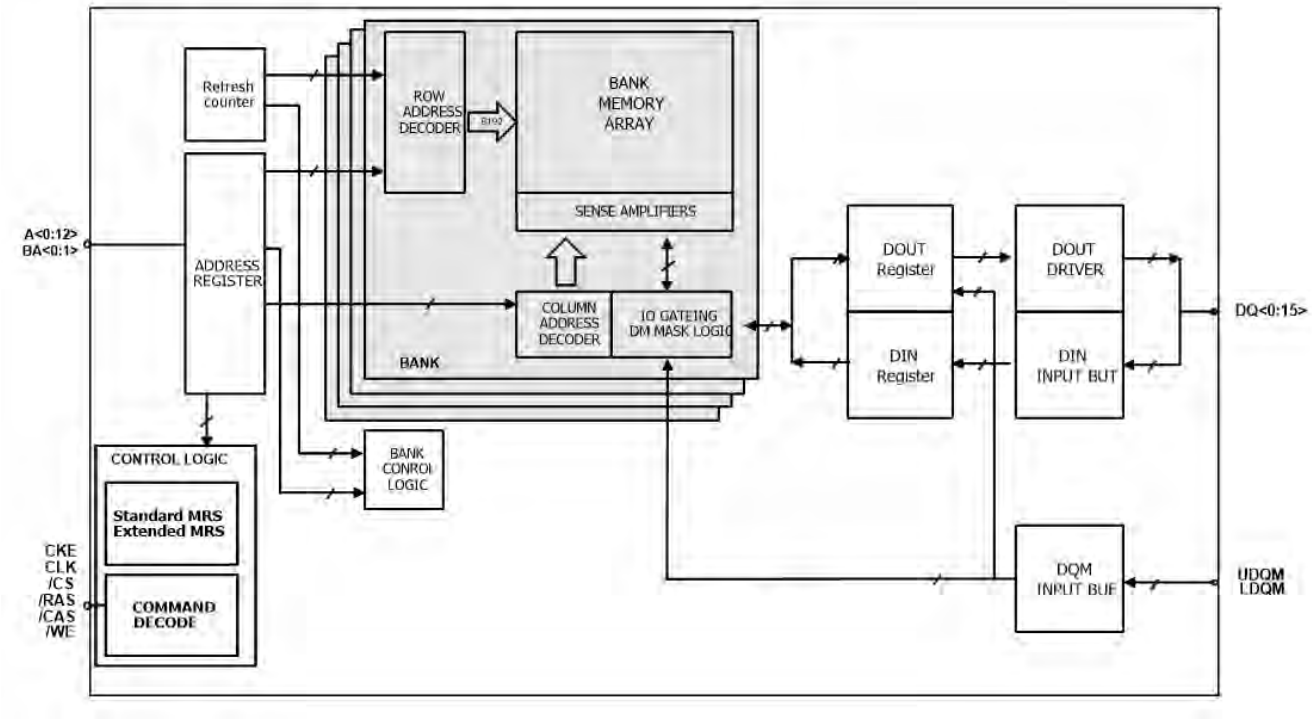
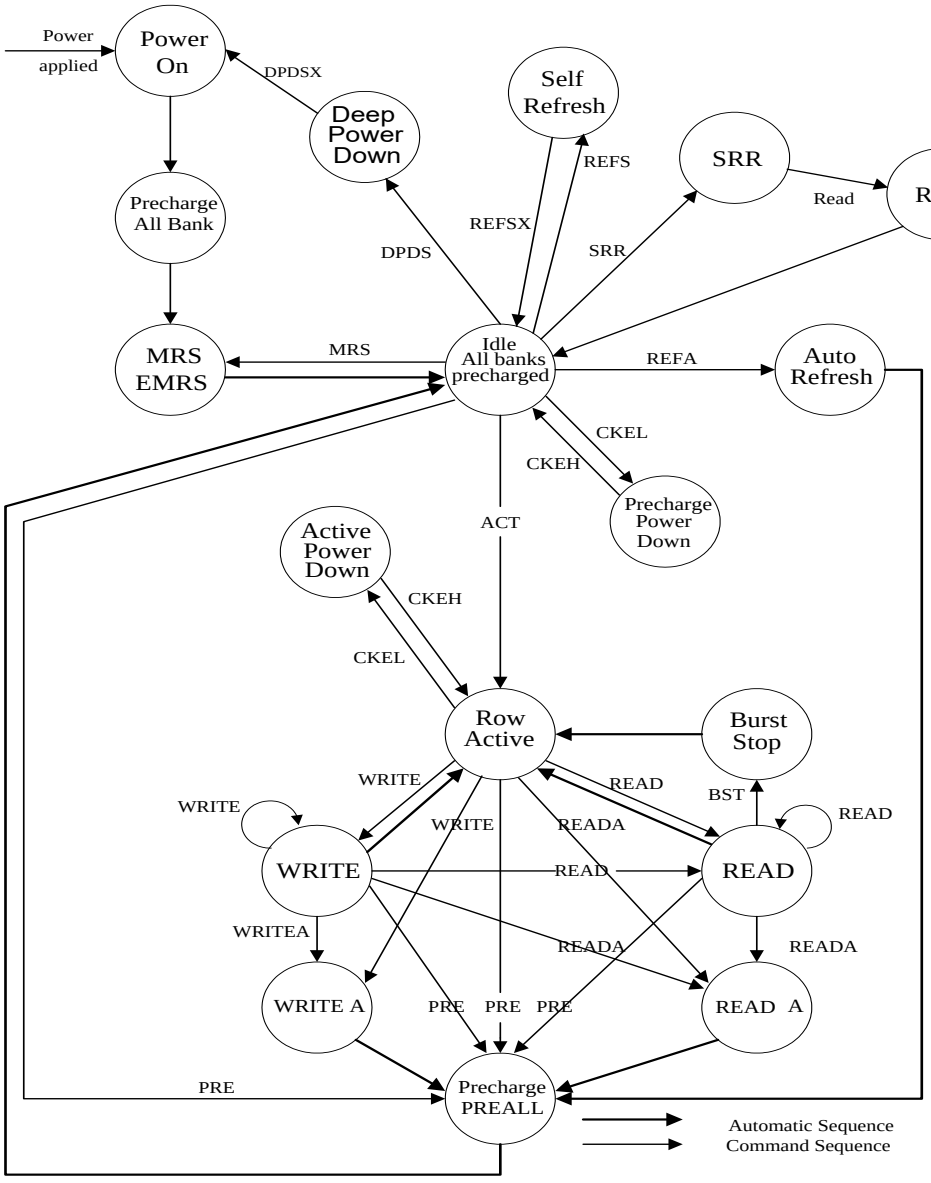


Figure.2 — Block Diagram

4.2 Simplified State Diagram



ACT = Active
BST = Burst Terminate
CKEL= Enter Power-Down
CKEH=Exit Power - Down
DPDS= Enter Deep Power Down
DPDSX= Exit Deep Power Down
MRS = Ext . Mode Reg . Set
MRS = Mode Register Set
PRE = Precharge
PREALL = Precharge All Bank
REFA = Auto Refresh
REFS = Enter Self Refresh
REFSX = Exit Self Refresh
READ = Read w/o Auto Precharge
READA = Read with Auto Precharge
WRITE = Write w/o Auto Precharge
WRITEA = Write with Auto Precharge
SRR = Status Register Read

Note: Use caution with this diagram . It is indented to provide a floorplan of the possible state transitions and commands to control them , not all details.In particular situations involving more than one bank are not captured in full detall .

Figure.3 — State Diagram

5. FUNCTION DESCRIPTION

The 256Mb SDRAM is quad-bank DRAM that operates at 1.8V and includes a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK).

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 and BA1 select the bank, A0-A12 select the row). The address bits (A0-A8) registered coincident with the READ or WRITE commands are used to select the starting column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

5.1 Initialization

SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power should be applied to VDD and VDDQ simultaneously. Once the power is applied to VDD and VDDQ, and the clock is stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin), the SDRAM requires a 200µs delay prior to issuing any command other than a DESELECT or NOP. Starting at some point during this 200µs period and continuing at least through the end of this period, DESELECT or NOP command should be applied.

Once the 200µs delay has been satisfied with at least one DESELECT or NOP command having been applied, a PRECHARGE command should be applied. All banks must then be precharged, thereby placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for mode register programming. Because the mode register will power up in an unknown state, it should be loaded prior to applying any operational command.

5.2 Register Definition

5.2.1 Mode Register

In order to achieve low power consumption, there are two mode registers in the mobile component, mode register and extended mode register. The mode register defines the specific mode of operation of the SDRAM, including burst length, burst type, CAS latency, operating mode, and write burst mode. The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.
Mode register bits A0-A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4-A6 specify the CAS latency, A7 and A8 specify the operating mode, A9 specifies the write burst mode. A10-A12 should be set to zero. BA0 and BA1 should be set to zero to prevent extended mode register.
The mode register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

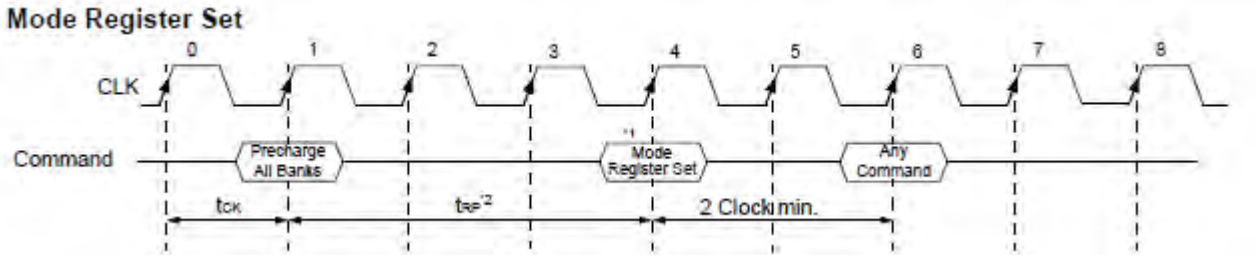
Address	BA0~BA1	A12~A10/AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	"0" Setting for Standard MRS	RFU	W.B.L	Operating Mode		CAS Latency			BT	Burst Length		

Table 3 –Register Programmed with standard MRS

Note:
1. RFU(Reserved for future use) should stay "0" during MRS cycle.

Operating Mode			CAS Latency				Burst Type		Burst Length				
A8	A7	Type	A6	A5	A4	Latency	A3	Type	A2	A1	A0	BT=0	BT=1
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential	0	0	0	1	1
0	1	Reserved	0	0	1	Reserved	1	Interleave	0	0	1	2	2
1	0	Reserved	0	1	0	2	Mode Select		0	1	0	4	4
1	1	Reserved	0	1	1	3	BA1	BA0 / Mode	0	1	1	8	8
Write Burst Length			1	0	0	Reserved	0	0 / Setting for Standard MRS	1	0	0	Reserved	Reserved
A9	Length		1	0	1	Reserved			1	0	1	Reserved	Reserved
0	Burst		1	1	0	Reserved			1	1	0	Reserved	Reserved
1	Single Bit		1	1	1	Reserved			1	1	1	Full Page	Reserved

Table 4 –Standard MRS Mode



NOTE :
1. MRS can be issued only at all bank precharge state.
2. Minimum tRP is required to issue MRS command.

5.2.1.1 Burst Length

Read and write accesses to the SDRAM are burst oriented, with the burst length being programmable. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command.
Burst lengths of 1, 2, 4, or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths. Reserved states should not be used, as unknown operation or incompatibility with future versions may result. When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached.

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
	A2	A1	A0	Sequential	Interleaved
2			0	0 – 1	0 – 1
			1	1 – 0	1 – 0
4		0	0	0 – 1 – 2 – 3	0 – 1 – 2 – 3
		0	1	1 – 2 – 3 – 0	1 – 0 – 3 – 2
		1	0	2 – 3 – 0 – 1	2 – 3 – 0 – 1
		1	1	3 – 0 – 1 – 2	3 – 2 – 1 – 0
8	0	0	0	0 – 1 – 2 – 3 – 4 – 5 – 6 – 7	0 – 1 – 2 – 3 – 4 – 5 – 6 – 7
	0	0	1	1 – 2 – 3 – 4 – 5 – 6 – 7 – 0	1 – 0 – 3 – 2 – 5 – 4 – 7 – 6
	0	1	0	2 – 3 – 4 – 5 – 6 – 7 – 0 – 1	2 – 3 – 0 – 1 – 6 – 7 – 4 – 5
	0	1	1	3 – 4 – 5 – 6 – 7 – 0 – 1 – 2	3 – 2 – 1 – 0 – 7 – 6 – 5 – 4
	1	0	0	4 – 5 – 6 – 7 – 0 – 1 – 2 – 3	4 – 5 – 6 – 7 – 0 – 1 – 2 – 3
	1	0	1	5 – 6 – 7 – 0 – 1 – 2 – 3 – 4	5 – 4 – 7 – 6 – 1 – 0 – 3 – 2
	1	1	0	6 – 7 – 0 – 1 – 2 – 3 – 4 – 5	6 – 7 – 4 – 5 – 2 – 3 – 0 – 1
	1	1	1	7 – 0 – 1 – 2 – 3 – 4 – 5 – 6	7 – 6 – 5 – 4 – 3 – 2 – 1 – 0
Full Page(y)	n=A0-A8(location 0-y)			Bn, Bn+1, Bn+2, …, Bn, …	Not supported

Table 5 – Burst Sequence

5.2.1.2 Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3.
The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address.

5.2.1.3 CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to one, two or three clocks.
If a READ command is registered at clock edge n, and the latency is m clocks, the data will be available by clock edge n + m. The DQs will start driving as a result of the clock edge one cycle earlier (n + m - 1), and provided that the relevant access times are met, the data will be valid by clock edge n + m.
Reserved states should not be used as unknown operation or incompatibility with future versions may result.

5.2.1.4 Operating Mode

The normal operating mode is selected by setting A7 and A8 to zero; the other combinations of values for A7 and A8 are reserved for future use and/or test modes. The programmed burst length applies to both read and write bursts.
Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

5.2.1.5 Write Burst Mode

When A9 = 0, the burst length programmed via A0-A2 applies to both READ and WRITE bursts; when A9 = 1, the programmed burst length applies to READ bursts, but write accesses are single-location (nonburst) accesses.

5.2.2 Extended Mode Register

The extended mode register controls functions specific to low power operation. These additional functions include drive strength, temperature compensated self refresh, and partial array self refresh.
This device has default values for the extended mode register (if not programmed, the device will operate with the default values . PASR = Full Array, DS = Full Drive).

Address	BA0~BA1	A12~A10/AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	Mode Select	RFU			DS			RFU		PASR		

Table 6 –Register Programmed with Extended MRS

NOTE :

1. RFU(Reserved for future use) should stay “0” during MRS and EMRS cycle.

Mode Select			Driver Strength				PASR			
BA1	BA0	MODE	A7	A6	A5	Driver Strength	A2	A1	A0	Size of Refresh Array
0	0	Standard MRS	0	0	0	Full	0	0	0	Full Array
0	1	Reserved	0	0	1	1/2	0	0	1	1/2 of Full Array
1	0	Extended MRS	0	1	0	1/4	0	1	0	1/4 of Full Array
1	1	Reserved	0	1	1	1/8	0	1	1	Reserved
Reserved Address			1	0	0	3/4	1	0	0	Reserved
A12~A10/AP	A9 A8 A4 A3		1	0	1	Reserved	1	0	1	1/8 array (BA1 = BA0 = Row Addr MSB = 0)
0	0 0 0 0		1	1	0	Reserved	1	1	0	1/16 array(BA1=BA0 = Row Addr 2 MSB = 0)
			1	1	1	Reserved	1	1	1	Reserved

Table 7 – EMRS for PASR(Partial Array Self Refresh) & DS (Driver Strength)

5.2.2.1 Partial Array Self Refresh

Partial Array Self Refresh (PASR) is an optional feature. With PASR, the self refresh may be restricted to a variable portion of the total array. The whole array (default), 1/2 array, or 1/4 array could be selected. Some vendors may have additional options of 1/8 and 1/16 array refreshed as well. Data outside the defined area will be lost. Address bits A0 to A2 are used to set PASR.

5.2.2.2 Temperature Compensated Self Refresh

For further power savings during SELF REFRESH, the PASR feature allows the controller to select the amount of memory that will be refreshed during SELF REFRESH. The refresh options are Full Array, 1/2 of Full Array, 1/4 of Full Array, 1/8 of Full Array and 1/16 of Full Array.

WRITE and READ commands occur to any bank selected during standard operation, but only the selected banks in PASR will be refreshed during self refresh.

5.2.2.3 Output Drive Strength

Because the Mobile SDRAM is designed for use in smaller systems that are mostly point to point, an option to control the drive strength of the output buffers is available. Drive strength should be selected based on the expected loading of the memory bus. Bits A5 and A6 of the extended mode register can be used to select the driver strength of the DQ outputs.

6. COMMANDS

6.1. Deselect

The DESELECT function(/CS HIGH) prevents new commands from being executed by the SDRAM, regardless of whether the CLK signal is enabled. The SDRAM is effectively deselected. Operations already in progress are not affected.

6.2 No Operation

The NO OPERATION (NOP) command is used to instruct the selected SDRAM to perform a NOP (/CS = LOW, /RAS = /CAS = /WE = HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

6.3 MODE REGISTER

The mode register is loaded via inputs A0-A12, BA0, BA1. The LOAD MODE REGISTER and LOAD EXTENDED MODE REGISTER commands can only be issued when all banks are idle, and a subsequent executable command cannot be issued until tMRD is met.
The values of the mode register and extended mode register will be retained even when exiting deep power-down.

6.4 Active

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A12 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

6.5 Read

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A8 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Read data appears on the DQ subject to the logic level on the DQM inputs 2 clocks earlier. If a given DQM signal was registered HIGH, the corresponding DQ will be High-Z two clocks later; if the DQM signal was registered LOW, the DQ will provide valid data.

6.6 Write

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A8 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DQM input logic level appearing coincident with the data. If a given DQM signal is registered LOW, the corresponding data will be written to memory; if the DQM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

6.7 Precharge

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only 1 bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

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6.8 Auto Precharge

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only 1 bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

6.9 Refresh Requirements

SDRAM devices require a refresh of all rows in any rolling 64ms interval. Each refresh is generated in one of two ways: by an

explicit AUTO REFRESH command, or by an internally timed event in SELF REFRESH mode. Dividing the number of device rows into the rolling 64ms interval defines the average refresh interval (tREFI), which is a guideline to controllers for distributed refresh timing.

6.10 Burst Terminate

The BURST TERMINATE command is used to truncate either fixed-length or full-page bursts. The most recently registered READ or WRITE command prior to the BURST TERMINATE command will be truncated.

6.11 Auto Refresh

AUTO REFRESH is used during normal operation of the SDRAM and is analogous to /CAS BEFORE-/RAS (CBR) refresh in conventional DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required. All active banks must be PRECHARGED prior to issuing an AUTO REFRESH command. The AUTO REFRESH command should not be issued until the minimum tRP has been met after the PRECHARGE command.

The addressing is generated by the internal refresh controller. This makes the address bits “Don’t Care” during an AUTO REFRESH command. The 256Mb SDRAM requires 8,192 AUTO REFRESH cycles every 64ms (tREF). Providing a distributed AUTO REFRESH command every 7.8µs will meet the refresh requirement and ensure that each row is refreshed. Alternatively, 8,192 AUTO REFRESH commands can be issued in a burst at the minimum cycle rate (tRFC), once every 64ms.

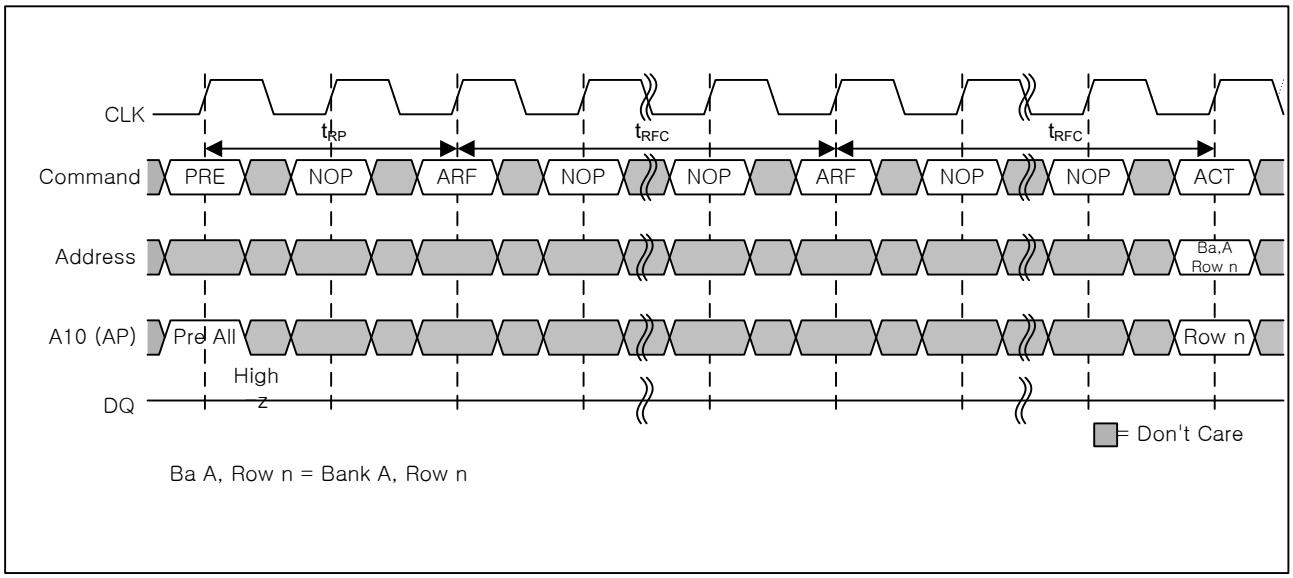


Figure 4 — Auto Refresh Cycles Back-to-Back

6.12 Self Refresh

The SELF REFRESH command can be used to retain data in the SDRAM, even if the rest of the system is powered down, as long as power is not completely removed from the SDRAM. When in the self refresh mode, the SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). Once the SELF REFRESH command is registered, all the inputs to the SDRAM become “Don’t Care” with the exception of CKE, which must remain LOW.

Once self refresh mode is engaged, the SDRAM provides its own internal clocking, causing it to perform its own auto refresh cycles. The SDRAM must remain in self refresh mode for a minimum period equal to tRAS and may remain in self refresh mode for an indefinite period beyond that.

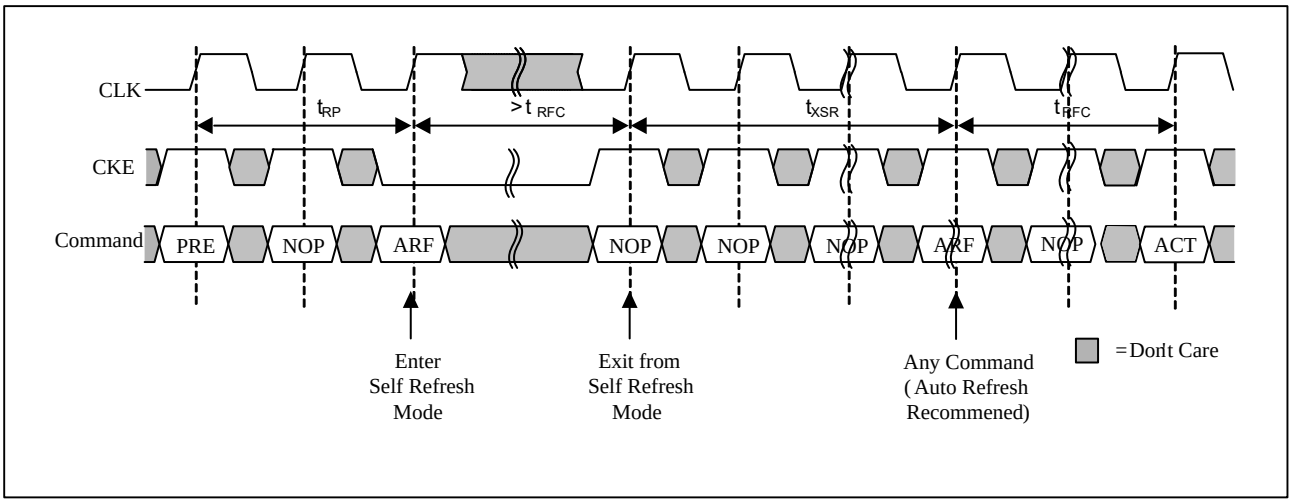


Figure 5 Self Refresh Entry and Exit

6.13 Deep Power Down

The operating mode deep power-down achieves maximum power reduction by eliminating the power of the whole memory array of the device. Array data will not be retained once the device enters deep power-down mode.

This mode is entered by having all banks idle then /CS and /WE held LOW with /RAS and /CAS held HIGH at the rising edge of the clock, while CKE is LOW. This mode is exited by asserting CKE HIGH.

7. OPERATIONS

7.1 Bank/Row Activation

The Bank Activation command is issued by holding /CAS and /WE high with /CS and /RAS low at the rising edge of the clock(CLK). The SDRAM has four independent banks, so two bank select addresses(BA0, BA1) are required. The Bank Activation command must be applied before any READ or WRITE operation is executed. The delay from the Bank Activation command to the first READ or WRITE command must meet or exceed the minimum of /RAS to /CAS delay time(tRCD min). Once a bank has been activated, it must be precharged before another Bank Activation command can be applied to the same bank. The minimum time interval between interleaved Bank Activation commands(Bank A to Bank B and vice versa) is the Bank to Bank delay time(tRRD min).

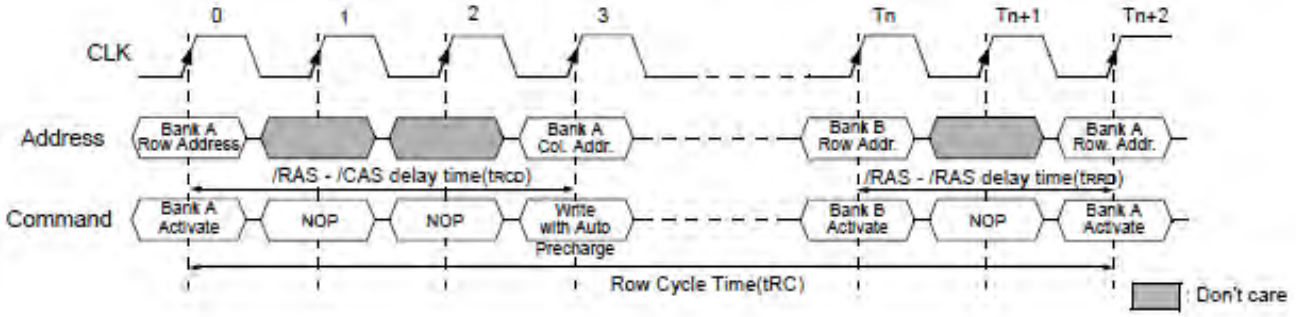
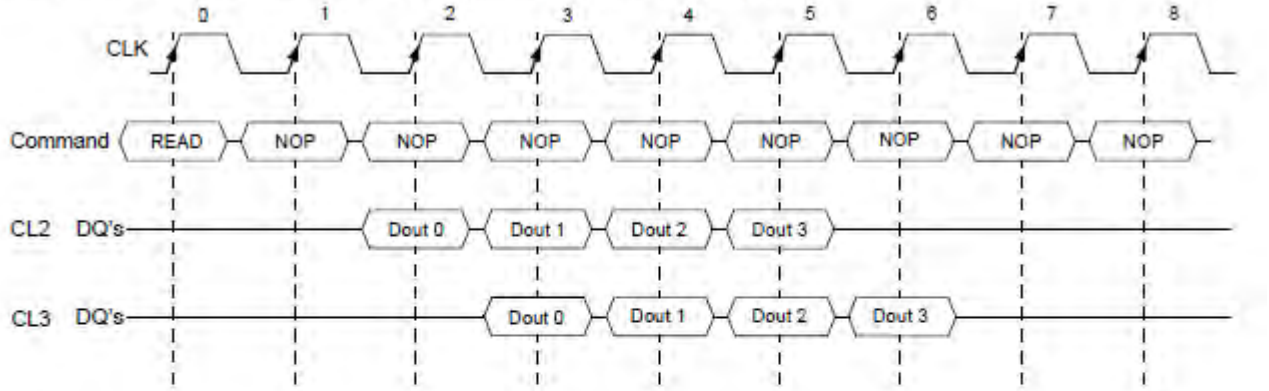


Figure 6 — Bank Activation Command Cycle

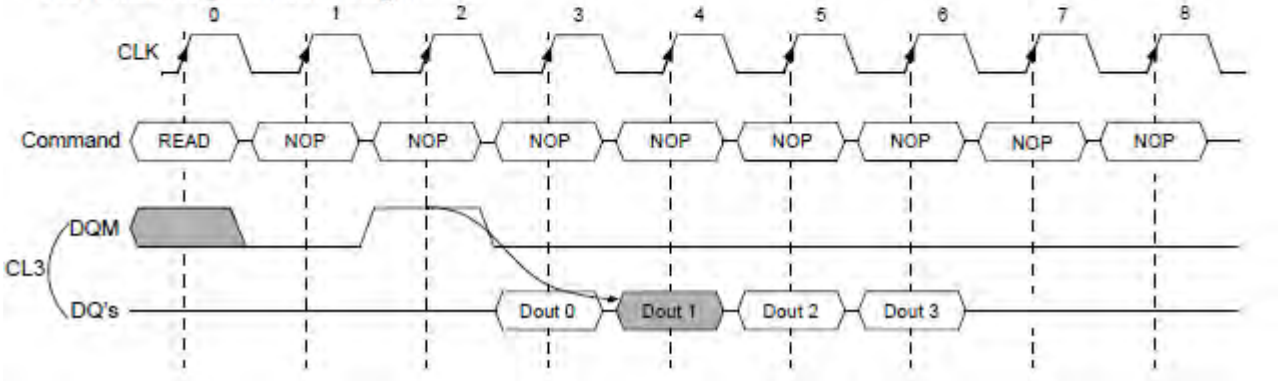
7.2 READs

READ bursts are initiated with a READ command. The starting column and bank addresses are provided with the READ command, and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data out element will be valid by the next positive clock edge. Upon completion of a burst, assuming no other commands have been initiated, the DQ will go High-Z. A full-page burst will continue until terminated. (At the end of the page, it will wrap to column 0 and continue.) Data from any READ burst may be truncated with a subsequent READ command, and data from a fixed-length READ burst may be immediately followed by data from a READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst that is being truncated. The new READ command should be issued x cycles before the clock edge at which the last desired data element is valid, where x equals the CAS latency minus one.

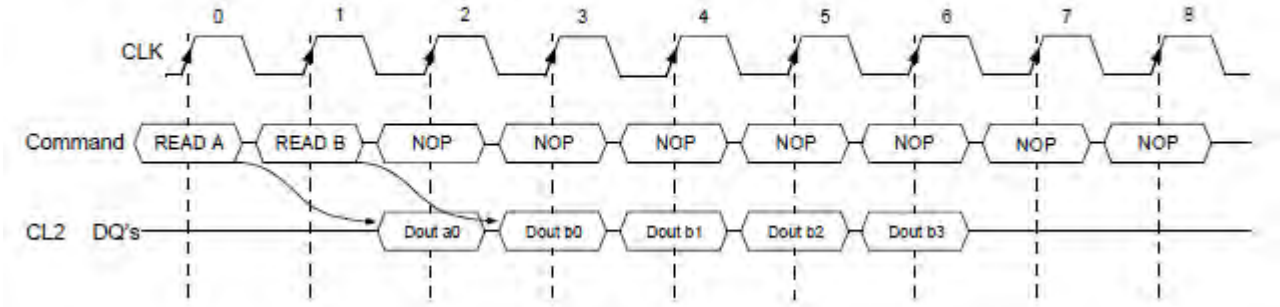
Burst Read Operation < Burst Length=4, CAS Latency=2, 3) >



DQM Masking < Burst Length = 4 >

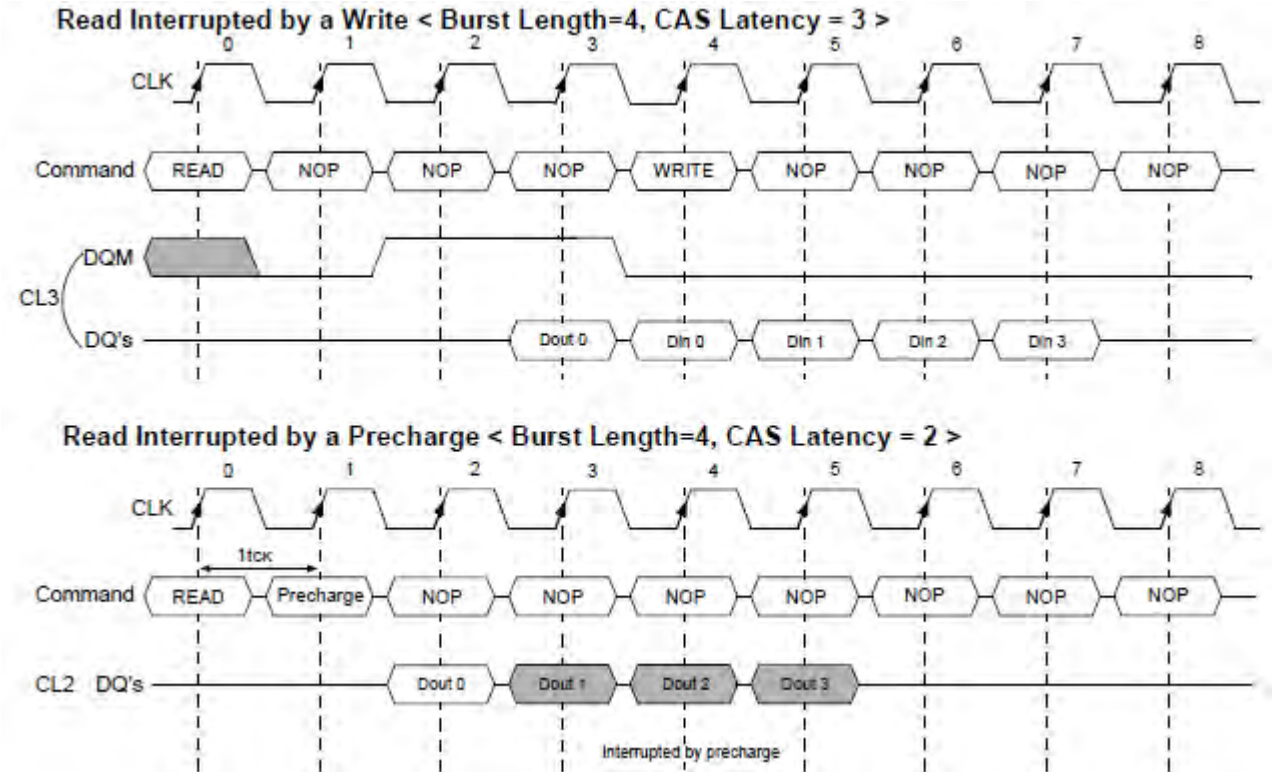


Read Interrupted by a Read < Burst Length=4, CAS Latency = 2 >



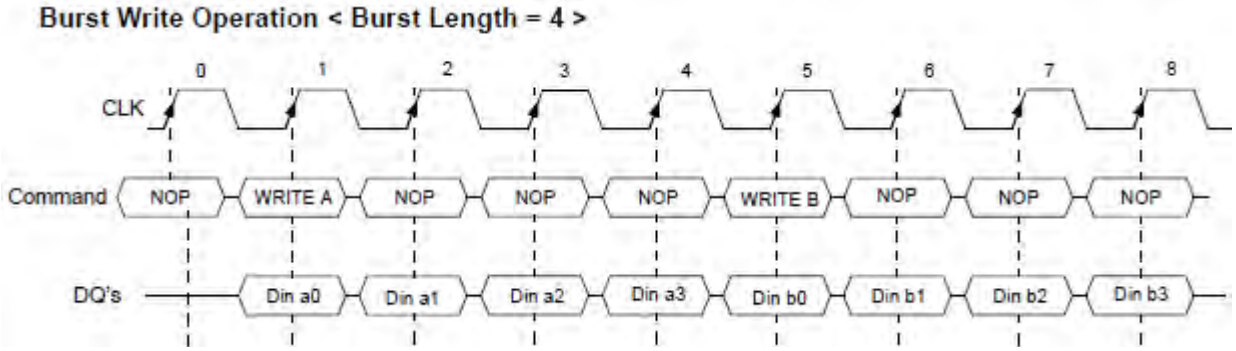
The DQM input is used to avoid I/O contention. The DQM signal must be asserted (HIGH) at least 2 clocks prior to the WRITE command (DQM latency is 2 clocks for output buffers) to suppress data-out from the READ. Once the WRITE command is registered, the DQ will go High-Z (or remain High-Z), regardless of the state of the DQM signal, provided the DQM was active on the clock just prior to the WRITE command that truncated the READ command. If not, the second WRITE will be an invalid WRITE.

The DQM signal must be de-asserted prior to the WRITE command (DQM latency is zero clocks for input buffers) to ensure that the written data is not masked.



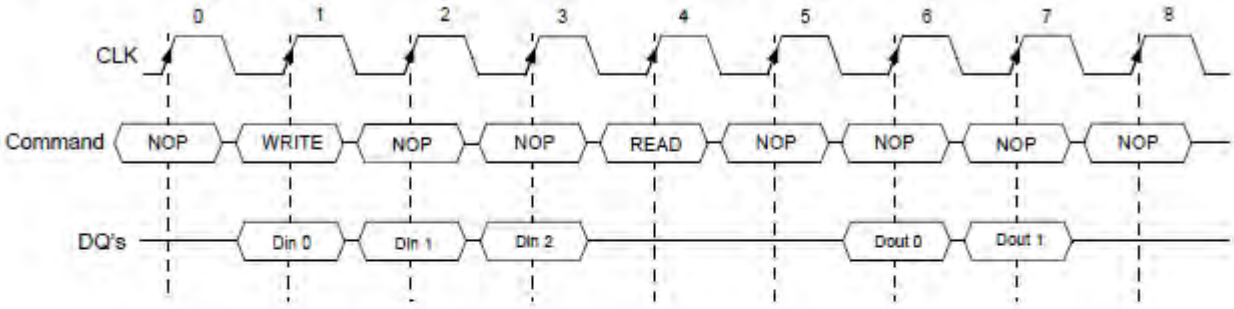
7.3 WRITEs

Data for any WRITE burst may be truncated with a subsequent WRITE command, and data for a fixed-length WRITE burst may be immediately followed by data for a WRITE command. The new WRITE command can be issued on any clock following the previous WRITE command, and the data provided coincident with the new command applies to the new command. Data n + 1 is either the last of a burst of two or the last desired of a longer burst. The SDRAM uses a pipelined architecture and therefore does not require the 2n rule associated with a prefetch architecture. A WRITE command can be initiated on any clock cycle following a previous WRITE command. Full-speed random write accesses within a page can be performed to the same bank or each subsequent WRITE may be performed to a different bank.

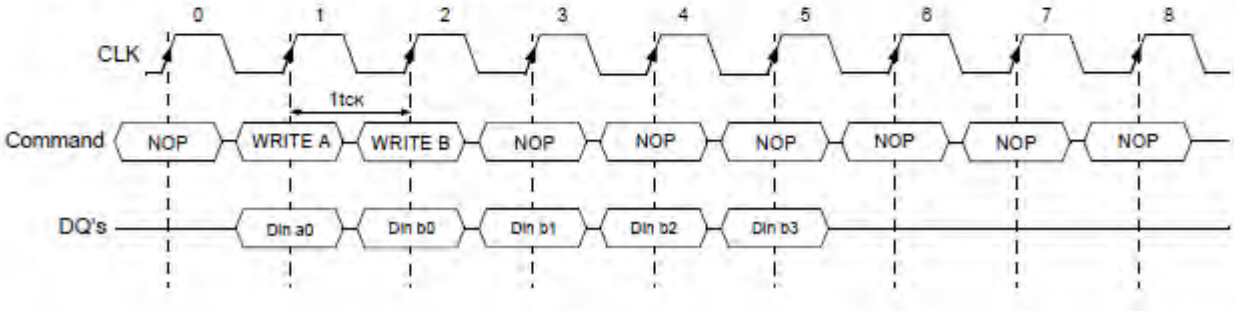


Data for any WRITE burst may be truncated with a subsequent READ command, and data for a fixed-length WRITE burst may be immediately followed by a READ command. Once the READ command is registered, the data inputs will be ignored, and WRITEs will not be executed. Data n + 1 is either the last of a burst of two or the last desired of a longer burst. Data for a fixed-length WRITE burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that auto precharge was not activated), and a full-page WRITE burst may be truncated with a PRECHARGE command to the same bank. The PRECHARGE command should be issued tWR after the clock edge at which the last desired input data element is registered. The auto precharge mode requires a tWR of at least one clock plus time, regardless of frequency.

Write Interrupted by a Read < Burst Length = 4, CAS Latency = 2 >

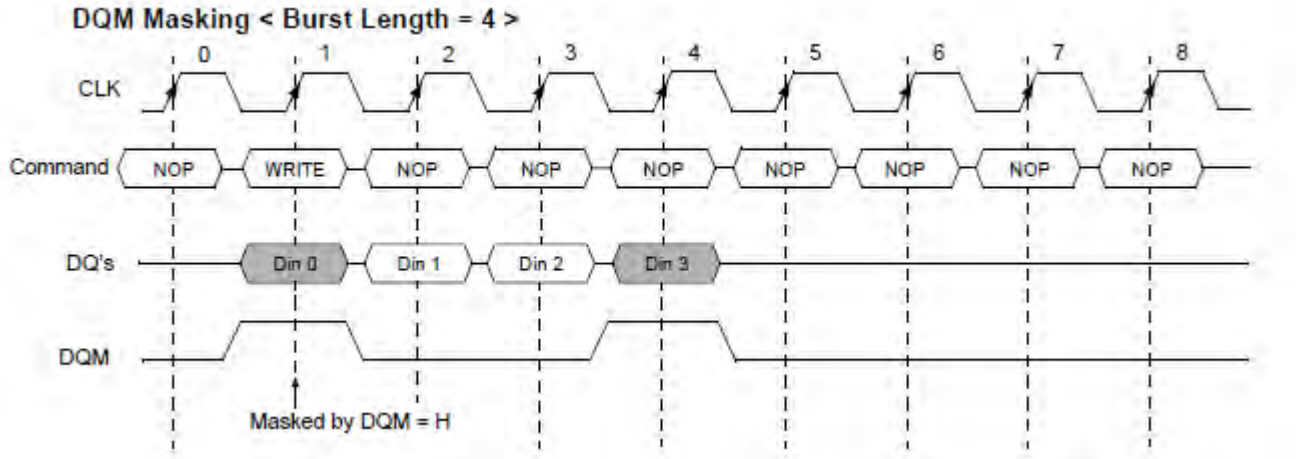


Write Interrupted by a Write < Burst Length = 4 >

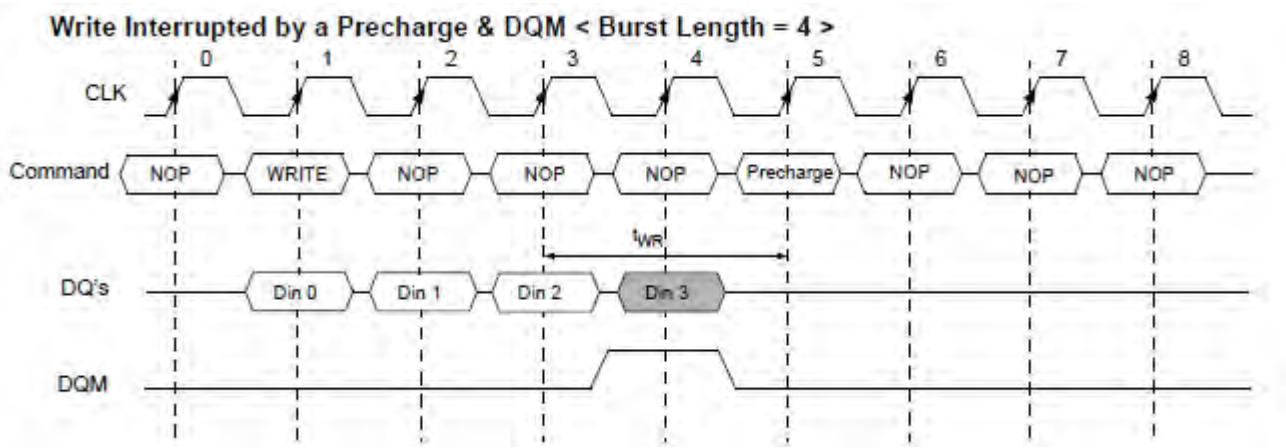


In addition, when truncating a WRITE burst, the DQM signal must be used to mask input data for the clock edge prior to, and the clock edge coincident with, the PRECHARGE command. Data n + 1 is either the last of a burst of two or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met.

DQM Masking < Burst Length = 4 >

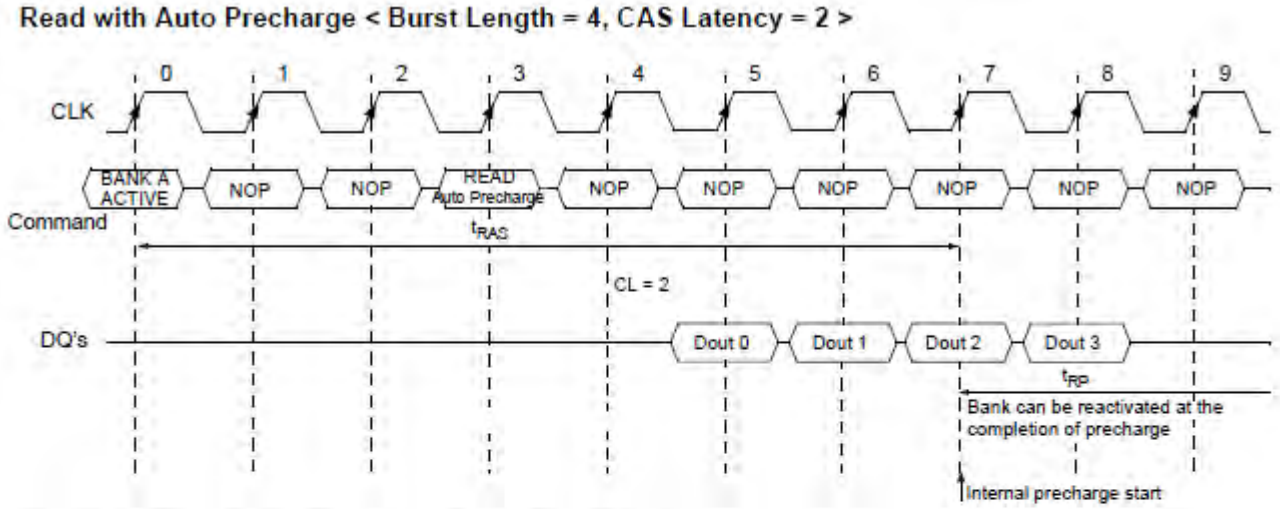


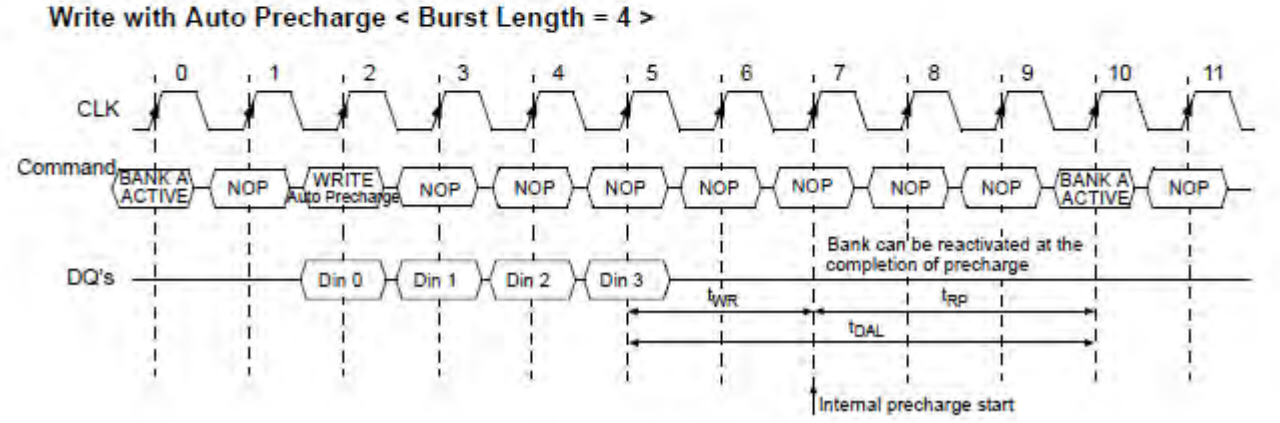
In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command; the advantage of the PRECHARGE command is that it can be used to truncate fixed-length or full-page bursts. Fixed-length or full-page WRITE bursts can be truncated with the BURST TERMINATE command. When truncating a WRITE burst, the input data applied coincident with the BURST TERMINATE command will be ignored. The last data written (provided that DQM is LOW at that time) will be the input data applied one clock previous to the BURST TERMINATE command.



7.4 Precharge

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (tRP) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

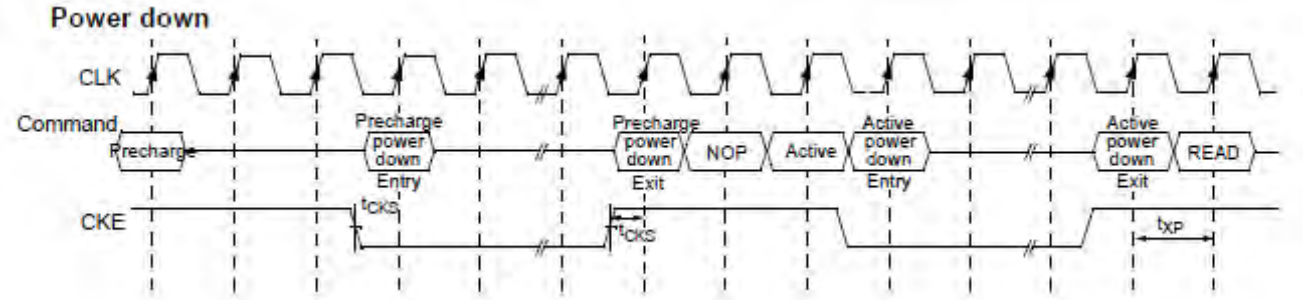




7.5 Power-Down

Power-down occurs if CKE is registered LOW coincident with a NOP or DESELECT when no accesses are in progress. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CKE, for maximum power savings while in standby. The device may not remain in the power-down state longer than the refresh period (64ms) since no refresh operations are performed in this mode.

The power-down state is exited by registering a NOP or DESELECT and CKE HIGH at the desired clock edge (meeting tCKS).



COMMAND			CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	DQM	BA0,1	A10/AP	A11, A12 A9~0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1,2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4,5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable										H		4,5
Deep Power down		Entry	H	L	L	H	H	L	X	X			
		Exit	L	H	H	X	X	X	X				9
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	H	H	H					
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	H	H	H					
DQM			H	X					V	X			7
No Operation Command(NOP)			H	X	H	X	X	X	X	X			8
					L	H	H	H					8

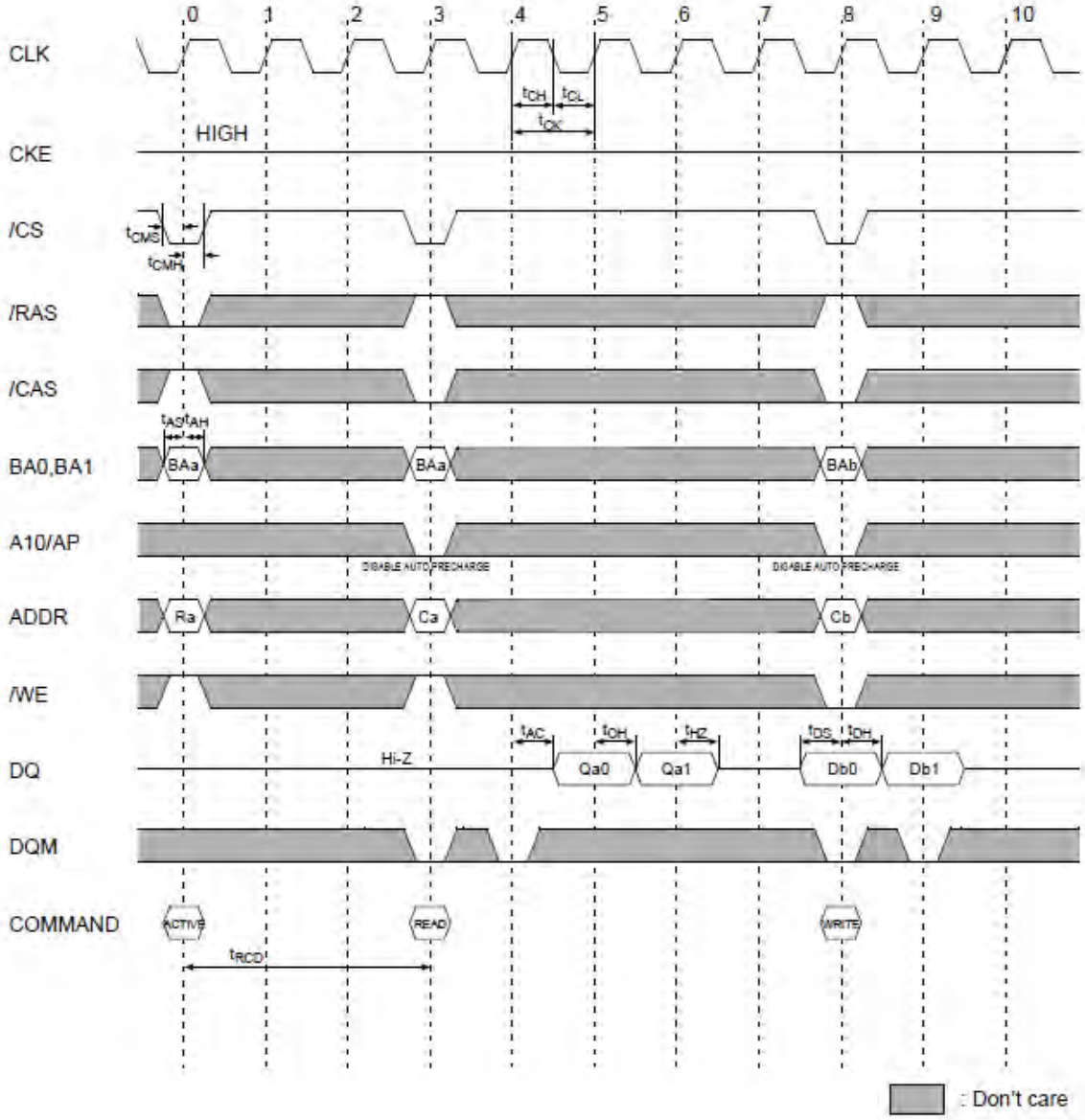
Table 8 –Simplified Truth Table

NOTE :

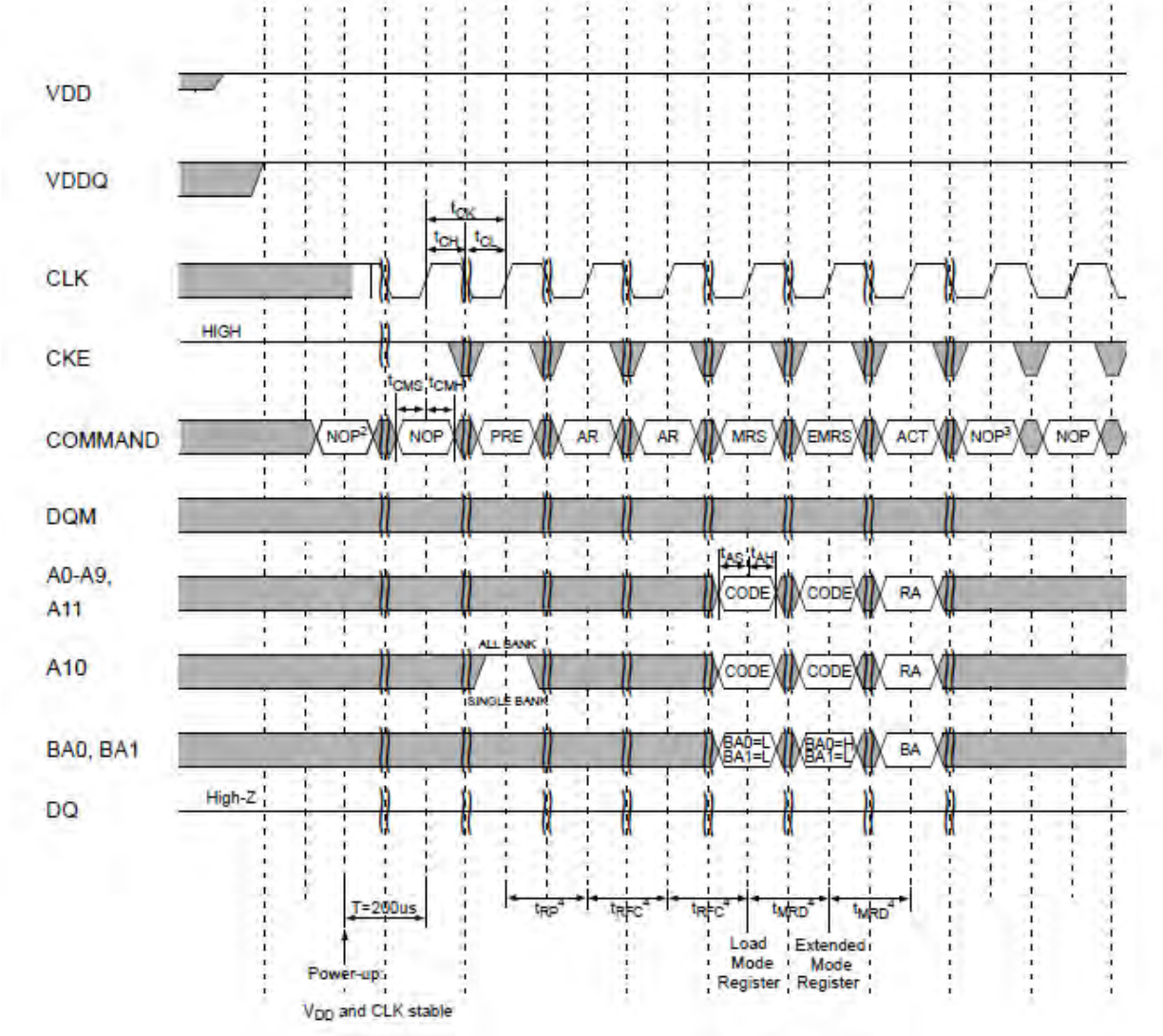
1. OP Code : Operand Code
   A0 ~ A12 & BA0 ~ BA1 : Program keys. (@EMRS/MRS)
2. EMRS/MRS can be issued only at all banks precharge state.
   A new command can be issued 2 CLK cycles after EMRS or MRS.
3. Auto refresh functions are the same as CBR refresh of DRAM.
   Auto/self refresh can be issued only at all banks precharge state.
4. 4. BA0 ~BA1 : Bank select addresses.
5. During burst read or write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at the positive going edge of CLK masks the data-in at that same CLK in write operation (Write DQM latency is 0), but in read operation, it makes the data-out Hi-Z state after 2CLK cycles. (Read DQM latency is 2).
8. This combination is not defined for any function, which means “No Operation(NOP)” in SDRAM.
9. The Deep Power Down Mode is exited by asserting CKE high and full initialization is required after exiting Deep Power Down Mode.

8. Timing Diagrams

8.1 Basic Timing (Setup, Hold and Access Time @ BL=2, CL=2)



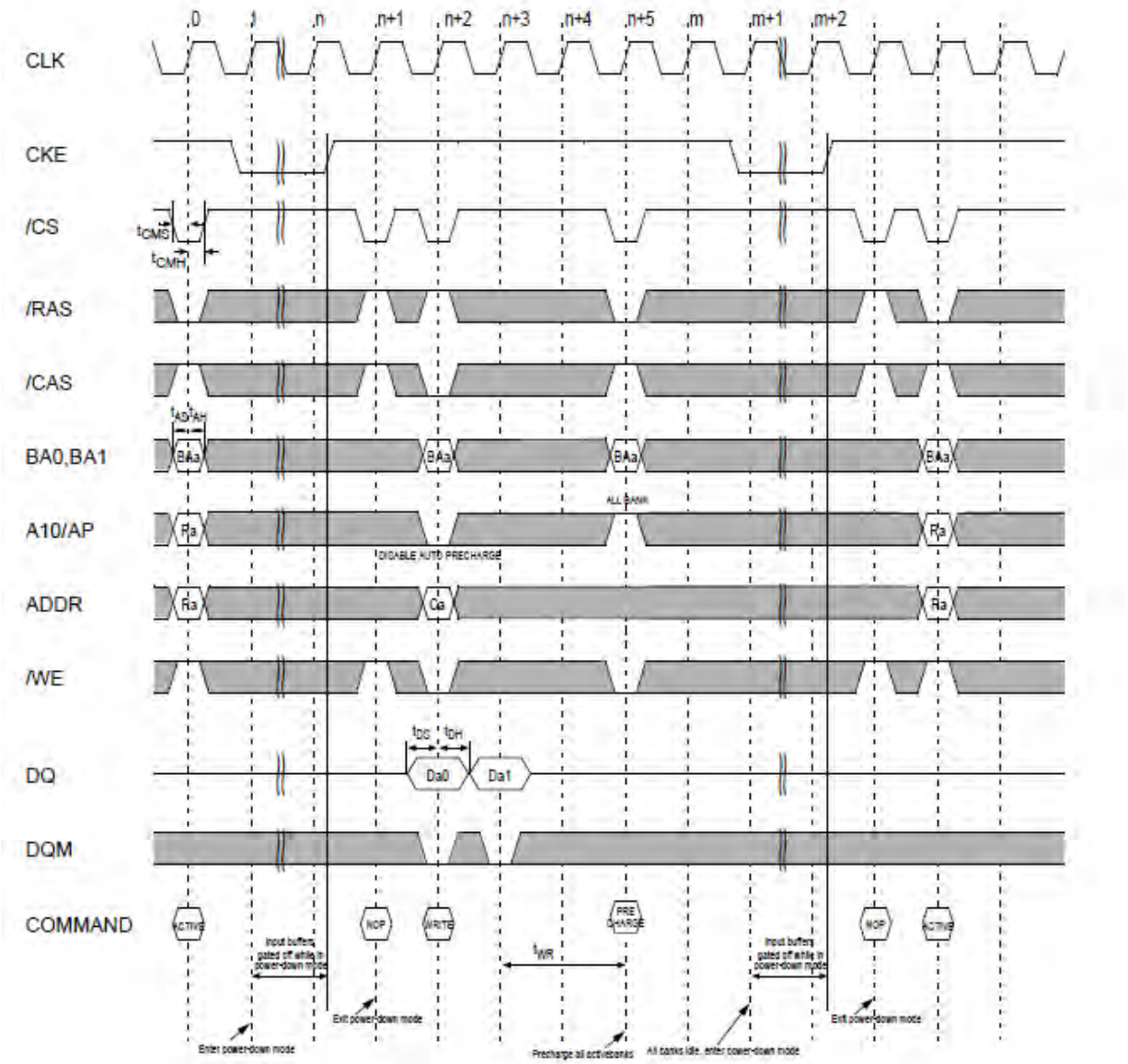
8.2 Power up & Initialization Sequence



NOTE :

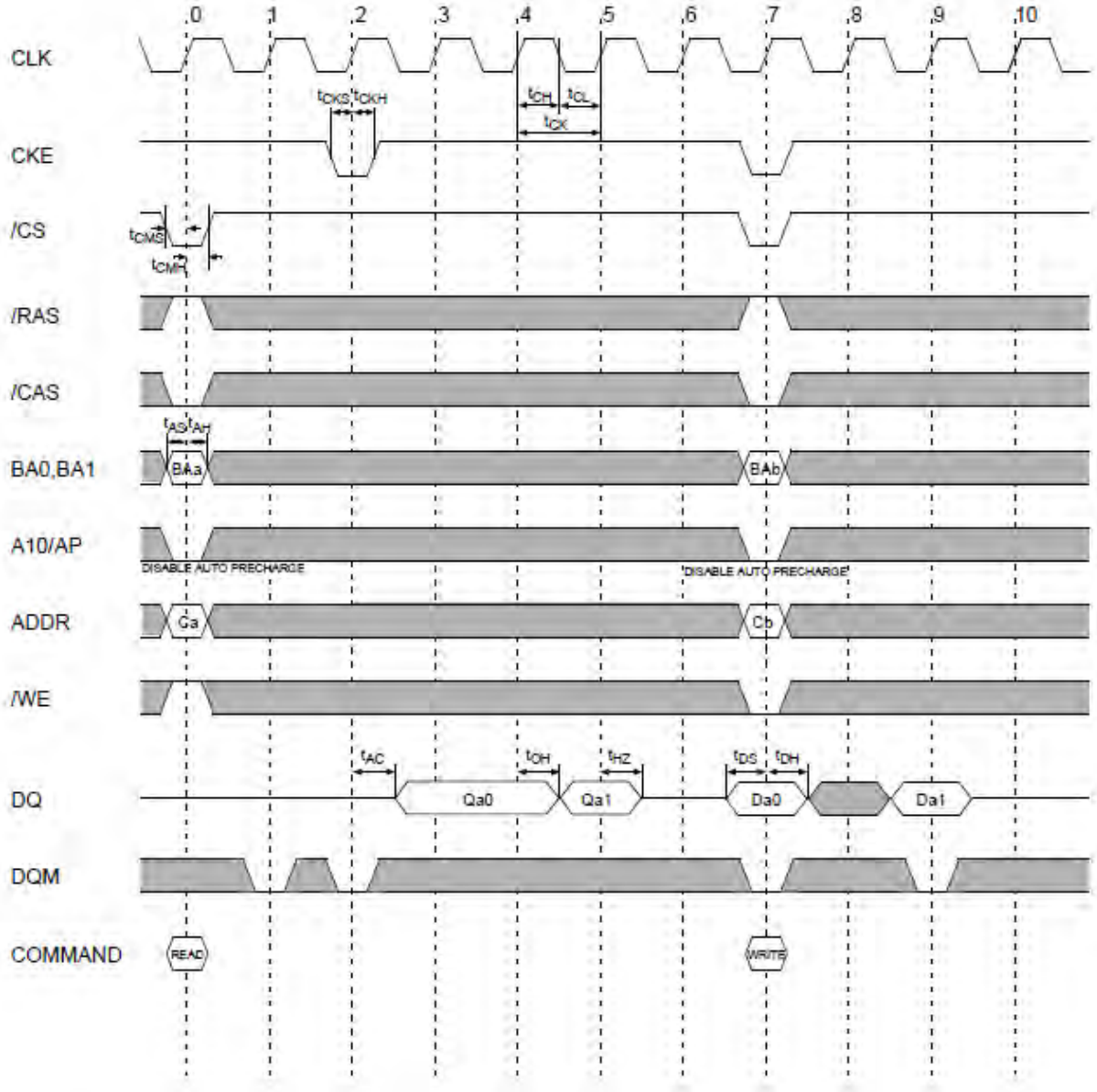
1. PRE = PRECHARGE command, MRS = LOAD MODE REGISTER command, AR = AUTO REFRESH command ACT = ACTIVE command, RA = Row address, BA = Bank address
2. NOP or DESELECT commands are required for at least 200us.
3. Other valid commands are possible.
4. NOPs or DESELECTs are required during this time.

8.3 Power down Mode

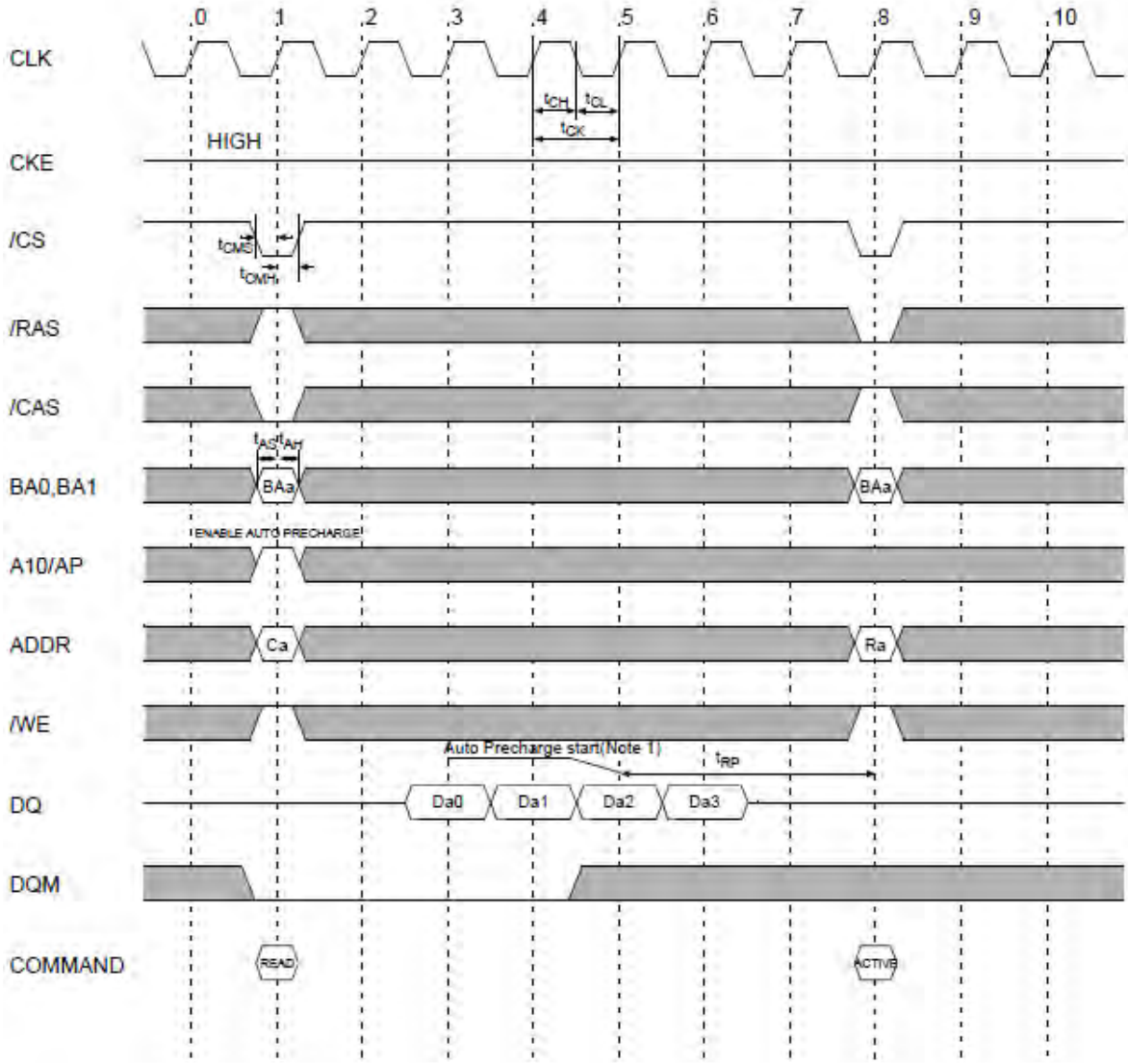


NOTE : Violating refresh requirements during power-down may result in a loss of data.

8.4 Clock Suspend Mode

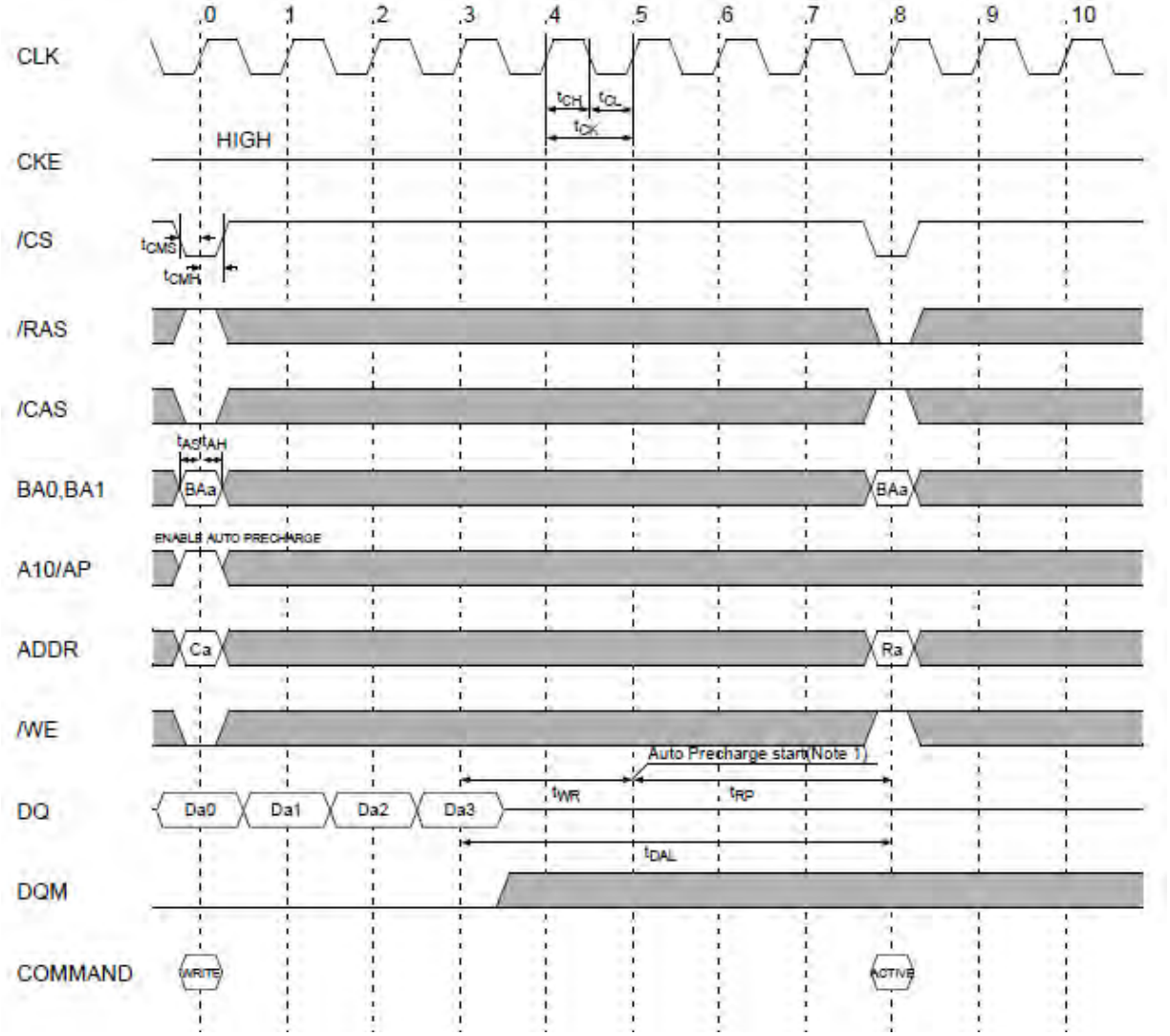


8.5 READ with Auto Precharge (@ BL=4, CL=2)

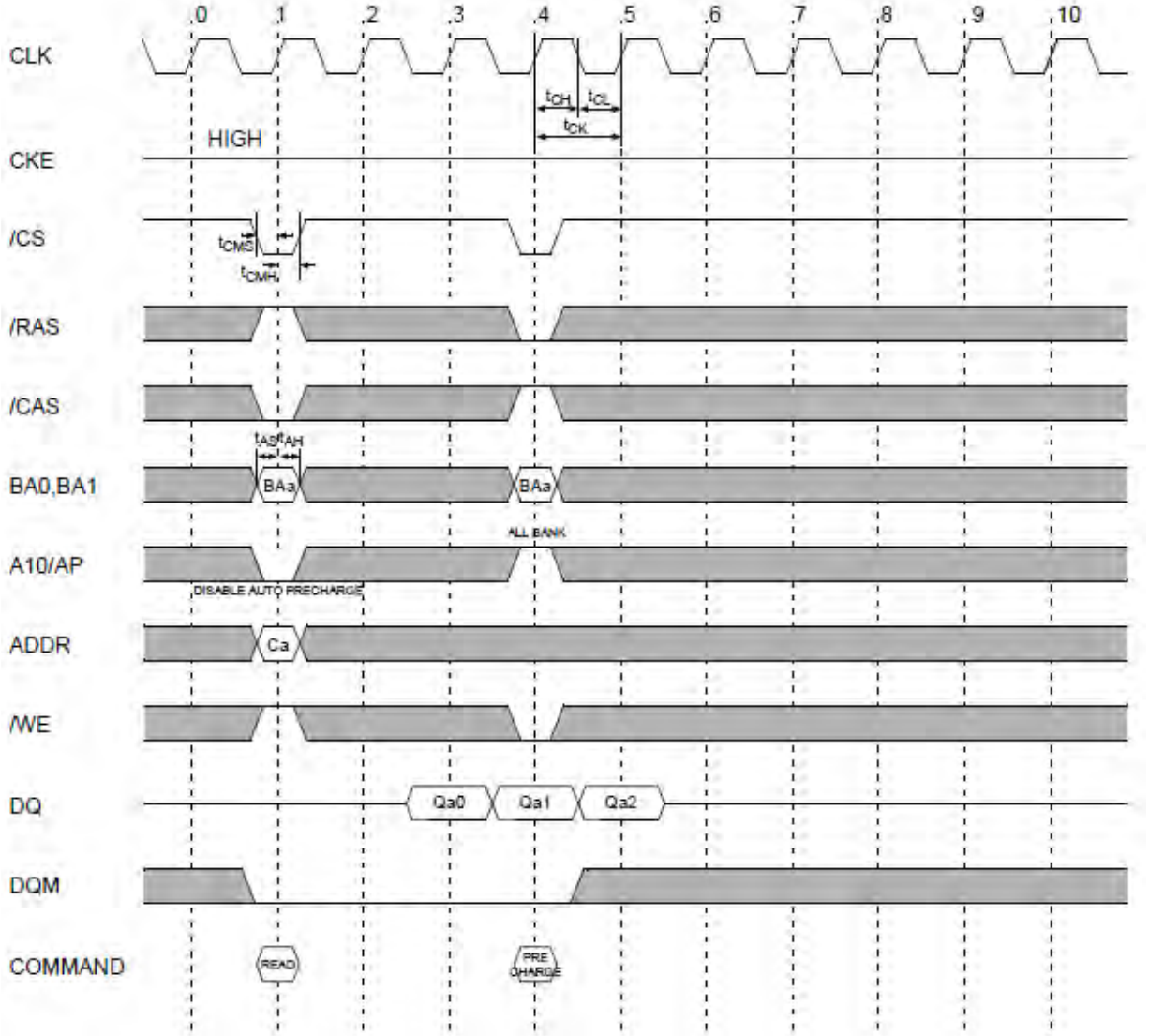


NOTE : The row active command of the precharged bank can be issued after tRP from this point.

8.6 WRITE with Auto Precharge (@ BL=4)



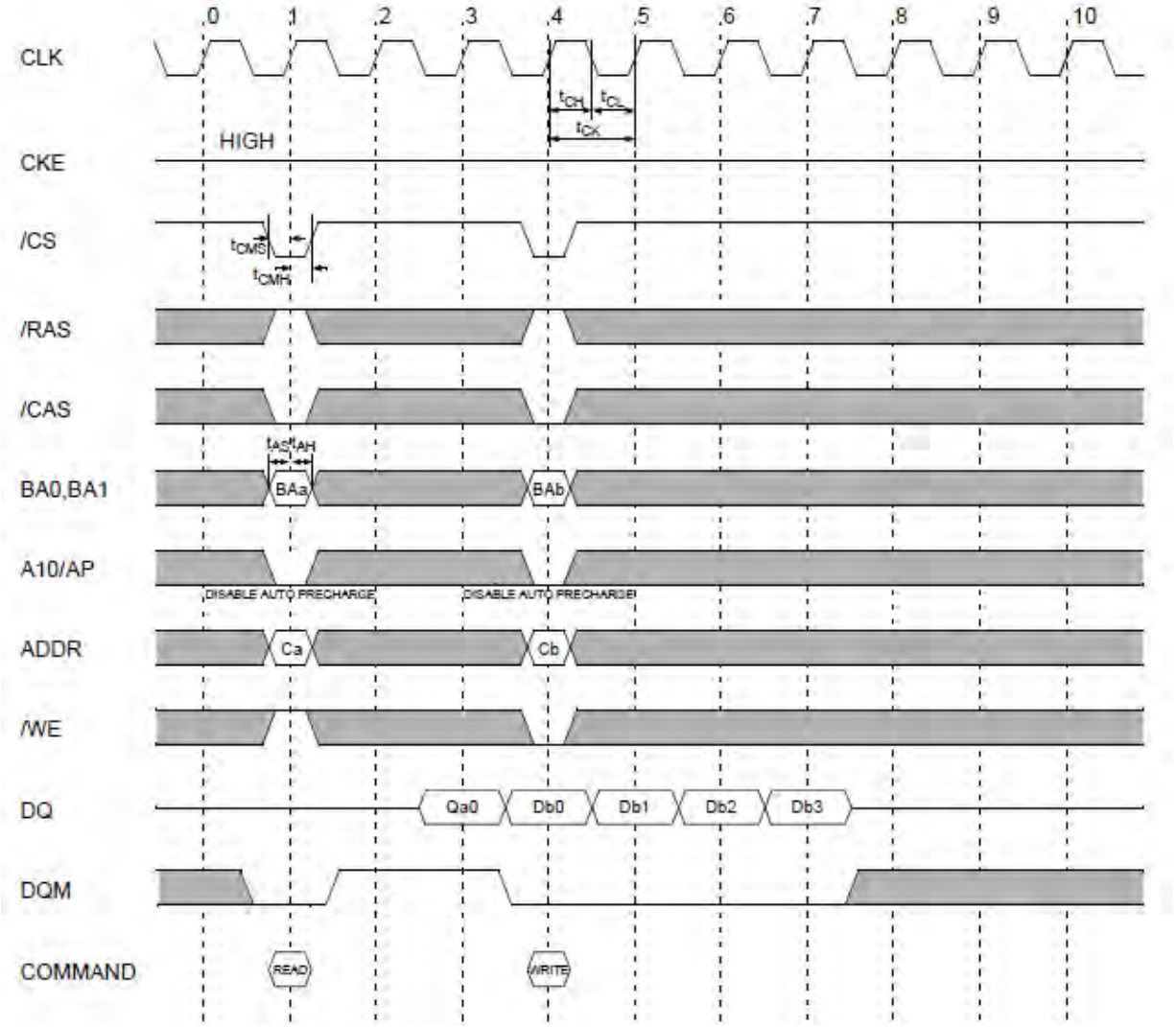
8.7 READ Interrupted by Precharge (@ BL=4, CL=2)



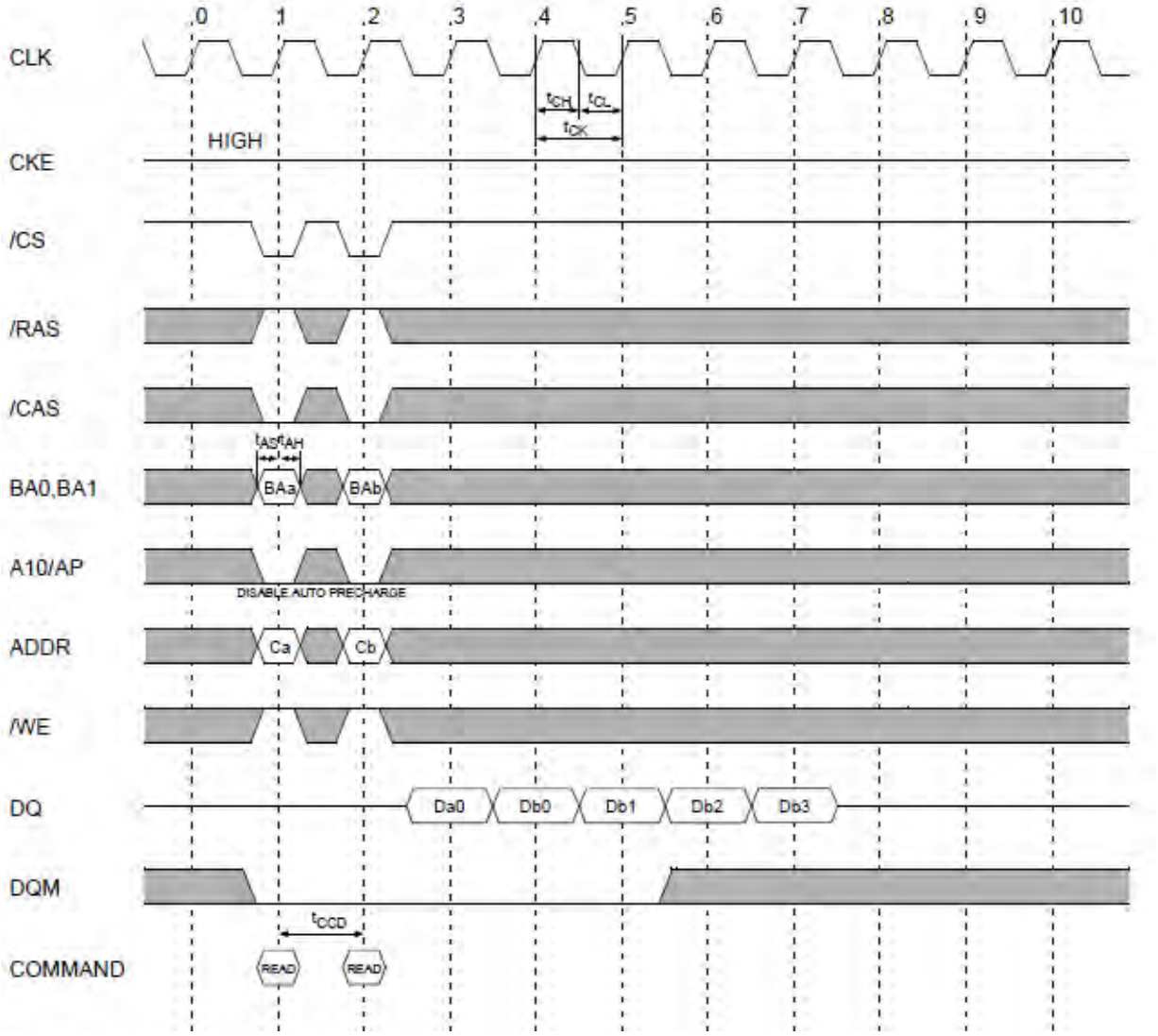
NOTE :
When a burst Read command is issued to a SDRAM, a Precharge command may be issued to the same bank before the Read burst is complete.
The following functionality determines when a Precharge command may be given during a Read burst and When a new Bank Activate command may be issued to the same bank.

1. For the earliest possible Precharge command without interrupting a Read burst, the Precharge command may be given on the rising clock edge which is CL clock cycles before the end of the Read burst where CL is the CAS Latency. A new Bank Activate command may be issued to the same bank after tRP(RAS Precharge time).
2. When a Precharge command interrupts a Read burst operation, the Precharge command may be given on the rising clock edge which is CL clock cycles before the last data from the interrupted Read burst where CL is the CAS Latency. Once the last data word has been output, the output buffers are tristated. A new Bank Activate command may be issued to the same bank after tRP.

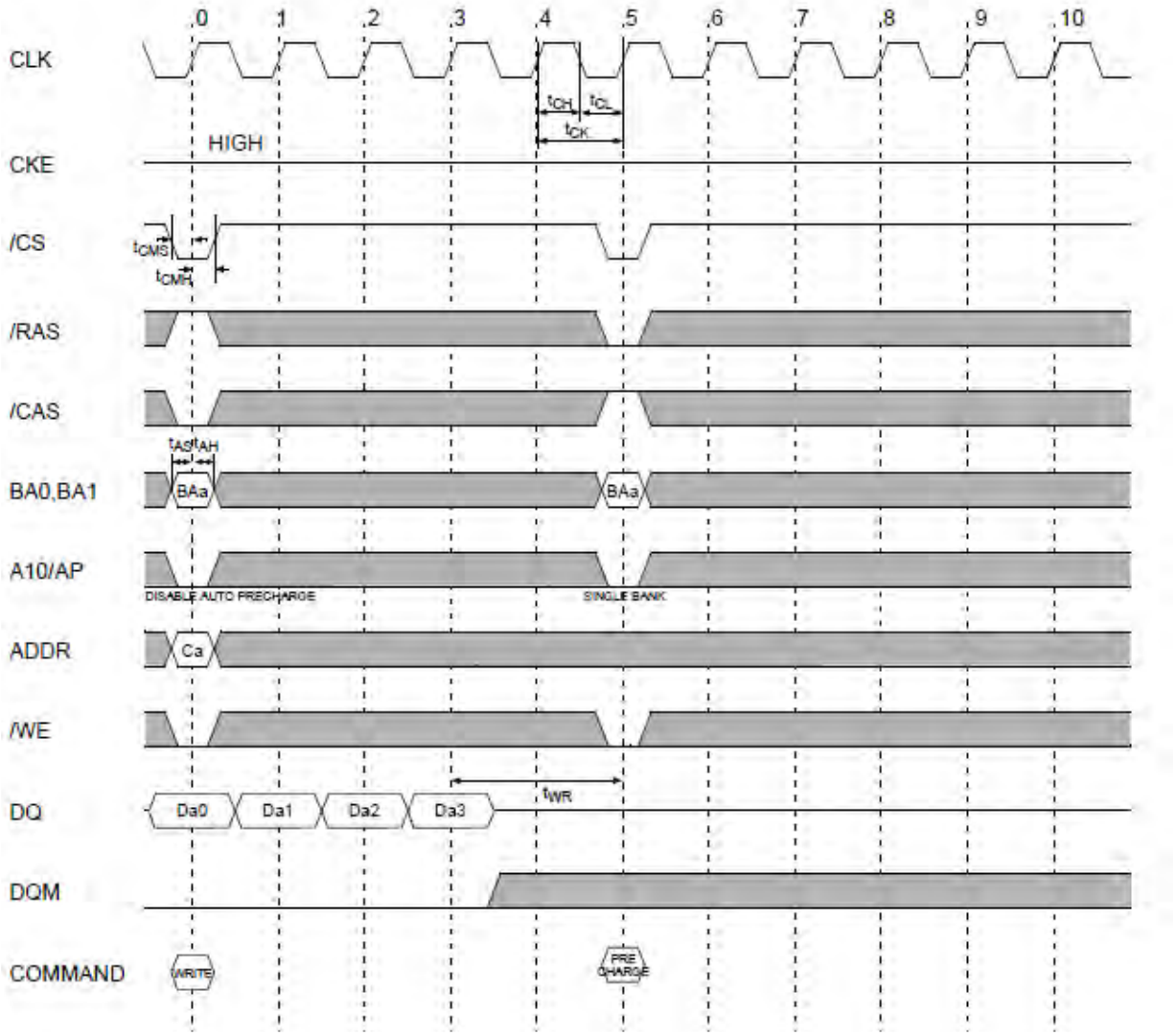
8.8 READ Interrupted by a WRITE (@ BL=4, CL=2)



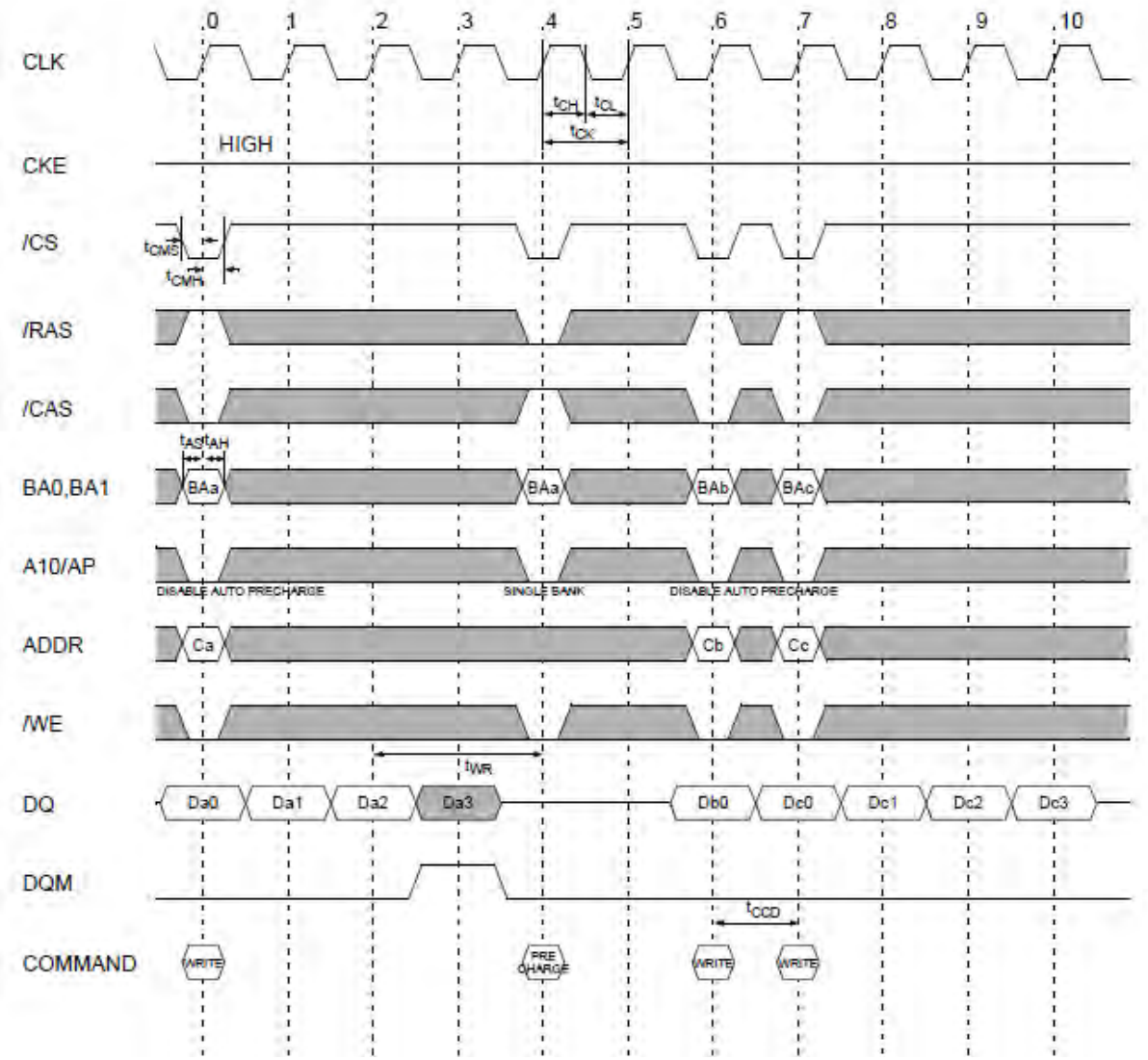
8.9 READ Interrupted by READ (@ BL=4, CL=2)



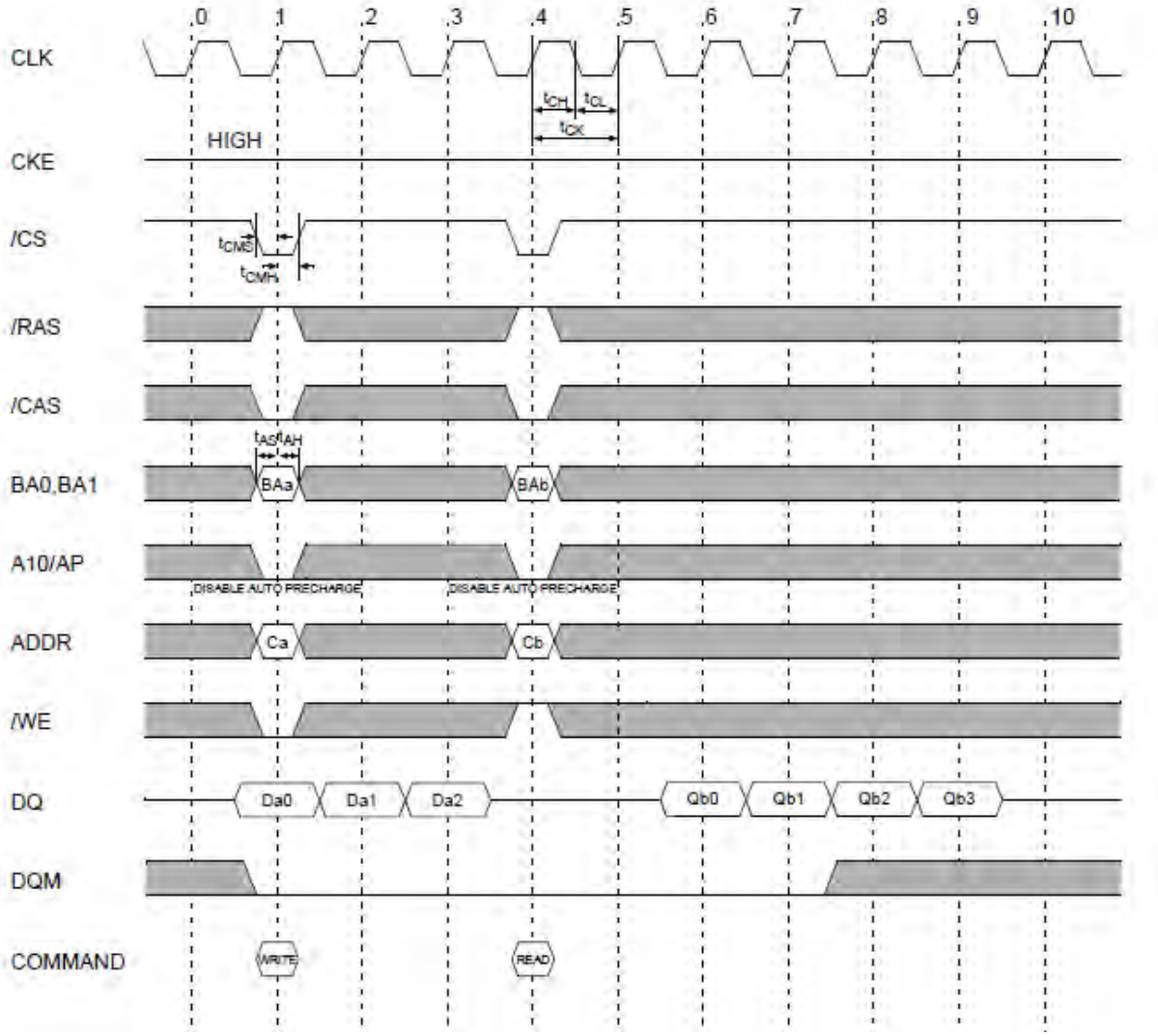
8.10 WRITE followed by Precharge (@ BL=4)



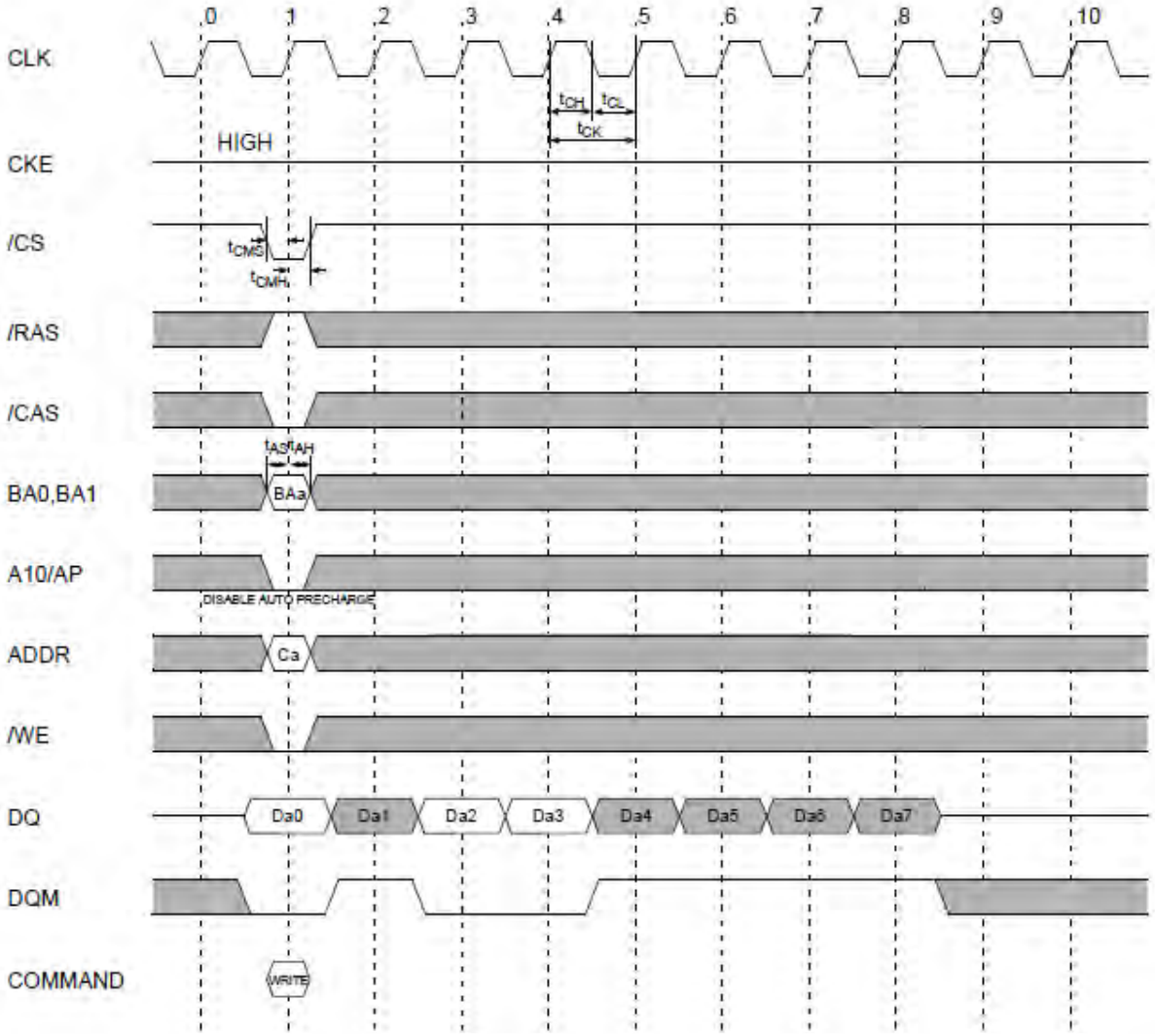
8.11 WRITE Interrupted by Precharge & DQM (@ BL=4)



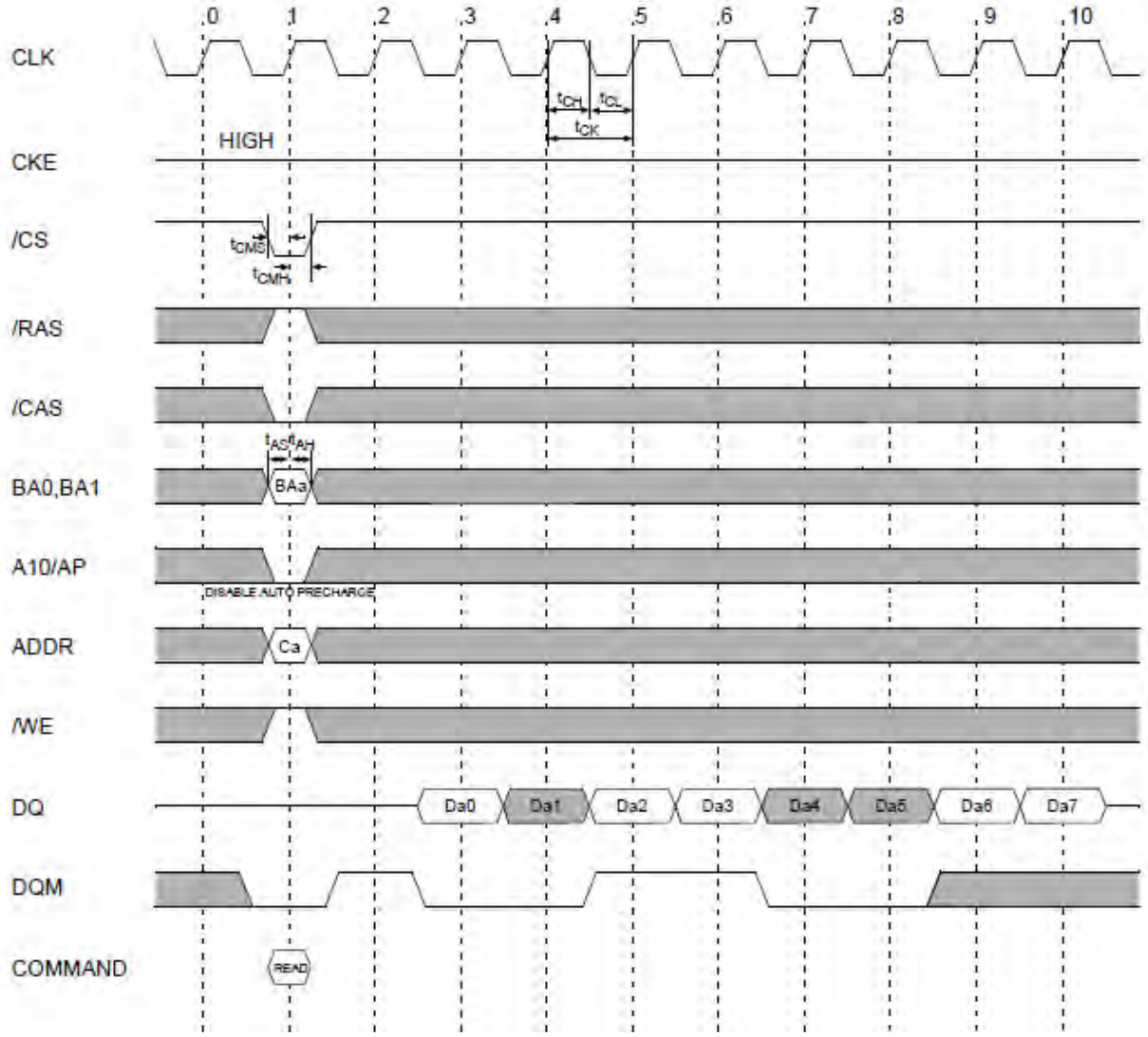
8.12 WRITE Interrupted by a READ (@ BL=4, CL=2)



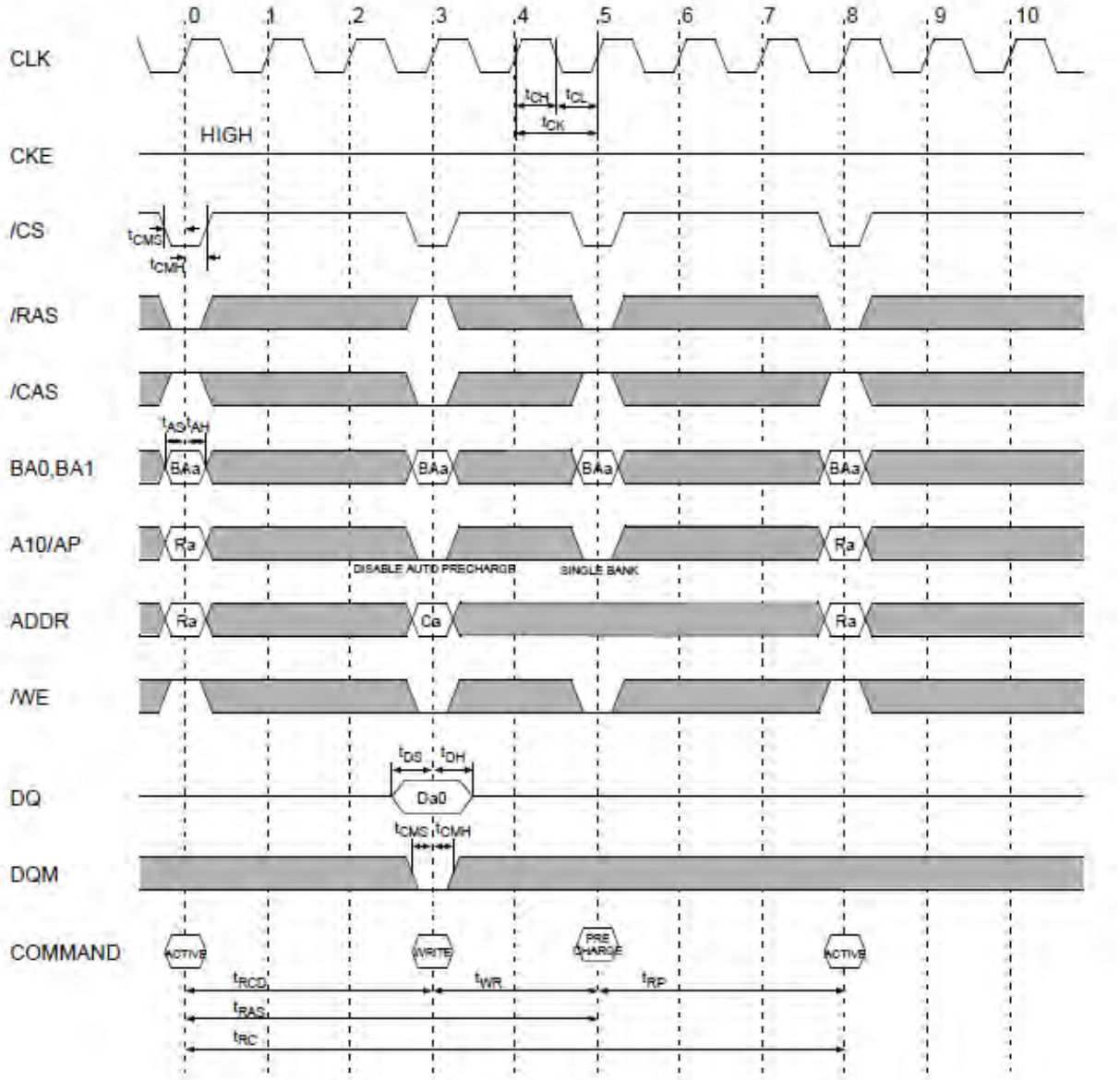
8.13 DQM Function (@BL=8) for WRITE



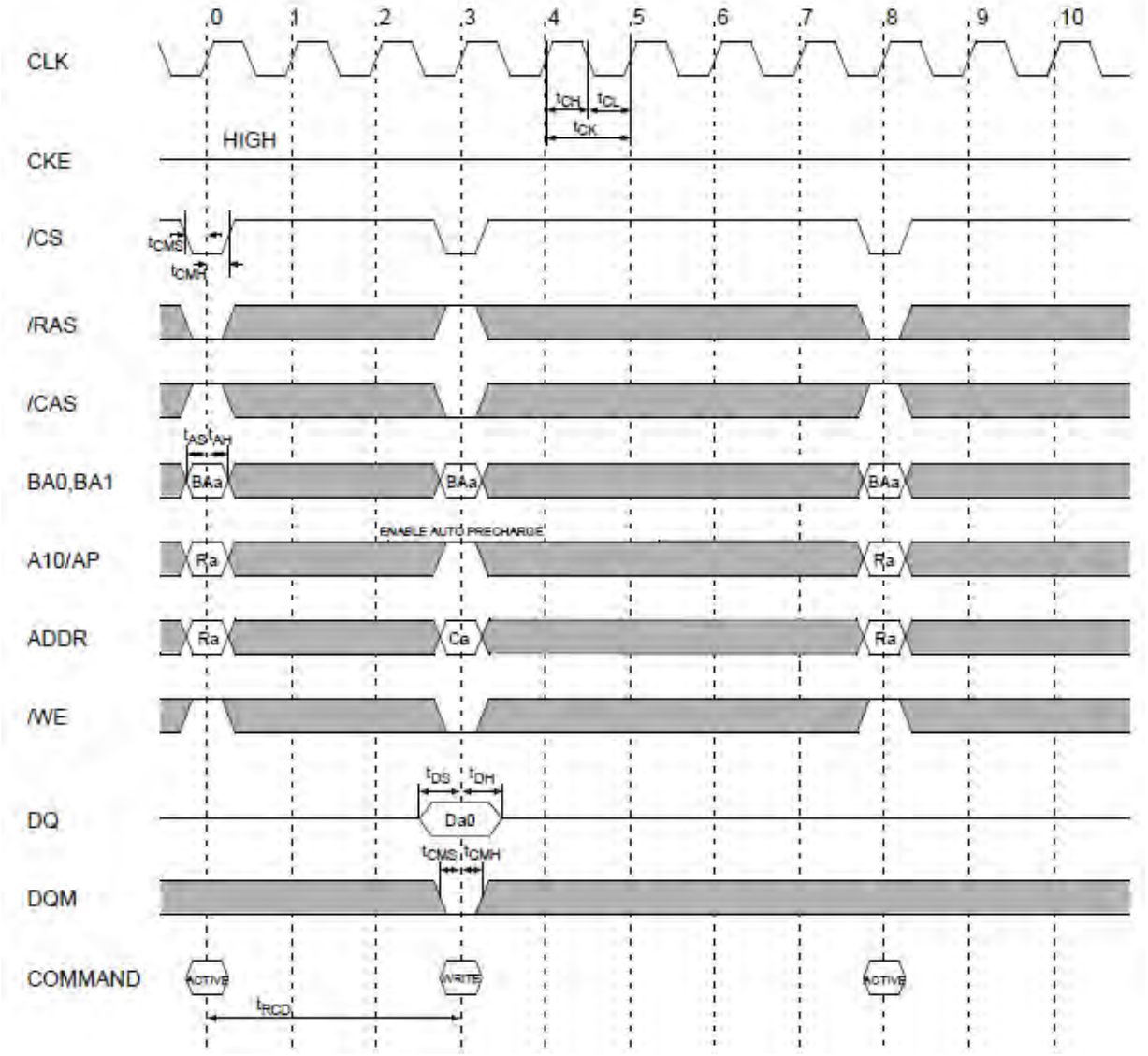
8.14 DQM Function (@BL=8, CL=2) for read



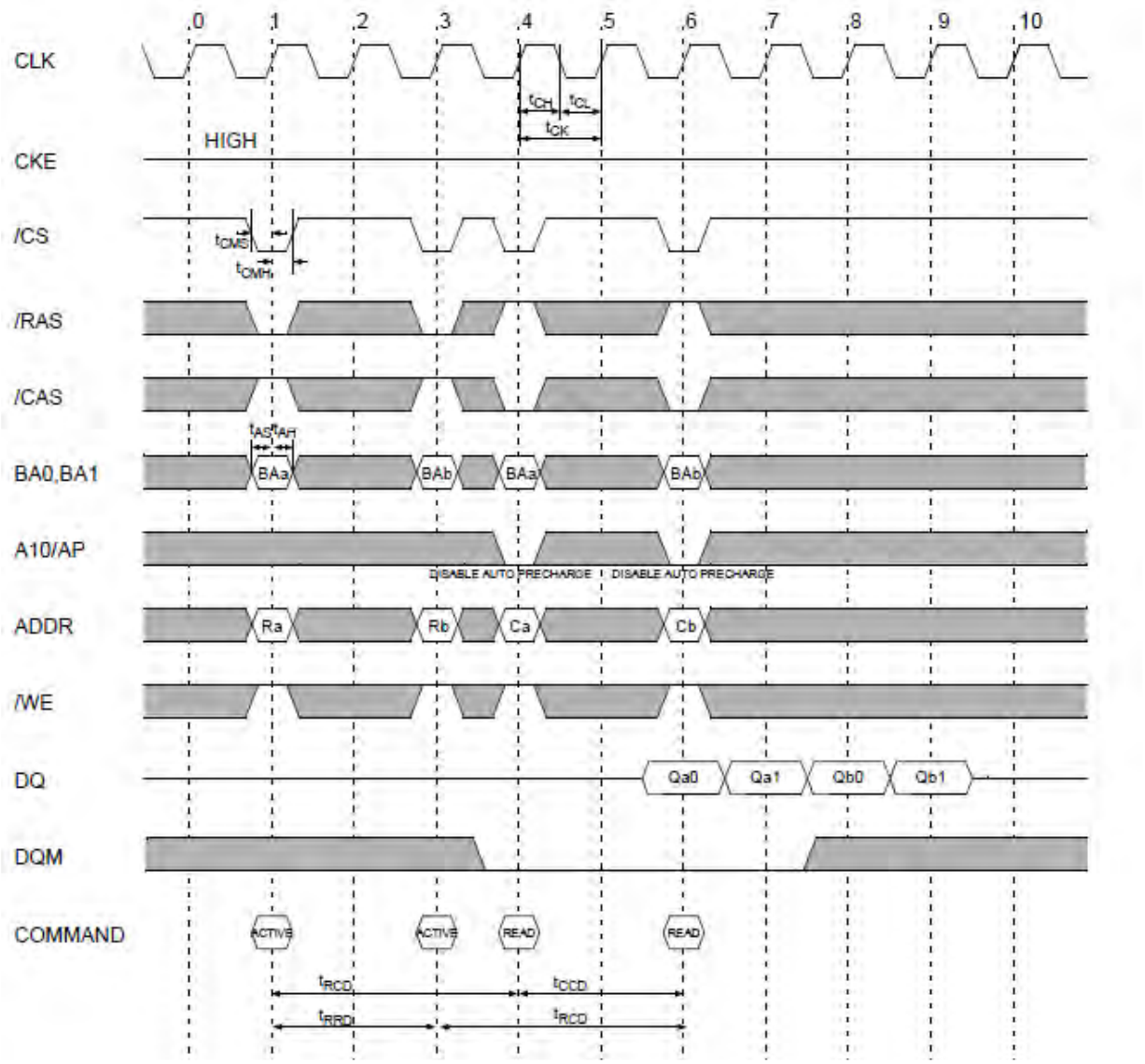
8.15 Single WRITE - Without Auto Precharge



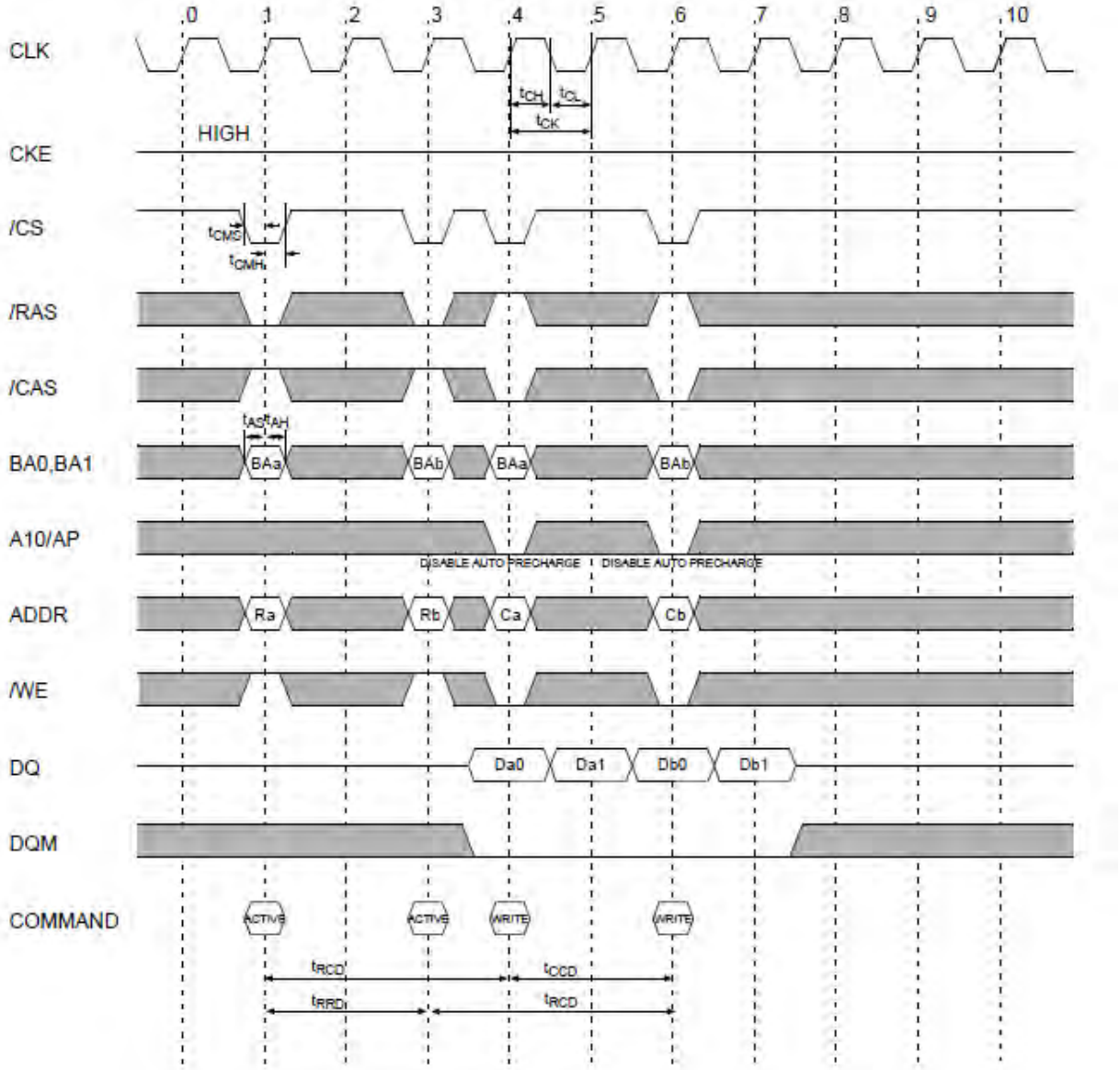
8.16 Single WRITE - With Auto Precharge



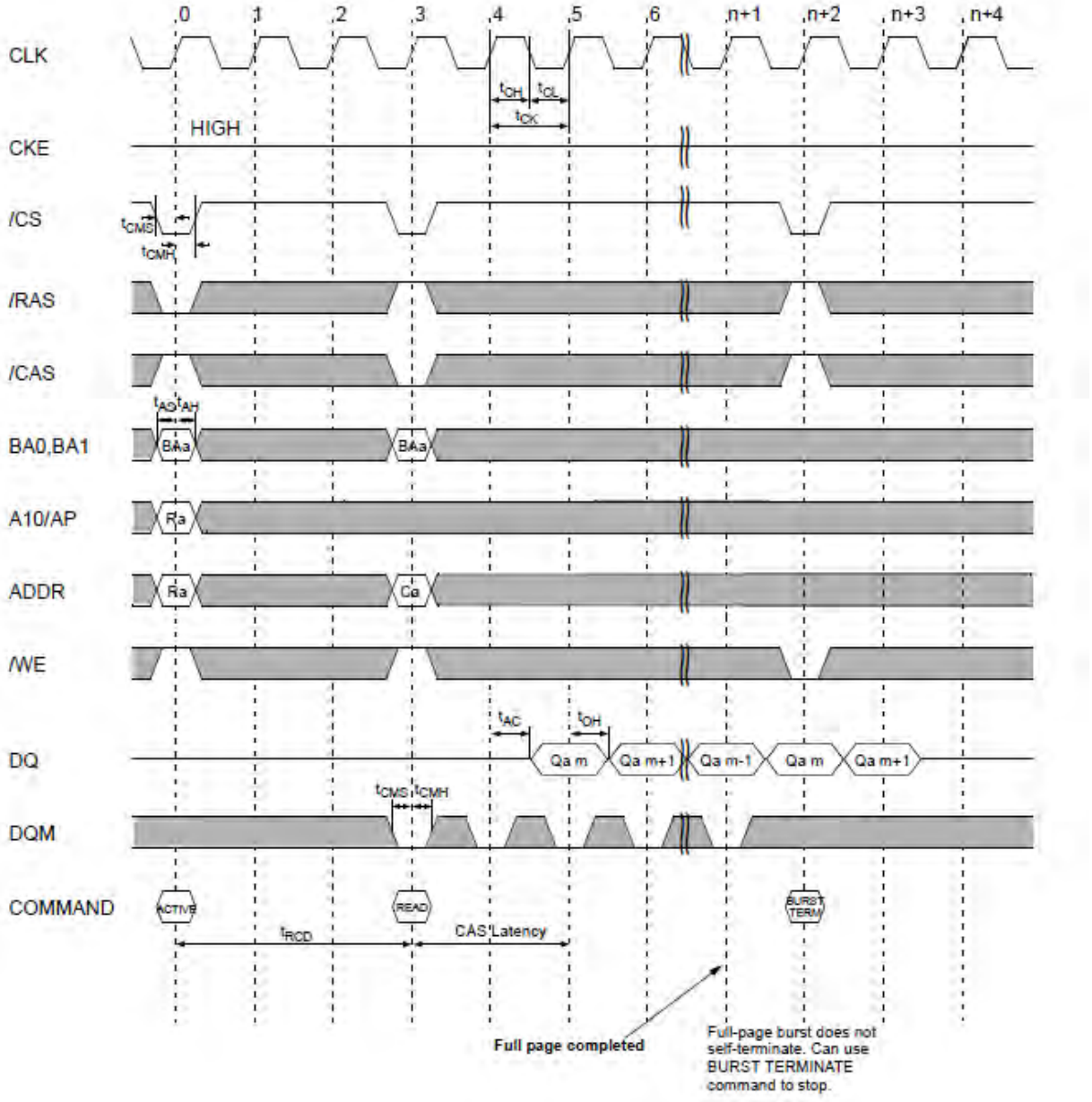
8.17 Multi Bank Interleaving READ (@ BL=2, CL=2)



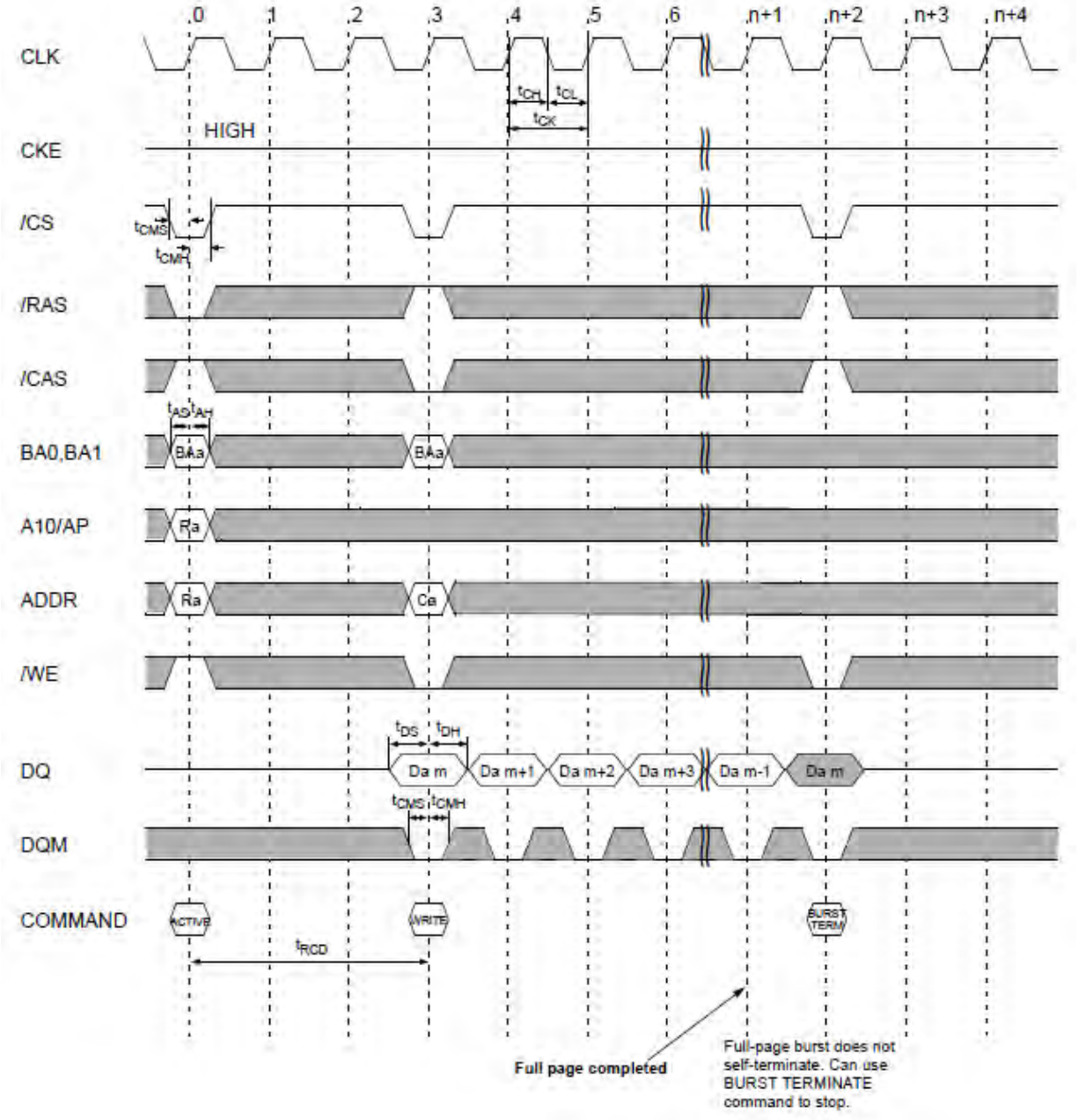
8.18 Multi Bank Interleaving WRITE (@ BL=2)



8.19 READ Full Page Burst



8.20 WRITE Full Page Burst



9. ELECTRICAL CHARACTERISTIC

9.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUES		UNITS
		MIN	MAX	
Voltage on VDD relative to VSS	VDD	−0.5	3.6	V
Voltage on VDDQ relative to VSS	VDDQ	−0.5	3.6	V
Voltage on any pin relative to VSS	VIN, VOUT	−0.5	3.6	V
Operating temperature :	Tj	-40	85	℃
Storage Temperature	TSTG	−55	150	℃
Short Circuit Output Current	IOUT		±50	mA
Power Dissipation	PD		1.0	W

NOTE :
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

9.2 DC Operating Conditions

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = -40°C~ 85°C for Industrial)

PARAMETER	SYMBOL	MIN	Typ	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	1.7	1.8	1.95	V	1
	V_{DDQ}	1.7	1.8	1.95	V	1
Input logic high voltage	V_{IH}	0.8 x V_{DDQ}	1.8	V_{DDQ} + 0.3	V	2
Input logic low voltage	V_{IL}	-0.3	0	0.2 x V_{DDQ}	V	3
Output logic high voltage	VOH	0.9 x V_{DDQ}	-	-	V	I_{OH} = -0.1mA
Output logic low voltage	VOL	-	-	0.1 x V_{DDQ}	V	I_{OL} = 0.1mA
Input leakage current	ILI	-2	-	2	uA	4

NOTE :
1. Under all conditions, VDDQ must be less than or equal to VDD.
2. VIH (max) = 3.0V AC. The overshoot voltage duration is ≤ 3ns.
3. VIL (min) = -1.0V AC. The undershoot voltage duration is ≤ 3ns.
4. Any input 0V ≤ VIN ≤ VDDQ
   Input leakage currents include Hi-Z output leakage for all bi-directional buffers with tri-state outputs.
5. Dout is disabled, 0V ≤ VOUT ≤ VDDQ.

9.3 Capacitance

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
CLK	C_{CLK}	1.5	3.5	pF	
/RAS,/CAS,/WE,/CS,CKE,DQM	C_{IN}	1.5	3.0	pF	
Address	C_{ADD}	1.5	3.0	pF	
DQ0~DQ15	C_{OUT}	2.0	4.5	pF	

9.4 IDD Specification Parameters and Test Conditions

[Recommended Operating Conditions; Notes 1-2]

(256Mb, X16)

PARAMETER	SYMBOL	TEST CONDITION		- 6	UNIT
Operating Current	IDD1	Active Mode; Burst = 2; Read or Write ; tRC ≥ tRCmin ; CAS Latency = 3		40	mA
Precharge power-down standby current	IDD2P	all banks idle, CKE is LOW; /CS is HIGH, tCK = tCKmin ; address and control inputs are SWITCHING; data bus inputs are STABLE		250	uA
Precharge non power-down standby current	IDD2N	all banks idle, CKE is HIGH; /CS is HIGH, tCK = tCKmin; address and control inputs are SWITCHING; data bus inputs are STABLE		10	mA
Active power-down standby current	IDD3P	one bank active, CKE is LOW; /CS is HIGH, tCK = tCKmin;address and control inputs are SWITCHING; data bus inputs are STABLE		2	mA
Active non power-down standby current	IDD3N	one bank active, CKE is HIGH; /CS is HIGH, tCK = tCKmin; address and control inputs are SWITCHING; data bus inputs are STABLE		15	mA
Operating Current	IDD4	Burst Mode : Continuous Burst ; Read or Write : All banks Active, CAS Latency = 3		70	mA
Auto-Refresh Current	IDD5	tRC = tRFCmin ; tCK = tCKmin ; burst refresh; CKE is HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE		50	mA
Self Refresh Current	IDD6	CKE ≤ 0.2v (85°C)	Full Array	450	uA
			1/2 of Full Array	400	
			1/4 of Full Array	350	
Deep Power-Down current	IDD7	Address and control inputs are STABLE; data bus inputs are STABLE		10	uA

NOTE :

1. IDD specifications are tested after the device is properly initialized.
2. Input slew rate is 1V/ns.

9.5 Electrical Characteristics

All values are recommended operating conditions unless otherwise noted.

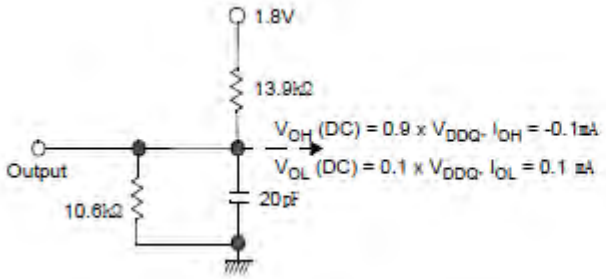
9.5.1 AC Operating Test Conditions

(VDD = 1.7V ~ 1.95V, TA = -40℃ ~ 85℃ for Industrial)

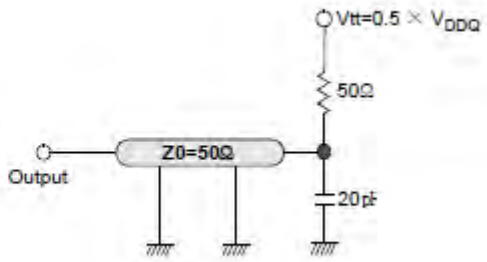
PARAMETER	MAX	UNITS	NOTES
AC input levels(Vih/Vil)	0.8 x V_{DDQ} /0.2 x V_{DDQ}	V	
Input timing measurement reference level	0.5 × V_{DDQ}	V	
Input rise and fall time	1.0	V/ns	
Output timing measurement reference level	0.5 × V_{DDQ}	V	
Output load condition	AC Output Load Circuit		

Notes:

1. Under all conditions, VDDQ must be less than or equal to VDD.
2. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation



DC Output Load Circuit



AC Output Load Circuit

9.5.2 AC Timings

[Recommended Operating Conditions: Notes 1-3]

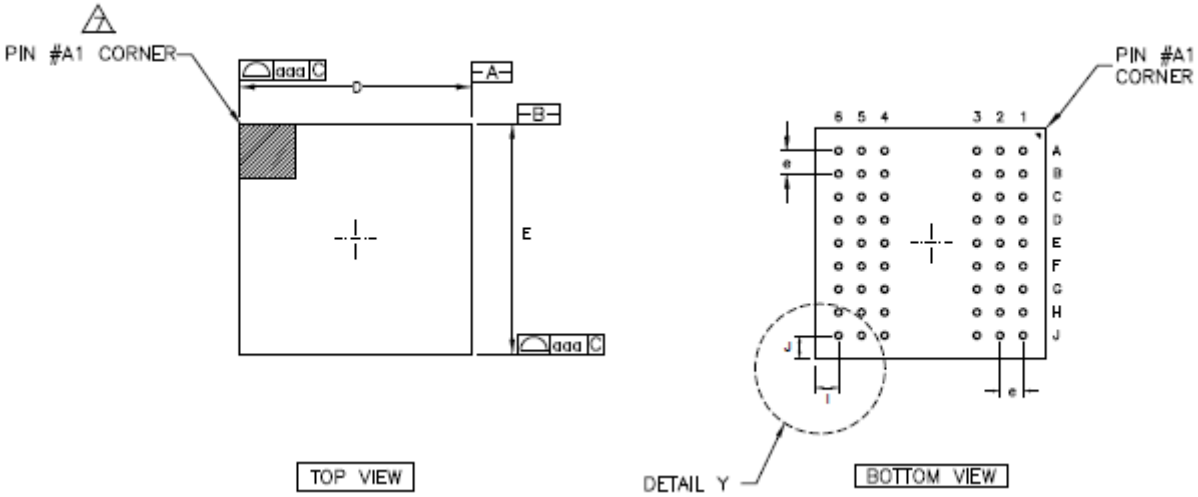
PARAMETER		SYMBOL	- 6		UNIT	NOTES
			MIN	MAX		
Ref/Active to Ref/Active Command Period		tRC	60		ns	
Active to precharge Command Period		tRAS	42	70,000	ns	
ACTIVE to READ or WRITE delay		tRCD	18		ns	
Read/Write(a) to Read/Write(b) Command Period		tCCD	1		tCK	
PRECHARGE command period		tRP	18		ns	
ACTIVE bank A to ACTIVE bank B delay		tRRD	12		ns	
WRITE recovery time		tWR	15		ns	
Internal write to Read command delay		tWTR	2		tCK	
Clock cycle time	CL=3	tCK	6	1000	ns	
	CL=2		12	1000	ns	
CLK High Level width		tCH	2.5		ns	
CLK Low Level width		tCL	2.5		ns	
Access Time from CLK	CL =3	tAC		5.5	ns	
	CL = 2			6	ns	
Output Data Hold Time		tOH	2.5		ns	
Output Data High impedance time	CL=3	tHZ		5.5	ns	
	CL=2			6		
Output Data Low Impedance Time		tLZ	1		ns	
Power Down Mode Entry Time		tSB	0	6	ns	
Transition Time of CLK(Rise and Fall)		tT	0.3	1.2	ns	
Data-in Set-up Time		tDS	1.5		ns	
Data-in Hold Time		tDH	1		ns	
Address Setup-Time		tAS	1.5		ns	
Address Hold Time		tAH	1		ns	
CKE Set-up Time		tCKS	1.5		ns	
ACTIVE bank A to ACTIVE bank B delay		tRRD	12		ns	
CKE Hold Time		tCKH	1		ns	
Command Set-up Time		tCMS	1.5		ns	
Command Hold Time		tCMH	1		ns	
Refresh Time		tREF		64	ms	
Mode register Set Cycle Time		tMRD	2		tCK	
Ref to Ref/Active Command period		tRFC	72		ns	
Self Refresh exit to next valid command delay		tXSR	80		ns	

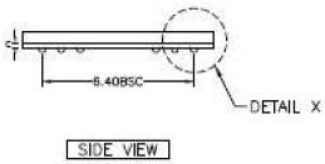
NOTE:

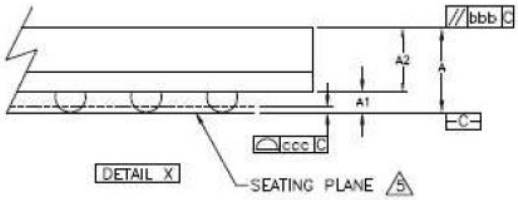
1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. t_{AC}(max) value is measured at the low Vdd(1.7V) and hot temperature(85°C).
   t_{AC} is measured in the device with full driver strength and under the AC output load condition.

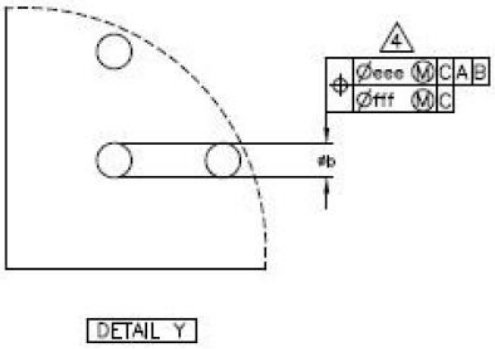
10. PACKAGE DIMENSION

54Ball Fine Pitch BGA (0.8mm ball pitch)









SYMBOL	MIN.	NOM.	MAX.
A	0.81	0.91	1.01
A1	0.20	0.25	0.30
A2	0.61	0.66	0.71
D	7.90	8.00	8.10
E	7.90	8.00	8.10
I	0.80 REF.		
J	0.80 REF.		
M	6X9 <DEPOPULATED>		
aaa			0.10
ccc			0.10
bbb			0.08
eee			0.15
fff			0.05
b	0.30	0.35	0.40
e	0.80 TYP.		
c	0.21 REF.		

PART NUMBERING SYSTEM

AS4C	16M16MSB	-6	B	I	N	XX
DRAM	16M16=16Mx16 MS=Mobile SDRAM B=B Die Rev.	-6=166MHz	B = FBGA	I=Industrial (-40° C~+85° C)	Indicates Pb and Halogen Free	Packing Type None:Tray TR:Reel

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