Lead-free Green

DGD05062

HIGH FREQUENCY HALF-BRIDGE GATE DRIVER WITH PROGRAMMABLE DEADTIME IN W-DFN3030-10

Description

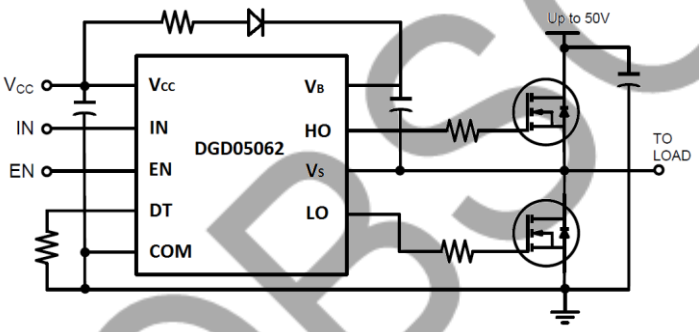
The DGD05062 is a high-frequency half-bridge gate driver capable of driving N-channel MOSFETs in a half-bridge configuration. The floating high-side driver is rated up to 50V.

The DGD05062 logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with MCUs. UVLO for high-side and low-side will protect a MOSFET with loss of supply. To protect MOSFETs, cross conduction prevention logic prevents the HO and LO outputs being on at the same time.

Fast and well-matched propagation delays allow a higher switching frequency, enabling a smaller, more compact power switching design using smaller associated components. The DGD05062 is offered in the W-DFN3030-10 package and operates over an extended -40°C to +125°C temperature range.

Applications

- DC-DC Converters
- Motor Controls
- Battery Powered Hand Tools
- eCig Devices
- Class D Power Amplifiers



Typical Configuration

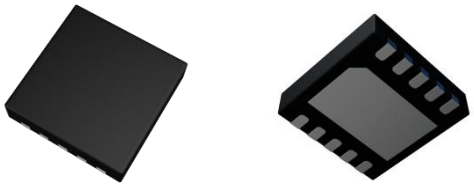
Features

- 50V Floating High-side Driver
- Drives Two N-channel MOSFETs in a Half-bridge Configuration
- 1.25A Source / 2.0A Sink Output Current Capability
- Undervoltage Lockout for High-side and Low-side Drivers
- Programmable Deadtime to Protect MOSFETs
- Logic Input (IN and EN) 3.3V Capability
- Ultra Low Standby Currents (<1µA)
- Extended Temperature Range: -40°C to +125°C
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.**
  https://www.diodes.com/quality/product-definitions/

Mechanical Data

- Case: W-DFN3030-10 (Type TH)
- Case Material: Molded Plastic. "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 3 per J-STD-020
- Terminals: Finish – Matte Tin Finish. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.017 grams (Approximate)

W-DFN3030-10



Top View | Bottom View

Ordering Information (Note 4)

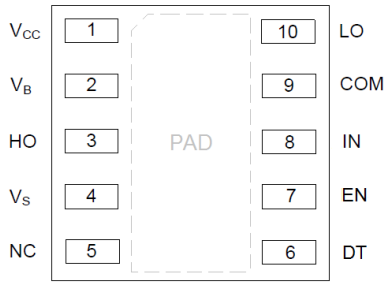
Part Number	Marking Code	Reel Size (inches)	Tape Width (mm)	Quantity per Reel
DGD05062FN-7	DGD05062	7	8	3,000

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

DGD05062 = Product Type Marking Code
YY = Year (ex: 21 = 2021)
WW = Week (01 to 53)

Pin Diagrams

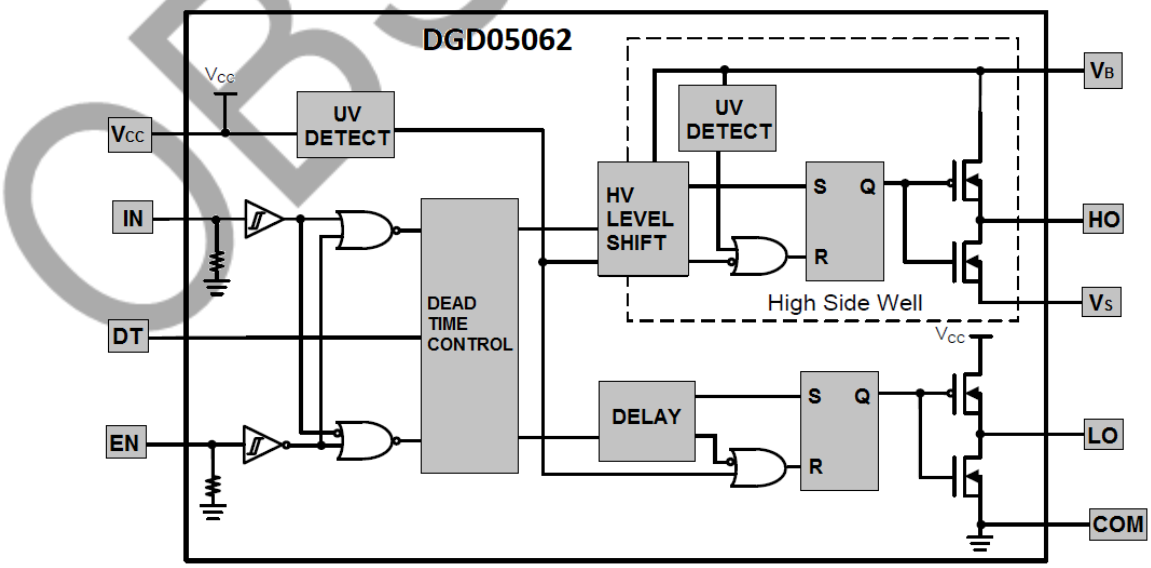


Top View: W-DFN3030-10

Pin Descriptions

Pin Number	Pin Name	Function
1	V_{CC}	Low-Side and Logic Supply
2	V_B	High-Side Floating Supply
3	HO	High-Side Gate Drive Output
4	V_S	High-Side Floating Supply Return
5	NC	No connection (No Internal Connection)
6	DT	Deadtime Control
7	EN	Logic Input Enable, a Logic Low turns off Gate Driver
8	IN	Logic Input for High-Side and Low-Side Gate Driver Outputs (HO and LO), in Phase with HO
9	COM	Low-Side and Logic Return
10	LO	Low-Side Gate Drive Output
PAD	Substrate	Connect to COM on PCB

Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
High-Side Floating Positive Supply Voltage	V_B	-0.3 to +50	V
High-Side Floating Negative Supply Voltage	V_S	V_B-14 to V_B+0.3	V
High-Side Floating Output Voltage	V_{HO}	V_S-0.3 to V_B+0.3	V
Offset Supply Voltage Transient	dV_S / dt	50	V/ns
Logic and Low-Side Fixed Supply Voltage	V_{CC}	-0.3 to +15	V
Low-Side Output Voltage	V_{LO}	-0.3 to V_{CC}+0.3	V
Logic Input Voltage (IN and EN)	V_{IN}	-0.3 to +15	V

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Power Dissipation Linear Derating Factor (Note 5)	P_D	0.4	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	64	°C/W
Thermal Resistance, Junction to Case (Note 5)	$R_{\theta JC}$	42	°C/W
Operating Temperature	T_J	+150	°C
Lead Temperature (Soldering, 10s)	T_L	+300	
Storage Temperature Range	T_{STG}	-55 to +150	

Note: 5. When mounted on a standard JEDEC 2-layer FR-4 board.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
High-Side Floating Supply	V_B	V_S + 8	V_S + 14	V
High-Side Floating Supply Offset Voltage	V_S	(Note 6)	50 (Note 7)	V
High-Side Floating Output Voltage	V_{HO}	V_S	V_B	V
Logic and Low Side Fixed Supply Voltage	V_{CC}	8	14	V
Low-Side Output Voltage	V_{LO}	0	V_{CC}	V
Logic Input Voltage (IN and EN)	V_{IN}	0	5	V
Ambient Temperature	T_A	-40	+125	°C

Notes: 6. Logic operation for V_S of -5V to +50V. Logic state held for V_S of -5V to -V_{BS}.
7. Provided V_B doesn't exceed absolute maximum rating of 50V.

DC Electrical Characteristics (V_{CC} = V_{BS} = 12V, COM = V_S = 0V, @T_A = +25°C, unless otherwise specified.) (Note 8)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Logic "1" Input Voltage	V_{IH}	2.4	—	—	V	—
Logic "0" Input Voltage	V_{IL}	—	—	0.8	V	—
Enable Logic "1" Input Voltage	V_{ENIH}	1.5	—	—	V	—
Enable Logic "0" Input Voltage	V_{ENIL}	—	—	0.7	V	—
Input Voltage Hysteresis	V_{INHYS}	—	0.6	—	V	—
High Level Output Voltage, V_{BIAS} - V_O	V_{OH}	—	0.45	0.6	V	I_{O+} = 100mA
Low Level Output Voltage, V_O	V_{OL}	—	0.15	0.22	V	I_{O-} = 100mA
Offset Supply Leakage Current	I_{LK}	—	10	50	µA	V_B = V_S = 50V
V_{CC} Shutdown Supply Current	I_{CCSD}	—	0	1	µA	V_{IN} = 0V or 5V, V_{EN} = 0V
V_{CC} Quiescent Supply Current	I_{CCQ}	—	0.32	0.5	mA	V_{IN} = 0V or 5V, R_{DT} = 100kΩ
V_{CC} Operating Supply Current	I_{CCOP}	—	2.1	—	mA	fs = 500kHz
V_{BS} Quiescent Supply Current	I_{BSQ}	—	62	100	µA	V_{IN} = 0V or 5V
V_{BS} Operating Supply Current	I_{BSOP}	—	1.1	—	mA	f_s = 500kHz
Logic "1" Input Bias Current	I_{IN+}	—	25	60	µA	V_{IN} = 5V
Logic "0" Input Bias Current	I_{IN-}	—	0	1	µA	V_{IN} = 0V
V_{BS} Supply Undervoltage Positive Going Threshold	V_{BSUV+}	5.9	6.9	7.9	V	—
V_{BS} Supply Undervoltage Negative Going Threshold	V_{BSUV-}	5.6	6.6	7.6	V	—
V_{CC} Supply Undervoltage Positive Going Threshold	V_{CCUV+}	5.9	6.9	7.9	V	—
V_{CC} Supply Undervoltage Negative Going Threshold	V_{CCUV-}	5.6	6.6	7.6	V	—
Output High Short Circuit Pulsed Current	I_{O+}	0.9	1.25	—	A	V_O = 0V, PW ≤ 10µs
Output Low Short Circuit Pulsed Current	I_{O-}	1.5	2.0	—	A	V_O = 15V, PW ≤ 10µs

Note: 8. The V_{IN} and I_{IN} parameters are applicable to the two logic pins: IN and EN. The V_O and I_O parameters are applicable to the respective output pins: HO and LO.

AC Electrical Characteristics (V_{CC} = V_{BS} = 12V, COM = V_S = 0V, C_L = 1000pF, @T_A = +25°C, unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Turn-on Propagation Delay, HO & LO	t_{ON}	65	96	125	ns	R_{DT} = 10kΩ
		350	463	580	ns	R_{DT} = 100kΩ
Turn-off Propagation Delay, HO & LO	t_{OFF}	—	22	56	ns	—
Turn-on Rise Time	t_R	—	17	35	ns	—
Turn-off Fall Time	t_F	—	12	25	ns	—
Delay Matching	t_{DM}	—	—	50	ns	—
Deadtime: $t_{DT\ LO-HO}$ & $t_{DT\ HO-LO}$	t_{DT}	40	70	100	ns	R_{DT} = 10kΩ
		300	430	560	ns	R_{DT} = 100kΩ
Deadtime Matching	t_{MDT}	—	—	50	ns	R_{DT} = 100kΩ

Timing Waveforms

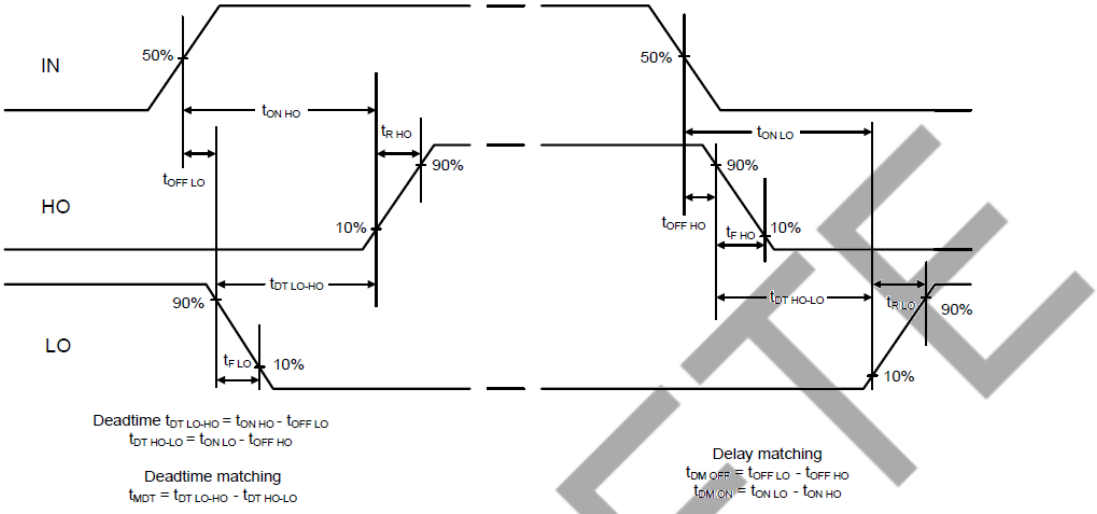


Figure 1. Switching Time Waveform Definitions

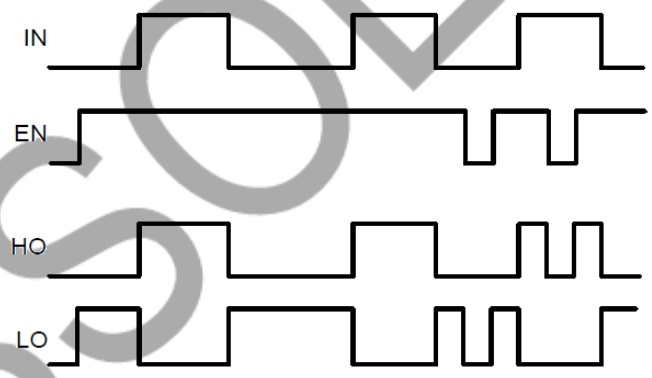
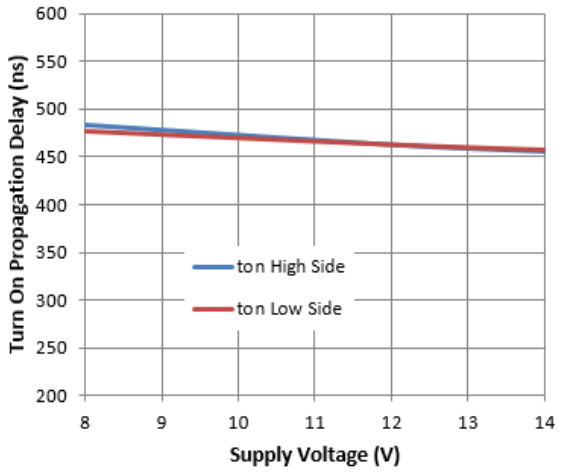
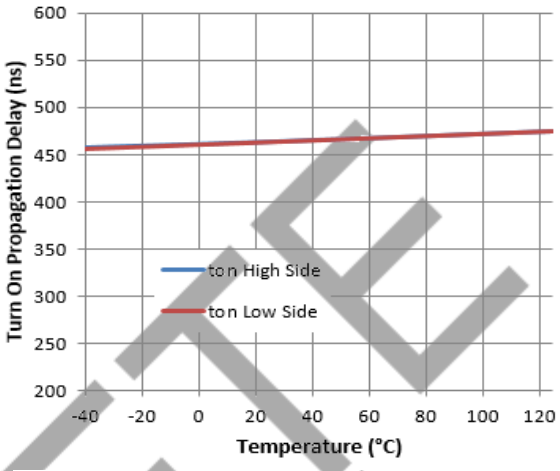


Figure 2. Input / Output Timing Diagram

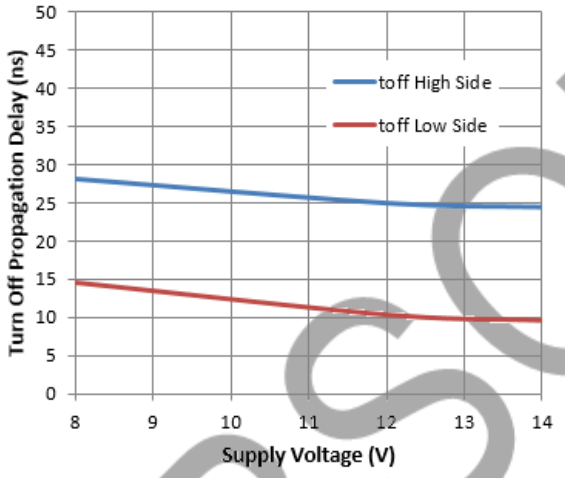
Typical Performance Characteristics (@T_A = +25°C, unless otherwise specified.)



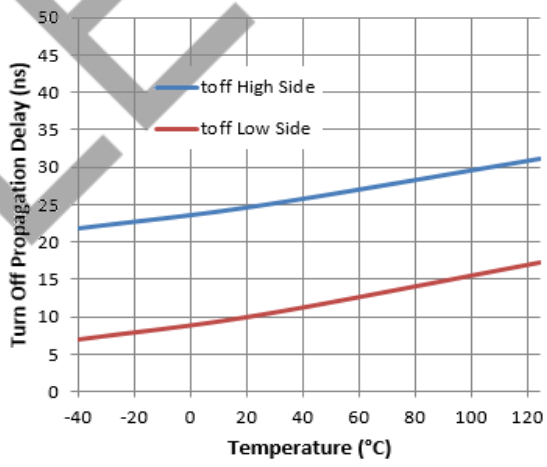
Turn-on Propagation Delay vs. Supply Voltage



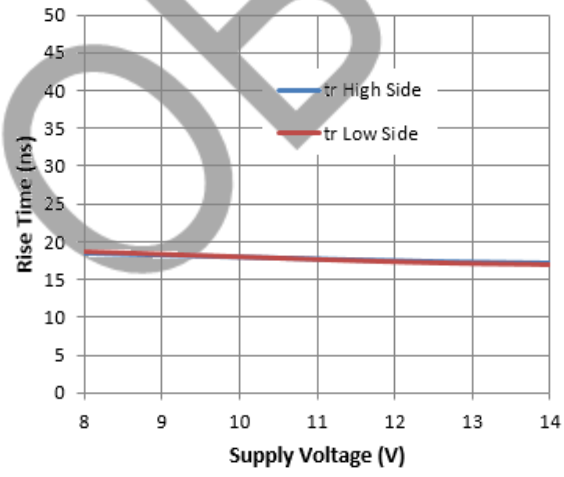
Turn-on Propagation Delay vs. Temperature



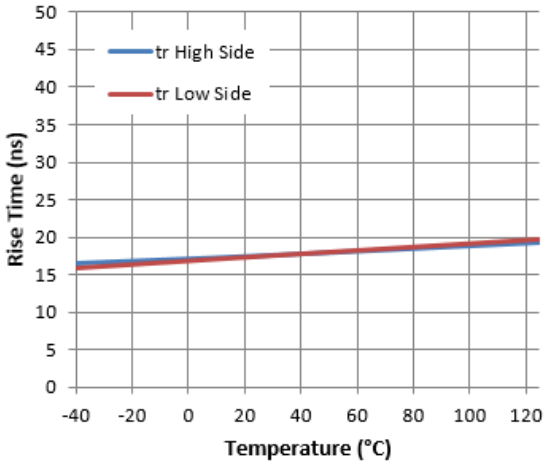
Turn-off Propagation Delay vs. Supply Voltage



Turn-off Propagation Delay vs. Temperature

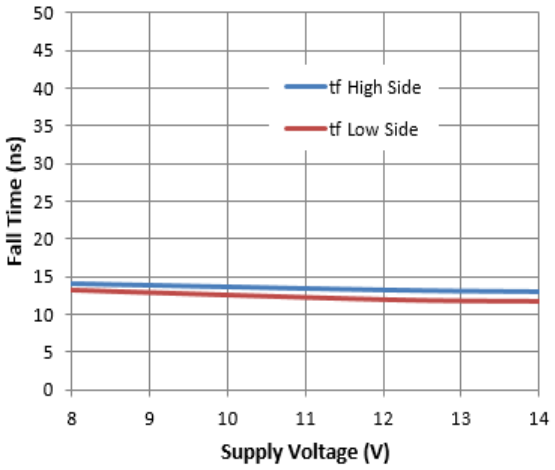


Rise Time vs. Supply Voltage

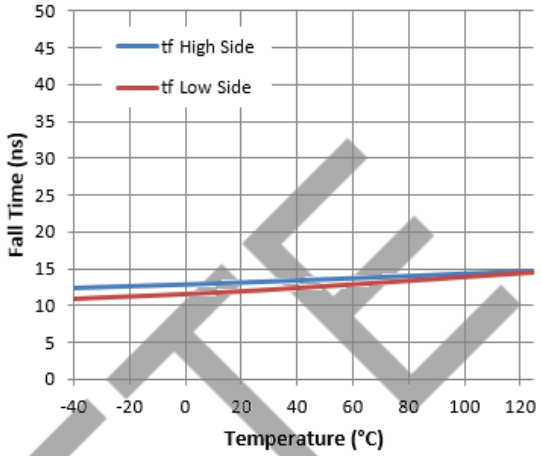


Rise Time vs. Temperature

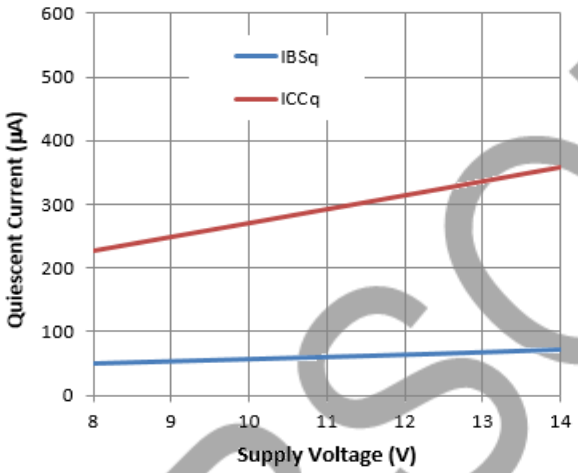
Typical Performance Characteristics (continued)



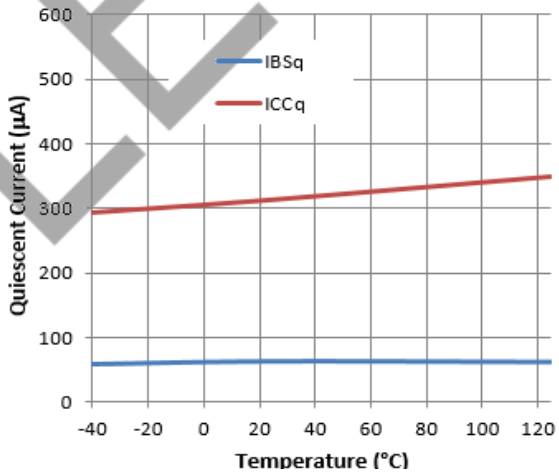
Fall Time vs. Supply Voltage



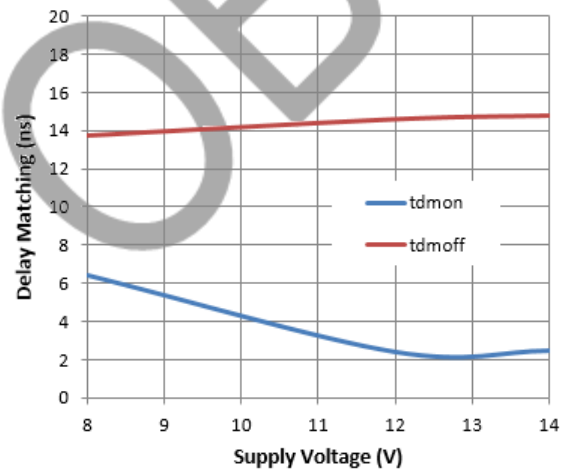
Fall Time vs. Temperature



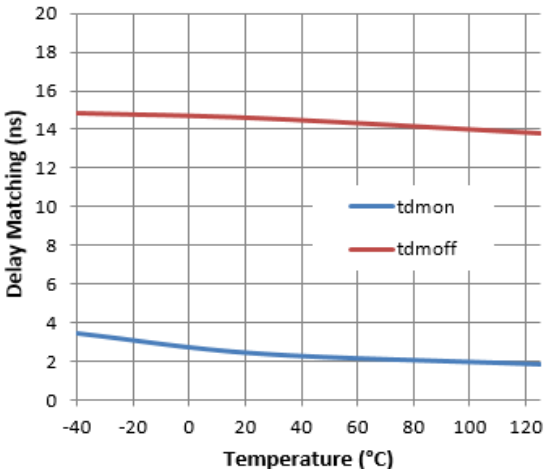
Quiescent Current vs. Supply Voltage



Quiescent Current vs. Temperature

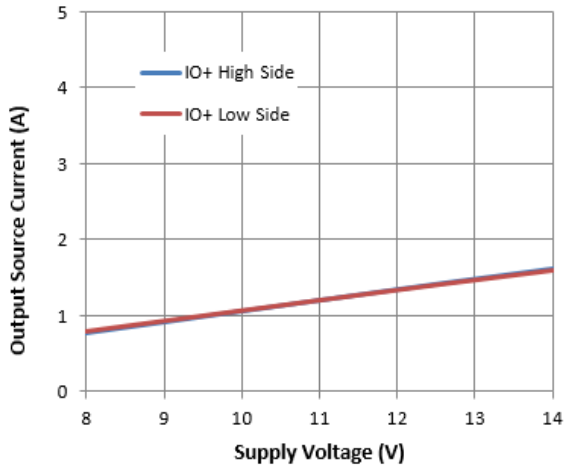


Delay Matching vs. Supply Voltage

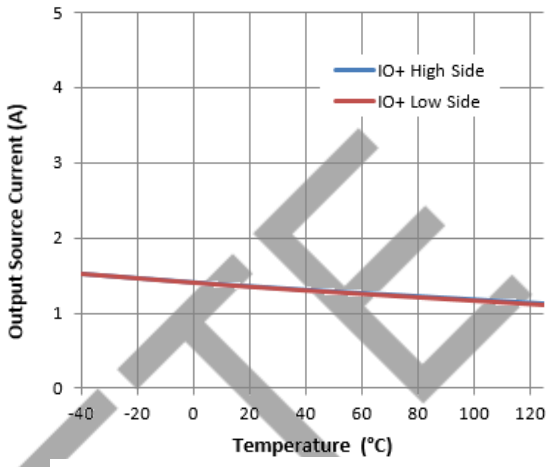


Delay Matching vs. Temperature

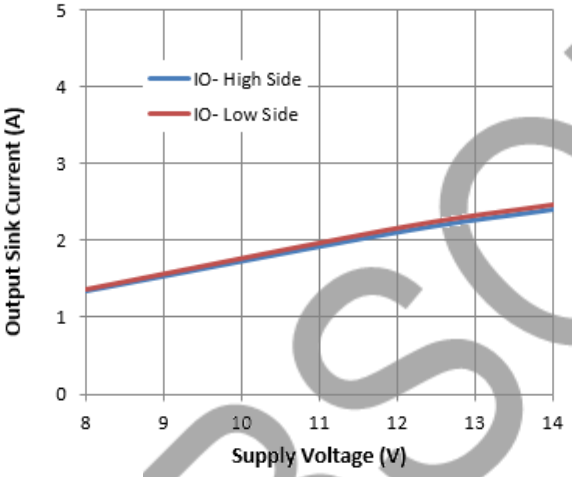
Typical Performance Characteristics (continued)



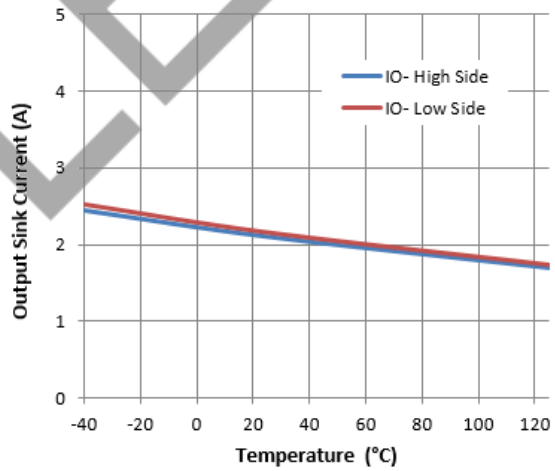
Output Source Current vs. Supply Voltage



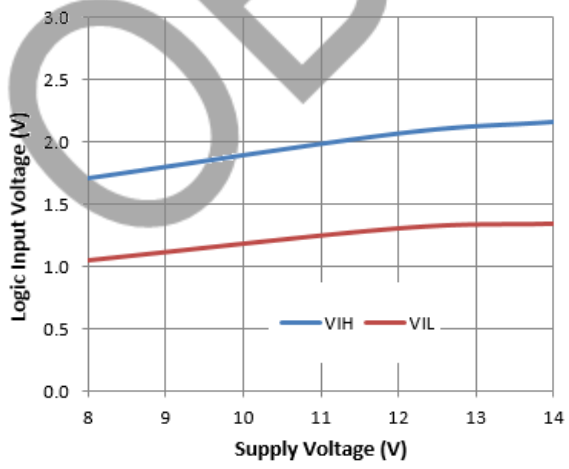
Output Source Current vs. Temperature



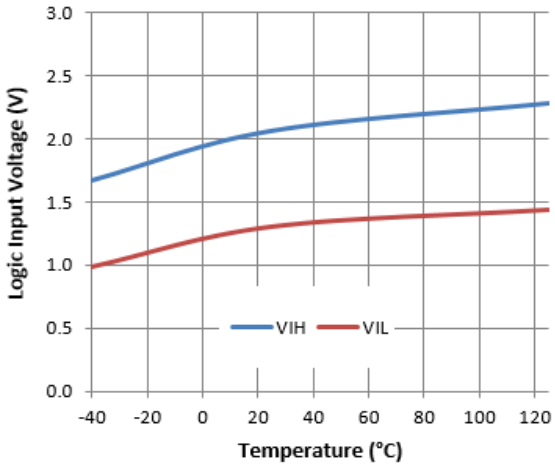
Output Sink Current vs. Supply Voltage



Output Sink Current vs. Temperature

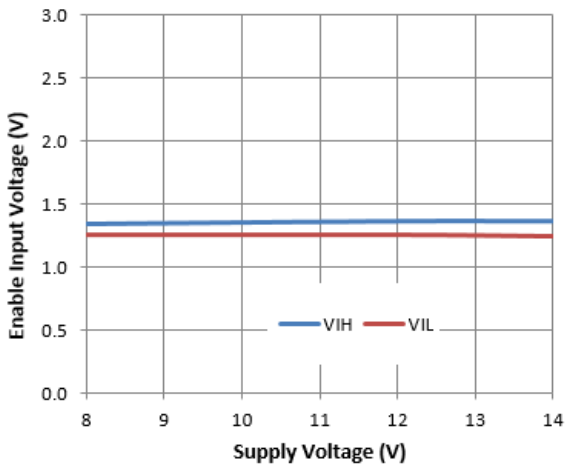


Logic Input Voltage vs. Supply Voltage

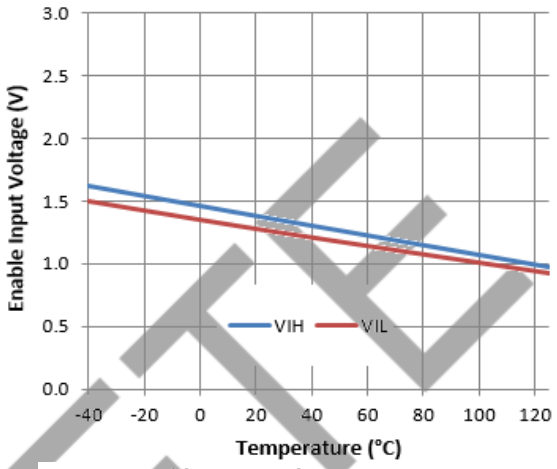


Logic Input Voltage vs. Temperature

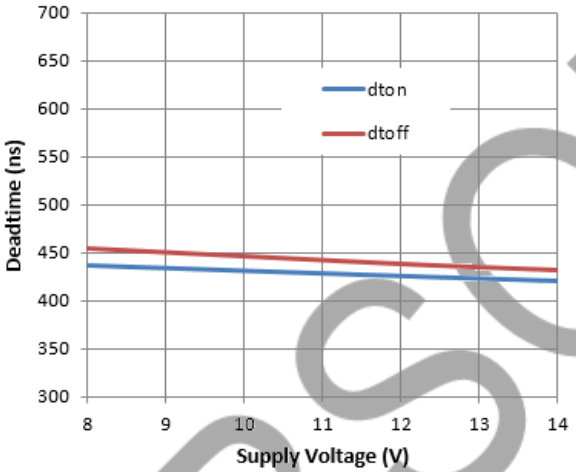
Typical Performance Characteristics (continued)



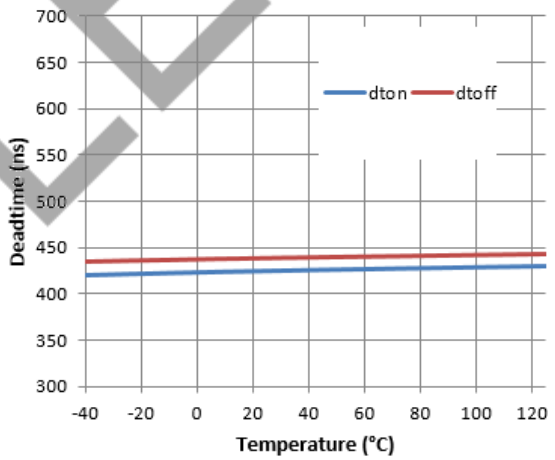
Enable Input Voltage vs. Supply Voltage



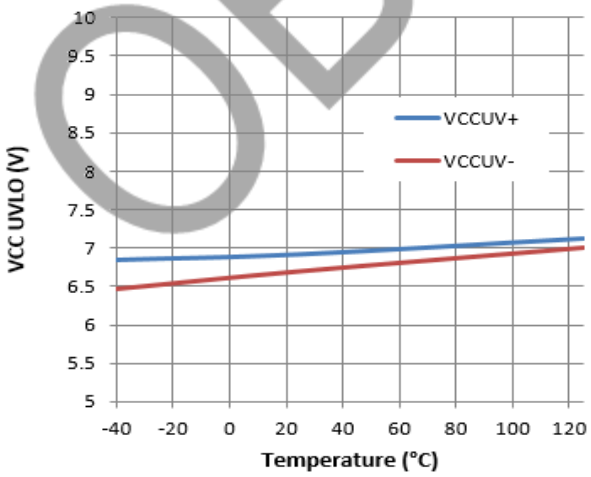
Enable Input Voltage vs. Temperature



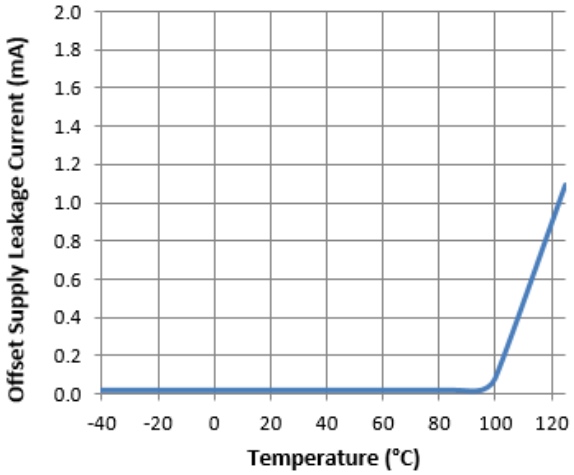
Deadtime vs. Supply Voltage



Deadtime vs. Temperature



VCC UVLO vs. Temperature



Offset Supply Leakage Current vs. Temperature

Application Information

Bootstrap Capacitor Selection

The capacitance of the bootstrap capacitor should be high enough to provide the charge required by the gate of the high side MOSFET with only a minimal loss of voltage across it. As a general guideline, it is recommened to make sure the charge stored by the bootstrap capacitor is about 50 times more than the required gate charge at operating V_{CC} (usually about 10V to 12V).

The formula to calculate the change in V_{BS} to provide a certain amount of gate charge is shown below;

Q = C * V where Q is the gate charge required by the external MOSFET to raise its gate voltage to 10V. C is the bootstrap capacitance and V is the voltage drop across the V_{BS}.

Example: To switch a high side MOSFET that requires 20nC of gate charge to raise its gate voltage to 10V, the capacitor size can be calculated as below;

$Q_{G(MOSFET)} = C_{(BOOTSTRAP)} * \Delta V_{BS}$;

ΔV_{BS} = voltage drop across the bootstrap capacitor while providing the required gate charge.

In this example, lets say the acceptable ΔV_{BS} is 200mV.

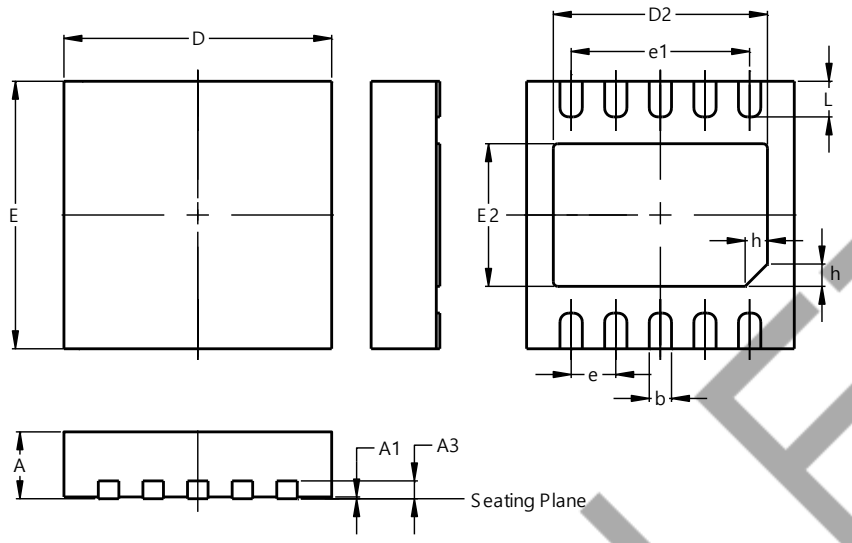
The required bootstrap capacitor for the job is;

$C_{(BOOTSTRAP)} = Q_{G(MOSFET)} / \Delta V_{BS} = 20nC/200mV = 100nF$

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-DFN3030-10 (Type TH)

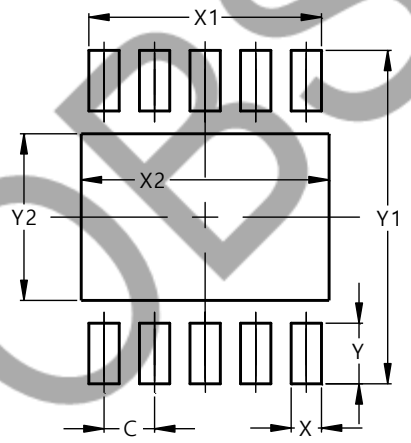


W-DFN3030-10 (Type TH)			
Dim	**Min**	**Max**	**Typ**
A	0.70	0.80	0.75
A1	--	0.05	0.02
A3	0.18	0.25	0.20
b	0.18	0.30	0.25
D	2.90	3.10	3.00
D2	2.40	2.60	2.50
e	0.50BSC		
e1	2.00BSC		
E	2.90	3.10	3.00
E2	1.45	1.65	1.55
h	0.20	0.30	0.25
L	0.30	0.50	0.40
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-DFN3030-10 (Type TH)



Dimensions	Value (in mm)
C	0.500
X	0.300
X1	2.300
X2	2.600
Y	0.600
Y1	3.300
Y2	1.650

Note : For high voltage applications, the appropriate industry sector guidelines should be considered with regards to creepage and clearance distances between device Terminals and PCB tracking.

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