Description

The AL58221 is a 12-channel (R/G/B x 4), constant-current, Adaptive Pulse Density Modulation (APDM) LED driver which operates over a 3V~5.5V input voltage range. The device provides 12 open-drain constant-current sinking outputs that are rated to 24V and delivers up to 60mA of high-accuracy current to each string of LED. Each channel's average output current can be individually programmable through a digital interface. The current at each output is set by three external current-setting resistors.

The AL58221 features a 10MHz double-edge trigger data clock input to reduce EMI. It offers a 2-wire serial interface to send grayscale data, control commands including 16/14/12/8-bit grayscale selection, grayscale clock frequency division selection, output polarity selection for high-power LED driving, output Trise and Tfall timing selection, current output waveform selection, and internal-latch function.

The device provides an adaptive pulse density modulation method to increase the visual refresh rate up to 1000 Hz @ 16-bit grayscale. It reduces flickers and provides output current bilateral processing for EMI reduction.

The AL58221 utilizes a clock duty recovery technique and pulse re-timing to support longer distance connection and multiple devices' cascading applications. It also provides typical ±1% channel-to-channel LED current accuracy. Additional features include a ±0.1% regulated output current capability and fast output transient response.

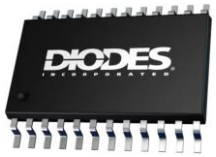
The AL58221 is available in the TSSOP-24EP (Type A1-B) package and is specified over the -40°C to +85°C ambient temperature range.

Features

- Input Voltage VDD: 3V to 5.5V
- Constant Current Output Range
  - 3~60mA@5V
  - 3~35mA@3.3V
- 12 Constant-Current Sink (R/G/B x 4) Output Channels
  - RGB Output Current setting by 3 external resistors
  - 24V Rated output channels for long LED strings
  - ±1% (typ.) LED Current accuracy between channels
  - ±2% (typ.) LED Current accuracy between devices
  - 16 / 14 / 12 / 8-bit grayscale selection
  - Grayscale clock source selection: internal or external
  - PWM or APDM control selection
  - Programmable Output Current Trise / Tfall time
  - Output Current Bilateral Processing for EMI reduction
- Diagnosis and Protections
  - Built-in internal grayscale clock supports refresh rate >1000Hz@16-bit grayscale, >256KHz@8-bit grayscale
  - Internal Grayscale clock frequency selection for High-Power LED driving application (min. 33.6KHz)
- 2-Wire Serial Interface (DI, DCKI)
  - 20Mbps (max.) ~ 140 Kbps(min.) data rate for EMI reduction data transfer
  - Cascaded capability (Max 1,030 devices)
  - Clock duty recovery for cascading applications
  - Schmitt trigger input
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1& 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

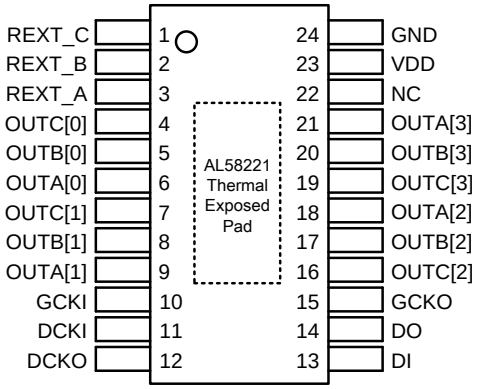
Pin Assignments

(3D Photo – Not to Scale)



(3D Step file available upon request)

(Top View – Not to Scale)



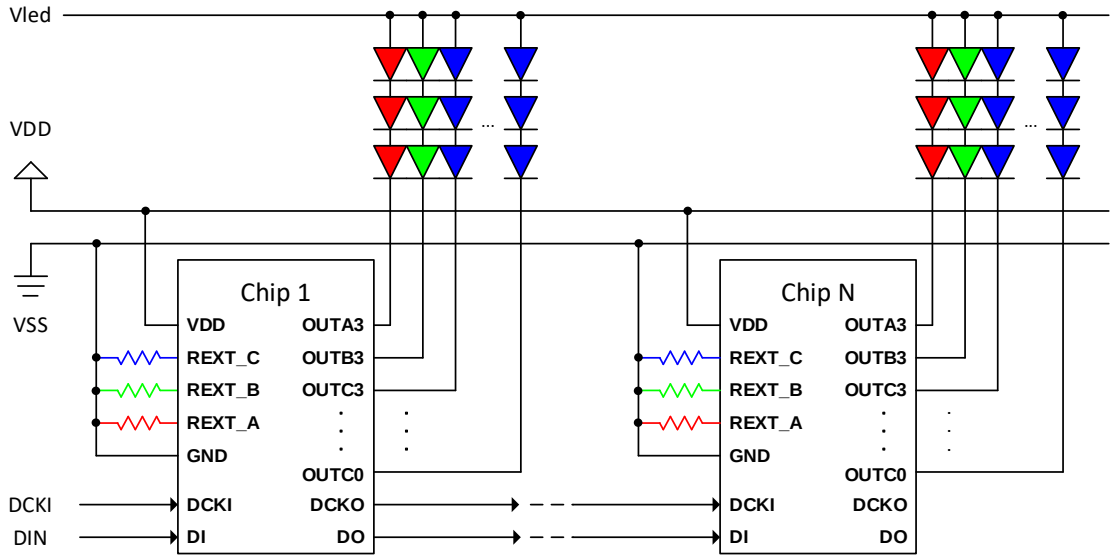
TSSOP-24EP (Type A1-B)

Applications

- Indoor and outdoor LED video displays
- Architectural and decorative lighting
- Digital signage and billboard applications
- LCD display backlighting
- Transportation signs

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit

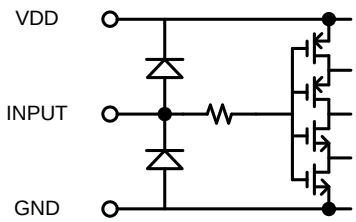


Pin Descriptions

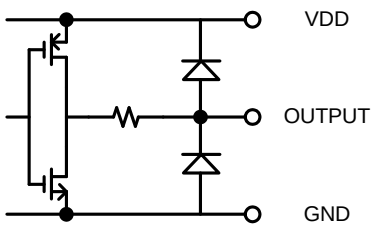
PIN NUMBER	PIN NAME	DESCRIPTION
1, 2, 3	REXT_C, REXT_B, REXT_A	External resistors connected between REXT and GND for individual output current value setting.
4, 7, 16,19	OUTC[0:3]	Constant current outputs
5, 8, 17, 20	OUTB[0:3]	
6, 9, 18, 21	OUTA[0:3]	
10	GCKI	External grayscale clock input for PWM/APDM operation.
11	DCKI	Clock input terminal for serial data transfer. Data is sampled at both rising edge and falling edge of DCKI.
12	DCKO	Clock output terminal for serial data transfer.
13	DI	Serial data input terminal.
14	DO	Serial data output terminal.
15	GCKO	Grayscale clock output When command data “osc” = ‘L’, GCKO comes from internal osc When command data “osc” = ‘H’, GCKO comes from GCKI
22	NC	No connect
23	VDD	Supply voltage terminal.
24	GND	Ground terminal

Equivalent Circuit of Inputs and Outputs

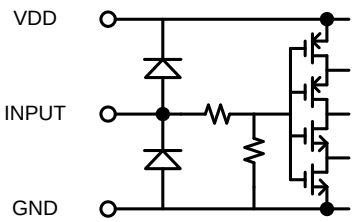
1. DI, DCKI terminals



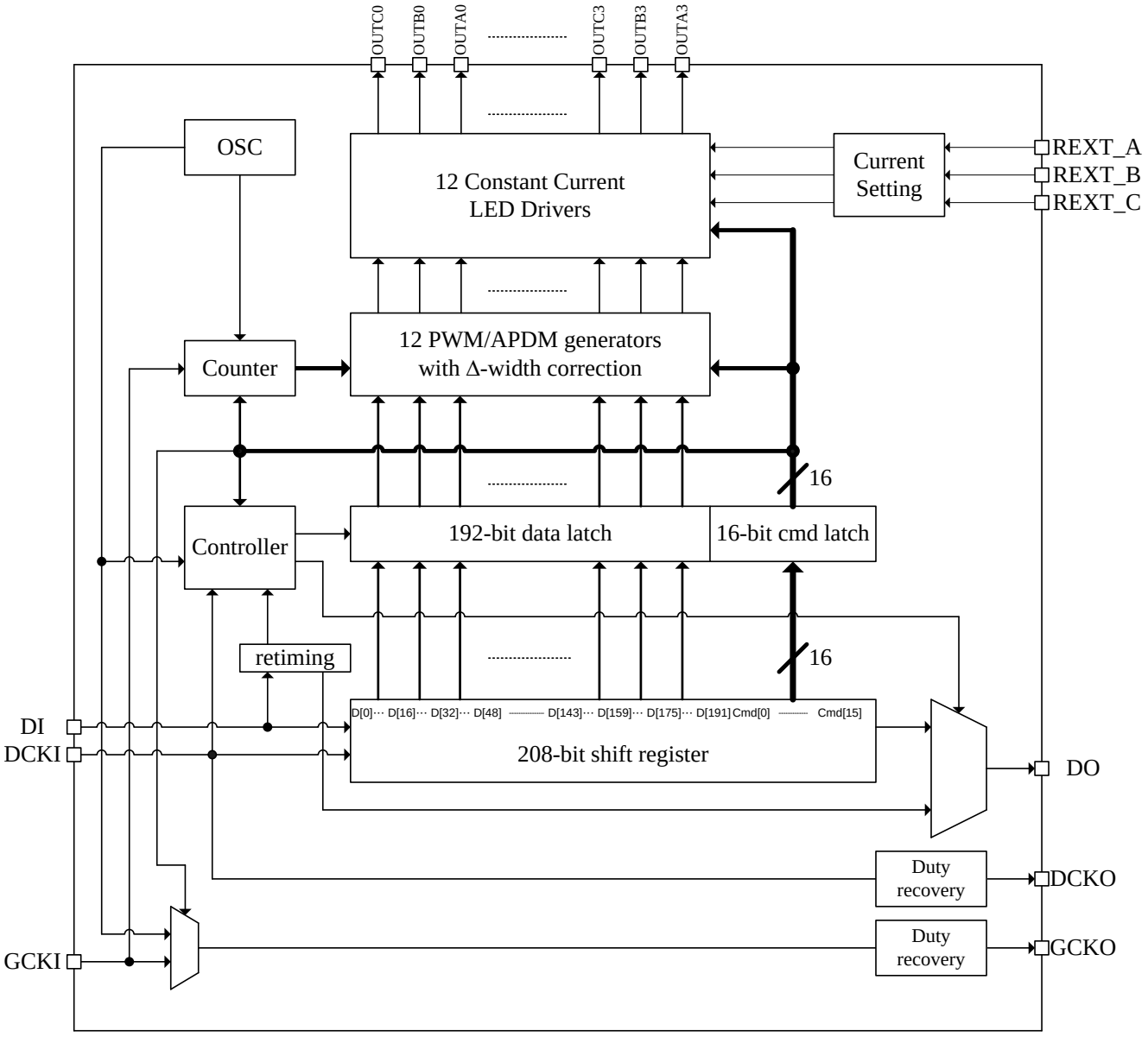
2. DO, DCKO, GCKO terminals



3. GCKI terminal



Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, Tj (max) = 150°C unless otherwise specified.) (Note 4, 5, 6)

Symbol	Parameters	Ratings	Unit
VDD	Supply Voltage	-0.3 ~ 7.0	V
V_{DI}, V_{DCKI}, V_{GCKI}	Input Voltage	-0.3 ~ VDD+0.3	V
IOUT	Output Current	62	mA
VOUT_off	Output Voltage @ Turn-off	-0.3 ~ 24	V
VOUT_on	Output Voltage @ Turn-on	-0.3 ~ 5.5	V
FDCK	Input Data Clock Frequency	0.07 ~ 10	MHz
FGCK	Input Grayscale Clock Frequency	10	MHz
IGND	GND Terminal Current	750	mA

Notes: 4. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only and functional operation of the device at these or any other condition beyond those specified is not supported.
5. All voltage values are with respect to ground terminal.
6. Operation at Tj(max) = 150°C may reduce the device reliability; therefore, the suggested junction temperature of the device is under 125 °C.

ESD Ratings

Symbol	Parameter	Rating	Unit
V_{ESD}	Human-Body Model (HBM)	2000	V
	Charged-Device Model (CDM)	750	V

Package Thermal Data (Note 7)

Package	θ_{JC} Thermal Resistance Junction-to-Case (°C/W)	θ_{JA} Thermal Resistance Junction-to-Ambient (°C/W)	P_{DIS} T_A = +25°C, T_J = +105°C
TSSOP-24EP (Type A1-B)	15	28	2.86

Note: 7. Test condition: Device mounted on FR-4 PCB (51mm x 51mm 2oz copper, minimum recommended pad layout on top layer and thermal vias to bottom layer with maximum area ground plane. For better thermal performance, larger copper pad for heat-sink is needed

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Operating supply voltage	3.0	3.3	5.5	V
I_{OUT}	Output Current (Note 8)	3	—	60	mA
V_{OUT}	Output Voltage	1	—	24	V
T_A	Ambient temperature (Note 8)	-40	—	+85	°C
T_J	Junction temperature	-40	—	+125	°C
Tstg	Storage Temperature	-55	—	+150	°C

Note: 8. Dependent on ambient temperature, LED voltage, package thermal limitation, and PCB layout.

Electrical Characteristics (VDD=5.0V @T_A = +25°C, unless otherwise specified.)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage “H” Level	VIH	CMOS logic level	0.7VDD	—	VDD	V
Input Voltage “L” Level	VIL	CMOS logic level	GND	—	0.3VDD	
Output Leakage Current	ILK	VOUT = 24 V	—	—	0.2	uA
Driving Current (DO)	IOL	VOL = 0.4V	3.5	4.6	8	mA
	IOH	VOH= VDD-0.4	-8	-4.6	-3	
Output Current Skew (Channel-to-Channel) (Note 9)	dIOUT1	VOUT = 1.0 V Rrext = 2340 Ω	—	±1	±3	%
Output Current Skew (Chip-to-Chip) (Note 10)	dIOUT2		—	±2	±6	%
Output Voltage Regulation (Note 11)	% / VOUT	Rrext = 2340 Ω VOUT = 1 V ~ 3 V	—	±.0.1	—	% / V
Supply Voltage Regulation (Note 12)	% / VDD	Rrext = 2340 Ω VDD = 3 V ~ 5.5 V	—	±0.6	±1	
Supply Current (Note 13)	$I_{DD1(off)}$	Rrext = 2340 Ω all outputs turn off	—	5.73	—	mA
	$I_{DD2(on)}$	Rrext = 2340 Ω all outputs turn on	2.93	5.85	11.5	
	$I_{DD3(off)}$	Rrext = 19.5 KΩ all outputs turn off	—	2.84	—	
	$I_{DD4(on)}$	Rrext = 19.5 KΩ all outputs turn on	1.42	2.84	8	

Notes: 9. Channel-to-channel skew is defined by the formula below:

$$\Delta(\%) = \left[\frac{Iout_n}{\frac{(Iout_0 + Iout_1 + ... + Iout_3)}{4}} - 1 \right] * 100\%$$

10. Chip-to-Chip skew is defined by the formula below:

$$\Delta(\%) = \left[\left(\frac{\frac{(Iout_0 + Iout_1 + ... + Iout_3)}{4} - (Ideal\ \ Output\ \ Current)}{(Ideal\ \ Output\ \ Current)} \right) \right] * 100\%$$

11. Output voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[\frac{Iout_n(@Vout_n = 3V) - Iout_n(@Vout_n = 1V)}{Iout_n(@Vout_n = 3V)} \right] * \frac{100\%}{3V - 1V}$$

12. Supply voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[\frac{Iout_n(@V_{DD} = 5.5V) - Iout_n(@V_{DD} = 3V)}{Iout_n(@Vcc = 3V)} \right] * \frac{100\%}{5.5V - 3V}$$

13. IO excluded.

Electrical Characteristics (VDD=3.3V @T_A = +25°C, unless otherwise specified.)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage “H” Level	VIH	CMOS logic level	0.7VDD	—	VDD	V
Input Voltage “L” Level	VIL	CMOS logic level	GND	—	0.3VDD	
Output Leakage Current	ILK	VOUT = 24 V	—	—	0.2	uA
Driving Current (DO) (Guarantee by design)	IOL	VOL = 0.4V	2	3.0	—	mA
	IOH	VOH= VDD-0.4	—	-2.9	-2	
Output Current Skew (Channel-to-Channel) (Note 14)	dIOUT1	VOUT = 1.0 V Rrext = 2340 Ω	—	±1	±3	%
Output Current Skew (Chip-to-Chip) (Note 15)	dIOUT2		—	±2	±6	%
Output Voltage Regulation (Note 16)	% / VOUT	Rrext = 2340 Ω VOUT = 1 V ~ 3 V	—	±0.1	—	% / V
Supply Voltage Regulation (Note 17)	% / VDD	Rrext = 2340 Ω VDD = 3 V ~ 5.5 V	—	±0.6	±1	
Supply Current (Note 18)	$I_{DD1(off)}$	Rrext = 2340 Ω all outputs turn off	—	5.22	—	mA
	$I_{DD2(on)}$	Rrext = 2340 Ω all outputs turn on	2.61	5.22	8	
	$I_{DD3(off)}$	Rrext = 19.5 KΩ all outputs turn off	—	2.74	—	
	$I_{DD4(on)}$	Rrext = 19.5 KΩ all outputs turn on	1.4	2.79	7	

Notes: 14. Channel-to-channel skew is defined by the formula below:

$$\Delta(\%)=\left[\ \frac{Iout_n}{\frac{(Iout_0+Iout_1+...+Iout_3)}{4}}-1\ \right]*100\%$$

15. Chip-to-Chip skew is defined by the formula below:

$$\Delta(\%)=\left[\ \left(\frac{\frac{(Iout_0+Iout_1+...+Iout_3)}{4}-(Ideal\quad Output\quad Current)}{(Ideal\quad Output\quad Current)}\right)\ \right]*100\%$$

16. Output voltage regulation is defined by the formula below:

$$\Delta(\%/V)=\left[\ \frac{Iout_n(@Vout_n=3V)-Iout_n(@Vout_n=1V)}{Iout_n(@Vout_n=3V)}\ \right]*\frac{100\%}{3V-1V}$$

17. Supply voltage regulation is defined by the formula below:

$$\Delta(\%/V)=\left[\ \frac{Iout_n(@V_{DD}=5.5V)-Iout_n(@V_{DD}=3V)}{Iout_n(@Vcc=3V)}\ \right]*\frac{100\%}{5.5V-3V}$$

18. IO excluded.

Switching Characteristics (VDD = 5.0V @T_A = +25°C, unless otherwise specified.) (Guarantee by design)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay ('L to 'H')	DCKI-to-DO	tpLH1	VIH = VDD VIL = GND Rrext = 2340 Ω VL =5.0 V RL = 150 Ω CL = 13 pF	—	29	39	ns
	DCKI-to-DCKO	tpLH2		—	6.3	19	
	GCKI-to-GCKO	tpLH3		—	10.5	19	
	DI-to-DO @ Internal-latch control cycle	tpLH4		—	12	—	
Propagation Delay ('H' to 'L')	DCKI-to-DO	tpHL1		—	39	59	
	DCKI-to-DCKO	tpHL2		—	6.3	19	
	GCKI-to-GCKO	tpHL3		—	9	19	
Pulse Duration	DCKI	$tw_{(DCK)}$		50	—	7200	
	GCKI	$tw_{(GCK)}$		50	—	—	
	DI @ Internal-latch control cycle	$twH_{(DI)}$		70	—	—	
	DI @ Internal-latch control cycle	$twL_{(DI)}$		230	—	—	
Setup Time	DI	$tsu_{(D)}$		10	—	—	
Hold Time	DI	$th_{(D)}$		10	—	—	
DI Retiming @ Internal-latch control cycle		Tw_re	—	70	90	110	
Internal-latch Start Time		Tstart	—	220	—	—	us
Internal-latch Stop Time (Note 19)		Tstop	—	200	—	—	ns
DCKI Freq.		F_{DCKI}	—	0.07	—	10	MHz
Internal OSC Freq.		F_{OSC}	—	6.4	8.1	9.8	MHz
GCKI Freq.		F_{GCKI}	—	—	—	10	MHz

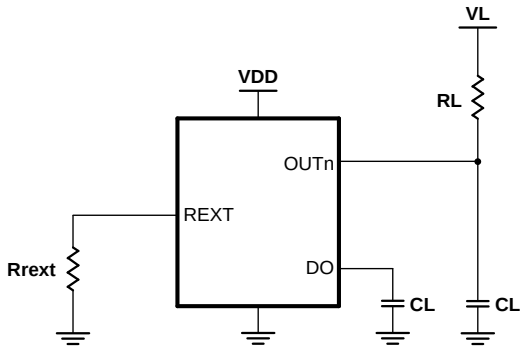
Note: 19. Tstop (min.) for cascade application must > "200ns + N*10ns" (N is the cascade number of drivers)

Switching Characteristics (VDD = 3.3V @T_A = +25°C, unless otherwise specified.) (Guarantee by design)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay ('L to 'H')	DCKI-to-DO	tpLH1	VIH = VDD VIL = GND Rrext = 2340 Ω VL =5.0 V RL = 150 Ω CL = 13 pF	—	34	39	ns
	DCKI-to-DCKO	tpLH2		—	7.9	19	
	GCKI-to-GCKO	tpLH3		—	12	19	
	DI-to-DO @ Internal-latch control cycle	tpLH4		—	18	—	
Propagation Delay ('H' to 'L')	DCKI-to-DO	tpHL1		—	40	59	
	DCKI-to-DCKO	tpHL2		—	8.2	19	
	GCKI-to-GCKO	tpHL3		—	10.5	19	
Pulse Duration	DCKI	$tw_{(DCK)}$		50	—	7200	
	GCKI	$tw_{(GCK)}$		50	—	—	
	DI @ Internal-latch control cycle	$twH_{(DI)}$		70	—	—	
	DI @ Internal-latch control cycle	$twL_{(DI)}$		230	—	—	
Setup Time	DI	$tsu_{(D)}$		10	—	—	
Hold Time	DI	$th_{(D)}$		10	—	—	
DI Retiming @ Internal-latch control cycle		Tw_re	—	90	110	130	
Internal-latch Start Time		Tstart	—	220	—	—	us
Internal-latch Stop Time (Note 20)		Tstop	—	200	—	—	ns
DCKI Freq.		F_{DCKI}	—	0.07	—	10	MHz
Internal OSC Freq.		F_{OSC}	—	6.25	7.95	9.65	MHz
GCKI Freq.		F_{GCKI}	—	—	—	10	MHz

Note: 20. Tstop (min.) for cascade application must > "200ns + N*10ns" (N is the cascade number of drivers)

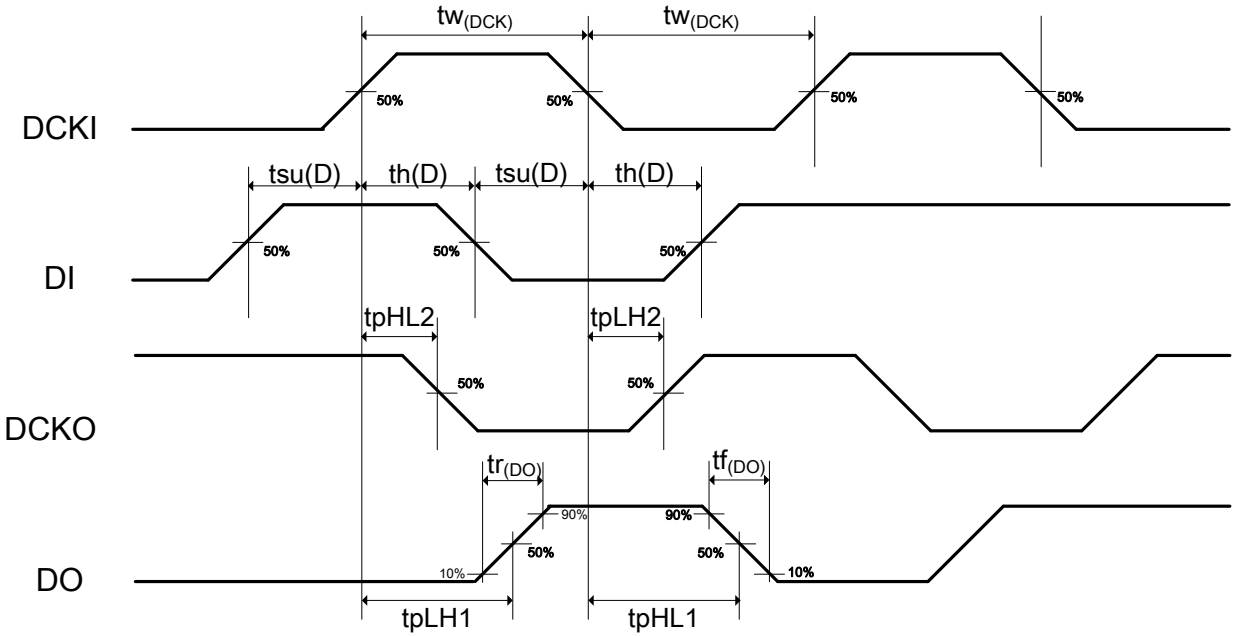
Switching Characteristics Test Circuit



Switching Characteristics Test Circuit

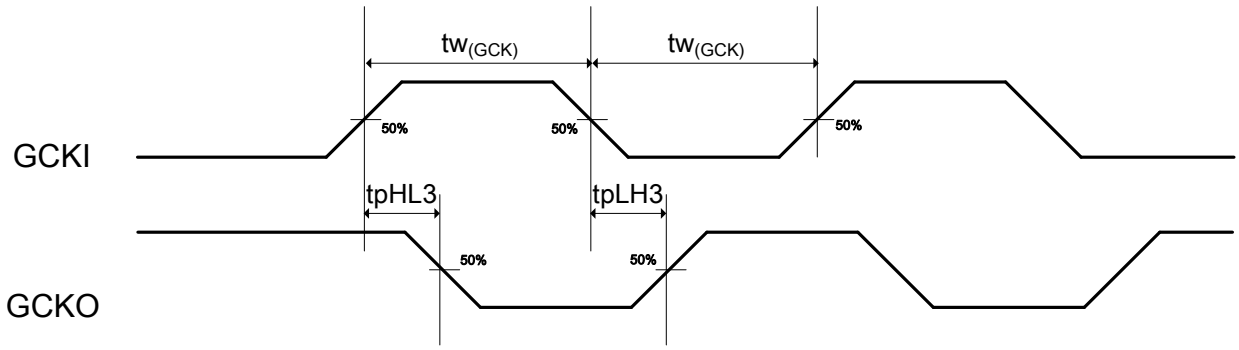
Timing Characteristics (@T_A = +25°C, unless otherwise specified.)

1. DCKI, DCKO - DI, DO

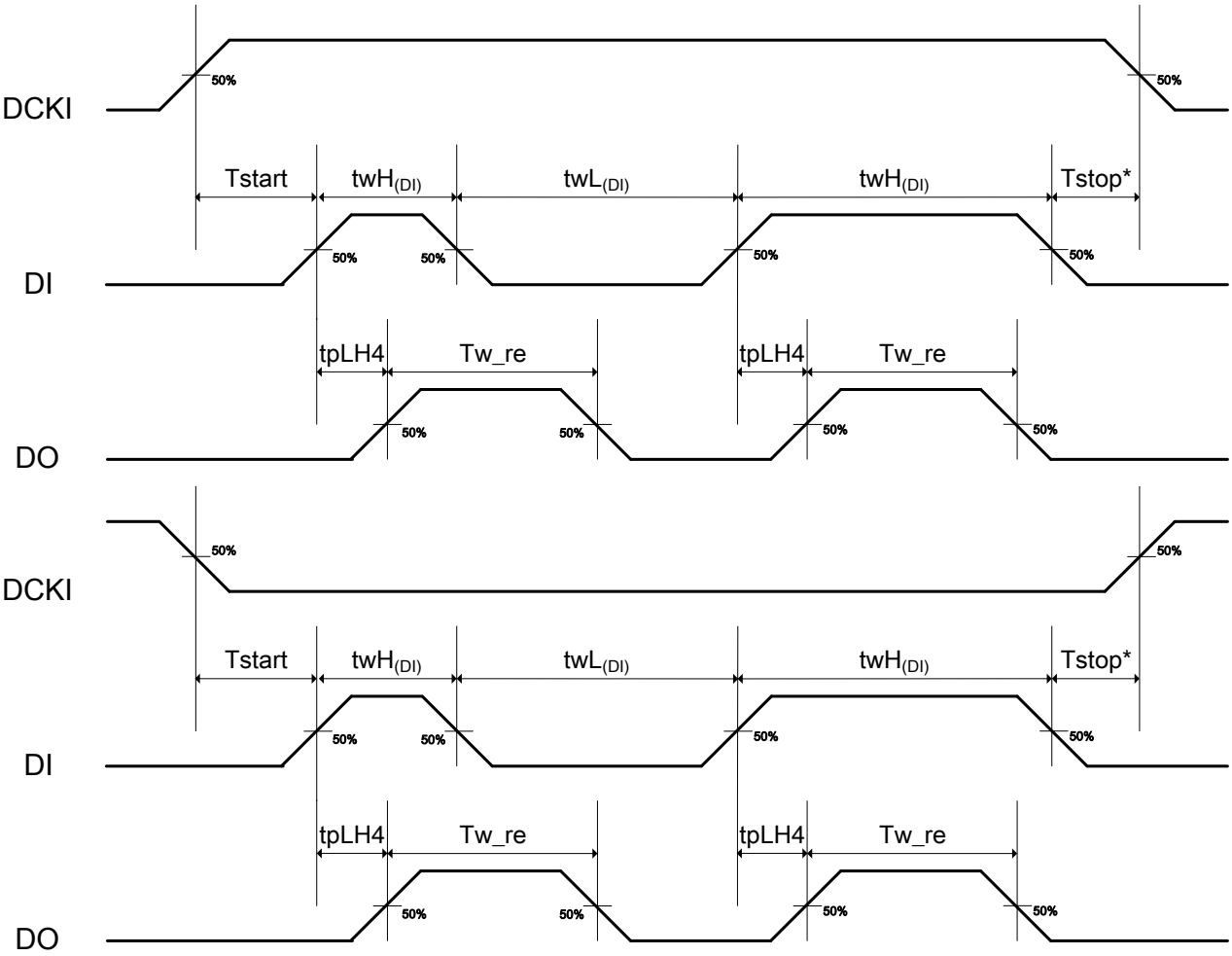


Switching Characteristics (@T_A = +25°C, unless otherwise specified.)

2. GCKI-GCKO



3. DCKI-DI & DI-DO @ Internal-latch control cycle



* Tstop (min.) for cascade application must > “200ns + N*10ns” (N is the cascade number of drivers)

Functional Description

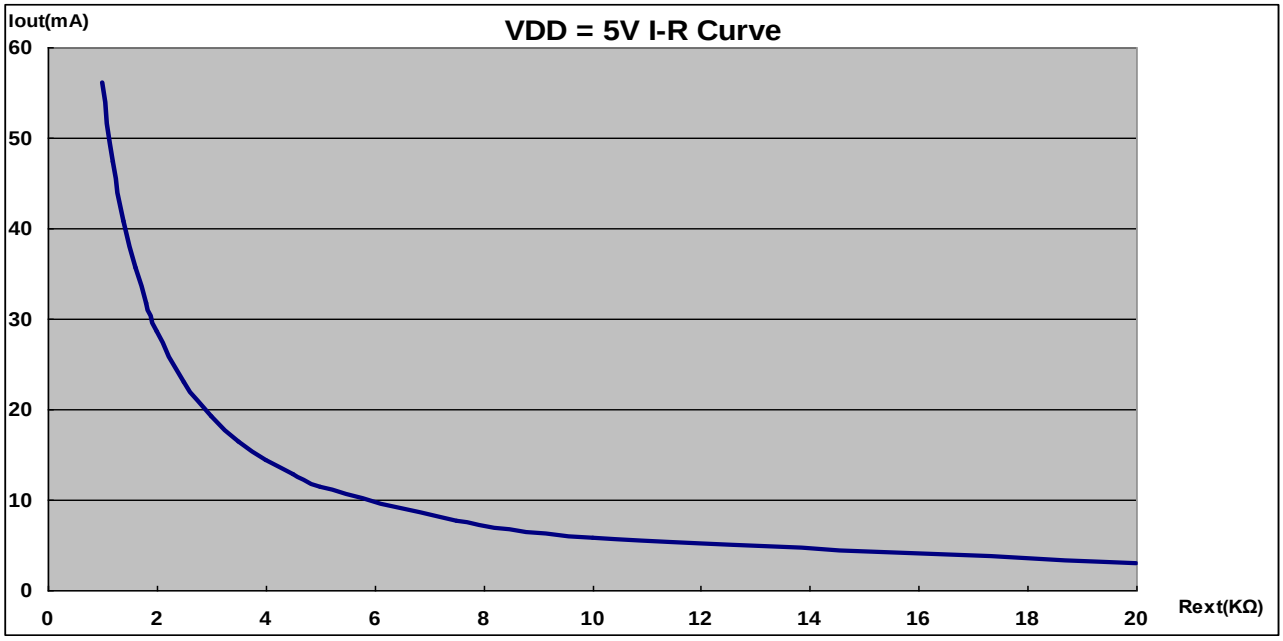
Reference Resistor

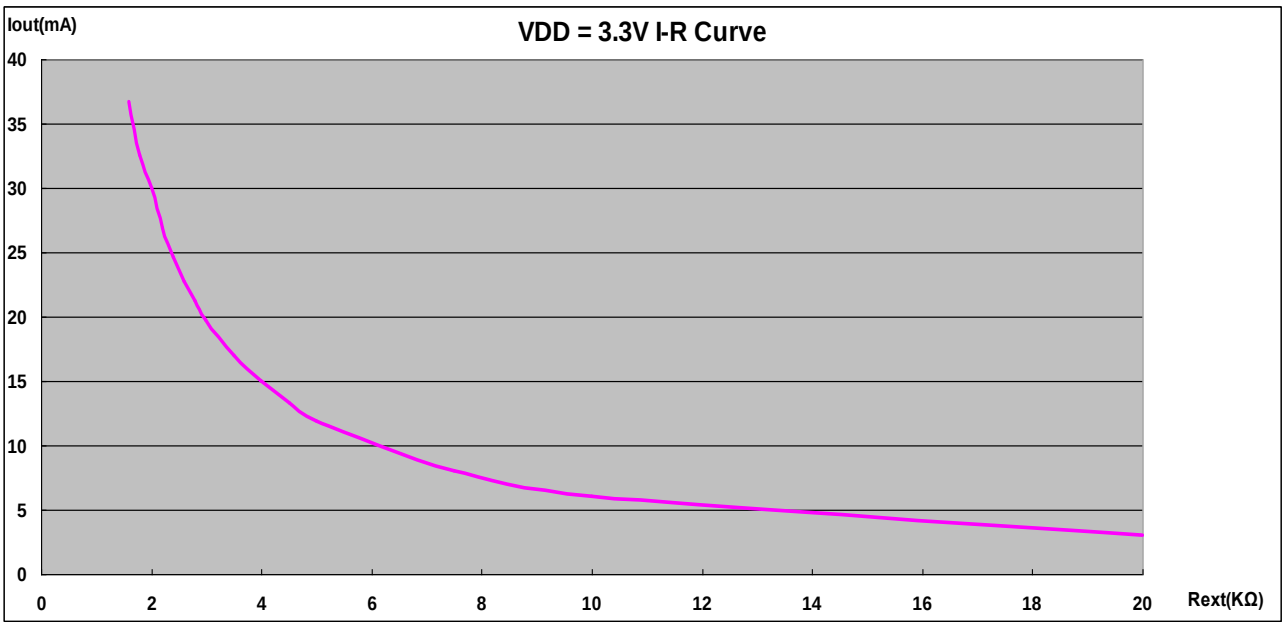
The constant current values are determined by an external resistor placed between REXT pin and GND pin. The following formula is utilized to calculate the current value:

$$Iout(mA) = \frac{1.28 * 45.5}{Rrext \ (K\Omega)}$$

Where Rrext is a resistor placed between REXT and GND

For example, Iout is 25mA when Rrext=2340Ω and Iout is 3mA when Rrext=19.5 KΩ

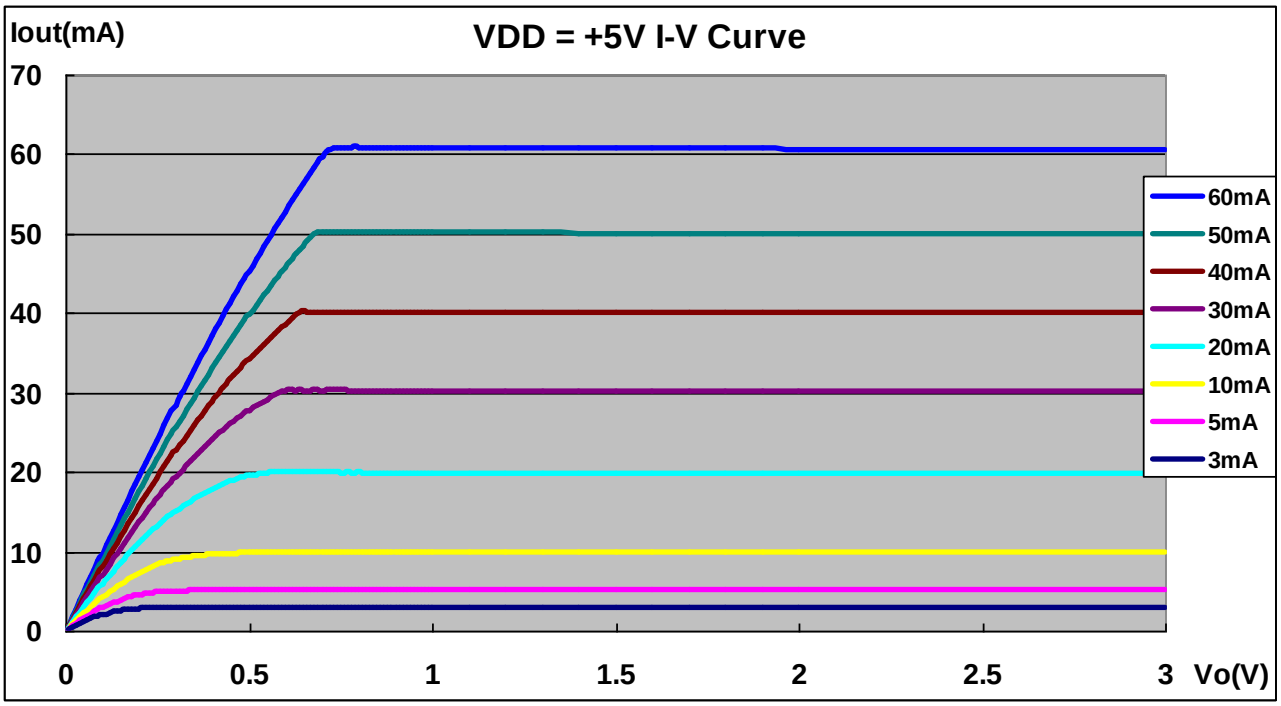


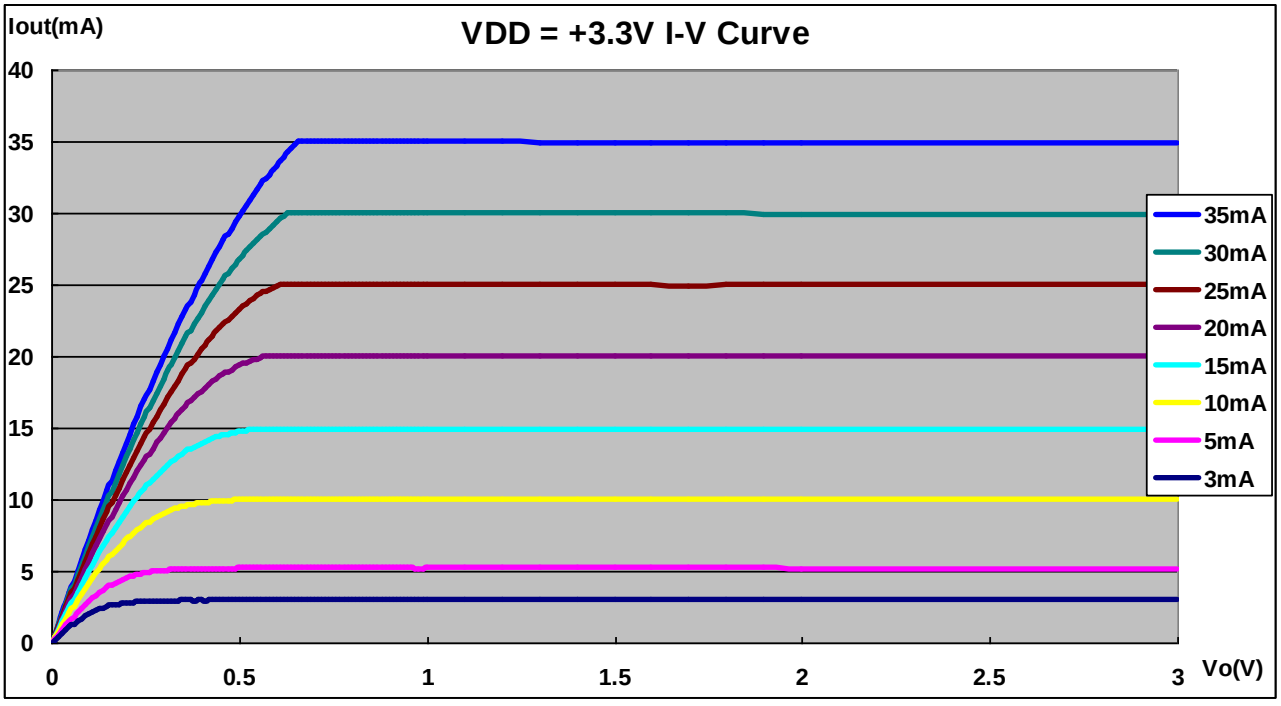


Functional Description (continued)

Constant-Current Output

The current characteristics may be invariable in the influence of the loading voltage. Therefore, the AL58221 can minimize the interference of different LED forward voltages and produce constant current. The following figures illustrate the suitable output voltage, which should be determined in order to maintain excellent performance.

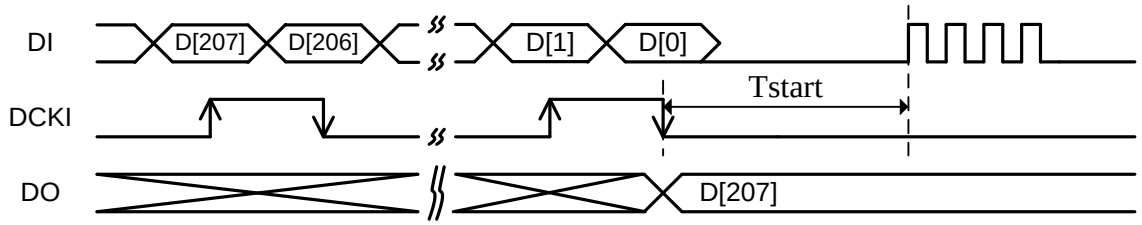




Functional Description (continued)

Serial Data Interface

The AL58221 transmits data from the DI pin on both rising and falling edge of the data clock (DCKI). After the whole given serial data are shifted into the 208-bit shift register, the data can then be loaded into the latch register by the internal-latch function. The serial data will be shifted out from the DO pin on the synchronization of the rising and falling edge of DCKI.



Data Format

16-bit command data and 12x16-bit PWM data. (Total: 208-bit)

MSB

D[207]															D[192]
Temp	Temp	Temp	Temp	Temp	hspd	bs[1]	bs[0]	gck[2]	gck[1]	gck[0]	sep	osc	pol	cntset	onest

D[191]															D[176]
A3[15]	A3[14]	A3[13]	A3[12]	A3[11]	A3[10]	A3[9]	A3[8]	A3[7]	A3[6]	A3[5]	A3[4]	A3[3]	A3[2]	A3[1]	A3[0]

D[175]															D[160]
B3[15]	B3[14]	B3[13]	B3[12]	B3[11]	B3[10]	B3[9]	B3[8]	B3[7]	B3[6]	B3[5]	B3[4]	B3[3]	B3[2]	B3[1]	B3[0]

D[159]															D[144]
C3[15]	C3[14]	C3[13]	C3[12]	C3[11]	C3[10]	C3[9]	C3[8]	C3[7]	C3[6]	C3[5]	C3[4]	C3[3]	C3[2]	C3[1]	C3[0]

D[143]															D[128]
A2[15]	A2[14]	A2[13]	A2[12]	A2[11]	A2[10]	A2[9]	A2[8]	A2[7]	A2[6]	A2[5]	A2[4]	A2[3]	A2[2]	A2[1]	A2[0]

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LSB

D[15]															D[0]
C0[15]	C0[14]	C0[13]	C0[12]	C0[11]	C0[10]	C0[9]	C0[8]	C0[7]	C0[6]	C0[5]	C0[4]	C0[3]	C0[2]	C0[1]	C0[0]

Functional Description (continued)

16-bit Command Data Description (CMD[15:0]) = D[207:192]) (Note 21)

BIT No.	Name	DESCRIPTION	FUNCTION
CMD[15:11]	Temp	Not used	Please filled with all “0”
CMD[10]	hspd	Iout Tr/Tf select	0 : Iout slow mode 1 : Iout fast mode
CMD[9:8]	bs[1:0]	Grayscale resolution select	00 : 8-bit grayscale application 01 : 12-bit grayscale application 10 : 14-bit grayscale application 11 : 16-bit grayscale application
CMD[7:5]	gck[2:0]	Internal oscillator freq. select	000 : original freq (8.6MHz) 001 : original freq/2 010 : original freq/4 011 : original freq/8 100 : original freq/16 101 : original freq64 110 : original freq/128 111 : original freq/256 If CMD[3]=1, please set CMD[7:5]=000
CMD[4]	sep	Output waveform select	0 : MY-PWM output waveform (similar to traditional waveform) 1 : APDM output waveform
CMD[3]	osc	Grayscale clock source select	0 : internal oscillator (8.6MHz) (internal GCK source) 1 : external clock from GCKI pin (external GCK source)
CMD[2]	pol	Output polarity select	0 : work as LED driver 1 : work as MY-PWM/APDM generator
CMD[1]	cntset	Counter reset select	0 : free running mode 1 : counter reset mode (Only usable when osc = “1”)
CMD[0]	onest	One-shot select	0 : frame cycle repeat mode 1 : frame cycle One-shot mode (Only usable when cntset = “1”)

Note: 21. For information about command data settings, please refer to page 19.

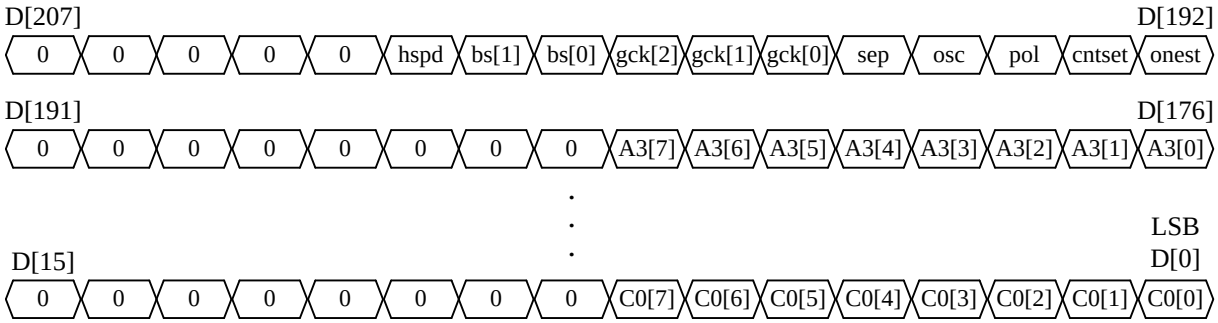
Grayscale data format

16-bit grayscale data for per channel (D[191:176], D[175:160], D[159:144], D[143:128]…D[15:0])

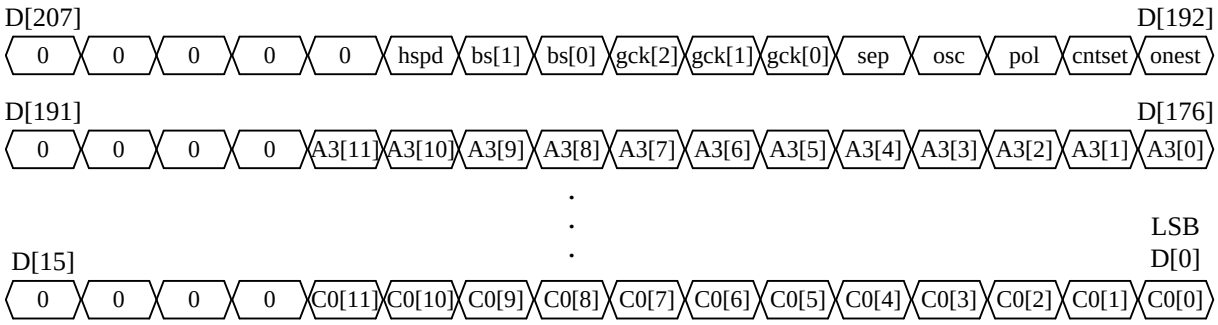
bs[1:0]	DESCRIPTION	PWM DATA FORMAT
00	8-bit grayscale mode	Fill the eight most significant bits with "0", Fill the eight least significant bits with 8-bit grayscale data.
01	12-bit grayscale mode	Fill the four most significant bits with "0", Fill the twelve least significant bits with 12-bit grayscale data.
10	14-bit grayscale mode	Fill the two most significant bits with "0", Fill the fourteen least significant bits with 14-bit grayscale data.
11	16-bit grayscale mode	Filled 16-bit grayscale data directly.

Functional Description (continued)

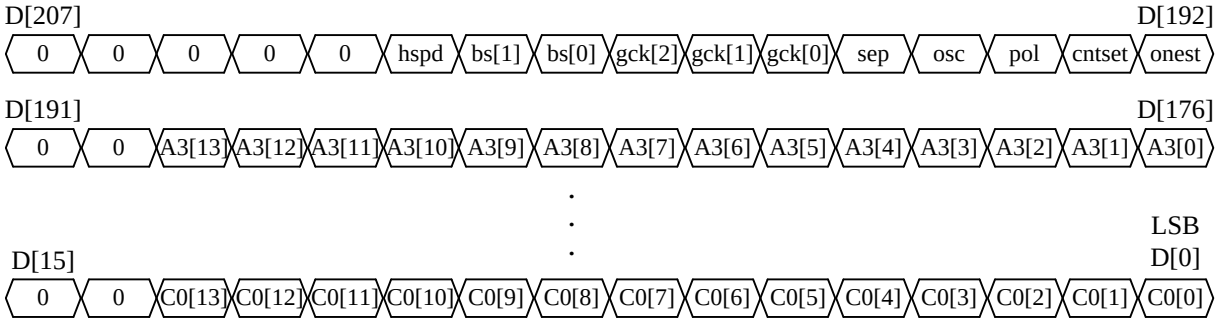
Data Format of 8-bit grayscale mode (bs[1:0]=00)



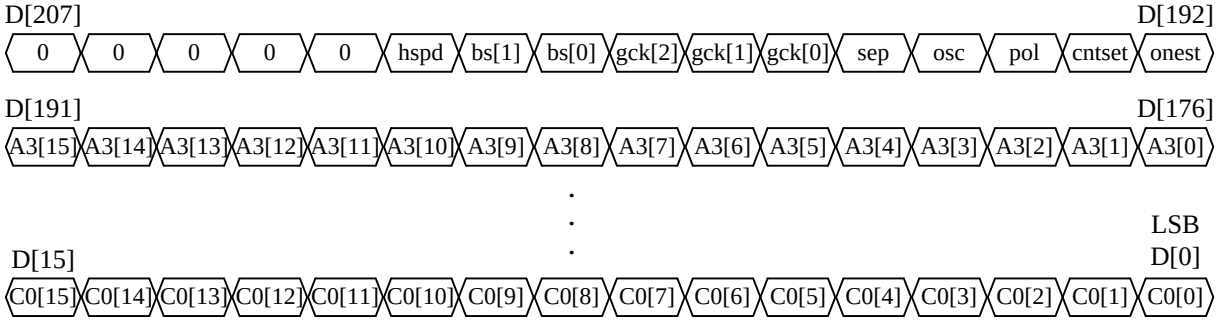
Data Format of 12-bit grayscale mode (bs[1:0]=01)



Data Format of 14-bit grayscale mode (bs[1:0]=10)



Data Format of 16-bit grayscale mode (bs[1:0]=11)

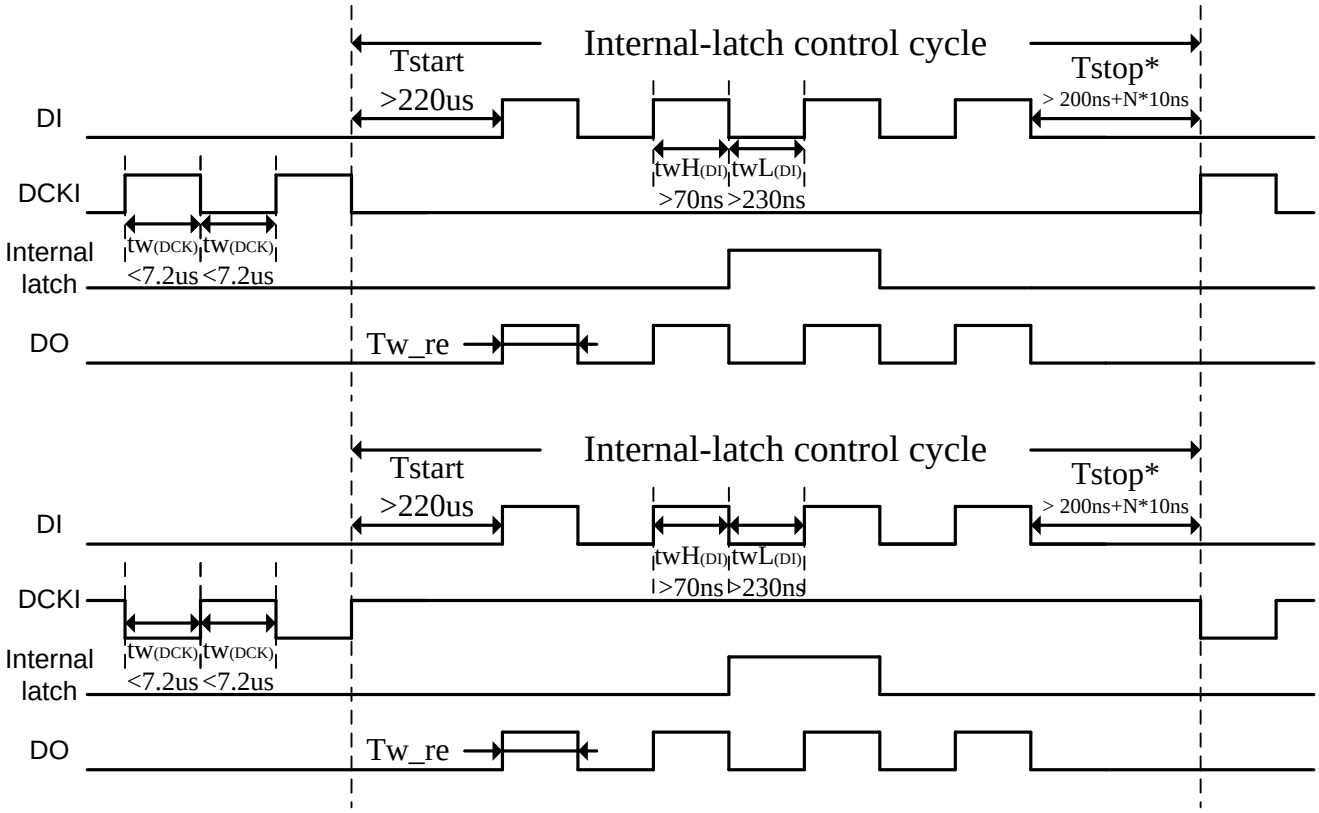


Functional Description (continued)

Internal-latch control cycle timing diagram

The steps to trigger internal-latch function are shown below:

1. After the entire given serial data shifts into the shift register, keep DCKI at a fixed level (no matter “high” or “low”) for more than 220us. (Tstart > 220us).
2. Send 4 DI pulses ($twH_{(DI)}$>70ns, $twL_{(DI)}$> 230ns, Tstop*).
3. Data is loaded into the latch register at the 2nd falling edge of the DI pulse.



*Tstop (min.) for cascade application must > “200ns + N*10ns”
(N is the cascade number of drivers)

*For tw(DCK) > 7.2us application, please refer to the document “AN-AL58221-05-Solution for tw_DCK_ longer than 7.2us.pdf”

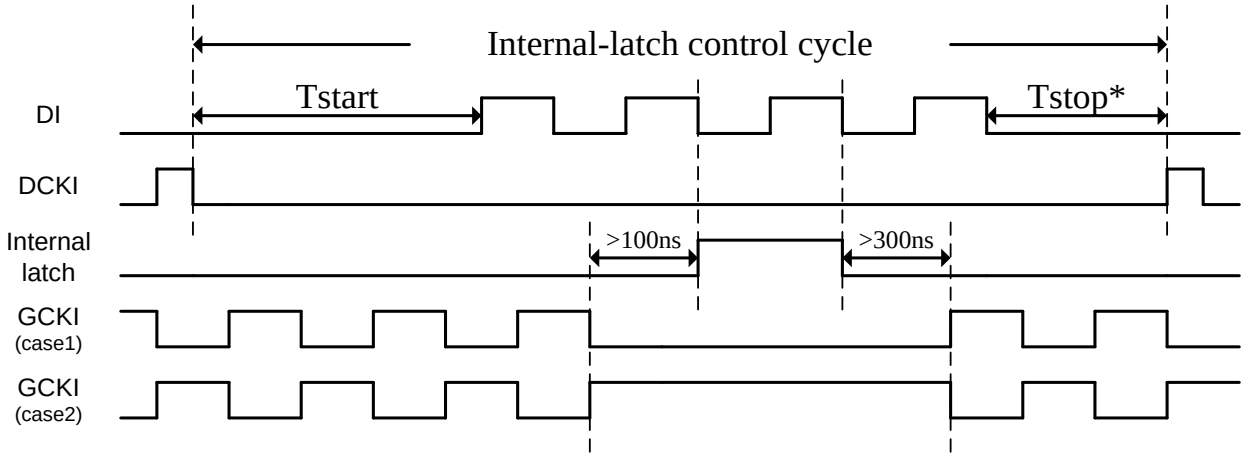
Pulse retiming at Internal-latch control cycle

The AL58221 provides DO signal retiming function, which is fixed at Tw_re = 90ns@VDD=5V under the internal-latch control cycle. This prevents variation of the duty ratio caused by long cascading.

Functional Description (continued)

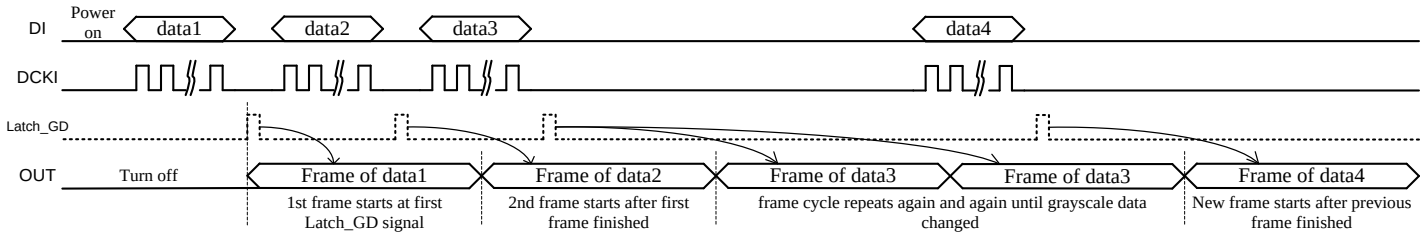
External Grayscale Clock Mode (CMD[3]=osc = "1")

When osc="1", users may use the external grayscale clock function. The grayscale clock is controlled by the GCKI pin. Both the rising and falling edge of the GCKI pulse can increase the grayscale counter by one. The AL58221 compares the grayscale data of each output with the grayscale counter value. If the grayscale data is larger than the grayscale counter value, the OUT will switch on. **The frequency of the external clock cannot be controlled by CMD[7:5]; please set CMD[7:5]=000 if CMD[3] = "1".** Some timing constrains must be obeyed, which are shown below:



Free Running Mode

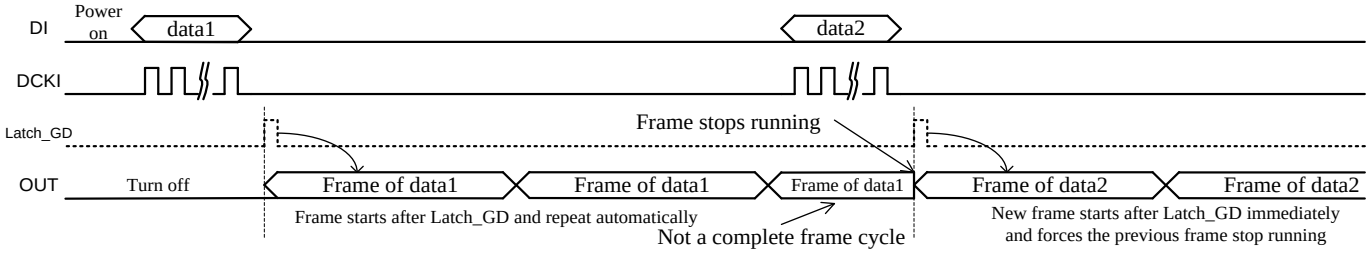
The first frame cycle after power-on will synchronize with the first Latch_GD signal (Latch_GD is the latch signal for grayscale data.). A new frame cycle for the new grayscale data will start after the previous frame cycle is finished. If the grayscale data does not change, the frame cycle will repeat automatically. This mode ensures every frame cycle will be performed completely.



Functional Description (continued)

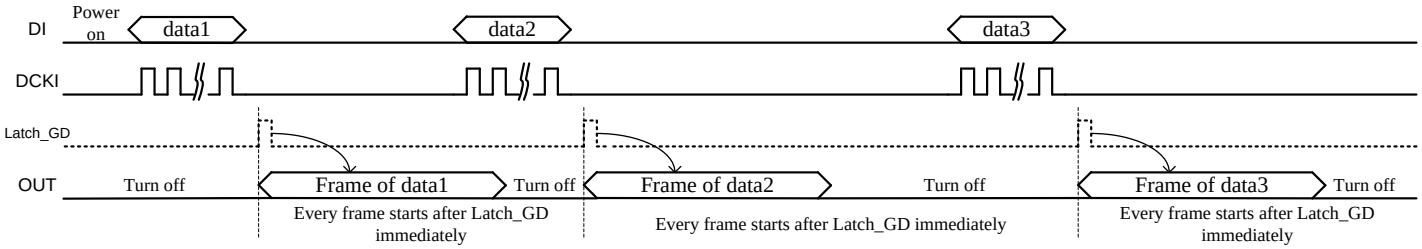
Grayscale Counter Reset Mode (Only usable when osc = ”1”: external grayscale clock mode)

Every new frame cycle of the new grayscale data will synchronize with the Latch_GD signal. Frame cycles of the same grayscale data will repeat automatically until the next grayscale data is loaded. When the next grayscale data is loaded, it will force the previous frame to stop running. This means that the previous frame cycle may not perform completely.



One-shot Mode (Only usable when cntset = “1”: grayscale counter reset mode)

Every new frame cycle of new grayscale data will synchronize with the Latch_GD signal. One grayscale data will only perform one complete frame cycle. After one complete cycle, the output current will turn off until the next grayscale data is loaded.

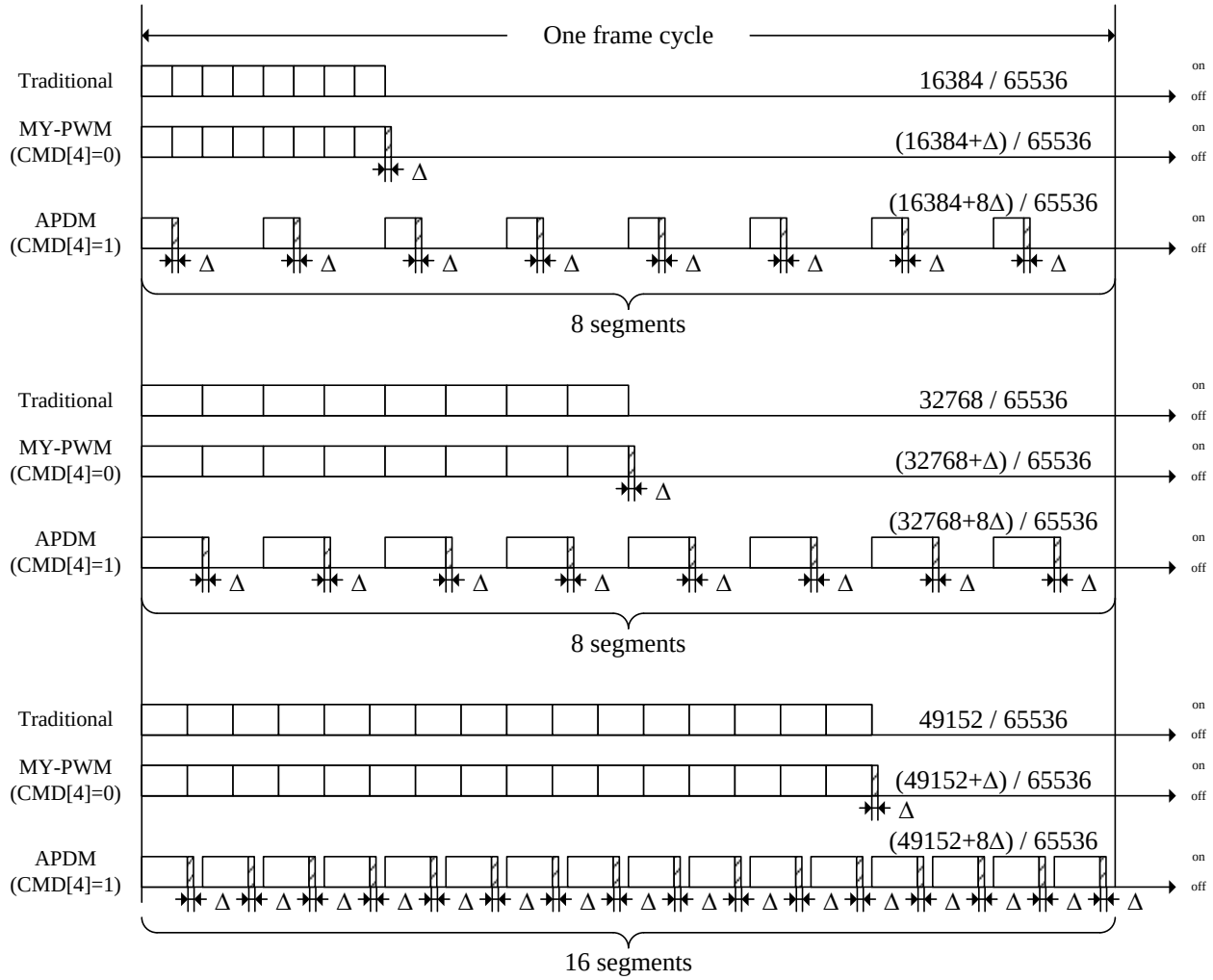


Functional Description (continued)

Adaptive Pulse Density Modulation with Δ-Width Correction

Adaptive Pulse Density Modulation (APDM) with Δ-Width Correction is a technique to improve output current waveform distortion and increase visual refresh rate. The adaptive output waveform is controlled by the grayscale value automatically. When all outputs operate at high grayscale resolution (grayscale resolution ≧ 75%), the output waveform is divided into more segments to increase visual refresh rate. Otherwise, the output waveform is divided into less segments at low grayscale resolution to improve output current linearity (grayscale resolution < 75%). The Δ-Width Correction (Δ ≠ 0) is used to compensate the non-ideal output current transient response.

(e.g. 16-bit grayscale application, Δ ≠ 0)



Application Information

Command Data Setting for Different Applications (Note 22)

1. Grayscale Clock from Internal Oscillator

Grayscale	CMD[15:11]	CMD[10]	CMD[9:8]	CMD[7:5]	CMD[4]	CMD[3]	CMD[2]	CMD[1]	CMD[0]	Image refresh Rate(Hz)
	temp	hspd	bs[1:0]	gck[2:0]	sep	osc	pol	cntset	onest	
16-bit	00000	d	11	000	1	0	d	0	0	1,001
16-bit	00000	d	11	011	1	0	d	0	0	125
14-bit	00000	d	10	000	1	0	d	0	0	4,004
14-bit	00000	d	10	011	1	0	d	0	0	500
12-bit	00000	d	01	000	1	0	d	0	0	16,016
12-bit	00000	d	01	100	1	0	d	0	0	1,001
12-bit	00000	d	01	101	1	0	d	0	0	250
8-bit	00000	d	00	000	1	0	d	0	0	256,250
8-bit	00000	d	00	100	1	0	d	0	0	16,016
8-bit	00000	d	00	101	1	0	d	0	0	4,004
8-bit	00000	d	00	111	1	0	d	0	0	1,001
8-bit	00000	d	00	000	0	0	d	0	0	32,031
8-bit	00000	d	00	011	0	0	d	0	0	4,004

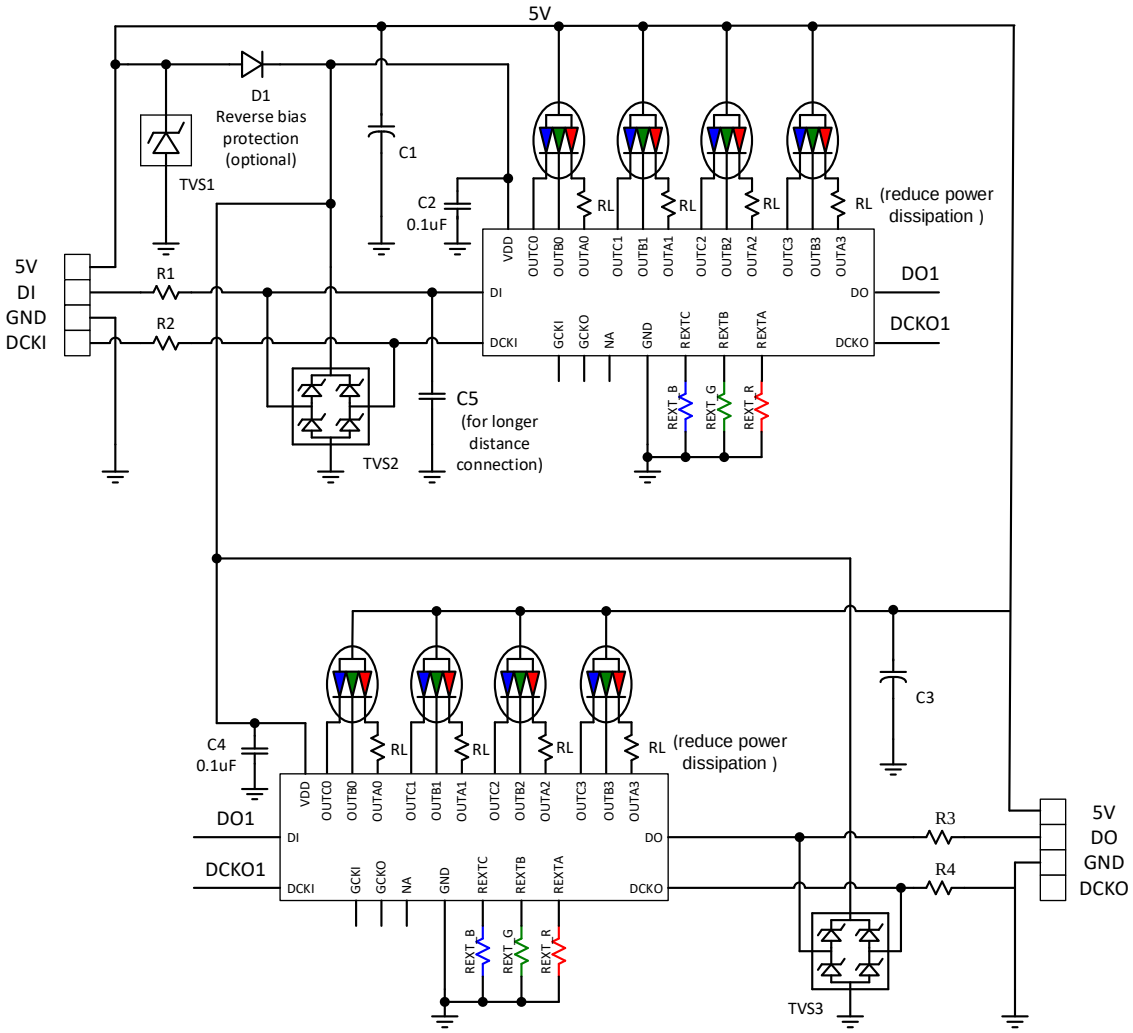
2. Grayscale Clock from External GCKI Pin

Grayscale	CMD[15:11]	CMD[10]	CMD[9:8]	CMD[7:5]	CMD[4]	CMD[3]	CMD[2]	CMD[1]	CMD[0]	GCKI Freq. (MHz)	Image refresh Rate(Hz)
	temp	hspd	bs[1:0]	gck[2:0]	sep	osc	pol	cntset	onest		
16-bit	00000	d	11	000	1	1	d	0	0	10	2,441
16-bit	00000	d	11	000	1	1	d	0	0	2	488
14-bit	00000	d	10	000	1	1	d	0	0	10	9,766
14-bit	00000	d	10	000	1	1	d	0	0	2	1,953
12-bit	00000	d	01	000	1	1	d	0	0	10	39,063
12-bit	00000	d	01	000	1	1	d	0	0	2	7,813
8-bit	00000	d	00	000	1	1	d	0	0	10	625,000
8-bit	00000	d	00	000	1	1	d	0	0	2	125,000
8-bit	00000	d	00	000	0	1	d	0	0	10	78,125
8-bit	00000	d	00	000	0	1	d	0	0	2	15,625

Note: 22. “d” means “don’t care” (dependent on application).

Application Information (continued)

1. Work as LED driver with system supply voltage = 5V (Set CMD[2] = "L")
   Use internal grayscale clock & Internal-latch function

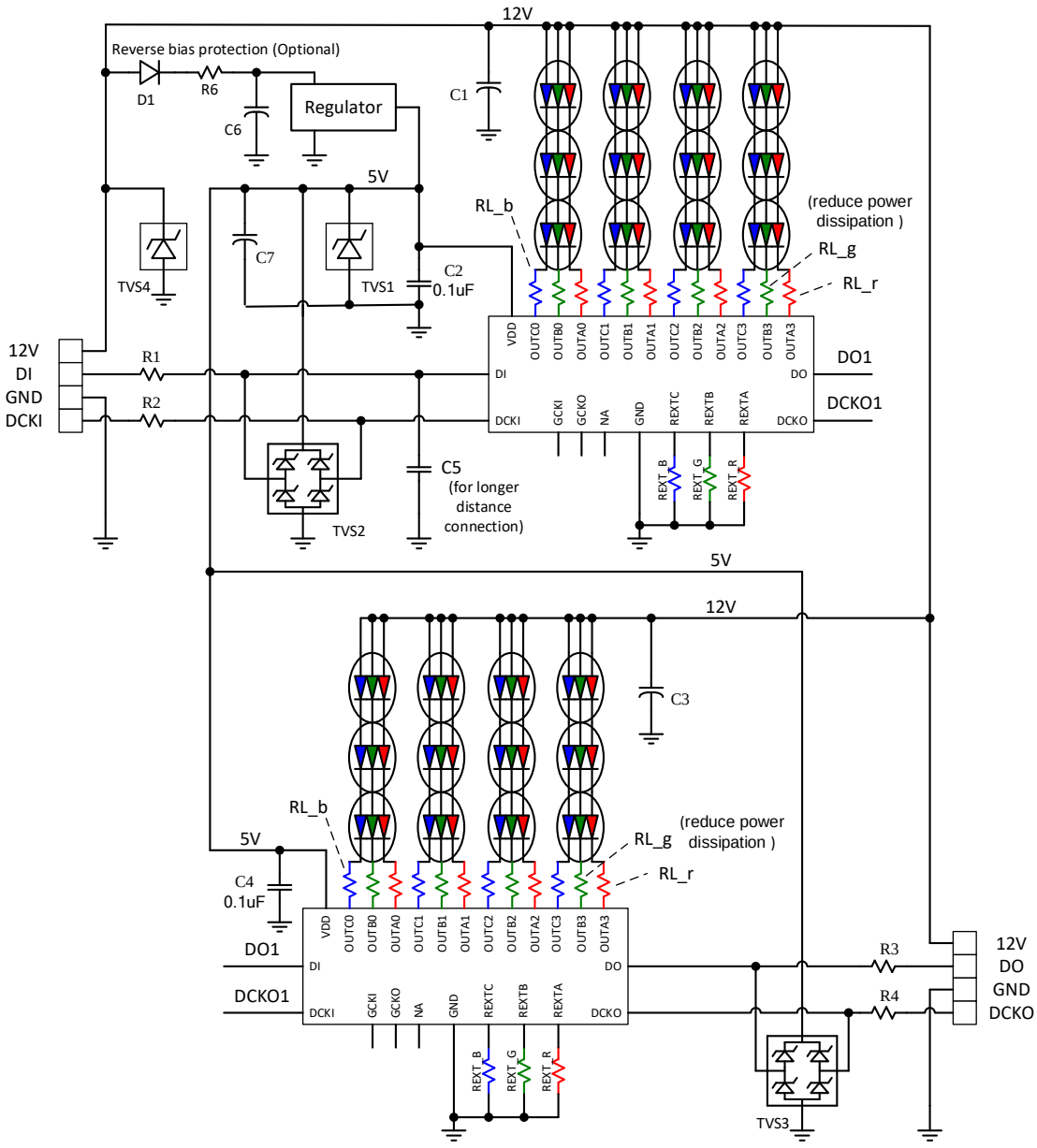


Symbol	Value (just for reference)	Description
R1, R2, R3, R4	33~100Ω	resistor for hot-plug protection
C1, C3	4.7~47uF	capacitor for voltage stability
C2, C4	0.1uF	decoupling capacitor
C5	33~130pF	capacitor for longer distance connection
D1	—	diode for reverse bias protection (optional)
RL	—	used to reduce the power dissipation of AL58221

*** Users may use suitable value for different applications.**

Application Information (continued)

2. Work as LED driver with system supply voltage = 12V (Set CMD[2] = "L")
   Use internal grayscale clock & Internal-latch function



Symbol	Value (just for reference)	Description
R1, R2, R3, R4	33~100Ω	resistor for hot-plug protection
R6	33~100Ω	resistor for the regulator
C1, C3	4.7~47uF	capacitor for voltage stability
C2, C4	0.1uF	decoupling capacitor
C5	33~130pF	capacitor for longer distance connection
C6, C7	1.0~3.3uF	capacitor for the regulator
D1	—	diode for reverse bias protection (optional)
RL_r, RL_g, RL_b	—	used to reduce the power dissipation of AL58221

*** Users may use suitable value for different applications.**

Application Information (continued)

Power Dissipation

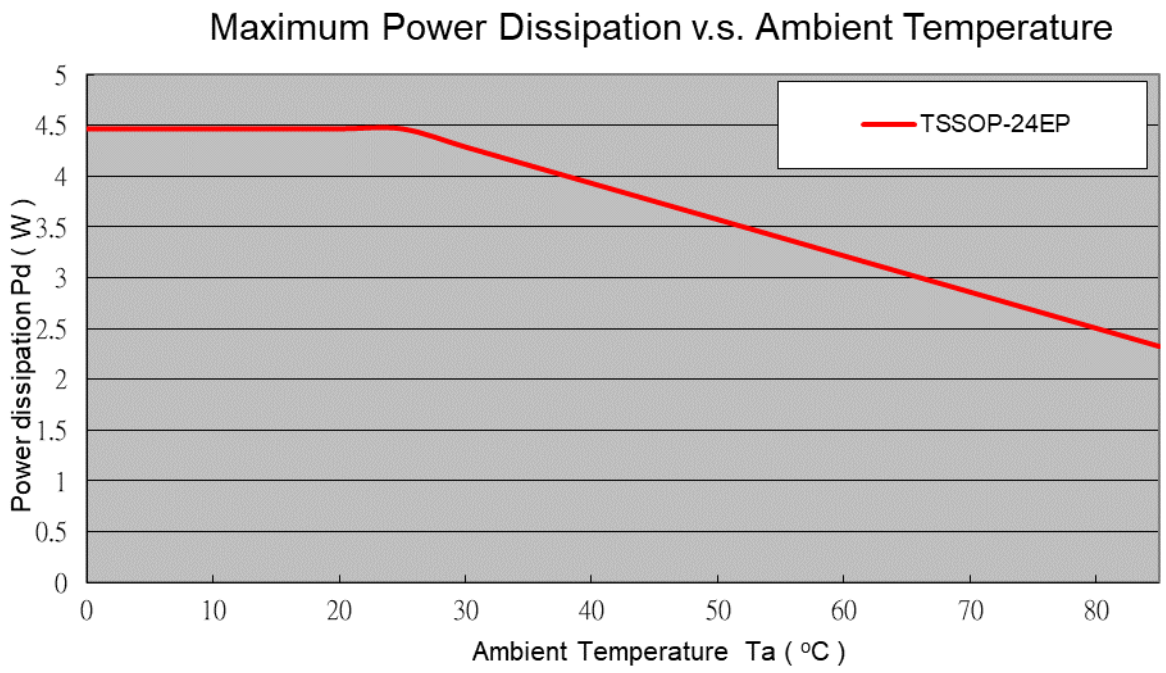
When the 12 output channels are turned on, the practical power dissipation is determined by the following equation:
("Vout" is the output voltage @ turn-on and "Duty" is the max. percentage of turn-on.)

$$PD\ (practical) = V_{DD} \times I_{DD} + VoutA3 \times IoutA3 \times DutyA3 + \ldots + VoutC0 \times IoutC0 \times DutyC0$$

In secure operating conditions, the power consumption of an integrated chip should be less than the maximum permissible power dissipation, which is determined by the package type and ambient temperature. The formula for maximum power dissipation is described as follows:

$$PD\ (max) = \frac{Tj(max)(^{\circ}C) - Ta(^{\circ}C)}{Rth(j\text{-}a)(^{\circ}C/Watt)}$$

The PD(max) declines as the ambient temperature rises. Therefore, suitable operating conditions should be designed with caution according to the chosen package and the ambient temperature. The following figure illustrates the relation between the maximum power dissipation and the ambient temperature in the TSSOP-24EP package.

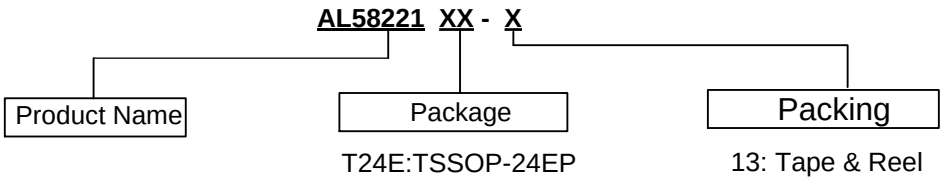


Design Tools (Note 23)

- AL58221 Demo Board
- Demo Board Gerber File for PCB Layout Reference

Note: 23. Diodes' design tools can be found on our website at https://www.diodes.com/design/tools/.

Ordering Information (Note 24)



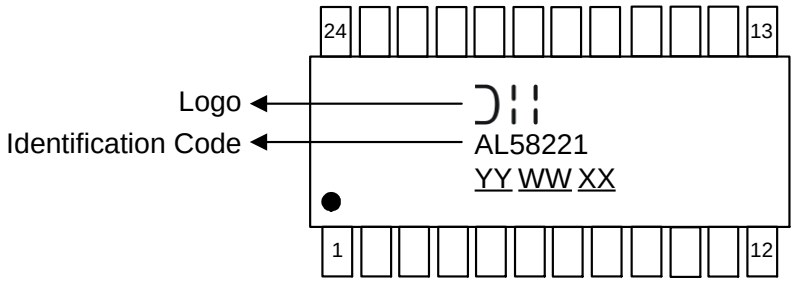
Orderable Part Number	Package	Packing		
		Quantity	Carrier	Part Number Suffix
AL58221T24E-13	TSSOP-24EP (Type A1-B)	2500	Tape & Reel	-13

Note: 24. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

Package: TSSOP-24EP (Type A1-B)

(Top View – Not to Scale)



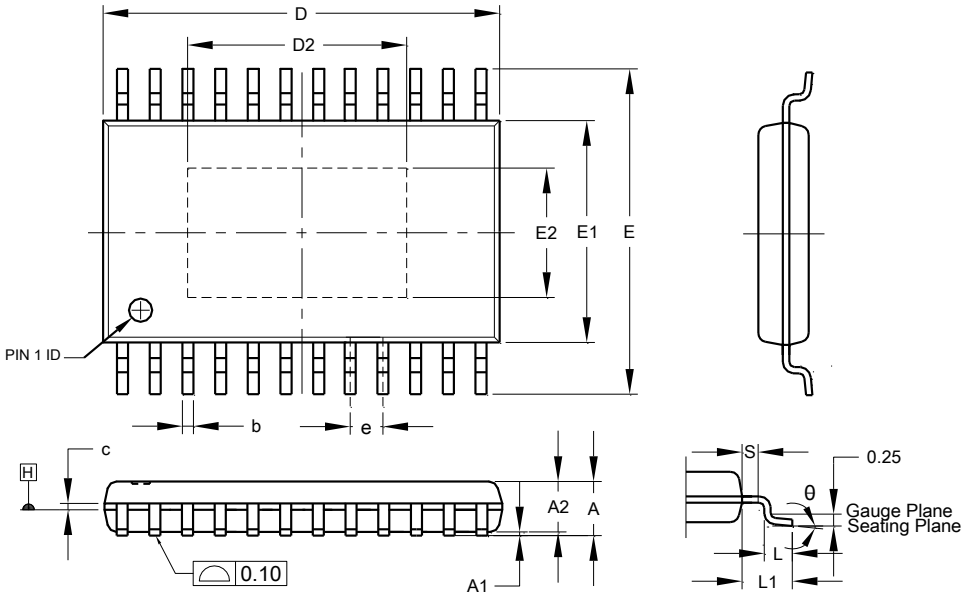
YY : Year : 23, 24, 25~
WW : Week : 01~52 ; 52 represents 52 and 53 week
XX : Internal Code

Orderable Part Number	Package	Identification Code
AL58221T24E-13	TSSOP-24EP (Type A1-B)	AL58221

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

TSSOP-24EP (Type A1-B)

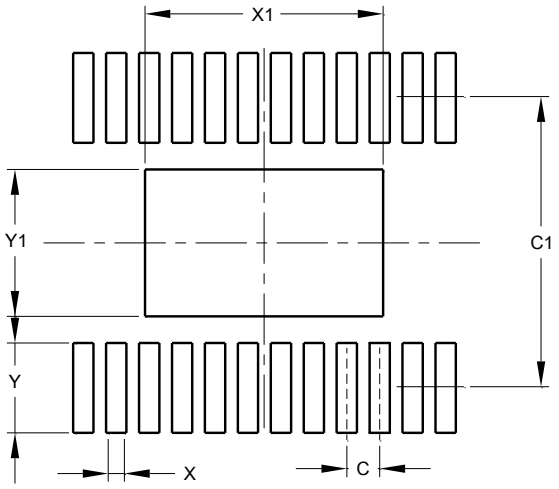


TSSOP-24EP (Type A1-B)			
Dim	**Min**	**Max**	**Typ**
A	--	1.20	--
A1	0.00	0.15	--
A2	0.80	1.05	1.00
b	0.19	0.30	--
c	0.09	0.20	--
D	7.70	7.90	7.80
D2	3.70	4.62	--
E	6.40 BSC		
E1	4.30	4.50	4.40
E2	2.28	2.85	--
e	0.65 BSC		
L	0.45	0.75	060
L1	1.00 REF		
S	0.20	--	--
θ	0°	8°	--
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

TSSOP-24EP (Type A1-B)



Dimensions	Value (in mm)
C	0.650
C1	5.600
X	0.400
X1	4.225
Y	1.800
Y1	2.640

Mechanical Data

- Moisture Sensitivity: Level 3 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.096 grams (Approximate)

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