BOS1921/BOS1931 Piezo Haptic Driver with Digital Front End

1 Features

- High-Voltage Low Power Piezo Driver
  - Drives 100 nF at 190 V_{pk-pk} and 300 Hz while consuming only 350 mW
  - Drives Capacitive Loads up to 820 nF
  - Energy Recovery
  - Differential Output
  - Small Solution Footprint, QFN & WLCSP
- Advanced Piezo Sensing Capabilities (BOS1921 only)
  - 7.6 mV Sensing Resolution
  - Interrupt Generation
  - Automatic Triggering of Haptic Feedback
- Integrated Digital Front End with I3C/I^2C
  - 1024 sample Internal FIFO Interface
  - 1.8 V to 5.0 V Digital I/O Supply
  - Waveform Synthesizer (WFS)
  - Supports Continuous Waveforms Playback
  - State Retention in SLEEP Mode
- Fast Start Up Time of Less Than 300 µs
- Multi-Actuator Synchronization
- Wide Supply Voltage Range of 3 V to 5.5 V

2 Applications

- Mobile Phones and Tablets
- Portable Computers, Keyboards and Mice
- Gaming Controllers, Wearables
- Electronic Cooling
- Micropump

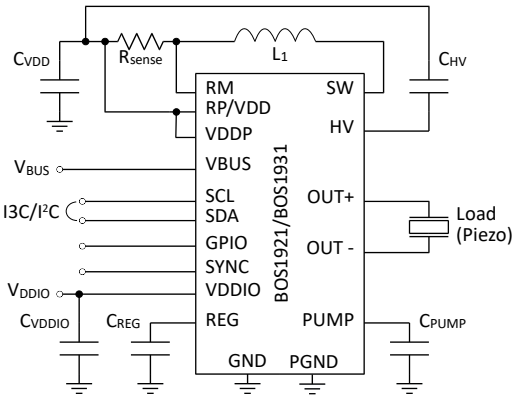

Figure 1: Simplified schematic

3 Description

The BOS1921 (driving + sensing) and BOS1931 (driving) are a single-chip piezo actuator driver with energy recovery, based on Boreas' patented CapDrive™ technology. It can drive actuators with waveforms up to 190 V_{pk-pk} while operating from a 3 to 5.5 V supply voltage. Its low power and small size make it ideal for a variety of applications requiring minimal power consumption.

The BOS1921 features high-resolution piezo sensing capabilities, allowing haptic feedback to be automatically played when detection conditions are met.

The BOS1921/BOS1931 differential driver achieves low distortion waveforms and quiet actuator operation. All settings are adjustable through the digital front end to reduce the BOM.

Data and configuration parameters are easily communicated to the BOS1921/BOS1931 through its two-wire MIPI I3C interface. The MIPI I3C is also backward compatible with I^2C for easy integration in most systems. A flexible deep FIFO enables the streaming of digital waveform data for playback or the transmission of burst data for more bandwidth efficiency. The BOS1921/BOS1931 also integrates a waveform synthesizer and 2 kB of RAM waveform memory to generate HD haptic waveforms with minimal communication bandwidth.

A dedicated SYNC pin can synchronize multiple BOS1921/BOS1931 controllers to simultaneously drive multiple actuators within 2 µs.

With a typical start-up time of less than 300 µs, the device latency is negligible in most systems.

Various safety systems protect the BOS1921/BOS1931 from damage in case of a fault.

See section 9 for package dimensions and section 11 for ordering information.

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4 Pins & Bumps Configuration and Functions

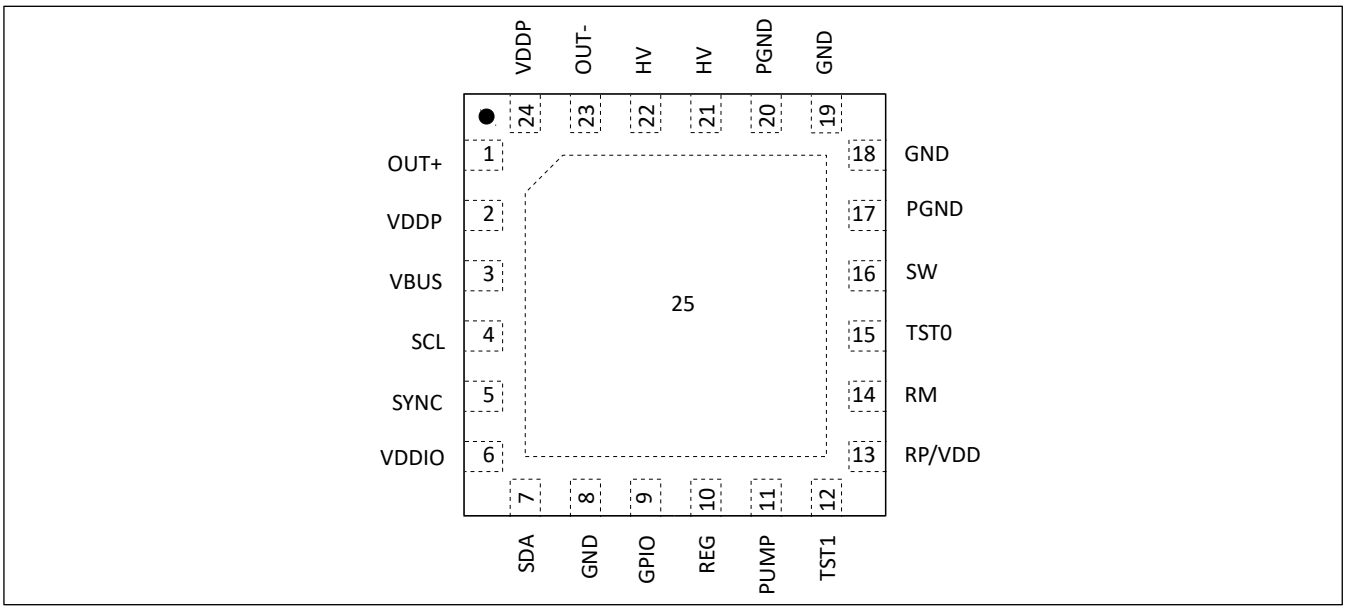


Figure 2: QFN 24L 4.0mm × 4.0mm package with exposed thermal pad (TOP VIEW; NOT TO SCALE)

Table 1: QFN package pins description

PIN NO.	NAME	TYPE	DESCRIPTION
1	OUT+	Output	Positive Differential Output
2	VDDP	Power	Intermediate Supply Voltage
3	VBUS	Power	Main Power Supply
4	SCL	Input	I3C/I^{2}C clock
5	SYNC	Input/Output	Synchronization pin, tie de ground if unused
6	VDDIO	Power	Digital IO Power Supply
7	SDA	Input/Output	I3C/I^{2}C data
8	GND	Power	Supply Ground
9	GPIO	Input/Output	General-purpose input output
10	REG	Power	Internal 1.8 V Regulator Output
11	PUMP	Power	Internal 5 V Charge Pump Voltage
12	TST1	-	No connect
13	RP/VDD	Power	Current Sense Positive Input / Supply Voltage
14	RM	Input	Current Sense Negative Input
15	TST0	-	Connect to GND
16	SW	Power	Internal Power Converter Switch Pin
17	PGND	Power	Supply Ground of the Power Stage
18	GND	Power	Supply Ground
19	GND	Power	Supply Ground
20	PGND	Power	Supply Ground of the Power Stage
21	HV	Power	High-Voltage Output
22	HV	Power	High-Voltage Output
23	OUT-	Output	Negative Differential Output
24	VDDP	Power	Intermediate Supply Voltage
25	GND	Power	Exposed thermal pad is GND and must be soldered to PCB

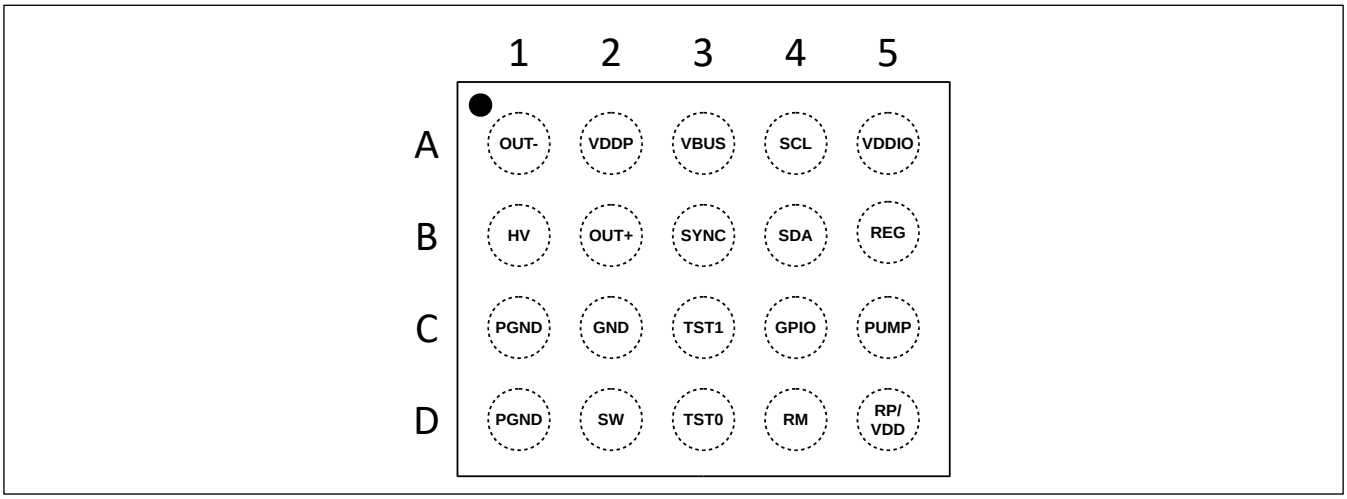


Figure 3: WLCSP 20B 2.1mm × 1.7mm package (TOP VIEW; NOT TO SCALE)

Table 2: WLCSP package bumps description

BUMP NO.	NAME	TYPE	DESCRIPTION
A1	OUT-	Output	Negative Differential Output
A2	VDDP	Power	Intermediate Supply Voltage
A3	VBUS	Power	Main Power Supply
A4	SCL	Input	I3C/I^2C clock
A5	VDDIO	Power	Digital IO Power Supply
B1	HV	Power	High-Voltage Output
B2	OUT+	Output	Positive Differential Output
B3	SYNC	Input/Output	Synchronization pin
B4	SDA	Input/Output	I3C/I^2C data
B5	REG	Power	Internal 1.8 V Regulator Output
C1	PGND	Power	Supply Ground of the Power Stage
C2	GND	Power	Supply Ground
C3	TST1	-	No connect
C4	GPIO	Input/Output	General-purpose input output
C5	PUMP	Power	Internal 5 V Charge Pump Voltage
D1	PGND	Power	Supply Ground of the Power Stage
D2	SW	Power	Internal Power Converter Switch Pin
D3	TST0	-	Connect to GND
D4	RM	Input	Current Sense Negative Input
D5	RP/VDD	Input	Current Sense Positive Input / Supply Voltage

5 Specifications

5.1 Absolute Maximum Ratings

Table 3: Absolute maximum ratings‡

	SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT
1		Voltage at pins HV, OUT+, OUT-, SW	-0.3		110	V
2		Voltage at all other pins	-0.3		7	V
3	T_{stg}	Storage temperature	-65		150	°C
4	T_J	Junction Temperature	-40		150	°C
5	SOA	Safe operating area	See *Figure* 14.			-

‡Exceeding these values may cause permanent damage. Functional operation under these conditions is not guaranteed.

5.2 Thermal Resistance

Table 4: Thermal resistance‡

	SYMBOL	PARAMETER	PACKAGE	MIN	NOM (1,2)	MAX	UNIT
1	Θ_{JA}	Thermal resistance: junction to ambient	QFN 24L 4.0mm × 4.0mm		TBD		°C/W
			WLCSP 20B 2.1mm × 1.7mm				°C/W

‡*Power dissipated in the package is not obvious to calculate. Please consult Boréas Technologies before using these parameters.*

5.3 Recommended Operating Conditions

Table 5: Recommended operating conditions

	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
1	T_A	Operating Temperature	Operating free-air temperature	-40		85	°C
2	V_{BUS}, V_{DD}(1)	Supply voltage		3.0		5.5	V
3	V_{DDIO}(2)	I/O Supply voltage		1.62		5.5	V
4	C_L	Load capacitance	V_{OUT} = 190 V_{pk-pk}, f_{OUT} = 300 Hz			100	nF
			V_{OUT} = 100 V_{pk-pk}, f_{OUT} = 220 Hz			470	nF
			V_{OUT} = 100 V_{pk-pk}, f_{OUT} = 130 Hz			820	nF
5	L_1	Inductance		10		68	µH
6	R_{sense}	Sense resistor		0.2		1.0	Ω
7	f_{OUT}	Output frequency	PLAY_MODE[1:0] = 0x3	3.9		1000	Hz
8	I_{SW}	Transient current at SW pin				1.3	A

(1) If the Unidirectional Power Input mode is enabled (UPI bit set to 0x1), V_{DD} may increase above the maximum recommended operating condition, see section 6.2.13.
(2) Digital I/O voltage (V_{DDIO}) must match the communication interface voltage.

5.4 Electrical Characteristics

Table 6: Electrical characteristics. Conditions: T_A = 25°C, V_{BUS} = 3.6 V (unless otherwise noted)

	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
1	V_{REG}	Voltage at REG pin		1.75	1.80	1.85	V
2	V_{IL}	Digital low-level input voltage	SDA, SCL, GPIO & SYNC pins			0.5	V
3	V_{IH}	Digital high-level input voltage		V_{DDIO}×0.7		V_{DDIO}+0.3	V
4	V_{OL}	Digital low-level output voltage				0.4	V
5	V_{OH}	Digital high-level output voltage		V_{DDIO}×0.8			
6	$V_{OUT(FS)}$	Full-scale output voltage		186	190	194	V_{pk-pk}
7	I_{Q_VBUS}	V_{BUS} Quiescent current	SLEEP State(1)(2) OE=0x0, DS=0x1, RET=0x1		0.6	10	µA
			SLEEP State OE=0x0, DS=0x1, RET=0x0		2.4		µA
			IDLE State OE=0x0, DS=0x0		530		µA
8	$I_{BUS,AVG}$	Average V_{BUS} supply current during operation & OE=0x1	SENSING=0x1(3)		1.9		mA
			F_{OUT} = DC V_{OUT} = 95 V C_{Load} = 100 nF		3.7		mA
			f_{OUT} = 300 Hz V_{OUT} = 190 V_{pk-pk} C_{Load} = 100 nF		90		mA
			f_{OUT} = 200 Hz V_{OUT} = 190 Vpk-pk C_L = 10 nF CCM = 0x0		14.5		mA
9	THD+N	Total Harmonic Distortion + Noise(2)	f_{OUT} = 300 Hz V_{OUT} = 190 V_{pk-pk} C_{Load} = 100 nF		0.3	1	%
10	f_{s-FIFO}	Programmable FIFO playback rate	PLAY_SRATE[2:0]=0x0 PLAY_SRATE[2:0]=0x7	1008 7.875	1024 8	1040 8.125	ksps
11	PSR(3)	Piezo Sensing Resolution	CONFIG.GAINS=0x1		7.6		mV
12	t_{start}(2)	Start-up Time	Time from SLEEP mode to haptic waveform playback			300	µs
13	DHL(2)(3)	Sensing Detection to Haptic Feedback Latency	Time from sensing detection event to automatic playback			30	µs

(1) The VDDIO supply should be powered off when state retention is disabled (RET bit set to 0x1) to minimize the total quiescent current of the device.
(2) Validated by design.
(3) BOS1921 only.

5.5 Timing Characteristics

5.5.1 I²C

Table 7: Timing characteristics. Condition: I²C communication mode, T_A = 25°C, V_{DDIO} = 1.8 V, SDA/SCL load = 50 pF

			FAST MODE		FAST MODE +		
	SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNIT
1	f_{SCL}	SCL clock frequency(1)	0	0.4	0	1.0	MHz
2	t_{LOW}	SCL low period	1300		500		ns
3	t_{HIGH}	SCL high period	600		260		ns
4	t_R	SDA/SCL rise time(1)	20	300	-	120	ns
5	t_F	SDA/SCL fall time(1)	-	300	-	120	ns
6	t_{SU_DAT}	Data setup time(1)	100		50		ns
7	t_{HD_DAT}	Data hold time(1)	0	-	0	-	ns
8	t_{SU_STA}	Setup time for a repeated START condition(1)	600		260		ns
9	t_{HD_STA}	Hold time for a (repeated) START condition(1)	600		260		ns
10	t_{SU_STO}	Setup time for STOP condition(1)	600		260		ns
11	t_{BUF}	Bus free time (time between the STOP and START conditions) (1)	1300		500		ns
12	t_{SPIKE}	Spike suppression pulse width(1)	0	50	0	50	ns

(1) Validated by design.

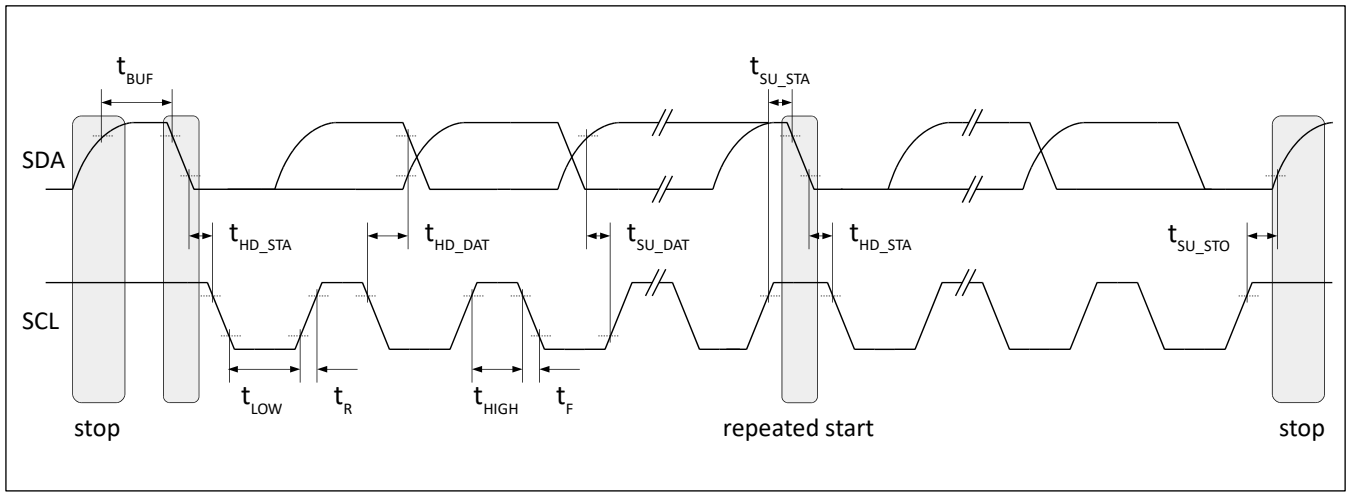


Figure 4: I²C timing diagram

5.5.2 I3C

Table 8: Timing characteristics. Condition: I3C push-pull, T_A = 25°C, V_{DDIO} = 1.8 V, SDA/SCL load = 50 pF

	SYMBOL	PARAMETER	MIN	MAX	UNIT
1	f_{SCL}	SCL clock frequency (1)	0.01	12.5	MHz
2	t_{LOW}	SCL low period	24		ns
3	t_{HIGH}	SCL high period	24	41 (2)	ns
4	t_{CR}	SCL rise time (1)		The minimum between whether 150×106/f_{SCL} or 60	ns
7	t_{CF}	SCL fall time (1)		The minimum between whether 150×106/f_{SCL} or 60	ns
8	t_{SU}	Data setup time	3		ns
9	t_{HD} (controller)	Data hold time	tCR +3, tCF +3		ns
10	$t_{HD\ (target)}$	Data hold time	0		ns
11	t_{CBSr}	Clock before repeated START condition (1)	19.2		ns
12	t_{CAS}	Clock after START condition (1)	38.4		ns
13	t_{CASr}	Clock after repeated START condition (1)	38.4		ns
14	t_{CBP}	Clock before STOP condition (1)	19.2		ns
15	t_{AVAL}	Bus available (1)	1		µs

(1) Validated by design.
(2) This maximum high period may be exceeded when the signals can be safely seen by legacy I^2C devices.

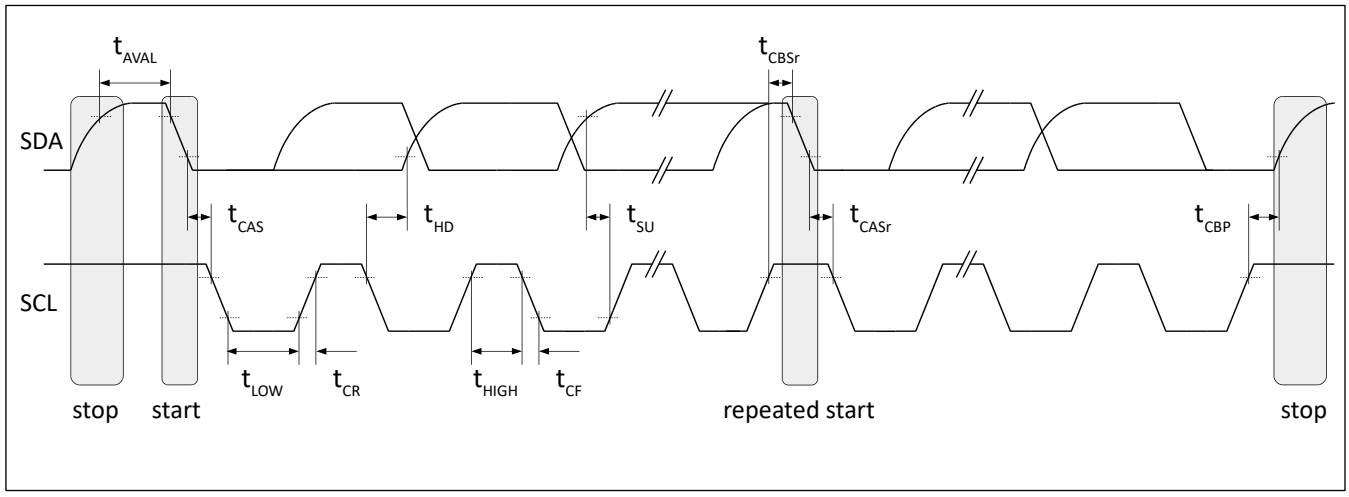


Figure 5: I3C push-pull timing diagram

5.6 Typical Performance Characteristics

Typical performance characteristics for the following conditions: T_A = 25°C, V_{BUS} = 3.6 V, C_L = 100 nF, V_{OUT} = 190 V_{pk-pk} and f_{OUT} = 200 Hz (unless otherwise noted).

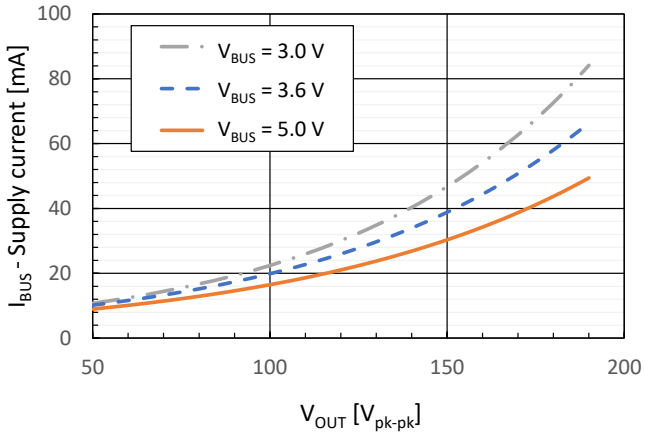


Figure 6: Supply Current vs Output Voltage

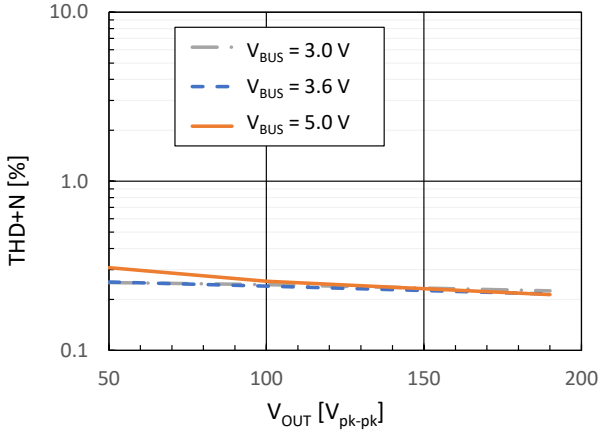


Figure 7: Total Harmonic Distortion + Noise vs Output Voltage

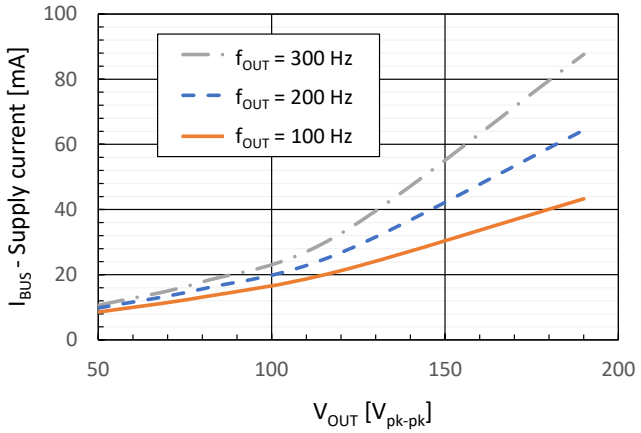


Figure 8: Supply Current vs Output Voltage

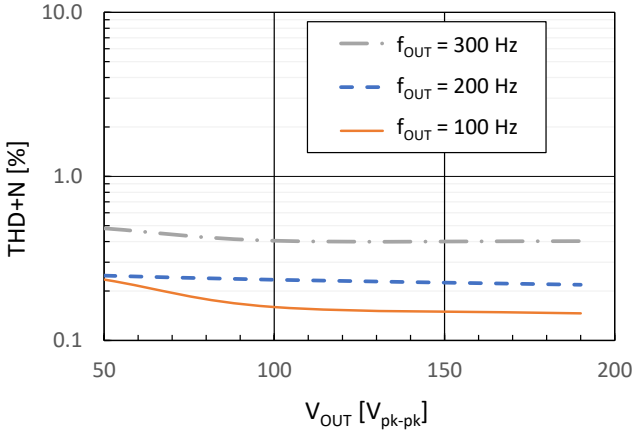


Figure 9: Total Harmonic Distortion + Noise vs Output Voltage

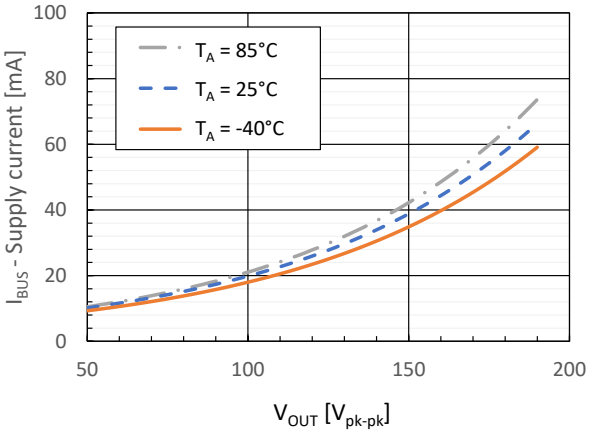


Figure 10: Supply Current vs Operating free-air Temperature

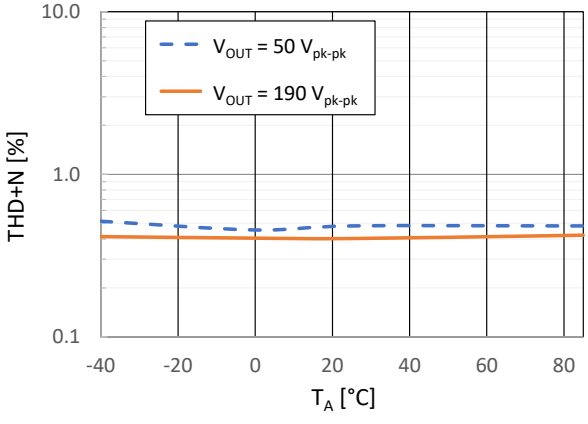


Figure 11: Total Harmonic Distortion + Noise vs Operating free-air Temperature

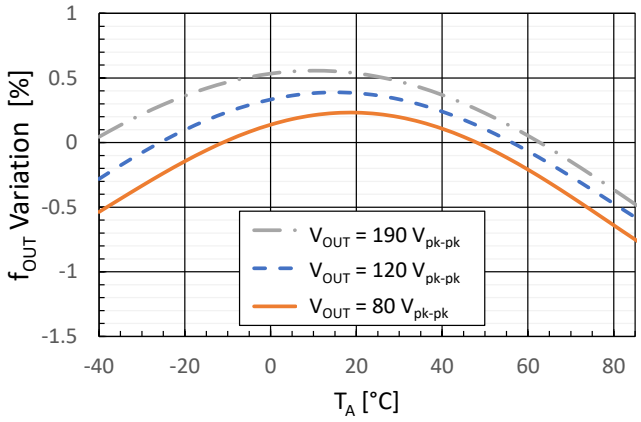


Figure 12: Output Frequency Variation vs Operating free-air Temperature

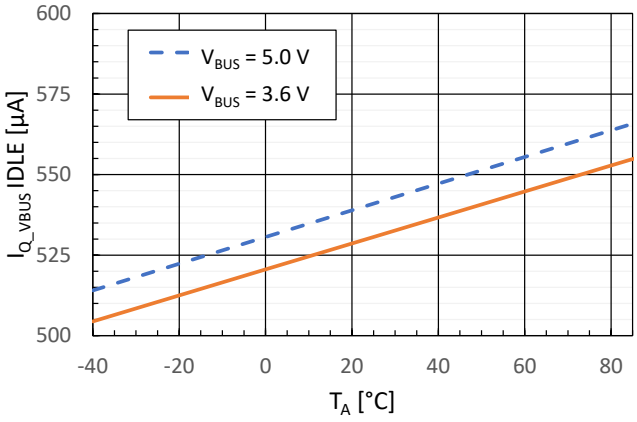


Figure 13: Supply Quiescent Current in IDLE Mode vs Operating free-air Temperature

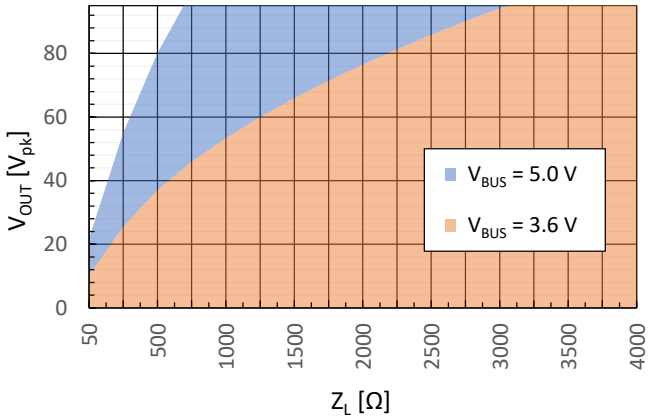


Figure 14: Safe Operating Area at I_{SW} max

6 Functional Description

6.1 Overview

The BOS1921/BOS1931 is a highly integrated low-power piezo actuator driver with an integrated digital front end and energy recovery, based on Boreas's patented CapDrive™ technology. The device requires a single low-voltage supply and 7 passive components to generate waveforms of up to 190 V_{pk-pk}.

The digital interface enables the transmission of the digital waveform data from any MCU with an I3C or I^2C interface to the BOS1921/BOS1931. A flexible FIFO interface enables the generation of haptic playback by streaming the digital waveform data or transmitting the digital waveform data in groups for more bandwidth efficiency. Waveforms can be generated by reading data from the FIFO at various sampling rates.

The BOS1921/BOS1931 integrates a Waveform Synthesizer (WFS) and a 2 kB on-chip 1024×16 RAM that enable haptic waveform generation using RAM Playback mode and RAM Synthesis mode. The WFS allows the generation of customized continuous haptic waveforms with minimal intervention by the host MCU.

The BOS1921 features an advanced sensing interface that allows mechanical buttons to be replaced with an enhanced user interface. Piezo actuator press/release trigger conditions allow the detection of an interaction with a piezo actuator and automatically trigger haptic waveform feedback within 30 µs. A GPIO pin can be used as an interrupt to indicate the MCU that a sensing voltage event has occurred or a change in the device state.

The BOS1921/BOS1931 can use any commercial off-the-shelf (COTS) inductor. The inductor value can be chosen to optimize the power, size or performance depending on the user's application. With a start-up time of less than 300 µs from its low-power mode, the device can be used in applications requiring low latency.

6.2 Features

6.2.1 Digital Front-End Interface

The BOS1921/BOS1931 uses an I3C target interface supporting SDR communication up to 12.5 Mbps. This high-speed communication interface enables multiple ICs to share a common communication bus. Its digital front-end enables waveform data to be stored in memory. The digital interface also provides access to internal registers which control the BOS1921/BOS1931 operation and performance, see section 6.3 for more details.

6.2.2 GPIO

A General-Purpose Input / Output (GPIO) pin in the VDDIO domain is available and supports an open-drain (default) or push-pull configuration. The GPIO is active-low and can be used as an interrupt to notify the host MCU of various events such as sense voltage events or an error. The GPIO can also be used as an input to trigger a predefined haptic waveform output.

The GPIO pin can be configured with the following register bits:

- COMM.GPIODIR is used to set the GPIO pin as input or output.
- COMM.GPIOSEL[2:0] is used to select the signal that is output to the GPIO pin.
- COMM.OD is used to set the GPIO pin to push-pull or open-drain configuration.

6.2.3 Flexible Waveform Generation

The output waveform voltage range can be selected between ±95 V and ±13.25 V as detailed in Table 9.

Table 9: Output Voltage Ranges List

REGISTER	REGISTER VALUE	OUTPUT RANGE (V)	OUTPUT RESOLUTION (V)
CONFIG.GAIND	0x1	±13.25	0.0076
CONFIG.GAIND	0x0	±95	0.0545

6.2.3.1 Direct Mode

With PLAY_MODE[1:0] bits set to 0x0, the haptic waveform samples are played as they are sent from the host MCU to the RAM using REFERENCE register. The rate at which the RAM data is read to generate the haptic waveform is set by PLAY_SRATE[2:0] bits. See section 6.5 for details.

6.2.3.2 FIFO Mode

The digital front-end gives access to RAM as a 1024-sample FIFO for waveform playback with PLAY_MODE[1:0] bits set to 0x1. FIFO entries are appended every time waveform samples are written in the REFERENCE register. Digital samples are represented as 12-bit unsigned values. If OE bit is set to 0x1, the FIFO entries are read automatically out of the FIFO at a rate set by PLAY_SRATE[2:0] bits. See section 6.6 for details.

6.2.3.3 RAM Playback Mode

RAM Playback mode is selected with PLAY_MODE[1:0] bits set to 0x2. In RAM Playback mode, on-chip RAM of 2 kB is used to store arbitrary haptic waveforms as waveform amplitude samples in 12-bit unsigned format. The waveform is sampled at a rate set by PLAY_SRATE[2:0] bits. See section 6.7 for more details.

6.2.3.4 RAM Synthesis Mode

RAM Synthesis mode is selected with bits PLAY_MODE[1:0] set to 0x3. With this mode, the BOS1921/BOS1931 uses the Waveform Synthesizer (WFS) to generate waveforms using parameters stored in the 2 kB RAM. RAM Synthesis mode allows generation of sine waveforms of various amplitudes and frequencies without having to send every sample of the waveform to RAM as is the case with RAM Playback mode. This allows complex waveforms to be produced with minimal data communication. See section 6.8 for details.

6.2.4 Piezo Sensing (BOS1921 Only)

The BOS1921 can use a piezo actuator as a force sensor by measuring the voltage across its terminals.

The BOS1921 also features an embedded sensing comparator that can be configured to automatically trigger an already programmed waveform.

The GPIO pin can inform the MCU that a sensing voltage event occurred or a triggered waveform has finished playing using GPIOSEL[2:0] bits. Voltage sensed is available with SENSE_VALUE[11:0] bits, which can be read at any time when sensing is activated (CONFIG.SENSE bit set to 0x1) and is useful for MCU-based customized sensing algorithms. See section 6.4 for more detail.

The sensing resolution can be selected between 7.6 mV and 54.5 mV as detailed in Table 10.

Table 10: Sensing Ranges List

REGISTER	REGISTER VALUE	INPUT RANGE (V)	SENSING RESOLUTION (V)
CONFIG.GAINS	0x1	±13.25	0.0076
CONFIG.GAINS	0x0	±95	0.0545

6.2.5 Continuous Mode

With RAM Synthesis or RAM Playback mode, it is possible to play a waveform for an indefinite amount of time without the intervention of an external MCU. This feature is well suited for cooling or micropump applications that need to operate for long periods of time while minimizing overall system power and resource usage.

6.2.6 SLEEP Mode

When no output waveform is being requested, no sensing is needed (BOS1921 only) and the output is disabled (bit OE set to 0x0), the device can enter in one of its two low-power modes by the use of the bit DS: IDLE or SLEEP mode. By default, power mode is IDLE (bit DS set to 0x0). SLEEP mode is selected when bit DS is set to 0x1.

In SLEEP mode, the BOS1921/BOS1931 preserve its RAM and the contents of the registers by default (RET bit set to 0x0). By setting RET bit set to 0x1, SLEEP mode does not preserve RAM and neither the contents of the registers to reduce the power consumption. Note that to reduce the total quiescent current of the device, the following should be done:

- Disabled state retention (set RET bit to 0x1)
- Power off VDDIO supply.

The BOS1921/BOS1931 wakes up from SLEEP mode when a communication occurs on its I^2C/I3C interface (the data will not have any effect on the configuration of the registers).

6.2.7 Low Latency Startup

The BOS1921/BOS1931 features a fast start-up time. From IDLE or SLEEP mode, the device takes less than 300 µs to start playing the waveform. This makes the device a very small contributor to system latency.

6.2.8 Device Reset

The BOS1921/BOS1931 device has software-based reset functionality. When RST bit is set to 0x1, all registers are set to their default value and IC goes in IDLE state. RST bit self-clears once the reset is complete.

The following sequence must be done to safely reset the device while playing a waveform in FIFO or Direct mode:

1. Set CONFIG.OE bit must be set to 0x0.
2. Wait for the device to be in IDLE by polling IC_STATUS.STATE[1:0] bits.
3. Reset the device by setting RST bit to 0x1.

6.2.9 Device Synchronization

Multiple BOS1921/BOS1931 devices can be synchronized using SYNC pin to play haptic waveforms simultaneously on their respective piezo actuator with a phase delay of less than 2 µs between them.

Synchronization is achieved by connecting the SYNC pin of all devices with each other. A 10 kΩ pull-up resistor is needed between SYNC node and V_{DDIO}. The sequence to use device synchronisation is the following:

1) Set OE bit and SENSE bit to 0x0 on all devices.
2) Set SYNC bit to 0x1 on all devices.
3) For Each devices set OE bit to 0x1. The devices will wait on each other before starting to play the waveform and will synchronize the haptic waveforms within less than 2 µs during playback.

Note that SYNC pin must be tied to ground if unused.

6.2.10 Adjustable Current Limit

The maximum current of the power converter must be limited to avoid damage to both the L_1 inductor and the BOS1921/BOS1931 device by selecting the appropriate R_{sense} value (see section 7.5.3). The BOS1921/BOS1931 determine the current flowing through the L_1 inductor by measuring the voltage drop across R_{sense}, which is positioned between the RP/VDD and RM pins.

The current limit flowing through SW pin should be selected based on the following:

- Ensure that the current is lower than the saturation limit of the inductor L1.
- Ensure that the current is high enough to allow sufficient energy transfer to and from the piezo actuator.

The solution should be tested during its worst-case operation to ensure that the BOS1921/BOS1931 meets the bandwidth requirement of the application.

6.2.11 Internal Charge Pump

The BOS1921/BOS1931 has an internal 5 V charge pump which requires a 0.1 µF capacitor (C_{PUMP}) with a 6.3 V voltage rating or more to be connected on HV pin.

6.2.12 Energy Recovery

The BOS1921/BOS1931 IC implements bidirectional power transfer: input to output, and output to input. Such architecture enables the recovery of the energy accumulated on the capacitive load and transfers it back to the input. The internal controller automatically determines the direction of the power flow during waveform playback.

6.2.13 Unidirectional Power Input (UPI)

The BOS1921/BOS1931 can sink and source current from the power delivery network (PDN) during normal operation thanks to its energy recovery feature. If the PDN can't sink current (e.g., if the device is powered by batteries), the Unidirectional Power Input (UPI) must be configured by setting UPI bit to 0x1. UPI allows the device to appear as a resistive load to the power supply (the device only sinks current) and reducing RMS current flowing in the PDN. UPI does not affect the efficiency of the BOS1921/BOS1931, but it causes the following to happen:

- First, power is drawn from the input source when the amplitude of the output waveform increases.
- Second, energy recovered accumulates on the input capacitor (C_{VDD}) when the amplitude of the output waveform decreases.

Energy accumulation on the C_{VDD} capacitor causes the voltage at VDDP pin to increase, as shown in Figure 16. The voltage increase can be adjusted by first calculating the maximum energy that may be recovered

from the load and then sizing C_{VDD} appropriately to achieve the desired voltage increase (see section 7.5.5). Voltage at VDDP pin should never exceed 5.5 V.

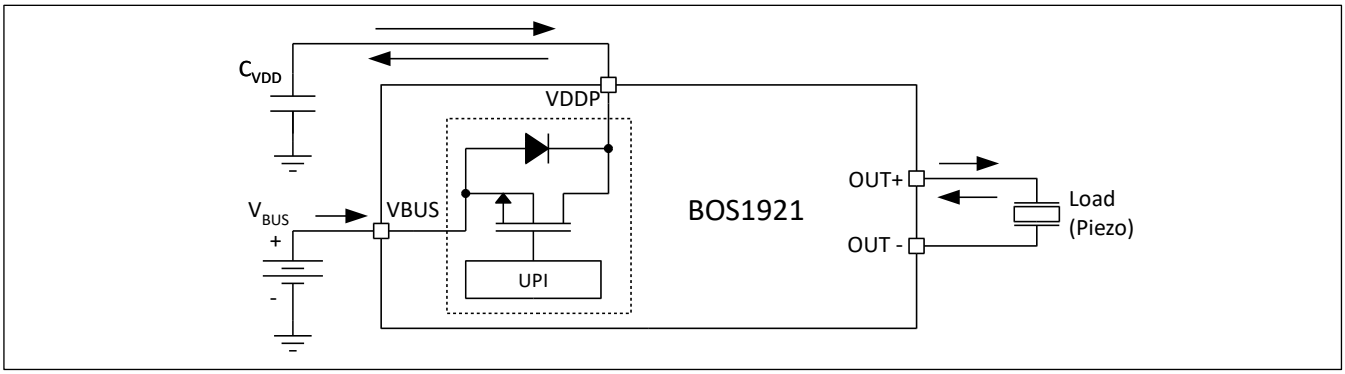


Figure 15: Block diagram of the Unidirectional Power Input (UPI)

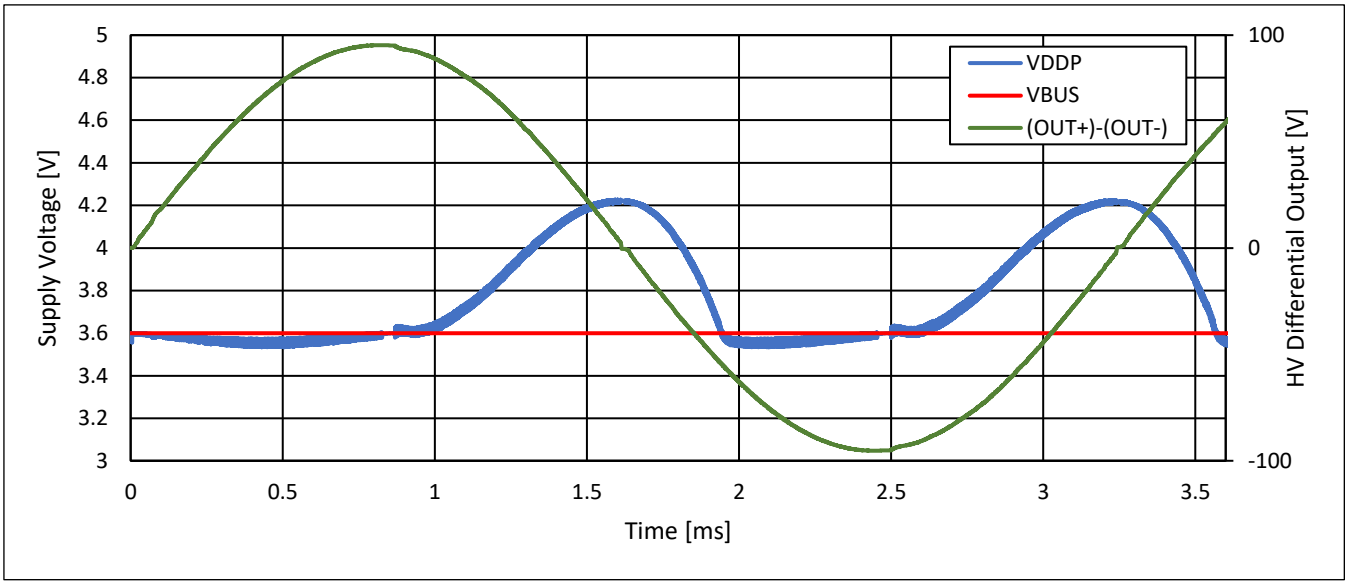


Figure 16: Voltage increases at VDDP pin during energy recovery when bit UPI is set to 0x1, C_{VDD} = 100 µF, C_{Load} = 100 nF

6.2.14 Adjustable Internal Clock

The internal clock oscillator frequency is trimmed during fabrication using hardware fuses. When initialized, the BOS1921/BOS1931 retrieves the hardware fuse values and push them to the TRIM block to adjust the oscillator frequency based on the fuse values (see Figure 34). The TRIM register allows modifying the TRIM values to adjust oscillator frequency.

The feature can be used to match the external system clock frequency with the BOS1921/BOS1931 internal clock frequency, which is used to determine the FIFO read-out rate. This might be needed to minimize waveform distortion if the user writes waveform data at a constant rate to the FIFO, without managing space available in it. To successfully adjust internal clock frequency, OE bit needs to be set to 0x0.

The internal oscillator can be adjusted with the following sequence:

1. Set CONFIG.OE bit to 0x0.
2. Set TRIM.TRIMRW[1:0] bits to one of the following values:
   a. Set to 0x1 to latch the Hardware Fuses to Trim Block and push them to the TRIM register, or
   b. Set to 0x2 to retrieve the oscillator trim value contained in the TRIM block and push the value to the TRIM register.
3. Wait 1 ms.
4. Read TRIM.TRIM_OSC[5:0] bits (using bits COMM.RDADDR[4:0]) to get the internal oscillator trim value specific to the device.
5. In one transaction, set the TRIM register with the following field:
   a. TRIM_OSC[5:0] bits set to the desired value.
   b. TRIMRW[1:0] bits set to 0x3 to write TRIM_OSC[5:0] value to TRIM block.

The same procedure can be used to adjust the internal 1.8 V regulator voltage (pin REG) using bits TRIM.TRIM_REG[2:0] instead of TRIM.TRIM_OSC[5:0] bits.

6.2.15 Fault and Warning Behaviour

This section lists the various faults detected by the device. Note that faults detected by the device may be caused by the following:

- Device operating outside of its safe operating conditions.
- Wrong component value (e.g., R_{sense}, C_{HV}, C_{VDD} or L_1).
- Noise induced by improper printed circuit board layout.

6.2.15.1 Overvoltage Fault

The overvoltage fault is triggered to prevent damage when voltage level on OUT+ or OUT- pin relative to V_{BUS} voltage is outside safe operating conditions. The fault is triggered in the following situations:

- When playing haptic waveforms with high gain in the following conditions:
  - OE bit set to 0x1.
  - SENSE bit set to 0x0.
  - GAIND bit set to 0x0.
  - Voltage level on OUT+ pin relative to V_{BUS} is above 100 V or voltage level on OUT- pin relative to V_{BUS} is below -100 V.
- When playing haptic waveforms with low gain in the following conditions:
  - OE bit set to 0x1.
  - SENSE bit set to 0x0.
  - GAIND bit set to 0x1.
  - Voltage level on OUT+ pin relative to V_{BUS} is above 14 V or voltage level on OUT- pin relative to V_{BUS} is below -14 V.
- When using piezo actuator sensing with the BOS1921 and high gain in the following conditions:
  - OE bit set to 0x1.
  - SENSE bit set to 0x1.
  - GAINS bit set to 0x0.
  - Voltage level on OUT+ pin relative to V_{BUS} is above 100 V or voltage level on OUT- pin relative to V_{BUS} is below -100 V.

- When using piezo actuator sensing with the BOS1921 and low gain in the following conditions:
  - OE bit set to 0x1.
  - SENSE bit set to 0x1.
  - GAINS bit set to 0x1.
  - Voltage level on OUT+ pin relative to V_{BUS} is above 14 V or voltage level on OUT- pin relative to V_{BUS} is below -14 V.

If an overvoltage condition is detected during waveform generation, the following events occur:

- IC_STATUS.OVV fault bit is set.
- IC_STATUS.STATE[1:0] bits are changed to 0x3 (ERROR state).
- Output voltage ramp down to VDD.

The OVV bit will clear automatically and the BOS1921/BOS1931 state will change to IDLE (bits STATE[1:0] set to 0x0) with the following conditions:

- OE bit is 0x0.
- Output voltage is lower than the maximum allowed $V_{OUT(FS)}$.

6.2.15.2 Output Short Circuit Fault

The BOS1921/BOS1931 has an output short circuit protection to prevent excessive current to flow because of a shorted load. In case a short circuit is detected, the following events occur:

- IC_STATUS.SC fault bit is set.
- IC_STATUS.STATE[1:0] bits are changed to 0x3 (ERROR state).
- Output voltage ramp down to VDD.

The SC bit will clear automatically and the BOS1921/BOS1931 state will change to IDLE (bits STATE[1:0] is 0x0) with the following conditions:

- Bit OE is 0x0.
- Output voltage is lower than the maximum allowed $V_{OUT(FS)}$.

6.2.15.3 Over Temperature Fault

The BOS1921 has an internal temperature sensor that puts the BOS1921/BOS1931 in ERROR state in case the die junction temperature exceeds 145 °C. In this case, the following events occur:

- IC_STATUS.OVT fault bit is set.
- IC_STATUS.STATE[1:0] bits are changed to 0x3 (ERROR state).
- Output voltage ramp down to VDD.

The OVT bit will clear automatically and the BOS1921/BOS1931 state will change to IDLE (STATE [1:0] bits are 0x0) with the following conditions:

- OE bit is 0x0.
- Output voltage is lower than the maximum allowed $V_{OUT(FS)}$.

The low power dissipation of the BOS1921/BOS1931 makes it unlikely that its temperature will reach 145 °C even when it is continuously operated at the maximum Z_L in the operating temperature range T_A.

6.2.15.4 Under Voltage Fault

The BOS1921/BOS1931 monitor V_{BUS}, and if its voltage is below 2.875 V during waveform generation, the following events occur:

- IC_STATUS.UVLO bit is set.
- IC_STATUS.STATE[1:0] bits are changed to 0x3 (ERROR state).
- Output voltage ramp down to V_{DD}.

UVLO bit will self-clear and the BOS1921/BOS1931 state will change to IDLE (STATE[1:0] bits are set to 0x0) with the following conditions:

- OE bit is 0x0.
- Output voltage is lower than the maximum allowed $V_{OUT(FS)}$.

6.2.15.5 Current Detection Status Fault

For proper operation, the BOS1921 monitors the current using R_{sense} resistor connected to RP and RM pins. If no current is detected during waveform generation, the following event occurs:

- IC_STATUS.IDAC fault bit is set.
- IC_STATUS.STATE[1:0] bits are changed to 0x3 (ERROR state).

IDAC errors are typically triggered by incorrect component sizing (see section 7.5) or inadequate waveform data. If component sizing and waveform data are correct, see section 6.2.18 for details on other circumstances that can cause an IDAC error and strategies to avoid them.

To recover from an IDAC error, a software reset must be done using CONFIG.RST bit. IC_STATUS.IDAC bit does not self-clear.

6.2.15.6 Maximum Power Warning

During waveform playback, if the current in R_{sense} is equal or greater to the current limit defined in section 7.5.3, a maximum power warning is raised, and the following happens:

- IC_STATUS.MXPWR warning bit is set.
- IC_STATUS.STATE[1:0] bits remain 0x2 (RUN state).
- The waveform continues to play but is likely distorted.

IC_STATUS.MXPWR bit does self-clears when the current in R_{sense} is lower than current limit defined in section 7.5.3.

6.2.15.7 Brownout

The BOS1921/BOS1931 has internal brownout protections and if V_{REG} goes below 1 V. In this case, the following event occurs:

- The chip issues a reset signal, and all registers are set to their default values.

When V_{REG} goes back to its specified operating voltage, the BOS1921/BOS1931 will be in IDLE state (STATE[1:0] bits set to 0x0).

6.2.16 Output Timeout

Setting TOUT bit to 0x1 enables a timeout mechanism that forces the BOS1921 into SLEEP mode if no new communication has been received within 4 ms while playing a waveform in Direct or FIFO mode (PLAY_MODE[1:0] bits set to 0x0 or 0x1).

Note that PLAY_SRATE[2:0] bits are reset to 0x7 when the device enters SLEEP following a timeout event.

More specifically, the BOS1921/BOS1931 enters SLEEP mode when the following conditions are met:

- COMM.TOUT bit is set to 0x1.
- CONFIG.OE bit is set to 0x1.
- PLAY_MODE[1:0] bits are set to 0x0 or 0x1.
- The FIFO is empty when using FIFO mode (PLAY_MODE[1:0] bits set to 0x1).
- The BOS1921/BOS1931 did not receive any communication on its digital interface for more than 4 ms.

6.2.17 Interrupt

The BOS1921/BOS1931 features interrupt capabilities for different events enabled with the INT_ENABLE register. The status of interrupts is read with the INT_STATUS register.

The GPIO pin can be used to notify the MCU when one of the interrupts has occurred by setting GPIOSEL[2:0] bits set to 0x5.

There are up to 7 distinct interrupt events that can be configured. Each event can be enabled by programming the corresponding bit in the INT_ENABLE register. A bit in the INT_STATUS register is set when the condition corresponding to its event changes from *false* to *true* (i.e. rising edge condition).

All the INT_STATUS register bits are automatically cleared in the following situations:

- INT_STATUS register is read
- A soft reset is performed
- Device goes to SLEEP

The INT_STATUS register bits are not cleared when setting its corresponding INT_ENABLE register bits to 0x0.

Note that if the interrupt condition is already *true* when the interrupt is enabled, the interrupt can be immediately triggered and its corresponding INT_STATUS register bits will be set to 0x1. It is thus recommended to clear any existing interrupt by reading INT_STATUS register after enabling interrupts.

Note that the desired PLAY_MODE bits should be set prior to configure interrupts.

The INT_ENABLE register can be used to enable interrupts on the following events:

- IE_FHE bit enables an interrupt when FIFO is at least half empty. Interrupt triggers when FIFO is more than half empty.
- IE_STCHG bit enables an interrupt when the BOS1921/BOS1931 state change. Interrupt triggers when STATE[1:0] bits changed.
- IE_MXERR bit enables an interrupt when there is a difference between the waveform played on the output and the setpoint.
- IE_SENSF bit enables an interrupt when a sensing event occurred (BOS1921 only), i.e., it triggers when SENS_FLAG bit is set to 0x1.
- IE_PLAY bit enables an interrupt when the waveform playback status is set, i.e., it triggers when PLAYST bit is set to 0x1.
- IE_MAXP enables an interrupt when a maximum power error occurred, i.e., it triggers when MXPWR bit is set to 0x1.
- IE_ERR enables an interrupt when the BOS1921/BOS1931 state changes for ERROR, i.e., it triggers when STATE[1:0] bits are set to 0x3.

The following sequence presents an example on how to use the interrupt feature along with FIFO mode:

1. Set CONFIG.PLAY_MODE[1:0] bits to 0x1 to select FIFO mode.
2. Set bit CONFIG.OE to 0x1 to enable the output.
3. Set INT_ENABLE.IE_FHE bit to 0x1 to enable the interrupt when the FIFO is half empty.
4. Set COMM.RDADDR[4:0] bits to 0x1F and read the INT_STATUS register to clear existing interrupt.
5. Set GPIOSEL[2:0] bits to 0x5 to output the interrupt on the GPIO pin.
6. Set COMM.RDADDR[4:0] bits to 0x11, read FIFO_STATE register and use FIFO_STATE.FIFO_SPACE[9:0] bits to determine space available in FIFO for new data.
7. Write as many 12-bit waveform data as possible according to space available in FIFO into the REFERENCE register.
8. Wait for a falling edge on the GPIO pin to occur, which indicates an interrupt occurred.
9. Set COMM.RDADDR[4:0] bits to 0x1F and read the INT_STATUS register. The INT_STATUS.IS_FHE bit should be 0x1 and will be immediately cleared after reading register.
10. Repeat steps 5 to 8 until the desired waveform is completed.

6.2.18 Output Bridge Protection

The BOS1921/BOS1931 includes a protection preventing the internal output bridge from changing polarity if a voltage greater than 4.4 V is present between the OUT+ and OUT- pins when playing a waveform. This protection is essential especially for BOS1921 when using sensing feature since the voltage on the piezoelectric ceramic terminal increases or decreases as it is deformed. Residual voltage can thus be present on the output of the BOS1921 when a waveform is requested to be played.

The bridge protection triggers in the following conditions:

- Play a positive haptic waveform when a negative voltage smaller than -4.4 V has built up on the piezoelectric ceramic.
- Play a negative haptic waveform when a positive voltage greater than 4.4 V has built up on the piezoelectric ceramic.

The bridge protection triggering causes a waveform played in the wrong polarity with or without IDAC error (see section 6.2.15.5). The bridge protection triggering can be caused by incorrect component sizing (see section 7.5) or inadequate waveform data.

To prevent the bridge protection to trigger, one could reset the voltage on the piezoelectric ceramic before starting to play the haptic waveform. This can be achieved by playing one of the following sets of data before the desired haptic waveform:

- Several 0 V data points.
- Voltage data points increasing from -2 V to 0 V if a positive waveform is intended to be played.
- Voltage data points decreasing from 2 V to 0 V if a if a negative waveform is intended to be played.

6.3 Digital Interface

A MIPI I3C target port enables communication with the BOS1921/BOS1931. I3C is backward compatible with legacy I^2C devices, but I3C bus supports significantly higher speed. It is used to write data to the registers, whose content can also be read back.

6.3.1 General Communication Protocol

The controller MCU can transfer data with the target BOS1921/BOS1931 using I3C or I^2C standards.

6.3.1.1 Write Transactions

Both I^2C and I3C can do write transactions with the following:

- The first byte contains the register address corresponding to the register to write to.
- Two bytes of register data; the first byte corresponds to the MSBs of the register data and the second byte corresponds to the LSBs of register data.

To write more than one register, three behaviours are possible:

1. Register address = 0x00: All subsequent 2-byte words will automatically be written to the REFERENCE register. The communication frame must be stopped from accessing the other registers.
2. STR bit set to 0x1: The register address other than 0x00 will automatically be incremented every two bytes to allow writing multiple registers in the same transmission frame and reduce the number of bits used in the communication. The communication frame must be stopped to skip the remaining register addresses.
3. STR bit set to 0x0: A byte of address for each target register must be sent (no automatic address incrementation).

6.3.1.2 Read transactions

Each communication transaction returns two bytes of data corresponding to the value of the register whose address is specified in RDADDR[4:0]. Burst reads are not supported, i.e., it is not possible to read multiple registers in a single access. However, the RDADDR[4:0] bits can automatically be incremented by 1 after each read by setting RDAI bit to 0x1. This allows setting RDADDR[4:0] bits once with the address of the first register to be read, then issuing a sequence of reading accesses to read a series of registers.

6.3.2 I3C Interface

The I3C target functionality implemented in the BOS1921/BOS1931 is based on MIPI® Alliance Specification for I3C℠, version 1.1.1. I3C is a 2-wire bidirectional serial bus which always has one controller and one or more targets. The two wires are designated SDA and SCL: SDA is a bidirectional data signal, SCL is a clock signal. They connect respectively to BOS1921/BOS1931 SDA and SCL pins.

Table 11: Serial interface pin description

PIN NAME	PIN DESCRIPTION
SDA	Bidirectional Data Signal
SCL	Controller Clock Signal

I3C communication is initiated by the controller which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. All I3C communication occurs within a frame. The basic frame begins with a START, followed by the header, the data, and a STOP (see Figure 17 for more details). The header following a START allows for bus arbitration. The controller uses the header to address target device(s). Each target is addressed by a unique 7-bit target address plus a read-write bit.

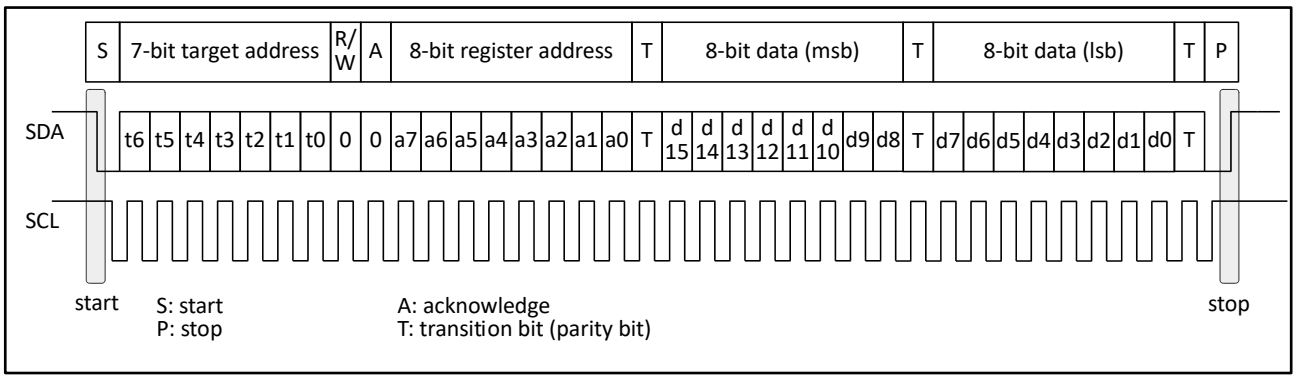


Figure 17: Typical I3C write communication frame

The I3C bus uses transitions on SDA while the clock is at logic high to indicate START and STOP conditions. A high-to-low transition on the SDA signal indicates a START, and a low-to-high transition indicates a STOP. All devices share the same SDA signals through a bidirectional bus using a wired-AND connection. The data transition on SDA must occur while the clock period is low.

The implemented I3C target of the BOS1921/BOS1931 has a legacy I^2C default static address (7'h44). The 4 LSBs of the address can be changed by assigning the I2C_ADDR bits. The BOS1921/BOS1931 will act as an I^2C target using that address up until it is assigned a dynamic address. Once assigned a dynamic address, the BOS1921/BOS1931 will only operate as an I3C target until it is reset.

A 50 ns spike filter is included in the BOS1921/BOS1931. By default, the spike filter is active at power up. To operate in I3C, the user first needs to write to the broadcast address 0x7E at I^2C speed. The filter will automatically be deactivated, and the user can then use I3C communication speed.

6.3.2.1 I^2C Communication

The BOS1921/BOS1931 acts by default as an I^2C target using its static address (7'h44). Figure 18 shows a basic data-transfer sequence with I^2C static addressing. Following a START, the controller generates the 7-bit target address and the read-write (R/W) bit to communicate with a target device. The target device then holds the SDA signal low during the next clock period to indicate acknowledgment to the controller. When this acknowledgment occurs, the controller transmits the next byte(s) of the sequence.

There are two addresses used to access a register. The first is the target address used to select the BOS1921/BOS1931. The second address is an 8-bit register address sent in the first byte transferred in a write operation. The register address points to a specific register (section 6.10). Automatic increments of address pointer can be set using STR bit. The address pointer is automatically incremented every two bytes, allowing continuous write operations.

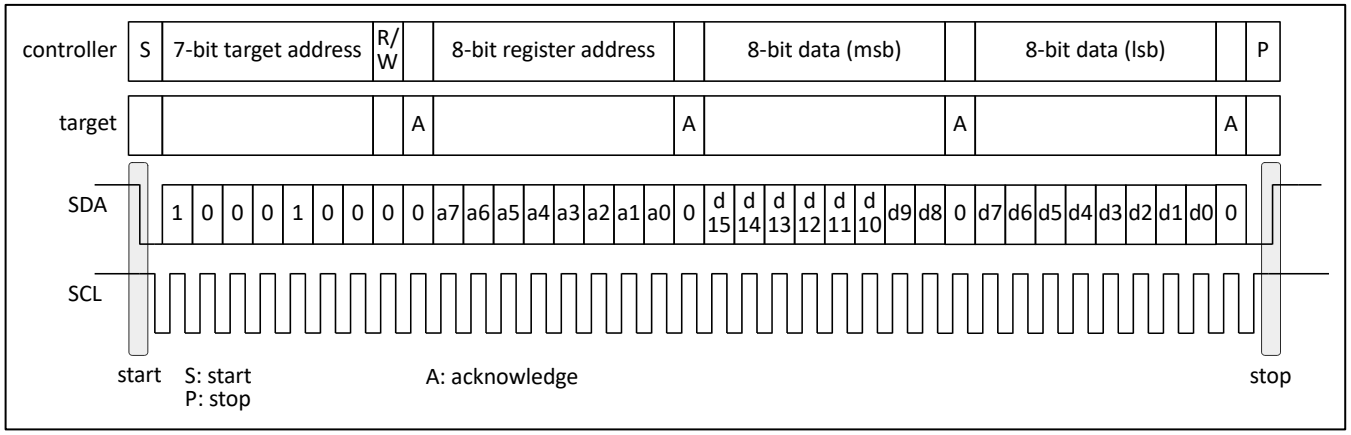


Figure 18: Basic data transfer write sequence with I²C static addressing

Figure 19 presents a typical communication sequence in I²C. MSB is always sent first.

A typical write sequence from power up is the following:

1. Write with static address 0x44 with dummy data to wake-up the device.
2. Configure registers as needed.

Figure 20 presents a single communication transaction to access several main registers using STR bit set to 0x1 to access several main registers.

A 50 ns spike filter is included and activated at power up.

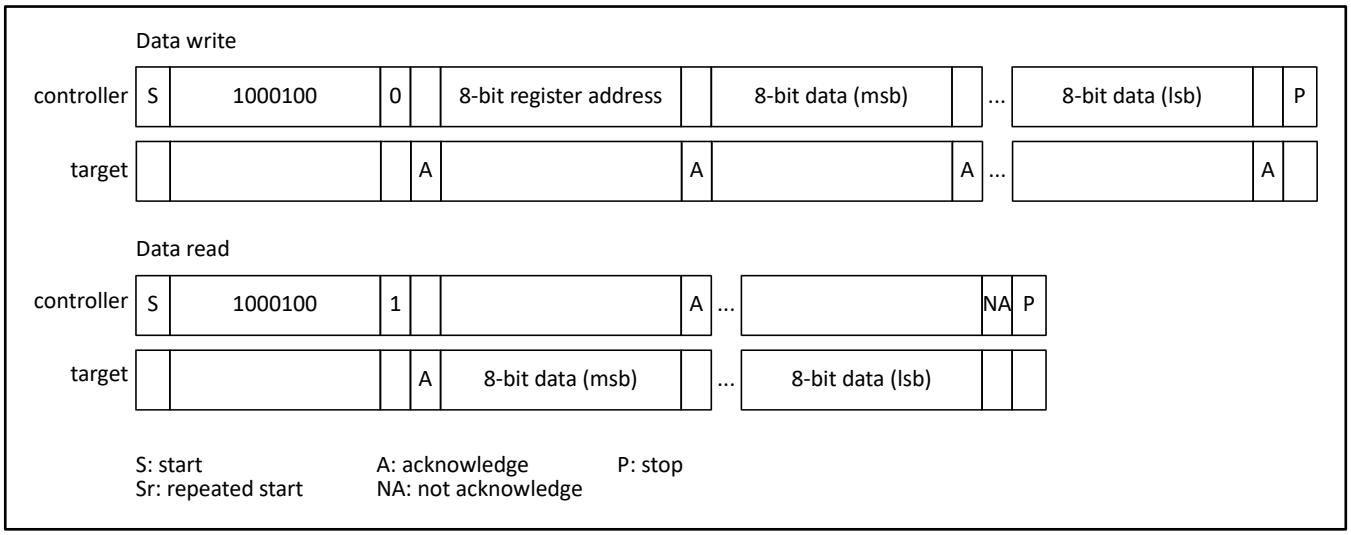


Figure 19: Typical data-transfer sequences with I²C static addressing

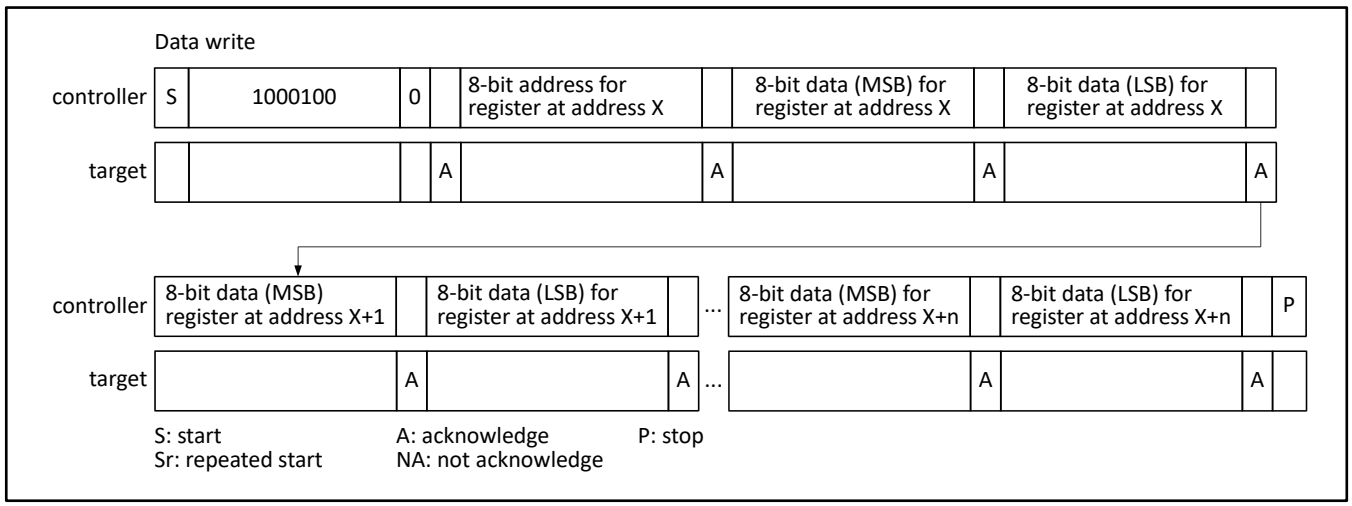


Figure 20: Typical data-transfer sequences with I²C static addressing with STR bit set to 0x1

6.3.2.2 I3C Communication

BOS1921/BOS1931 I3C interface is compliant with MIPI® Alliance Specification for I3C^{SM}, version 1.1.1 and features the following:

1. Target only
2. SDR (Single Data RATE) up to 12.5 MHz
3. I²C compatibility with static address: 7'h44
4. Supports basic Common Command Codes (CCC) (see Table 12 for more details)
5. Does not support Hot Join (HJM)
6. Does not support In-Band Interrupt (IBI)
7. Provisional ID = 0x08A207814000 (see Table 13 or more details)
8. Bus Characteristic Register = 0x00
9. Device Characteristic Register = 0x25

Table 12: Common Command Codes (CCC) support

COMMAND NAME	TYPE	CODE	DESCRIPTION
ENEC	Broadcast	0x00	Enable events command
DISEC	Broadcast	0x01	Disable events command
ENTAS0	Broadcast	0x02	Enter activity state 0
ENTAS1	Broadcast	0x03	Enter activity state 1
ENTAS2	Broadcast	0x04	Enter activity state 2
ENTAS3	Broadcast	0x05	Enter activity state 3
RSTDAA	Broadcast	0x06	Reset dynamic address assignment
ENTDAA	Broadcast	0x07	Enter dynamic address assignment
ENEC	Direct	0x80	Enable events command
DISEC	Direct	0x81	Disable events command
ENTAS0	Direct	0x82	Enter activity state 0
ENTAS1	Direct	0x83	Enter activity state 1

COMMAND NAME	TYPE	CODE	DESCRIPTION
ENTAS2	Direct	0x84	Enter activity state 2
ENTAS3	Direct	0x85	Enter activity state 3
RSTDAA	Direct	0x86	Reset dynamic address assignment
SETNEWDA	Direct	0x88	Set new dynamic address
GETPID	Direct	0x8D	Get provisional ID
GETBCR	Direct	0x8E	Get bus characteristics register
GETDCR	Direct	0x8F	Get device characteristics register
GETSTATUS	Direct	0x90	Get device status
GETCAPS	Direct	0x95	Get HDR Capability

Table 13: Defaults provisional ID details

FIELD	WIDTH	VALUE
Provisional ID (default)	48	0x08A207814000
Manufacturer ID	15	0x0451
Part ID	16	0x0781
Instance ID	4	0x4 (I2C_ADDR[3:0])
Vendor Defined	12	0x000

The BOS1921/BOS1931 will operate as an I3C target only after it is assigned a dynamic address by the controller using command ENTDAA with I^2C timing constraints. A dummy write to address 0x7E can be performed prior to ENTDAA command to clear the 50 ns spike filter and enable communication at I3C speed without I^2C constraints. A typical write sequence from devices power up is the following:

1. Send start condition with broadcast address 0x7E at I^2C speed to clear I^2C spike filter.
2. Send ENTDAA command.
3. Wake-up the chip with a dummy write.
4. Configure registers as needed.

6.3.3 Resolving I^2C/I3C Address Conflicts

It is possible to connect multiple BOS1921/BOS1931 on the same I^2C or I3C bus. By default, they all have the same address, so they all respond simultaneously to the same commands. However, it is possible to assign different addresses to each IC to allow accessing each one individually. The process requires to first configure the GPIO as a "Chip Select" before setting the I2C_ADDR[3:0] bits. The procedure is the same for I^2C or I3C protocols, but I3C mode requires the additional steps of resetting and reassigning the dynamic address after having set I2C_ADDR[3:0] bits (see section 6.3.2.2).

The steps to reassign the I²C target address are the following:

1. Set the COMM.GPIODIR bit to 0x1 bit to use the GPIO as an input.
2. Apply a logic level low on the target device GPIO pin.
3. Set the SUP_RISE.I2C_ADDR[3:0] bits with the desired target device address. The new address will take effect immediately.
4. Wait at least 1 µs after the completion of the I²C access performed during the previous step, after which the GPIO pin no longer needs to be used to access to the target device.
5. Using the new I²C address, perform a register access to make sure that the address change was successful.

Note that in I3C Mode the SUP_RISE.I2C_ADDR[3:0] bits are used to set the 4-bit Instance ID (i.e., bits [15:12] of the Provisional ID, see Table 13).

6.4 Piezo Actuator Sensing (BOS1921 Only)

The BOS1921 can sense the voltage across a piezo actuator and use it as a force sensor. The sensed voltage can be read to implement a custom detection algorithm.

The device can also be configured to generate an event when a sensing voltage threshold has been crossed. The sensed voltage event can result in the following:

1. Sense Voltage Alert: alert a MCU of the sensed voltage event.
2. Sense Voltage Trigger for Automatic Haptic Playback: The communication frame must be stopped to access other registers.

The following notes apply to the piezo actuator sensing feature:

- The CONFIG.SENSE bit activates the sensing of the actuator voltage without forcing a voltage on OUT+ and OUT- pins. This bit allows the piezo actuator voltage to vary freely as the user physically interacts with it.
- The CONFIG.OE bit enables the measurement of the HV pin voltage by the device, which is required for sensing feature to work.
- No haptic waveform should be playing while setting CONFIG.SENSE bit to 0x1. Wait until the IC_STATUS.PLAYST bit is 0x1 before setting CONFIG.SENSE bit to 0x1.
- When sensing is activated, no haptic waveform can be output.
- One can activate piezo actuator sensing feature after playing a haptic waveform by simply setting the CONFIG.SENSE bit to 0x1 (no need to reset the CONFIG.OE bit to 0x0 and set it back to 0x1).
- To stop the sensing feature, it is recommended to reset the device using RST bit to reset registers and RAM.

6.4.1 Sensed Voltage Reading

The sensed voltage can be read at any time to implement more complex sensing algorithms running in a MCU such as slope detection or voltage profile pattern recognition.

When sensing is activated, sensed voltage is continually updated and pushed to the SENSE_VALUE register so the latest value can be read at any time. There is no required reading rate.

Note that SENSE_VALUE[11:0] bits set to 0x0 means that the differential voltage is 0 V. However, when the circuit is in sensing and no signal is generated by a piezo actuator, a negative differential voltage of approximately -350 mV is read.

The following bits of the SENSE_VALUE register are used to read sensed voltage:

- SENSE_VALUE[11:0] bits are the 12-bit signed representation of the sensed voltage.
- SENSE bit indicates if sensing mode is activated.

6.4.1.1 Polling Sequence Example

A typical communication sequence to poll the sensed voltage is as follows:

1. Set CONFIG.ONCOMP to 0x0 to prevent sensed voltage from triggering a sensing event.
2. Set CONFIG.SENSE to 0x1 to enable piezo actuator sensing.
3. Set CONFIG.OE to 0x1 to start sensing.
4. Read SENSE_VALUE[11:0] bits.
5. Repeat the step 4) as needed.

6.4.2 Sense Voltage Alert

An internal sensing comparator allows to detect when the sensed voltage on the piezo actuator crosses a configurable threshold voltage. When the detection conditions are met, the SENSE_FLAG bit is set to 0x1. The SENSE_FLAG bit can be reset by reset ONCOMP bit to 0x0.

The sensing voltage alert settings are the following:

- CONFIG.ONCOMP bit enables the embedded comparator which triggers the alert. It must be set to 0x1 to enable comparison.
- SENSING.SIGN defines whether the voltage feedback value must be above or below the threshold for the detection to succeed.
- SENSING.REP[2:0] bits define how long the voltage must be above or below the threshold for detection to succeed (hold time).
- SENSING.STHRESH[11:0] bits define a differential voltage threshold to be crossed for the detection to succeed.
- SENSE_VALUE.SENSE_FLAG bit indicates when a detection has occurred.
- COMM.GPIOSEL[2:0] bits set to 0x6 configure the GPIO pin to indicate when a sense voltage alert has occurred (note that the interrupt mechanism can also be used by setting GPIOSEL[2:0] to 0x5).

6.4.3 Sense Voltage Trigger for Automatic Haptic Playback

The BOS1921 can detect force on the piezo actuator and automatically play a pre-programmed waveform using FIFO (section 6.6), RAM Playback (section 6.7) or RAM Synthesis (section 6.8) modes with minimal intervention needed by the MCU.

GPIO pin can notify the MCU that the waveform playback is completed.

The following is used to enable and monitor Automatic Haptic Playback:

- A waveform must be armed (see section 6.8.7 for an example). The waveform must be armed again each time an automatic waveform playback occurs.
- CONFIG.SENSE bit enables piezo actuator sensing. The bit self-clears and must be enabled again each time an automatic waveform playback occurs.
- CONFIG.ONCOMP bit enables the embedded comparator which triggers the automatic waveform playback. ONCOMP bit must be disabled and then enabled again each time an automatic waveform playback occurs.
- CONFIG.AUTO bit enable Automatic Haptic Playback. The bit self-clears and must be enabled again each time an automatic waveform playback occurs.
- SENSE_VALUE.SENSE_FLAG bit indicates when a detection has occurred.
- IC_STATUS.PLAYST bit indicates when waveform playback has finished.
- COMM.GPIOSEL[2:0] bits set to 0x6 configure the GPIO pin to notify that a sense voltage event has occurred. Note that the interrupt mechanism can also be used by setting GPIOSEL[2:0] to 0x5.

6.4.3.1 Sequence Example for Button Press Sensing with Automatic Playback

A typical communication sequence to configure a press button Automatic Haptic Playback is as follows:

1. Program waveform using RAM Playback (section 6.5) or RAM Synthesis (section 6.8) mode.
2. Set COMM.GPIOSEL[2:0] to 0x6 to be notified on the GPIO pin that a sense voltage event has occurred .
3. Set SENSING.REP[2:0] to 0x5 to set 2048 µs hold time.
4. Set SENSING.THRESH[11:0] to 0x7 to set 750 mV threshold.
5. Set SENSING.SIGN bit to 0x0 to trigger on a voltage above the threshold (detect an increasing voltage).
6. Set CONFIG.AUTO bit to 0x1 to play a pre-programmed RAM Playback or RAM Synthesis waveform automatically on a successful detection.
7. Set CONFIG.ONCOMP bit to 0x1 to enable the embedded sensing comparator.
8. Set CONFIG.SENSE bit to 0x1 to enable piezo actuator sensing.
9. Set CONFIG.OE bit to 0x1 to start sensing.

Note that all bits in CONFIG register may be set in the same I^2C/I3C instruction.

6.4.3.2 Sequence Example for Button Release Sensing with Automatic Playback

Once a detection occurred, sensing can be set again for a release button Automatic Playback using a communication sequence as follows:

1. Set CONFIG.ONCOMP bit to 0x0 to reset the sensing comparator.
2. Arm the next waveform depending on playback mode used as follows:
    a. RAM Playback: issue an RAM PLAYBACK WFS command.
    b. RAM Synthesis: issue an RAM Synthesis WFS command
3. Set SENSING.REP[2:0] to 0x5 to set 2048 µs hold time.
4. Set SENSING.THRESH[11:0] bits to 0xFFE to set -200mV threshold.
5. Set CONFIG.SIGN to 0x1 to trigger a haptic playback on voltage below the threshold (detect a decreasing voltage).
6. Set CONFIG.ONCOMP to 0x1 to enable the sensing comparator.
7. Set CONFIG.SENSE bit to 0x1 to enable piezo actuator sensing.
8. Set CONFIG.AUTO bit to 0x1 to play a pre-programmed RAM Playback or RAM Synthesis waveform automatically on a successful detection.
9. Set CONFIG.OE to 0x1 to start sensing.

Note that all bits in CONFIG register may be set in the same I^2C/I3C instruction.

6.5 Direct Mode

In Direct mode (PLAY_MODE[1:0] bits set to 0x0), the haptic waveform samples are played as they are sent from the host MCU to the REFERENCE register. The rate at which the data is read to generate the haptic waveform is set by PLAY_SRATE[2:0] bits. An interpolation is done between user samples to generate the output waveform when PLAY_SRATE[2:0] bits are 0x1 to 0x7.

Data management and synchronization can be facilitated by setting GPIOSEL[2:0] bit to 0x5 and IE_PLAY to 0x1 to allow the corresponding GPIO to generate an interruption that notifies the MCU when the BOS1921/BOS1931 is ready to receive the next sample. Interpolation between user samples is done to generate the output waveform.

In Direct mode, the RAM is not used, and its content previously written using RAM Playback mode (section 6.7) or RAM Synthesis mode (section 6.8) is preserved.

Note that waveforms should begin and end with 0 V amplitude.

6.5.1 Typical Operation Sequence

The following sequence shows how to use Direct mode to play haptic waveforms:

1. Set COMM.GPIOSEL[2:0] bits to 0x1 to monitor when one more sample is ready to be sent.
2. Set CONFIG.PLAY_MODE[1:0] bits to 0x0 to select Direct mode.
3. Set CONFIG.OE bit to 0x1 to enable output.
4. Write a waveform sample to the REFERENCE[11:0] bits.
5. On a GPIO pin falling edge, go to step 4. to send the next waveform sample to the device.
6. Set CONFIG.OE bit to 0x0 once the desired waveform is completed.

6.6 FIFO Mode

In FIFO mode, the device uses RAM to implement a 1024-sample FIFO. The FIFO entries are appended every time waveform data is written in the REFERENCE register. When output is enabled, the FIFO entries are read automatically out of the FIFO at a rate set by PLAY_SRATE[2:0] bits to output a haptic waveform. An interpolation is done between user samples to generate the output waveform when PLAY_SRATE[2:0] bits are 0x1 to 0x7.

Note the following:

- For waveform playback streaming, the FIFO data write rate must match the readout rate of the waveform playback set by PLAY_SRATE[2:0] bits to always keep valid data inside the FIFO. The PLAYST bit is set to 0x1 when the FIFO becomes empty, causing the FIFO to hold the last valid data and keep the output waveform in a steady state.
- Burst data transfers can be used to minimize the communication interface usage. Packets of 16-bit words can be sent in the same data payload to be written in the FIFO. The FULL bit is set when the FIFO becomes full and cannot accept more data. The FIFO_SPACE[9:0] bits can be read to check available space before sending new data.
- In case OE bit is set to 0x0 during waveform playback, the waveform will continue to play until the FIFO is empty.
- When the FIFO is empty, the last FIFO entry will remain on the device output.
- It is recommended to start and end waveforms with 0 V.
- It is recommended to terminate waveforms with 0 V before setting the OE bit to 0x0, otherwise the output voltage will slowly decrease to 0 V.

6.6.1 FIFO Depth

FIFO mode uses the RAM to implement the FIFO. Using FIFO mode with the default FIFO depth of 1024 locations could overwrite any waveform previously programmed using RAM Playback and RAM Synthesis modes.

FIFO mode can be used jointly with either RAM Synthesis or RAM Playback mode by configuring the FIFO dimension with a smaller number of RAM locations using the FIFO DEPTH command.

6.6.2 Typical Operation Sequence

The following sequence shows how to use FIFO mode to play haptic waveforms:

1. Set CONFIG.PLAY_MODE[1:0] bits to 0x1 to select FIFO mode.
2. Set CONFIG.OE bit to 0x1 to enable the output.
3. Set COMM.RDADDR[4:0] bits to 0x11 and read FIFO_STATE register.
    a. If FIFO_STATE.FULL bit is 0x1 skip to step 5.
    b. If FIFO_STATE.FULL bit is 0x0, use FIFO_STATE.FIFO_SPACE[9:0] bits to determine space available in FIFO for new data.
4. Write as many 12-bit waveform data as possible according to space available in FIFO into the REFERENCE register.
5. Repeat steps 3 and 4 until the desired waveform is completed.
6. Set CONFIG.OE bit to 0x0 once the desired waveform is completed.

In the above example, the output is enabled prior to start filling the FIFO with data. It is also possible to fill the waveform in the FIFO before enabling the output, and then add samples to the FIFO as needed.

6.7 RAM Playback Mode

In RAM Playback mode (PLAY_MODE[1:0] bits set to 0x2), a point-by-point waveform need to be stored in chronological order in the RAM using BURST RAM WRITE command. The waveform is played when the output is enabled (OE bit is set to 0x1).

Note that waveforms should begin and end with 0 V amplitude.

6.7.1 RAM Programming

The samples are written to the RAM using BURST RAM WRITE command. More than one waveform can be stored in the RAM. The 2 kB RAM can store up to 1024 words of 16 bits. Each word is defined by 12-bit data in the same format as the REFERENCE[11:0] bits. Start and end addresses are defined using the RAM PLAYBACK command and indicate the samples to be fetched when the playback is initiated.

When playback starts, the data is read out sequentially at the sample rate set by PLAY_SRATE[2:0] bits. An interpolation is done between user samples to generate the output waveform when PLAY_SRATE[2:0] bits are 0x1 to 0x7.

Once the waveform has been played, it must be rearmed to be played again by writing the RAM start and end addresses again using the RAM PLAYBACK command. The waveform will immediately start if these addresses are set while OE bit is already set to 0x1.

No waveform should be playing while programming RAM to avoid unexpected behaviour.

6.7.2 Continuous Waveform Playback

A waveform can be played continuously by using the RAM PLAYBACK command with the following field:

1. Set the RPT field to 0x1.
2. Set the REPEAT START ADDRESS[9:0] to the RAM address at which the desired continuous waveform starts.
3. Set the END ADDRESS[9:0] to the RAM address at which the desired continuous waveform goes back to the REPEAT START ADDRESS[9:0].
4. Set the START ADDRESS[9:0] to the RAM address at which the waveform starts. The START ADDRESS[9:0] may be different or identical to the REPEAT START ADDRESS[9:0].

The RAM PLAYBACK command allows playing an initial waveform segment only once before looping over an adjacent segment continuously. This is done by specifying a REPEAT START ADDRESS[9:0] located between the START ADDRESS[9:0] and the END ADDRESS[9:0]. The segment between START ADDRESS[9:0] and REPEAT START ADDRESS[9:0] will be played once, then the segment between REPEAT START ADDRESS[9:0] and END ADDRESS[9:0] will be repeated continuously. By specifying the START ADDRESS[9:0] the same as the REPEAT START ADDRESS[9:0], the entire segment is repeated.

To end a waveform being played continuously, a new RAM PLAYBACK command must be issued with RPT field set to 0x0 and the END ADDRESS[9:0] equals to or greater than the END ADDRESS[9:0] of the previous command (the START ADDRESS[9:0] and REPEAT START ADDRESS[9:0] fields will be ignored). Specifying an END ADDRESS[9:0] greater than the previously entered END ADDRESS[9:0] allows a final waveform segment to be played only once. Specifying an END ADDRESS[9:0] smaller than the previous END ADDRESS[9:0] is not advised as it can result in unpredictable behaviour.

It is also possible to send consecutive RAM_PLAYBACK commands with RPT field set to 0x1. When a segment is being played continuously and a new RAM PLAYBACK command is received with RPT field set to 0x1, the following applies:

- The END ADDRESS[9:0] of the new command must be equal to or greater than the previously entered END ADDRESS[9:0].
- The REPEATED START ADDRESS of the new command must be smaller than or equal to the new END ADDRESS[9:0].
- The START ADDRESS[9:0] field is ignored.
- If REPEATED START ADDRESS is greater than the previous END ADDRESS[9:0], the segment between the previous END ADDRESS[9:0] and the new REPEATED START ADDRESS, referred as the *middle segment*, will be played only once.
- It is not possible to play non-contiguous segments when RPT field is set to 0x1, i.e., the *middle segment,* between the two non-contiguous segments will always be played.

6.7.3 Typical Operation Sequences

The following sections show different methods of launching a haptic waveform using RAM Playback mode.

Note that any previous waveform must have finished playing before programming RAM.

6.7.3.1 Triggered Start Sequence

The triggered start sequence is used to start playing a haptic waveform after programming the CONFIG.OE bit to 0x1.

The sequence is the following:

1. If not already done, set CONFIG.OE bit to 0x0.
2. Set CONFIG.PLAY_MODE[1:0] bits to 0x2 to select RAM playback mode.
3. Write waveform data to RAM using BURST RAM WRITE command. See section 6.7.5 for a detailed example.
4. Write the RAM start and end addresses using RAM PLAYBACK WFS command.
5. Set CONFIG.OE bit to 0x1 when ready for haptic waveform playback.
6. The haptic waveform starts playing.
7. CONFIG.OE bit self-clears once the waveform is completed.

6.7.3.2 Immediate Start Sequence

The immediate start sequence is used to start a haptic waveform playback after issuing the RAM PLAYBACK WFS command. The sequence requires the CONFIG.OE bit to be set to 0x1 before issuing the RAM PLAYBACK WFS command.

The sequence is the following:

1. If not already done, set CONFIG.OE bit to 0x0.
2. Set CONFIG.PLAY_MODE[1:0] bits to 0x2 to select RAM playback mode.
3. Set CONFIG.OE bit to 0x1 to enable output.
4. Write waveform data to RAM using BURST RAM WRITE command. See section 6.7.5 for a detailed example.
5. Write the RAM start and end addresses using RAM PLAYBACK command.
6. The haptic waveform starts playing.
7. CONFIG.OE bit is set to 0x0 once the waveform is completed.

6.7.3.3 Sensing Detection Sequence (BOS1921 Only)

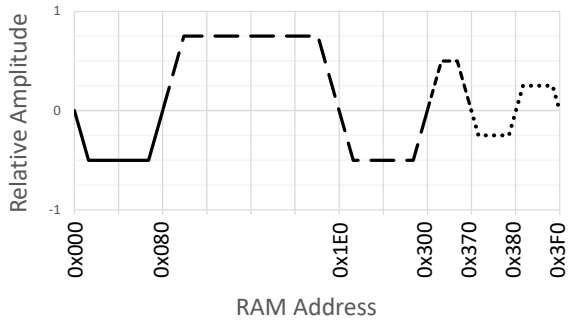
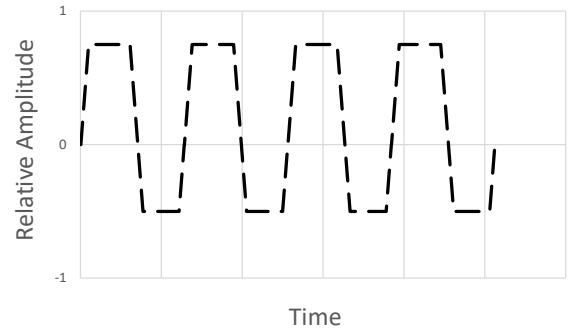
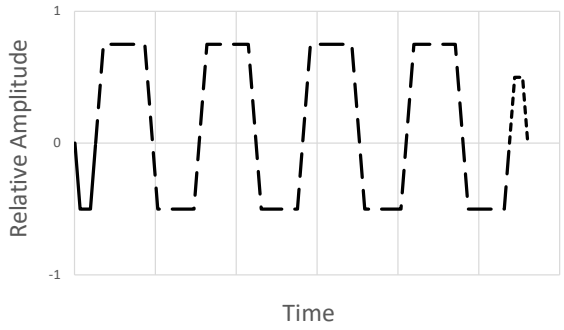
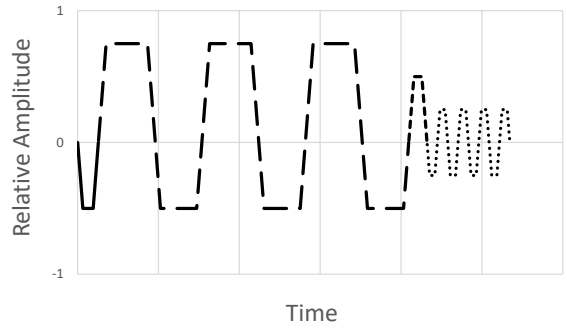
The sequence is used to start haptic waveform playback when previously establish sensing detection conditions are met. The sequence requires the CONFIG.AUTO, CONFIG.ONCOMP and CONFIG.SENSE bits to be set to 0x1.

The sequence is the following:

1. If not already done, set CONFIG.OE bit to 0x0.
2. Set CONFIG.PLAY_MODE[1:0] bits to 0x2 to select RAM playback mode.
3. Write waveform data to RAM using BURST RAM WRITE command. See section 6.7.5 for a detailed example.
4. Write the RAM start and end addresses using RAM PLAYBACK command.
5. Configure sensing detection condition as per section 6.4.3.
6. Set CONFIG.OE bit 0x1 to enable output.
7. The haptic waveform starts playing once sense detection conditions are met.

6.7.4 Waveform Example

Table 14 RAM PLAYBACK waveform examples

#	RAM PLAYBACK COMMAND CONTENT	WAVEFORM PLAYBACK
1	**Reference waveform for further examples.** RAM PLAYBACK command 1: - *RPT = 0x0* - START *ADDRESS[9:0] = 0x000* - REPEAT *START ADDRESS[9:0] = 0x000*[1] - *END ADDRESS[9:0] = 0x3F0*	
2	RAM PLAYBACK command 1 (start): - *RPT = 0x1* - START *ADDRESS[9:0] = 0x080,* - REPEAT *START ADDRESS[9:0] = 0x080* - *END ADDRESS[9:0] = 0x300* RAM PLAYBACK command 2 (stop): - *RPT = 0x0* - START *ADDRESS[9:0] = 0x000*[1] - REPEAT *START ADDRESS[9:0] = 0x000*[1] - END *ADDRESS[9:0] = 0x300*	
3	RAM PLAYBACK command 1 (start): - *RPT = 0x1* - *START ADDRESS[9:0] = 0x000* - *REPEAT START ADDRESS[9:0] = 0x080* - END *ADDRESS[9:0] = 0x300* RAM PLAYBACK command 2 (stop): - *RPT = 0x0* - *START ADDRESS[9:0] = 0x000*[1] - *REPEAT START ADDRESS[9:0] = 0x000*[1] - *END ADDRESS[9:0] = 0x370*	
4	RAM PLAYBACK command 1 (start): - *RPT = 0x1* - *START ADDRESS[9:0] = 0x000* - *REPEAT START ADDRESS[9:0] = 0x080* - *END ADDRESS[9:0] = 0x300* RAM PLAYBACK command 2: - *RPT = 0x1* - *START ADDRESS[9:0] = 0x000*[1] - *REPEAT START ADDRESS[9:0] = 0x370* - *END ADDRESS[9:0] = 0x3F0* RAM PLAYBACK command 3 (stop): - *RPT = 0x0* - START *ADDRESS[9:0] = 0x000*[1] - REPEAT *START ADDRESS[9:0] = 0x000*[1] - *END ADDRESS[9:0] = 0x3F0*	

6.7.5 I²C Communication Example

In RAM Playback, waveform samples need to be first stored in the RAM to be fetched later. A typical RAM programming sequence is presented in Figure 21 which consist of programming a waveform using 10 samples to be played. The OE bit is set to 0x1 to start playing immediately after the RAM Playback command is issued.

I²C Communication Sequence

Transaction 1	
Code	Description / Configure RAM Playback Mode
0x44	I²C address
0x05	Select CONFIG register
0x1407	Set RAM Playback Mode

Transaction 2	
Code	Description / Configure Burst RAM Write
0x44	I²C address
0x00	Select REFERENCE register to use a WFS command
0x0014	WFS command : BURST RAM WRITE
0x0000	Set RAM start address
0x000A	Set Data count (10 samples to be written starting at address 0x0000).
0x0000	Sample data
0x00AE	Sample data
0x015C	Sample data
0x020A	Sample data
0x02B8	Sample data
0x02B8	Sample data
0x020A	Sample data
0x015C	Sample data
0x00AE	Sample data
0x0000	Sample data

Transaction 3	
Code	Description / Set RAM Playback Start and End Addresses
0x44	I²C address
0x00	Select REFERENCE register to use a WFS command
0x0013	WFS command : RAM Playback
0x0009	Set RAM playback end address.
0x0000	Set start address and no repetition

RAM Content

RAM Address	*RSVD*	*Samples*
0x0000	0x0	0x000
0x0001	0x0	0x0AE
0x0002	0x0	0x15C
0x0003	0x0	0x20A
0x0004	0x0	0x2B8
0x0005	0x0	0x2B8
0x0006	0x0	0x20A
0x0007	0x0	0x15C
0x0008	0x0	0x0AE
0x0009	0x0	0x000

Figure 21: RAM Playback setup example

[1] The field is ignored.

6.8 RAM Synthesis Mode

In RAM Synthesis mode (PLAY_MODE[1:0] bits set to 0x3), sine wave parameters stored by the user in RAM are used to generate simple to complex waveforms. Two types of information are stored in RAM:

1) SLICEs, written in the RAM using the RAM ACCESS command. Each SLICE contains a group of parameters used to produce a sine wave of defined amplitude, frequency, and number of cycles. It may also be ramped up and down (as shown in Figure 24). See section 6.8.1 for more details.
2) WAVEs, written in the RAM in predefined location using the RAM ACCESS command. A maximum of 15 WAVE blocks can be written in predefined RAM address. A WAVE defines a series of SLICEs to be played successively. All SLICEs of a WAVE must be written in order and contiguously in the RAM. See section 6.8.2 for more details.

A SEQUENCE is defined using the RAM SYNTHESIS command and point to 1 to 15 WAVE block RAM addresses to be played sequentially to create an output haptic waveform. See section 6.8.3 for more details.

A haptic waveform can be played by sending the desired START and END WAVE number using the RAM SYNTHESIS command. Once the waveform has been played, it can be played again by setting the START and END WAVE number again in the RAM SYNTHESIS command. The waveform will immediately start playing if the RAM SYNTHESIS command is issued while OE bit is set to 0x1.

No waveform should be playing while programming RAM using the RAM ACCESS command to avoid unexpected behaviour.

The WAVE and SLICE data are stored in RAM, as shown in Figure 22. WAVE must be located between RAM address 0x00 and 0x2C. SLICE blocks can be located at any free locations and arranged in any order, but they must not overlap.

Note that waveforms should begin and end with 0 V amplitude.

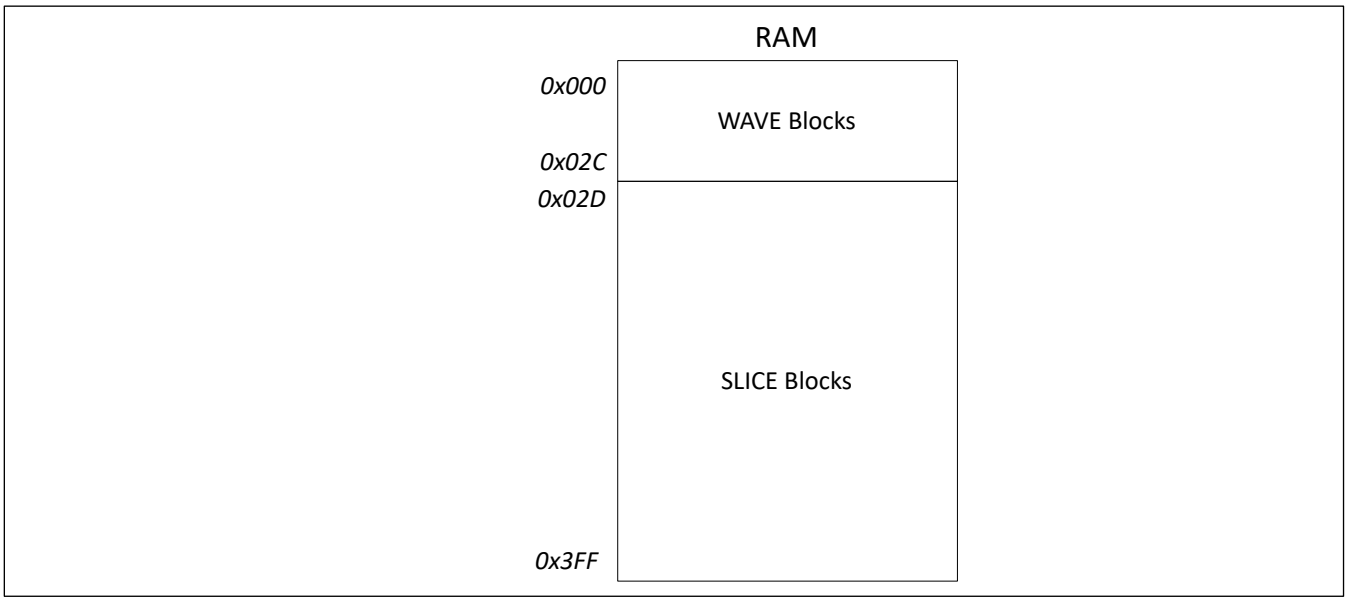


Figure 22: Representation of WAVE and SLICE blocks organized in RAM

6.8.1 SLICE Blocks

SLICE blocks in RAM contains the parameters used to synthesize sine waveforms. Each SLICE block contains three words grouping all parameters needed as described in Table 15. Figure 23 shows an example on how several SLICEs can be organized in RAM. Figure 24 illustrates an example of how these parameters shape a SLICE waveform. Many SLICES may be successively played to form more complex waveforms.

Note that SLICE.MODE[1:0] should be unipolar (set to 0x1 or 0x3) if SLICE.AMPLITUDE[11:0] is set to 0.

Table 15: SLICE block description

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOT USED: 0x0				AMPLITUDE[11:0]											
CYCLES[7:0]								FREQUENCY[7:0]							
NOT USED: 0x0			CONT	MODE[1:0]		HCYC	P180	SHAPEUP[3:0]				SHAPEDN[3:0]			

WORD	BITS	NAME	DESCRIPTION
1	11:0	AMPLITUDE	Sets the voltage amplitude of the output waveform. For bipolar waveforms (SLICE.MODE[1:0] set to 0x0), the relation between the output peak-to-peak voltage ($V_{OUT-pkpk}$) and AMPLITUDE[11:0] is defined as follows: $$AMPLITUDE[11:0] = \frac{4095 \times V_{OUT-pkpk}}{190}$$ For unipolar waveforms (SLICE.MODE[1:0] set to 0x1 or 0x3), the relation between the output peak voltage(V_{OUT-pk}) and AMPLITUDE[11:0] is defined as follows: $$AMPLITUDE[11:0] = \frac{4095 \times V_{OUT-pk}}{95}$$ This AMPLITUDE[11:0] value calculation is valid only for RAM Synthesis mode (PLAY_MODE[1:0] bits set to 0x3). Note that the SLICE must be unipolar positive (SLICE.MODE[1:0] set to 0x1) if AMPLITUDE[11:0] is set to 0.
2	15:8	CYCLES	Sets the number of times a full sine wave period is repeated, excluding SHAPEUP[3:0] & SHAPEDN[3:0] ramp times. The field is ignored if CONT is set to 0x1. The total number of sine wave cycles played, $CYCLE_{TOTAL}$, (excluding ramp-up and ramp-down) is defined by: $$CYCLE_{TOTAL} = \text{CYCLES}[7:0] + HCYC \times 0.5$$ Note that $\text{CYCLE}_{\text{TOTAL}}$ must be greater than 0.
2	7:0	FREQUENCY	Defines the sine wave frequency. The waveform synthesizer has a frequency resolution of 3.9 Hz. FREQUENCY value must be greater than 0. The synthesized sine wave frequency (f_{OUT}) is defined by: $$f_{OUT}[HZ] = 3.9 \times FREQUENCY$$
3	12	CONT	Enables the SLICE repeat for continuous waveform playback. When enabled, the sine wave period is repeated until either a STOP or NXTSL bit is set to 0x1 is sent using the RAM SYNTHESIS command. 0x0: Continuous waveform playback disabled. 0x1: Continuous waveform playback enabled.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOT USED: 0x0				AMPLITUDE[11:0]											
CYCLES[7:0]								FREQUENCY[7:0]							
NOT USED: 0x0			CONT	MODE[1:0]		HCYC	P180	SHAPEUP[3:0]				SHAPEDN[3:0]			

WORD	BITS	NAME	DESCRIPTION
3	11:10	MODE	Sets the waveform type. 0x0: Bipolar wave. 0x1: Unipolar & positive: In this mode, the amplitude of the waveform is half a bipolar waveform and shifted up by half the maximum amplitude of a bipolar waveform. 0x2: Reserved. 0x3: Unipolar & negative: In this mode, the amplitude of the waveform is half a bipolar waveform and shifted up by half the maximum amplitude of a bipolar waveform.
3	9	HCYC	Plays an additional half cycle at the end of the SLICE. When CONT is set to 0x1, an extra half cycle will be played at the end of the slice after a SLICE termination request has been made with either a STOP or NXTSL bit set to 0x1 using the RAM SYNTHESIS command. 0x0: Do not add half-cycle at the end of the waveform. 0x1: Add half-cycle at the end of the waveform.
3	8	P180	Adds a 180° phase shift on the waveform. 0x0: No phase shift added. SLICE starts at min peak and increments. 0x1: A 180° phase shift is added. SLICE starts at max peak and decrements.
3	7:4	SHAPEUP[3:0]	SHAPEUP[3:0] sets the ramp-up time of the waveform from 0 V to V_{pk}. SHAPEDN[3:0] sets the ramp-down time of the waveform from V_{pk} to 0 V. SHAPEUP and SHAPEDN duration must be greater than the waveform period and are added to the total SLICE waveform duration (t_{SLICE}), which can be calculated as follows: $t_{SLICE}[ms] = SHAPEUP[ms] + \frac{\text{CYCLES}[7:0] + HCYC \times 0.5}{f_{OUT}[HZ]} + SHAPEDN[ms]$ 0x0: 0 ms 0x1: 32 ms 0x2: 64 ms 0x3: 96 ms 0x4: 128 ms 0x5: 160 ms 0x6: 192 ms 0x7: 224 ms 0x8: 256 ms 0x9: 512 ms 0xA: 768 ms 0xB: 1024 ms 0xC: 1280 ms 0xD: 1536 ms 0xE: 1792 ms 0xF: 2048 ms
3	3:0	SHAPEDN[3:0]	

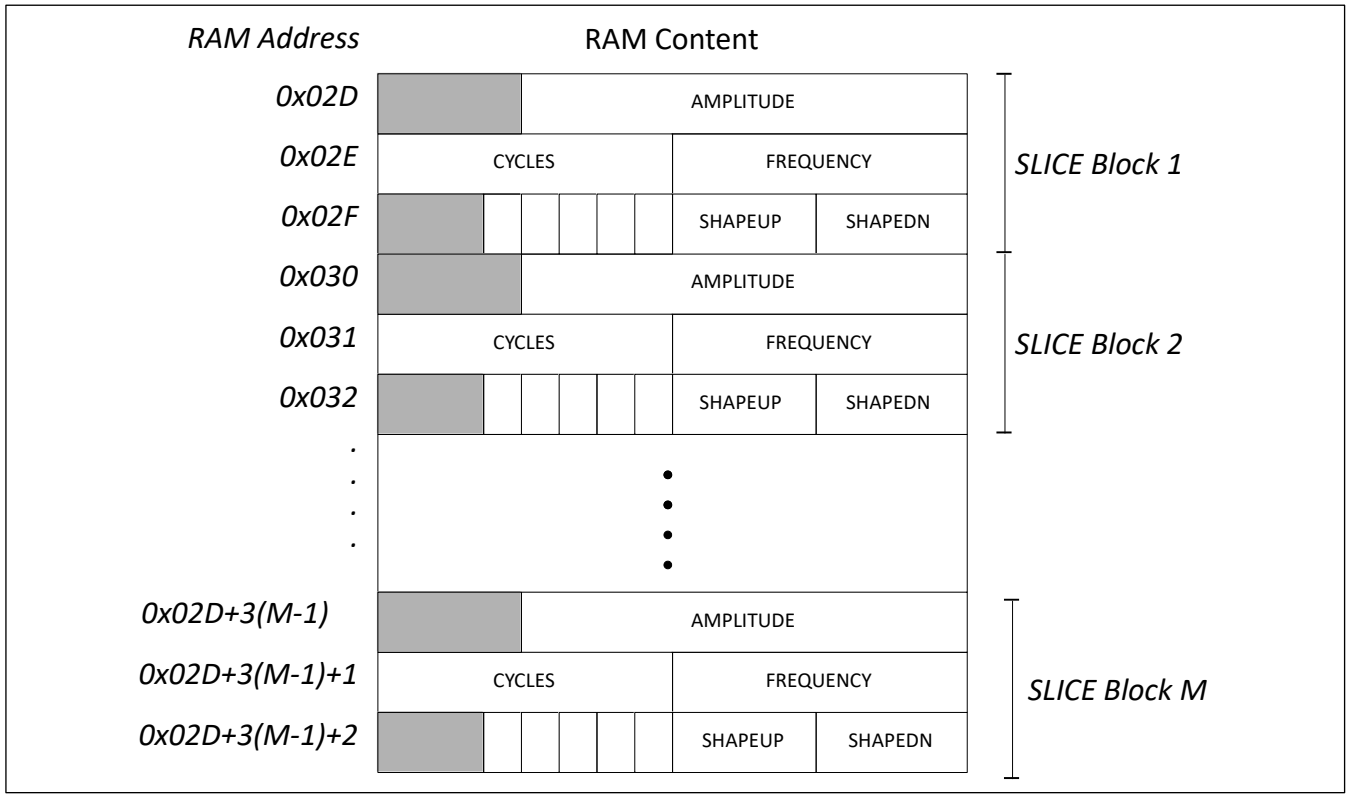


Figure 23: Sine wave SLICE parameters illustration

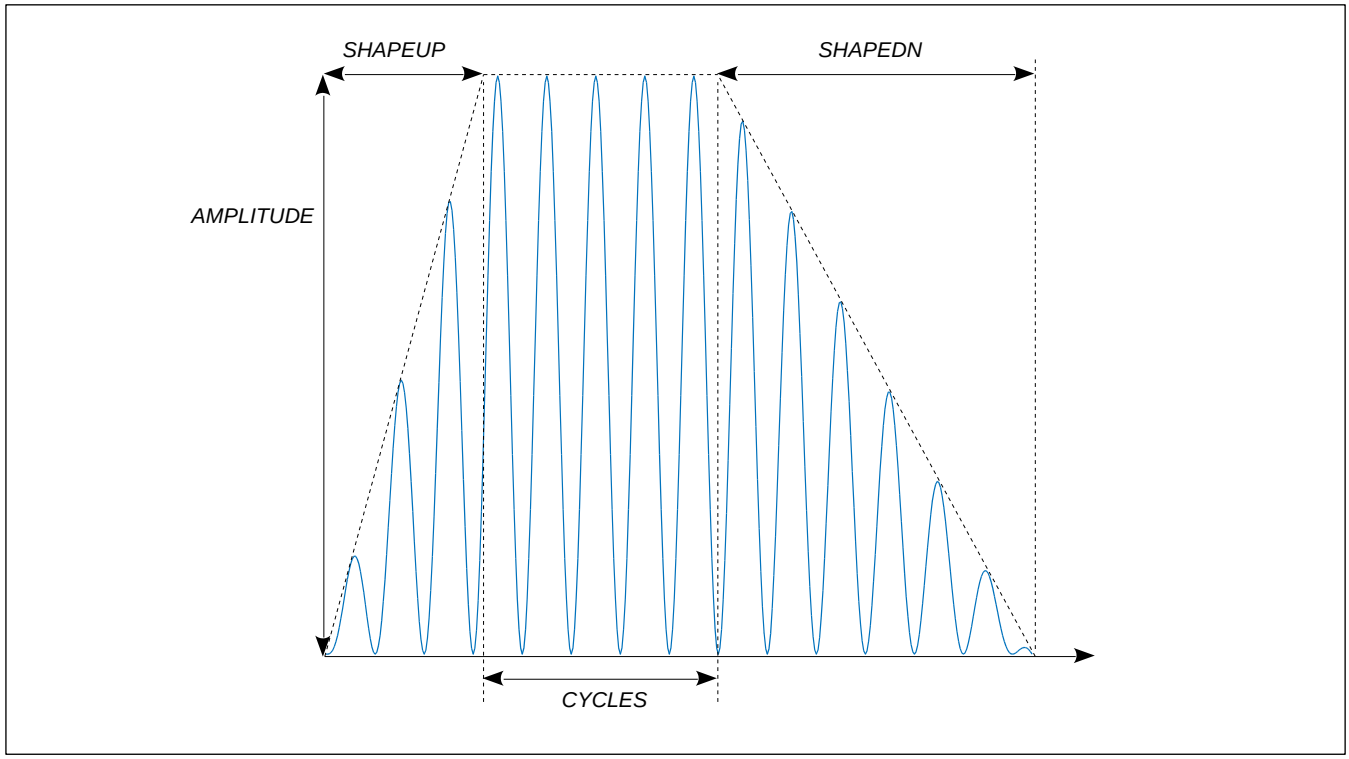


Figure 24: Sine wave SLICE parameters illustration

6.8.2 WAVE Blocks

A maximum of 15 WAVE blocks (numbered 0x0 to 0xE) can be written in RAM in fixed predefined location between RAM address 0x0000 and 0x002A as detailed in Table 17. Figure 25 presents how the WAVE blocks are organized in RAM.

A WAVE block in RAM contains three words and is described Table 16.

1. The SLICE START ADDRESS[11:0].
2. The SLICE END ADDRESS[11:0].
3. The WAVE COUNT[15:0].
4. SLICEs to be played sequentially must be placed in order and contiguously in RAM between the SLICE START ADDRESS[11:0] and the SLICE END ADDRESS[11:0].

Table 16: WAVE block description

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOT USED: 0x0				SLICE START ADDRESS[11:0]											
NOT USED: 0x0				SLICE END ADDRESS[11:0]											
COUNT[15:0]															

WORD	BITS	NAME	DESCRIPTION
1	11:0	SLICE START ADDRESS	Defines RAM address of the first word of the first SLICE to be fetched for waveform playback.
2	11:0	SLICE END ADDRESS	Defines RAM address of the third word of the last SLICE to be fetched for waveform playback.
3	15:0	COUNT	Sets the number of times the WAVE block is repeated from SLICE START ADDRESS[11:0] to SLICE END ADDRESS[11:0] for waveform playback. If COUNT[15:0] is set to 0x0, the WAVE block will repeat indefinitely for continuous waveform playback until either a STOP or NXTW bit set to 0x1 is sent using the RAM SYNTHESIS command.

Table 17: WAVE block number association with WAVE RAM ADDRESS.

WAVE BLOCK NUMBER	PREDEFINED WAVE RAM ADDRESS
0x0[2]	0x0000
0x1[3]	0x0003
0x2	0x0006
0x3	0x0009
0x4	0x000C
0x5	0x000F
0x6	0x0012
0x7	0x0015
0x8	0x0018
0x9	0x001B
0xA	0x001E
0xB	0x0021
0xC	0x0024
0xD	0x0027
0xE	0x002A

[2] WAVE block number 0x0 can be triggered using GPIO pin and KP.XTRIGR configuration bit.

[3] WAVE block number 0x1 can be triggered using GPIO pin and KP.XTRIGF configuration bit.

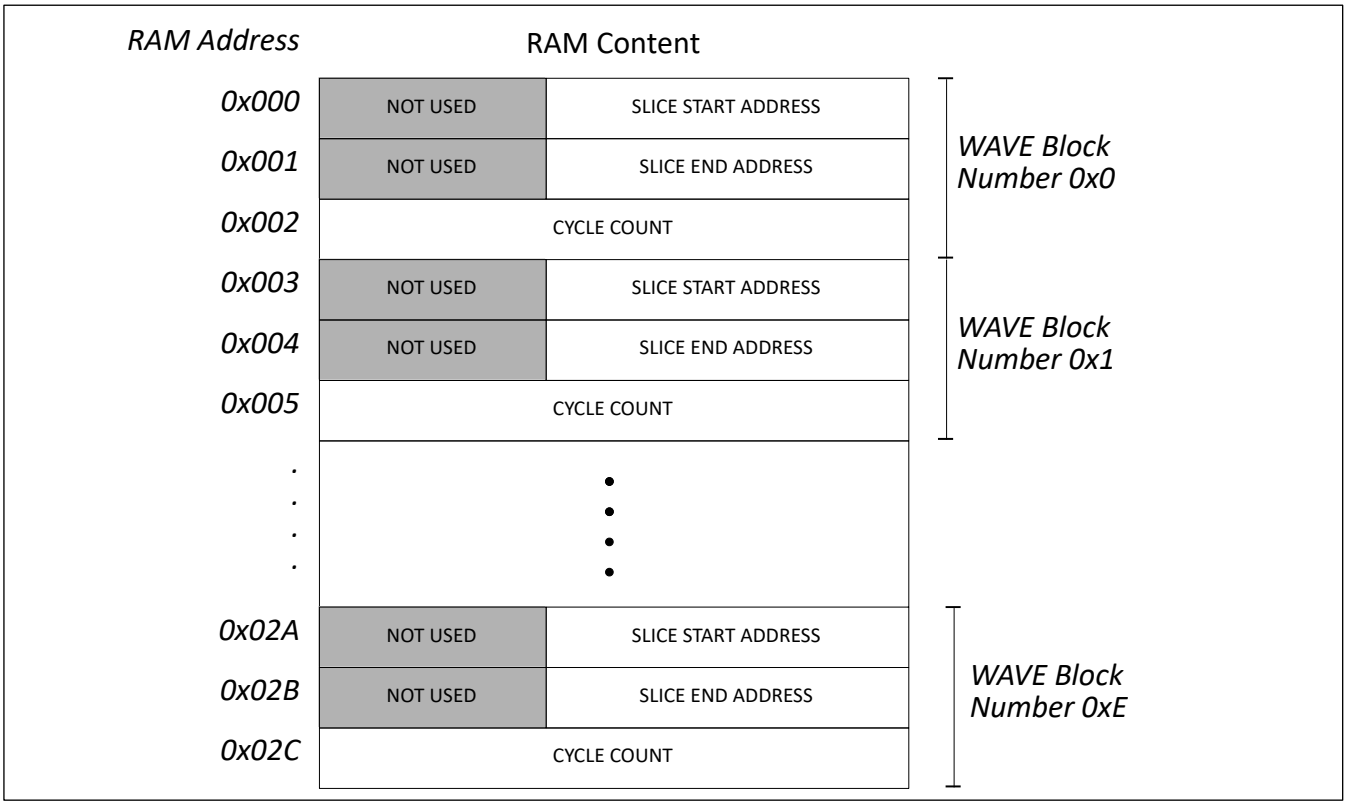


Figure 25: All 15 WAVE Blocks in RAM organized in RAM

6.8.3 SEQUENCE

A SEQUENCE is a haptic waveform to be played defined by the START and END WAVE number sent using the RAM SYNTHESIS command. For example, if START WAVE[3:0] is set to 0x3 and END WAVE[3:0] is set to 0x5, the waveform played will be composed of the WAVE blocks at RAM addresses 0x9, 0xC and 0xF, played sequentially.

The smallest sequence is when START WAVE[3:0] is equal to END WAVE[3:0] and thus only one WAVE block is played.

The largest waveform SEQUENCE to be played covers the 15 WAVE blocks, from WAVE number 0x0 to 0xE.

A SEQUENCE is repeated by issuing the RAM SYNTHESIS command with RPT field set to 0x1.

6.8.4 Continuous Waveform Playback

In RAM SYNTHESIS mode, any type of waveform segments (SEQUENCE, WAVE or SLICE) may be repeated indefinitely.

The Table 18 details how to start and stop the continuous waveform playback of any segment type.

A SEQUENCE that is being played continuously can be terminated by issuing a new RAM SYNTHESIS command with its field contents identical to the initial RAM SYNTHESIS command except with the RPT field set to 0x0.

A WAVE block being repeated continuously can be stopped by issuing a RAM SYNTHESIS command with the NXTWV field set to 0x1, which will instruct the WFS to play the next WAVE block of the SEQUENCE or end the waveform playback if the current WAVE block is the last one of the SEQUENCE. Similarly, a

SLICE block being repeated continuously can be stopped by issuing a RAM SYNTHESIS command with NXTSL field set to 0x1, which will instruct the WFS to play the next SLICE block or end the waveform if the current SLICE is the last SLICE of the SEQUENCE.

Using RAM SYNTHESIS command with NXTSL or NXTWV field set to 0x1 does not necessarily stop playback: any subsequent SLICE or WAVE block of the SEQUENCE will finish playing and may repeat indefinitely if configured that way.

Issuing a RAM SYNTHESIS command with STOP field set to 0x1 will play the next SLICE or WAVE block in the SEQUENCE only once, regardless of the state of SLICE.CYCLES[7:0], SLICE.CONT, WAVE.COUNT[15.0] or RAM SYNTHESIS.RPT and thus preventing any of them of being repeated indefinitely. There are no options to force an immediate and sudden end of the haptic waveform playback.

Note the following:

- Issuing a RAM SYNTHESIS command with any of NXTWV, NXTSL or STOP field set to 0x1, stop the current SLICE or WAVE block being played even if it is not configured to play continuously. For instance, such a command could be used to put an early end to a long duration waveform.
- When a RAM SYNTHESIS command with any of NXTWV, NXTSL or STOP field set to 0x1 to stop a waveform of being played, the START WAVE[3:0] and END WAVE[3:0] fields must be set again.

Table 18: Summary of how to start and stop the continuous waveform playback.

SEGMENT TYPE	HOW TO START CONTINUOUS PLAYBACK	HOW TO STOP CONTINUOUS PLAYBACK
SEQUENCE	Issue an RAM SYNTHESIS command with RPT bit set to 0x1.	Issue an RAM SYNTHESIS command with RPT bit set to 0x0.
WAVE	WAVE.COUNT[15:0] is set to 0x0.	Issue an RAM SYNTHESIS command with NXTWV bit set to 0x1.
SLICE	SLICE.CONT is set to 0x1.	Issue an RAM SYNTHESIS command with NXTSL bit set to 0x1.

6.8.5 Typical Operation Sequences

The following sections show different methods of launching a haptic waveform using RAM Synthesis mode.

Note that any previous waveform must have finished playing before programming RAM.

6.8.5.1 Triggered Start Sequence

The triggered start sequence is used to start playing a haptic waveform after programming the CONFIG.OE bit to 0x1.

The sequence is the following:

1. If not already done, set CONFIG.OE bit to 0x0.
2. Set CONFIG.PLAY_MODE[1:0] bits to 0x3 to select RAM synthesis mode.
3. Use RAM_ACCESS WFS command to write WAVE and SLICE blocks in RAM. Multiple write sequences might be required, see section 6.8.7 for some examples.
4. Write START and END WAVE number to be played using RAM SYNTHESIS WFS command.
5. Set CONFIG.OE bit to 0x1 when ready for haptic waveform playback.
6. The haptic waveform starts playing.
7. CONFIG.OE bit is set to 0x0 once the waveform is completed.

6.8.5.2 GPIO Triggered Start Sequence

The GPIO triggered start sequence is used to start playing a haptic waveform using a GPIO falling edge signal and/or rising edge signal.

Note that KP.XTRIGR bit enables the GPIO rising edge triggering of WAVE block number 0x0 and KP.XTRIGF bit enables the GPIO falling edge triggering of WAVE block number 0x1.

The sequence is the following:

1. If not already done, set CONFIG.OE bit to 0x0.
2. Set CONFIG.PLAY_MODE[1:0] bits to 0x3 to select RAM synthesis mode.
3. Use RAM_ACCESS WFS command to write WAVE and SLICE blocks in RAM. Multiple write sequences might be required, see section 6.8.7 for some examples.
4. Write START and END WAVE number to be played using RAM SYNTHESIS WFS command.
5. Set COMM.GPIODIR to 0x1 to configure GPIO pin as an input.
6. Set KP.XTRIGR to 0x1 to enable rising edge triggering and/or set KP.XTRIGF bit to 0x1 to enable falling edge triggering.
7. Set CONFIG.OE bit to 0x1 when ready for haptic waveform playback.
8. The haptic waveform starts playing on GPIO signal.
9. CONFIG.OE bit is set to 0x0 once the waveform is completed.

6.8.5.3 Immediate Start Sequence

The immediate start sequence is used to start a haptic waveform playback after issuing the RAM SYNTHESIS WFS command. The sequence requires the CONFIG.OE bit to be set to 0x1 before issuing the RAM SYNTHESIS WFS command.

The sequence is the following:

1. If not already done, set CONFIG.OE bit to 0x0.
2. Set CONFIG.PLAY_MODE[1:0] bits to 0x3 to select RAM synthesis mode.
3. Set CONFIG.OE bit to 0x1 to enable output.
4. Use RAM_ACCESS WFS command to write WAVE and SLICE blocks in RAM. Multiple write sequences might be required, see section 6.8.7 for some examples.
5. Write START and END WAVE number to be played using RAM SYNTHESIS WFS command.
6. The haptic waveform starts playing.
7. CONFIG.OE bit is set to 0x0 once the waveform is completed.

6.8.5.4 Sensing Detection Sequence (BOS1921 Only)

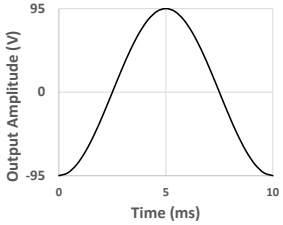
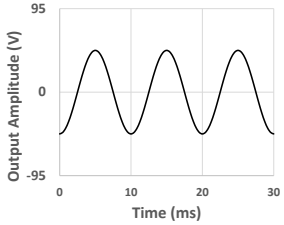
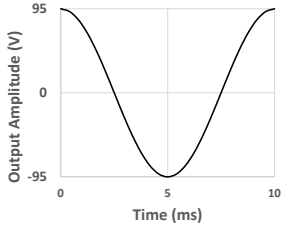
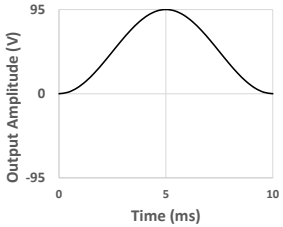
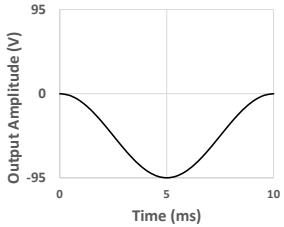
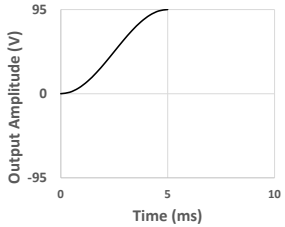
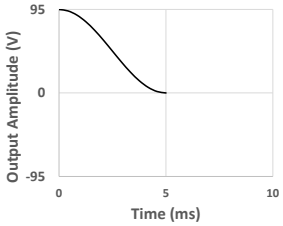
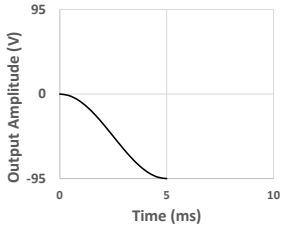
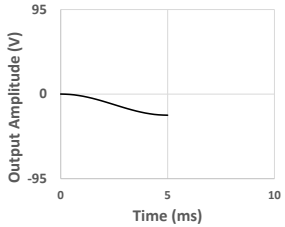
The sequence is used to start haptic waveform playback when previously establish sensing detection conditions are met. The sequence requires the CONFIG.AUTO, CONFIG.ONCOMP and CONFIG.SENSE bits to be set to 0x1.

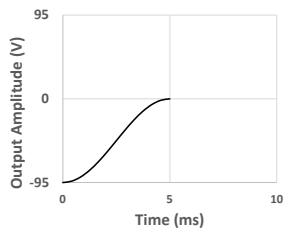
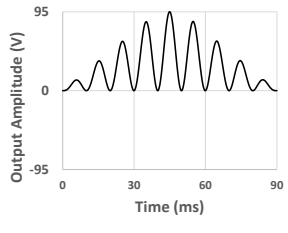
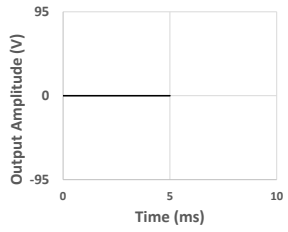
The sequence is the following:

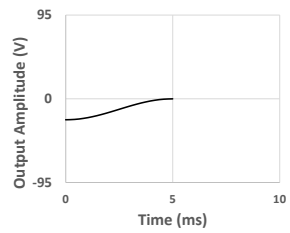
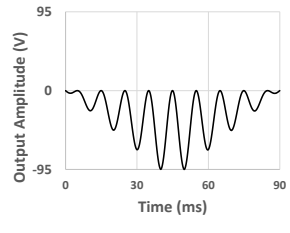
1. If not already done, set CONFIG.OE bit to 0x0.
2. Set CONFIG.PLAY_MODE[1:0] bits to 0x3 to select RAM synthesis mode.
3. Use RAM_ACCESS WFS command to write WAVE and SLICE blocks in RAM. Multiple write sequences might be required, see section 6.8.7 for some examples.
4. Write START and END WAVE number to be played using RAM SYNTHESIS WFS command.
5. Configure sensing detection condition as per section 6.4.3.
6. Set CONFIG.OE bit to 0x1 to enable output.
7. The haptic waveform starts playing once sense detection conditions are met.

6.8.6 Waveform Examples

Table 19: SLICE waveforms examples

OUTPUT WAVEFORM	SLICE PARAMETERS		OUTPUT WAVEFORM	SLICE PARAMETERS		OUTPUT WAVEFORM	SLICE PARAMETERS	
SLICE A 	AMPLITUDE[11:0]	= 0xFFF	SLICE B 	AMPLITUDE[11:0]	= 0x7FF	SLICE C 	AMPLITUDE[11:0]	= 0xFFF
	CYCLES[7:0]	= 0x01		CYCLES[7:0]	= 0x03		CYCLES[7:0]	= 0x01
	FREQUENCY[7:0]	= 0x1A		FREQUENCY[7:0]	= 0x1A		FREQUENCY[7:0]	= 0x1A
	CONT	= 0x0		CONT	= 0x0		CONT	= 0x0
	MODE[1:0]	= 0x0		MODE[1:0]	= 0x0		MODE[1:0]	= 0x0
	HCYC	= 0x0		HCYC	= 0x0		HCYC	= 0x0
	P180	= 0x0		P180	= 0x0		P180	= 1x0
	SHAPEUP[3:0]	= 0x0		SHAPEUP[3:0]	= 0x0		SHAPEUP[3:0]	= 0x0
	SHAPEDN[3:0]	= 0x0		SHAPEDN[3:0]	= 0x0		SHAPEDN[3:0]	= 0x0
SLICE D 	AMPLITUDE[11:0]	= 0xFFF	SLICE E 	AMPLITUDE[11:0]	= 0xFFF	SLICE F 	AMPLITUDE[11:0]	= 0xFFF
	CYCLES[7:0]	= 0x01		CYCLES[7:0]	= 0x01		CYCLES[7:0]	= 0x00
	FREQUENCY[7:0]	= 0x1A		FREQUENCY[7:0]	= 0x1A		FREQUENCY[7:0]	= 0x1A
	CONT	= 0x0		CONT	= 0x0		CONT	= 0x0
	MODE[1:0]	= 0x1		MODE[1:0]	= 0x3		MODE[1:0]	= 0x1
	HCYC	= 0x0		HCYC	= 0x0		HCYC	= 0x1
	P180	= 0x0		P180	= 0x1		P180	= 0x0
	SHAPEUP[3:0]	= 0x0		SHAPEUP[3:0]	= 0x0		SHAPEUP[3:0]	= 0x0
	SHAPEDN[3:0]	= 0x0		SHAPEDN[3:0]	= 0x0		SHAPEDN[3:0]	= 0x0
SLICE G 	AMPLITUDE[11:0]	= 0xFFF	SLICE H 	AMPLITUDE[11:0]	= 0xFFF	SLICE I 	AMPLITUDE[11:0]	= 0x3FF
	CYCLES[7:0]	= 0x00		CYCLES[7:0]	= 0x00		CYCLES[7:0]	= 0x00
	FREQUENCY[7:0]	= 0x1A		FREQUENCY[7:0]	= 0x1A		FREQUENCY[7:0]	= 0x1A
	CONT	= 0x0		CONT	= 0x0		CONT	= 0x0
	MODE[1:0]	= 0x1		MODE[1:0]	= 0x3		MODE[1:0]	= 0x3
	HCYC	= 0x1		HCYC	= 0x1		HCYC	= 0x1
	P180	= 0x1		P180	= 0x1		P180	= 0x1
	SHAPEUP[3:0]	= 0x0		SHAPEUP[3:0]	= 0x0		SHAPEUP[3:0]	= 0x0
	SHAPEDN[3:0]	= 0x0		SHAPEDN[3:0]	= 0x0		SHAPEDN[3:0]	= 0x0

OUTPUT WAVEFORM	SLICE PARAMETERS
SLICE J 	AMPLITUDE[11:0] = 0xFFF CYCLES[7:0] = 0x00 FREQUENCY[7:0] = 0x1A CONT = 0x0 MODE[1:0] = 0x3 HCYC = 0x1 P180 = 0x0 SHAPEUP[3:0] = 0x0 SHAPEDN[3:0] = 0x0
SLICE M 	AMPLITUDE[11:0] = 0xFFF CYCLES[7:0] = 0x03 FREQUENCY[7:0] = 0x1A CONT = 0x0 MODE[1:0] = 0x1 HCYC = 0x0 P180 = 0x1 SHAPEUP[3:0] = 0x1 SHAPEDN[3:0] = 0x1
SLICE P 	AMPLITUDE[11:0] = 0x000 CYCLES[7:0] = 0x01 FREQUENCY[7:0] = 0x34 CONT = 0x0 MODE[1:0] = 0x1 HCYC = 0x0 P180 = 0x0 SHAPEUP[3:0] = 0x0 SHAPEDN[3:0] = 0x0

OUTPUT WAVEFORM	SLICE PARAMETERS
SLICE K 	AMPLITUDE[11:0] = 0x3FF CYCLES[7:0] = 0x00 FREQUENCY[7:0] = 0x1A CONT = 0x0 MODE[1:0] = 0x3 HCYC = 0x1 P180 = 0x0 SHAPEUP[3:0] = 0x0 SHAPEDN[3:0] = 0x0
SLICE N 	AMPLITUDE[11:0] = 0xFFF CYCLES[7:0] = 0x03 FREQUENCY[7:0] = 0x1A CONT = 0x0 MODE[1:0] = 0x3 HCYC = 0x0 P180 = 0x1 SHAPEUP[3:0] = 0x1 SHAPEDN[3:0] = 0x1

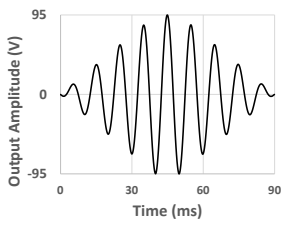
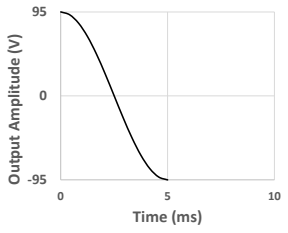
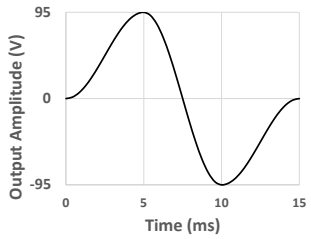
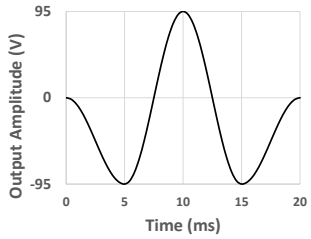
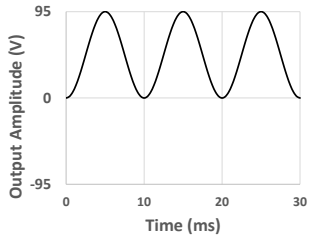
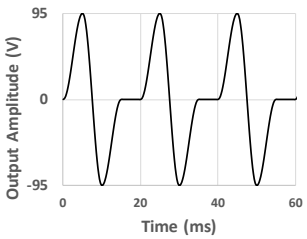
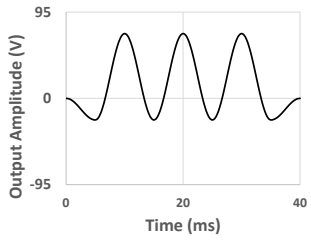
OUTPUT WAVEFORM	SLICE PARAMETERS
SLICE L 	AMPLITUDE[11:0] = 0xFFF CYCLES[7:0] = 0x03 FREQUENCY[7:0] = 0x1A CONT = 0x0 MODE[1:0] = 0x0 HCYC = 0x0 P180 = 0x0 SHAPEUP[3:0] = 0x1 SHAPEDN[3:0] = 0x1
SLICE O 	AMPLITUDE[11:0] = 0xFFF CYCLES[7:0] = 0x00 FREQUENCY[7:0] = 0x1A CONT = 0x0 MODE[1:0] = 0x0 HCYC = 0x1 P180 = 0x1 SHAPEUP[3:0] = 0x0 SHAPEDN[3:0] = 0x0

Table 20: Waveform examples built from a single WAVE block

WAVE BLOCK CONTENT	WAVEFORM
SLICEs : F + O + J WAVE.COUNT[15:0] = 0x1 RELOFF = 0x0 *Note that waveform features a smooth start and stop for optimal integrity.*	
SLICEs : H + A + J WAVE.COUNT[15:0] = 0x1 RELOFF = 0x0 *Note that SLICE A can be repeated to output a sinewave.*	
SLICE : D WAVE.COUNT[15:0] = 0x3 RELOFF = 0x0	
SLICEs : F + O + J + P WAVE.COUNT[15:0] = 0x3 RELOFF = 0x0	
SLICEs: I + B + K WAVE.COUNT[15:0] = 0x1 RELOFF = 0x1	

6.8.7 I²C Communication Examples

Figure 26 to Figure 29 give two examples showing how to program in RAM a waveform:

- Example 1 uses only 1 SLICE and 1 WAVE programmed with a single communication transaction.
- Example 2 uses 4 SLICEs and 3 WAVEs programmed with a communication transaction for each WFS command.

Both examples use OE bit set to 0x1 to start playing immediately after the RAM SYNTHESIS command is issued.

I²C Communication Sequence

Transaction 1 :	
Code	Description / Configure RAM Synthesis Mode
0x44	I²C address
0x05	Select CONFIG register
0x1600	Set RAM Synthesis Mode

Code	Description / Program one WAVE in RAM
0x0001	WFS command : set to RAM ACCESS
0x0000	Set RAM start address for WAVE block programming
0x0100	WAVE Data : Set RAM start address of first SLICE
0x0102	WAVE Data : Set RAM end address of last SLICE
0x0001	WAVE Data : Set WAVE cycle count (played once)

Code	Description / Program one SLICE in RAM
0x0001	WFS command : set to RAM ACCESS
0x0100	Set RAM ADDRESS for SLICE block programming
0x0FFF	SLICE Data : Set AMPLITUDE (full scale)
0x0440	SLICE Data : Set CYCLES (4) and FREQUENCY (250 Hz)
0x0000	SLICE Data : Set bipolar waveform

Code	Description / Set Start and End Sequencer Entries
0x0012	WFS command : set sequencer start and end numbers
0x0000	Set start and end sequence to 0x0

RAM Content

RAM Address	*WAVE*	
0x0000	0x00	0x100
0x0001	0x00	0x102
0x0002	0x0001	

RAM Content

RAM Address	*SLICE*		
0x0100	0x0	0xFFF	
0x0101	0x04	0x40	
0x0102	0x00	0x0	0x0

Figure 26: RAM synthesis mode setup example 1

I²C Communication Sequence

Transaction 1	
Code	Description / Configure RAM Synthesis Mode
0x44	I²C address
0x05	Select CONFIG register
0x1600	Set RAM Synthesis Mode

Transaction 2	
Code	Description / Program WAVE #1 in RAM
0x44	I²C address
0x00	Select REFERENCE register to access to WFS Register
0x0001	WFS command : RAM ACCESS
0x0000	Set RAM start address for WAVE block programming
0x0100	WAVE #1 Data : Set RAM start address of SLICE #1
0x0102	WAVE #1 Data : Set RAM end address of SLICE #1
0x000E	WAVE #1 Data : Set WAVE cycle count (14 times)

Transaction 3	
Code	Description / Program SLICE #1 in RAM
0x44	I²C address
0x00	Select REFERENCE register to access to WFS Register
0x0001	WFS command : RAM ACCESS
0x0100	Set RAM address for SLICE block programming
0x0FFF	SLICE #1 Data : Set AMPLITUDE (full scale)
0x01FF	SLICE #1 Data : Set CYCLES (1) and FREQUENCY (995 Hz)
0x0000	SLICE #1 Data : Set bipolar waveform

Transaction 4	
Code	Description / Program WAVE #2 in RAM
0x44	I²C address
0x00	Select REFERENCE register to access to WFS Register
0x0001	WFS command : RAM ACCESS
0x0003	Set RAM address for WAVE block programming
0x0200	WAVE #2 Data : Set RAM start address of SLICE #2
0x0202	WAVE #2 Data : Set RAM end address of SLICE #2
0x001D	WAVE #2 Data : Set WAVE cycle count (29 times)

Transaction 5	
Code	Description / Program SLICE #2 in RAM
0x44	I²C address
0x00	Select REFERENCE register to access to WFS Register
0x0001	WFS command : RAM ACCESS
0x0200	Set RAM start address for SLICE block programming
0x0CCC	SLICE #2 Data : Set AMPLITUDE (156V)
0x1033	SLICE #2 Data : Set CYCLES (16) and FREQUENCY (200 Hz)
0x0021	SLICE #2 Data : Set SHAPEUP (64 ms) and SHAPEDN (32 ms)

RAM Content

RAM Address	WAVE #1	
0x0000	0x00	0x100
0x0001	0x00	0x102
0x0002	0x000E	

RAM Content

RAM Address	SLICE #1		
0x0100	0x0	0xFFF	
0x0101	0x01	0xFF	
0x0102	0x00	0x0	0x0

RAM Content

RAM Address	WAVE #2	
0x0003	0x00	0x200
0x0004	0x00	0x202
0x0005	0x001D	

RAM Content

RAM Address	SLICE #2		
0x0200	0x0	0xCCC	
0x0201	0x10	0x33	
0x0202	0x00	0x2	0x1

Figure 27: RAM synthesis mode setup example 2

I²C Communication Sequence

Transaction 6	
Code	Description / Program WAVE #3 in RAM
0x44	I²C address
0x00	Select REFERENCE register to access to WFS Register
0x0001	WFS command : RAM ACCESS
0x0006	Set RAM start address for WAVE block programming
0x0203	WAVE #3 Data : Set RAM start address of SLICE #3
0x0208	WAVE #3 Data : Set RAM end address of SLICE #4
0x01EE	WAVE #3 Data : Set WAVE cycle count (494 times)

RAM Content

RAM Address	*WAVE #3*	
0x0006	0x00	0x203
0x0007	0x00	0x208
0x0008	0x01EE	

Transaction 7	
Code	Description / Program SLICE #3 in RAM
0x44	I²C address
0x00	Select REFERENCE register to access to WFS Register
0x0001	WFS command : RAM ACCESS
0x0203	Set RAM start address for SLICE block programming
0x0AAA	SLICE #3 Data : Set AMPLITUDE (130V)
0x0A1A	SLICE #3 Data : Set CYCLES (10) and FREQUENCY (100 Hz)
0x0012	SLICE #3 Data : Set SHAPEUP (32 ms) and SHAPEDN (64 ms)

RAM Content

RAM Address	*SLICE #3*		
0x0203	0x0	0xAAA	
0x0204	0x0A	0x1A	
0x0205	0x00	0x1	0x2

Transaction 8	
Code	Description / Program SLICE #4 in RAM
0x44	I²C address
0x00	Select REFERENCE register to access to WFS Register
0x0001	WFS command : set to RAM SYNTHESIS WRITE
0x0206	Set RAM start address for SLICE block programming
0x0000	SLICE #4 Data : Set AMPLITUDE (0 V)
0x1F1A	SLICE #4 Data : Set CYCLES (31) and FREQUENCY (100 Hz)
0x0000	SLICE #4 Data : Set SHAPEUP (0 ms) and SHAPEDN (0 ms)

RAM Content

RAM Address	*SLICE #4*		
0x0206	0x0	0x000	
0x0207	0x1F	0x1A	
0x0208	0x00	0x0	0x0

Transaction 10	
Code	Description / Set Start and End Sequencer Entries
0x44	I²C address
0x00	Select REFERENCE register to access to WFS Register
0x0012	WFS command : RAM Synthesis
0x2000	Set start to SEQUENCE 0x0 and end to SEQUENCE 0x2

Figure 28: RAM synthesis mode setup example 2 (continued)

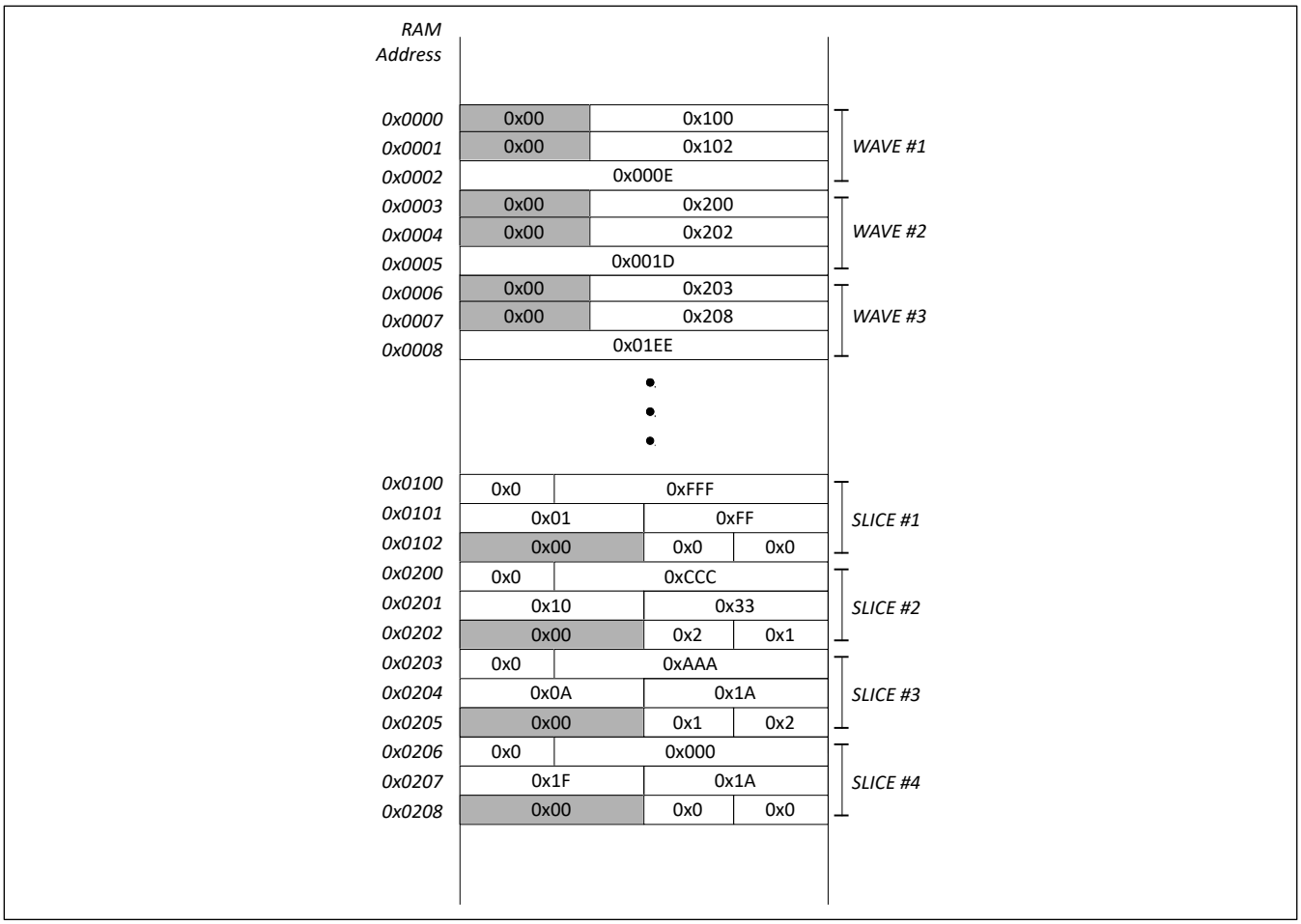


Figure 29: RAM Synthesis mode setup example 2 RAM summary

6.9 WFS Command Interpreter

The BOS1921/BOS1931 RAM is programmed using the WFS Command Interpreter accessible through REFERENCE register. WFS commands interpreter are used to store RAM Playback data and RAM Synthesis configuration data into RAM or to set FIFO DEPTH. WFS command list is summarized in Table 21, where word 0 is the command and the following words are the command payload.

Table 21 WFS commands list

COMMAND	WORD	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAM ACCESS	0	COMMAND[15:0] = 0x0001															
	1						R/W	ADDRESS[9:0]									
	2	DATA1[15:0]: required when write access is requested by setting R/W bit to 0x0															
	3	DATA2[15:0]: required when write access is requested by setting R/W bit to 0x0															
	4	DATA3[15:0]: required when write access is requested by setting R/W bit to 0x0															
FIFO DEPTH	0	COMMAND[15:0] = 0x0003															
	1														FIFO DEPTH[2:0]		
RAM SYNTHESIS	0	COMMAND[15:0] = 0x0012															
	1	END WAVE[3:0]				START WAVE[3:0]							RELOFF	STOP	NXTWV	NXTSL	RPT
RAM PLAYBACK	0	COMMAND[15:0] = 0x0013															
	1	RPT	START ADDRESS[4:0]					END ADDRESS[9:0]									
	2		START ADDRESS[9:5]					REPEAT START ADDRESS[9:0]									
BURST RAM WRITE	0	COMMAND[15:0] = 0x0014															
	1							START ADDRESS[9:0]									
	2							DATA COUNT [9:0]									
	3	DATA1[15:0]															
	…	…															
	2+n	DATAn (n = DATA COUNT[9:0])															
FULL RAM READ	0	COMMAND[15:0] =0x0015															
FULL RAM READ BREAK	0	COMMAND[15:0] = 0xFF15															

Figure 30 and Figure 31 present two different I^2C communication sequence examples using either a single communication transaction for each WFS command or a single communication transaction to use several WFS commands. The first word of each WFS command is the command identifier. The number of following words to send depends on the command used.

Transaction 1	
Code	Description / WFS command 1
0x44	I²C address
0x00	Select REFERENCE register to use a WFS command
0x0000	WFS command 1
0x0000	Expected word for command 1

Transaction 2	
Code	Description / WFS command 2
0x44	I²C address
0x00	Select REFERENCE register to use a WFS command
0x0000	WFS comamnd 2
0x0000	Expected word for command 2

Transaction 3	
Code	Description / WFS command 3
0x44	I²C address
0x00	Select REFERENCE register to use a WFS command
0x0000	WFS command 3
0x0000	Expected word for command 3

Figure 30: Generic I²C communication sequence example to use a WFS command with a transaction

Transaction 1	
Code	Description / WFS command 1
0x44	I²C address
0x00	Select REFERENCE register to use a WFS command
0x0000	WFS command 1
0x0000	Write expected word for command 1

Code	Description / WFS command 2
0x0000	WFS command 2
0x0000	Write expected word for command 2

Code	Description / WFS command 3
0x0000	WFS command 3
0x0000	Write expected word for command 3

Figure 31: Generic I²C communication sequence example to use several WFS commands with a single transaction

6.9.1 0x0001 RAM ACCESS

Table 22: RAM ACCESS details

	COMMAND: 0x0001 RAM ACCESS															
Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	COMMAND[15:0] = 0x0001															
1	NOT USED: 0x00					R/W	ADDRESS [9:0]									
2	DATA1 [15:0]: required when write access is requested by setting R/W bit to 0x0															
3	DATA2 [15:0]: required when write access is requested by setting R/W bit to 0x0															
4	DATA3 [15:0]: required when write access is requested by setting R/W bit to 0x0															

WORD, BIT	NAME	DESCRIPTION
Word 1, Bit [10]	R/W	0: RAM Write Enable 1: RAM Read Enable
Word 2, Bit [9:0]	ADDRESS	Write/read start address within the RAM

The RAM ACCESS command is used to either read a single location from RAM or writing a block of 3 words to RAM.

In RAM Synthesis mode, a WAVE or SLICE block can be written to RAM with the following sequence (as described in Figure 32):

1. Set PLAY_MODE[1:0] to 0x3 to select RAM Synthesis mode.
2. Write 0x0001 to the REFERENCE register to use the RAM ACCESS command
3. Write the following to the REFERENCE register:
    a. Set R/W to 0x0 and set the ADDRESS [9:0] to the RAM start address.
    b. Write the three words of either a WAVE or SLICE block to the REFERENCE register to store in RAM. See section 6.8 for details on the content of these words. The RAM address is automatically incremented between each word.

In either RAM Synthesis or RAM Playback, an RAM location can be read with the following sequence (as described in Figure 33):

1. Set PLAY_MODE[1:0] to 0x2 or 0x3 to select RAM Playback or RAM Synthesis mode.
2. Set RDADDR[4:0] to 0x1B to select RAM_DATA reading.
3. Write 0x0001 to the REFERENCE register to use the RAM ACCESS command.
4. Write the following to the REFERENCE register:
    a. R/W bit set to 0x1.
    b. ADDRESS [9:0] bits set to the RAM address to read.
5. Read 2 bytes.

Transaction 1 : Set RAM Synthesis Mode	
Code	Description
0x44+ W	I²C address, write access
0x05	Select CONFIG register
0x2697	Set RAM Synthesis Mode

Transaction 2 : Set the RAM SYNTHESIS WRITE register	
Code	Description
0x44+ W	I²C address
0x00	Select REFERENCE register to access to WFS Register
0x0001	WFS command : set to RAM SYNTHESIS WRITE
0x0063	Set RAM start address 0x063 for write access
0x0100	DATA 1
0x0102	DATA 2
0x000E	DATA 3

Figure 32: I²C communication sequence for RAM write using RAM ACCESS command

Transaction 1 : Set RAM Synthesis Mode	
Code	Description
0x44+ W	I²C address, write access
0x05	Select CONFIG register
0x2697	Set RAM Synthesis Mode

Transaction 2 : Configure Broadcast	
Code	Description
0x44+ W	I²C address, write access
0x02	Select READ register
0x002B	Set bit BC for RAM_DATA reading

Transaction 3 : Set the RAM SYNTHESIS WRITE register	
Code	Description
0x44+ W	I²C address, write access
0x00	Select REFERENCE register to access to WFS Register
0x0001	WFS command : set to RAM SYNTHESIS WRITE
0x0463	Set RAM address 0x063 for read access

Transaction 4 : Set the RAM SYNTHESIS WRITE register	
Code	Description
0x44+ R	I²C address, read access
0x0000	Read 2-byte

Figure 33: RAM ACCESS sequence for RAM read

6.9.2 0x0003 FIFO DEPTH

Table 23: FIFO DEPTH details

COMMAND: 0x0003 FIFO DEPTH															
Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	COMMAND[15:0] = 0x0003															
1	NOT USED: 0x0000													FIFO DEPTH[2:0]		

WORD, BIT	NAME	DESCRIPTION
Word 1, Bit [2:0]	FIFO DEPTH	0x0: 1024 locations (default) 0x1: 512 locations 0x2: 256 locations 0x3: 128 locations 0x4: 64 locations All other values: 1024 locations. The RAM address ranges are detailed in Table 24.

The FIFO DEPTH command defines RAM locations to be used as a FIFO, used in FIFO mode. The RAM address ranges are detailed in Table 24.

By default, the FIFO depth corresponds to full 1024 RAM locations. Using a smaller FIFO allows preserving sections of RAM that could be used for RAM Synthesis or RAM Playback modes.

PLAY_MODE bits must first be set to RAM PLAYBACK or RAM SYNTHESIS mode (0x2 or 0x3) and CONFIG.OE bit must be set to 0x0 before issuing a FIFO DEPTH command.

Table 24: RAM address range used by FIFO according to FIFO DEPTH value

FIFO DEPTH[2:0]	NUMBER OF RAM LOCATION	RAM ADDRESS RANGE FOR FIFO	
		BEGIN	END
0	1024	0x000	0x3FF
1	512	0x200	0x3FF
2	256	0x300	0x3FF
3	128	0x380	0x3FF
4	64	0x3C0	0x3FF

6.9.3 0x0012 RAM SYNTHESIS

Table 25: RAM SYNTHESIS command details

COMMAND: 0x0012 RAM SYNTHESIS																
Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	COMMAND[15:0] = 0x0012															
1	END WAVE[3:0]				START WAVE[3:0]				NOT USED: 0x0			RELOFF	STOP	NXTWV	NXTSL	RPT

WORD, BIT	NAME	DESCRIPTION
Word 1, Bits [15:12]	END WAVE	Sets the WAVE number (numbered 0x0 to 0xE), which points to the first word of the last WAVE block of the SEQUENCE to play (see section 6.8.2).
Word 1, Bits [11:8]	START WAVE	Sets the WAVE number (numbered 0x0 to 0xE), which points to the first word of the first WAVE block of the SEQUENCE to play (see section 6.8.2).

COMMAND: 0x0012 RAM SYNTHESIS															
Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	COMMAND[15:0] = 0x0012															
1	END WAVE[3:0]				START WAVE[3:0]				NOT USED: 0x0			RELOFF	STOP	NXTWV	NXTSL	RPT

WORD, BIT	NAME	DESCRIPTION
Word 1, Bit [3]	RELOFF	Add a DC offset to each SLICE of the waveform matching the last sample of its previous SLICE. The offset added on the first SLICE is calculated so that it starts at 0V. The RELOFF option can be used to add a DC offset to the waveform played. When RELOFF is used and set to 0x1, the SLICE.MODE of each SLICE blocks of the waveform must be 0x0. Note the following: • Waveform will begin at 0 V amplitude. • Waveform should end with 0 V amplitude. • The SLICE parameters SHAPEUP[3:0] and SHAPEDN[3:0] must be set to 0x0.
Word 1, Bit [3]	STOP	Request to stop playing waveform by preventing SLICEs, WAVEs and SEQUENCE from being repeated (see section 6.8.2). Once the STOP command is issued, the WFS will play only a single cycle (or half-cycle) of all the remaining SLICE or WAVE block(s) of the SEQUENCE. There are no options to force an immediate and sudden end of the haptic waveform playback. This option applies to any waveform being played whether continuously or not. The RPT field must be set to 0x0 when setting STOP to 0x1.
Word 1, Bit [2]	NXTWV	Plays the next WAVE of the SEQUENCE after reaching the end of the current WAVE. This option is used to stop a WAVE being played continuously.
Word 1, Bit [1]	NXTSL	Plays the next SLICE of the SEQUENCE after reaching the end of the current SLICE. This option is used to stop a SLICE being played continuously.
Word 1, Bit [0]	RPT	Enables the SEQUENCE to be repeated indefinitely. When the WAVE block associated with the END WAVE[3:0] has been played, the WAVE block associated with the START WAVE[3:0] will start playing again.

In RAM Synthesis (bits PLAY_MODE[1:0] set to 0x3), the device plays all WAVE blocks starting from START WAVE[3:0] up to END WAVE[3:0], which is referred as the SEQUENCE.

Any write with the RAM SYNTHESIS command indicates that the waveform from START WAVE[3:0] up to END WAVE[3:0] is ready to be played. If OE bit is already set to 0x1, the waveform will start to play immediately after the RAM SYNTHESIS command is issued.

If the AUTO bit is set to 0x1, the waveform will be automatically played upon a sense voltage event. See section 6.4.3 for more detail.

The communication sequence to use the RAM SYNTHESIS command includes the following:

1. Write 0x0012 to REFERENCE register to use the RAM SYNTHESIS command.
2. Write the following word to REFERENCE register:
    a. Bits 15:12 with END WAVE[3:0] (0x0 to 0xE).
    b. Bits 11:8 with START WAVE[3:0] (0x0 to 0xE).
    c. Bits 3:0 with STOP, NXTWV, NXTSL & RPT.

Note that the communication sequence assumes that bits PLAY_MODE[1:0] are set to 0x3.

6.9.4 0x0013 RAM PLAYBACK

Table 26: RAM PLAYBACK command details

	COMMAND: 0x0013 RAM PLAYBACK															
Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	COMMAND[15:0] = 0x0013															
1	RPT	START ADDRESS[4:0]					END ADDRESS[9:0]									
2	0x0	START ADDRESS[9:5]					REPEAT START ADDRESS[9:0]									

WORD, BIT	NAME	DESCRIPTION
Word 1, Bit [15]	RPT	Enables waveform repeat for continuous waveform playback. When enabled, the next sample after the sample fetched at END ADDRESS[9:0] is at REPEAT START ADDRESS[9:0]. When disabled, the waveform ends after fetching the sample at END ADDRESS[9:0]. 0x1: Waveform repeat enabled. 0x0: Waveform repeat disabled.
Word 1, Bits [14:10]	START ADDRESS[4:0]	Sets the 10-bit RAM start address for fetching RAM Playback samples where the 5 LSBs (START ADDRESS[4:0]) are sent in Word 1 and the 5 MSBs (START ADDRESS[9:5]) are sent in Word 2. The START ADDRESS[9:0] field is ignored when continuous waveform playback is already in progress and RPT bit has been set to 0x1 in a previous RAM PLAYBACK command.
Word 2, Bits [14:10]	START ADDRESS[9:5]	
Word 1, Bits [9:0]	END ADDRESS	Sets the 10-bit RAM end address for fetching RAM Playback samples, which corresponds to the address of the last sample to be played before the playback ends (if RPT bit is set to 0x0) or before the playback is repeated (if RPT bit is set to 0x1).
Word 2, Bits [9:0]	REPEAT START ADDRESS	Sets the 10-bit RAM repeat start address for fetching RAM Playback samples when RPT bit is set to 0x1. The field is ignored if RPT bit is set to 0x0.

The START and END ADDRESS[9:0] entered with the RAM PLAYBACK command indicate the location in RAM of the samples to be fetched for waveform playback when the RAM Playback is initiated.

The waveform segment between REPEAT START ADDRESS[9:0] and END ADDRESS[9:0] is repeated when setting RPT to 0x1. To end a waveform playback repetition, a new RAM PLAYBACK command must be issued with RPT set to 0x0 with the END ADDRESS equals to or greater than the initial END ADDRESS[9:0].

The 16-bit samples in RAM use the same format as for Direct Mode (see section 6.5) and FIFO mode (see section 6.6) and includes the bits [11:0] as the waveform amplitude, see REFERENCE[11:0] bits description.

The samples in RAM are written using BURST RAM WRITE command.

The use of the RAM PLAYBACK command indicates that the waveform is ready to be played. Thus, if OE bit is set 0x1, the waveform will start to play when issuing a RAM Playback command.

The communication sequence to program the START ADDRESS[9:0] and END ADDRESS[9:0] using the RAM PLAYBACK command includes the following:

1. Write waveform data in RAM using BURST RAM WRITE command.
2. Write 0x0013 to the REFERENCE register to use the RAM PLAYBACK command.
3. Write word 1 to the REFERENCE register.
4. Write word 2 to the REFERENCE register.

Note that the communication sequence assumes that bits PLAY_MODE[1:0] are set to 0x2.

6.9.5 0x0014 BURST RAM WRITE

Table 27: BURST RAM WRITE command details

	COMMAND: 0x0014 BURST RAM WRITE															
Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	COMMAND[15:0] = 0x0014															
1	NOT USED: 0x00						START ADDRESS [9:0]									
2	NOT USED: 0x00						DATA COUNT [9:0]									
3	DATA [15:0]															

WORD, BIT	NAME	DESCRIPTION
Word 1, Bits [9:0]	START ADDRESS	Defines the 10-bit address from where to start writing in the RAM with the following constraint: 0 ≤ START ADDRESS ≤ 1023
Word 2, Bits [9:0]	DATA COUNT	Defines the number of data words to be written on the RAM with the following constraint: DATA COUNT has a maximum value of 1023. DATA COUNT ≤ 1023 – START ADDRESS
Word 3, Bits [15:0]	DATA	Defines data to be written in the RAM using the same format as the REFERENCE[11:0] bits.

The BURST RAM WRITE command is used to write multiple words to the RAM when using RAM Playback mode (PLAY_MODE[1:0] set to 0x2). The data format uses the same format as the REFERENCE[11:0] bits.

The communication sequence to write to RAM using the BURST RAM WRITE WFS command includes the following:

1. Write 0x0014 to the REFERENCE register to use the BURST RAM WRITE command.
2. Write the RAM START ADDRESS word to the REFERENCE register.
3. Write the DATA COUNT word to the REFERENCE register.
4. Write the number of REFERENCE[15:0] words equal to DATA COUNT. RAM write address is incremented automatically between words.

Note that the communication sequence assumes that PLAY_MODE[1:0] bits are set to 0x2.

6.9.6 0x0015 FULL RAM READ

Table 28: FULL RAM READ command details

COMMAND: 0x0015 FULL RAM READ															
Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	COMMAND[15:0] = 0x0015															
In RAM Synthesis or RAM Playback mode (PLAY_MODE[1:0] set to 0x2 or 0x3), the FULL RAM READ command is used to read the full RAM content on the communication interface. The device will stay in this mode until all the 1024 RAM addresses have been read or until the FULL RAM READ BREAK command is used. The communication sequence to use the FULL RAM READ command includes the following: 1. Set bits RDADDR[4:0] to 0x1B to select RAM_DATA reading. 2. Write 0x0015 to REFERENCE register to use the FULL RAM READ command. 3. Write 0x0000 (or any value except 0xFF15) to REFERENCE register. 4. Read 2 bytes 5. Repeat step 3) and 4) until the last RAM address or until using the FULL RAM READ BREAK command. The RAM address is automatically incremented. Note that the communication sequence requires that PLAY_MODE[1:0] bits are set to 0x2 or 0x3.															

6.9.7 0xFF15 FULL RAM READ BREAK

Table 29: FULL RAM READ BREAK command

COMMAND: 0xFF15 FULL RAM READ BREAK															
Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	COMMAND[15:0] = 0xFF15															
The FULL RAM READ BREAK command 0xFF15 is used to stop the RAM content reading loop started with the FULL RAM READ command.																

6.10 Register Map

Table 30: Main register map

ADDR.	NAME	DEFAULT VALUE	TYPE[4]	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	REFERENCE	0x0000	RW	DATA[15:0]															
0x01	ION_BL	0x03A0	RW	RSVD				FSWMAX[1:0]		SB[1:0]		I_ON_SCALE[7:0]							
0x02	DEADTIME	0x046A	RW	RSVD				DHS[6:0]							DLS[4:0]				
0x03	KP	0x0080	RW	RSVD			XTRIGF	XTRIGR	KP[10:0]										
0x04	KPA_KI	0x02A0	RW	RSVD				KIBASE[3:0]				KPA[7:0]							
0x05	CONFIG	0x1000	RW	ONCOMP[1]	AUTO[1]	SENSE[1]	GAINS[1]	GAIND	PLAY_MODE[1:0]		RET	SYNC	RST	POL_SENS[1]	OE	DS	PLAY_SRATE		
0x06	PARCAP	0x003A	RW	RSVD					CCM	UPI	RSVD	PARCAP							
0x07	SUP_RISE	0x4967	RW	I2C_ADDR[3:0]				LP	VDD[4:0]					TI_RISE[5:0]					
0x08	INT_ENABLE	0x0000	RW	RSVD									IE_FHE	IE_STCHG	IE_MXERR	IE_SENSF[1]	IE_PLAY	IE_MAXP	IE_ERR
0x09	SENSING[1]	0x0000	RW	SIGN	REP[2:0]			STHRESH[11:0]											
0x0A	TRIM	0x0000	RW	TRIMRW[1:0]		RSVD				TRIM_OSC							TRIM_REG[2:0]		
0x0B	COMM	0x001E	RW	RSVD			RDAI	STR	OD	GPIOSEL[2:0]			GPIODIR	TOUT	RDADDR[4:0]				
0x10	IC_STATUS	0x0001	RO	RSVD						STATE[1:0]		OVV	OVT	MXPWR	IDAC	UVLO	SC	FULL	PLAYST
0x11	FIFO_STATE	0x4400	RO	RSVD			ERROR	FULL	EMPTY	FIFO_SPACE[9:0]									
0x18	SENSE_VALUE[1]	0x06CF	RO	POL_SENS	SENSE	GAIN	SENS_FLAG	SENSE_VALUE[11:0]											
0x1B	RAM_DATA	0x0000	RO	RAM_DATA[15:0]															
0x1E	CHIP_ID	0x3781[1]	RO	CHIP_REV[3:0]				CHIP_ID[11:0]											
0x1F	INT_STATUS	0x0000	RO	RSVD									IS_FHE	IS_STCHG	IS_MXERR	IS_SENSF	IS_PLAY	IS_MAXP	IS_ERR

(1) BOS1921 only.

[4] RO are read-only registers.
RW are read/write registers.

6.10.1 0x00 REFERENCE

Table 31: REFERENCE register details

ADDRESS: 0x00			REFERENCE			DEFAULT: 0x0000									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				REFERENCE[11:0]											
REFERENCE[15:0]															

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
11:0	REFERENCE	0x000	RW	In Direct or FIFO mode (PLAY_MODE[1:0] set to 0x0 or 0x1), defines the desired amplitude of the output in 12-bit two's complement format. The device will work with a lower-resolution waveform: shift data left to align MSBs. The amplitude in volts is determined by: $$Amplitude[V_{pk}] = \frac{REFERENCE}{2^{11}-1} \times V_{ref} \times FB_{ratio}$$ Where REFERENCE is REFERENCE[11:0] decimal value, V_{ref} = 3.6 is the internal ADC input range and FB_{ratio} is the feedback ratio of the device defined by GAIND. REFERENCE[11:0] must be set between 0x931 and 0x6CF to output ±95 V when GAIND is set to 0x0, and output ±13.3 V when GAIND is set to 0x1.
15:0	REFERENCE	0x0000	RW	In RAM Playback or RAM Synthesis mode (PLAY_MODE[1:0] set to 0x2 or 0x3), defines the Waveform Synthesizer (WFS) commands, see section 6.9 for more detail.

6.10.2 0x01 ION_BL

Table 32: ION_BL register details

ADDRESS: 0x01			ION_BL			DEFAULT: 0x03A0									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				FSWMAX[1:0]		SB[1:0]		I_ON_SCALE[7:0]							

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
11:10	FSWMAX	0x0	RW	Sets boost converter maximum switching frequency. 0x0: 1 MHz 0x1: 833 kHz 0x2: 666 kHz 0x3: 500 kHz A value of 0x1 is recommended.
9:8	SB	0x3	RW	Sets boost converter blanking time. 0x0: 35 ns 0x1: 44 ns 0x2: 53 ns 0x3: 62 ns Default value should work for most applications.

ADDRESS: 0x01				ION_BL			DEFAULT: 0x03A0								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				FSWMAX[1:0]		SB[1:0]		I_ON_SCALE[7:0]							

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
7:0	I_ON_SCALE	0xA0	RW	Sets the minimum current required to turn on High-Side (HS) switch. I_ON_SCALE[7:0] is determined by: $I\_ON\_SCALE[7:0] = round\left(\frac{Latency}{L_1 \times 2^{-12}} \times R_{sense} \times FB_{ratio}\right)$ Where Latency = 50 ns and FB_{ratio} is the feedback ratio of the device defined by GAIND.

6.10.3 0x02 DEADTIME

Table 33: DEADTIME register details

ADDRESS: 0x02				DEADTIME			DEFAULT: 0x046A								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				DHS[6:0]							DLS[4:0]				

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
11:5	DHS	0x23	RW	Sets the delay between the Low-Side (LS) switch turns off and the High-Side (HS) switch turns on ($t_{dead-HS}$), as per: $t_{dead-HS} = DHS[6:0]{:}\times 1.1\ ns$ DHS[6:0] can be adjusted using the following relation: $DHS[6:0] = \frac{2\pi\sqrt{L_1 \times C_{SW}}}{4 \times 1.1 \times 10^{-9}}$ Where C_{SW} is the parasitic capacitance measured on the node connecting SW pin to L_1. C_{SW} is influenced by the parasitic capacitance and & PCB metal trace connected on SW pin. DHS[6:0] can be adjusted for optimization.
4:0	DLS	0x0A	RW	Sets the delay between the High-Side (HS) switch turn off and the Low-Side (LS) switch turn on ($t_{dead-LS}$), as per: $t_{dead-LS} = DLS[4:0] \times 4.4\ ns$ Default value provides a delay of 44 ns minimum and should work for most applications but DLS[4:0] can be adjusted for optimization.

6.10.4 0x03 KP

Table 34: KP register details

ADDRESS: 0x03			KP			DEFAULT: 0x0080									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD			XTRIGF	XTRIGR		KP[10:0]									

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
12	XTRIGF	0x0	RW	Activates waveform triggering of WAVE block number 0x1 (see Table 17) on GPIO falling edge using RAM Synthesis (PLAY_MODE[1:0] bits set to 0x3). GPIODIR must be set to 0x1 to set the GPIO as an input and use the GPIO external trigger functionality. 0x1: Falling edge external trigger activated on GPIO 0x0: Falling edge external trigger disabled.
11	XTRIGR	0x0	RW	Activates waveform triggering of WAVE block number 0x0 (see Table 17) with GPIO rising edge using RAM Synthesis (PLAY_MODE[1:0] bits set to 0x3). GPIODIR must be set to 0x1 to set the GPIO as an input and use the GPIO external trigger functionality. 0x1: Rising edge external trigger activated on GPIO 0x0: Rising edge external trigger disabled.
10:0	KP	0x080	RW	Sets the physical value ($kp_{physical}$) of the integrated PI controller proportional gain, which is determined by: $$Kp_{physical}[{}^{A}/_{V}] = \frac{KP \times 2^{-14}}{R_{sense}}$$

6.10.5 0x04 KPA_KI

Table 35: KPA_KI register details

ADDRESS: 0x04			KPA_KI			DEFAULT: 0x02A0									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				KIBASE[3:0]				KPA[7:0]							

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
11:8	KIBASE	0x2	RW	Determines the pole location (f_{pole}) of the integrated PI controller, which is determined by: $$f_{pole}[kHz] = \frac{1024}{2^{KIBASE}}$$
7:0	KPA	0xA0	RW	Determines the proportional gain (KPc) used in the integrated PI controller, which is calculated by: $$KPc = KP + 2 \times KPA \times \text{AMPLITUDE}$$ Where KP is KP[10:0] and AMPLITUDE is REFERENCE[11:0] decimal values.

6.10.6 0x05 CONFIG

Table 36: CONFIG register details

ADDRESS: 0x05			CONFIG				DEFAULT: 0x1000								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ONCOMP	AUTO	SENSE	GAINS	GAIND	PLAY_ MODE[1:0]		RET	SYNC	RST	POL_ SENSE	OE	DS	PLAY_SRATE[2:0]		

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
15	ONCOMP (BOS1921 only)	0x0	RW	Activates the sensing comparator to detect a piezo signal meeting the threshold defined by STHRESH[11:0] and automatically set SENS_FLAG to 0x1. SENSE needs to be set to 0x1 to use the sensing comparator. 0x1: Active 0x0: Inactive ONCOMP needs to be set back to 0x0 to clear SENS_FLAG after a detection. Set ONCOMP back to 0x1 to reactivate an automatic detection.
14	AUTO (BOS1921 only)	0x0	RW	Enables a programmed waveform to be triggered automatically. This feature needs ONCOMP and SENSE set to 0x1. See section 6.4.3 for more detail on for Automatic Haptic Playback. 0x1: Enable 0x0: Disable The AUTO bit is cleared automatically after the waveform is played. Set AUTO bit back to 0x1 to enable again the programmed waveform to be triggered automatically.
13	SENSE BOS1921 only)	0x0	RW	Enables piezo sensing by setting OUT+ and OUT- pins to high impedance to read the piezo actuator voltage that can be read with SENSE_VALUE[11:0]. 0x1: Enable 0x0: Disable Note the following: - PLAYST bit must be 0x1 before setting SENSE bit to 0x1. - ONCOMP, SIGN & AUTO bits and SENSING register have no effect if SENSE bit is set to 0x0. - If AUTO is set to 0x1, a successful detection clears SENSE bit.
12	GAINS (BOS1921 Only)	0x1	RW	Sets the sensing resolution by fixing the gain of the feedback loop (FB_{ratio}). 0x0: SENSE_VALUE[11:0] LSB is set to 54.5 mV & FB_{ratio} is set to 31 0x1: SENSE_VALUE[11:0] LSB is set to 7.6 mV & FB_{ratio} is set to 4.33
11	GAIND	0x0	RW	Sets the output voltage (V_{OUT}) range by fixing the gain of the feedback loop (FB_{ratio}). 0x0: V_{OUT} range set to ±95 V & FB_{ratio} set to 31 0x1: V_{OUT} range set to ±13.28 V & FB_{ratio} set to 4.33
10:9	PLAY_MODE	0x0	RW	Sets haptic waveform playback mode. 0x0: Direct mode (see section 6.5) 0x1: FIFO mode (see section 6.6) 0x2: RAM Playback mode (see section 6.7) 0x3: RAM Synthesis mode (see section 6.8)

ADDRESS: 0x05			CONFIG				DEFAULT: 0x1000								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ONCOMP	AUTO	SENSE	GAINS	GAIND	PLAY_ MODE[1:0]		RET	SYNC	RST	POL_ SENSE	OE	DS	PLAY_SRATE[2:0]		

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
8	RET	0x0	RW	Enables state and data retention of registers and RAM when using SLEEP mode (DS set to 0x1). 0x0: Registers and RAM data retention is enabled 0x1: Registers and RAM data retention is disabled
7	SYNC	0x0	RW	Activates multi-chip synchronization. 0x1: Enable 0x0: Disable
6	RST	0x0	RW	Initiates a software reset. The device resets internal registers to default values and goes to IDLE mode. RST bit self-clears once the reset is completed. Make sure REFERENCE[11:0] is 0x0 when setting RST to 0x1 in Direct or FIFO mode. 0x1: Device software reset 0x0: Normal operation
5	POL_SENSE (BOS1921 Only)	0x0	RW	Defines the polarity of the OUT+/OUT- pins when the device is sensing (SENSE bit is set to 0x1). 0x1: OUT+ pin is connected to VDD 0x0: OUT- pin is connected to VDD
4	OE	0x0	RW	Enables haptic waveform playback or piezo actuator sensing (BOS1921 only). 0x1: Enable 0x0: Disable OE bit will clear automatically at the end of a waveform if PLAY_MODE[1:0] is set to 0x2 or 0x3.
3	DS	0x0	RW	Sets the power mode when the device is not playing waveform (e.g., bit OE is set to 0x0). 0x0: IDLE 0x1: SLEEP
2:0	PLAY_SRATE	0x0	RW	Defines the sample rate used to create the haptic waveform in Direct, FIFO or RAM Playback mode (PLAY_MODE[1:0] bits set to 0x0, 0x1 or 0x2), as follows: 0x0: 1024 ksps 0x1: 512 ksps 0x2: 256 ksps 0x3: 128 ksps 0x4: 64 ksps 0x5: 32 ksps 0x6: 16 ksps 0x7: 8 ksps

6.10.7 0x06 PARCAP

Table 37: PARCAP register details

ADDRESS: 0x06			PARCAP			DEFAULT: 0x003A									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD					CCM	UPI	RSVD	PARCAP[7:0]							

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
10	CCM	0x0	RW	Enables the BOS1921/BOS1931 to automatically choose whether to operate the buck-boost converter in continuous conduction mode (CCM) or discontinuous conduction mode (DCM). Otherwise, the device operates only in DCM mode. 0x0: DCM mode only 0x1: BOS1921/BOS1931chooses between DCM or CCM mode It is recommended to set CCM bit to 0x1 only when the inductor in the design has a value of 10 µH. Using CCM mode allow for greater device output drive capacity at the expense of more noise.
9	UPI	0x0	RW	Enables the Unidirectional Power Input. 0x0: Disable 0x1: Enable
7:0	PARCAP	0x3A	RW	Internal parameter determined by: $$PARCAP[7:0] = \frac{\sqrt{\frac{C_{SW}}{L_1}}}{2^{-11}} \times R_{sense} \times FB_{ratio}$$ Where C_{SW} is the parasitic capacitance measured on the node connecting SW pin to L_1. C_{SW} is influenced by the parasitic capacitance and & PCB metal trace connected on SW pin and PCB layout and FB_{ratio} is the feedback ratio of the device defined by GAIND.

6.10.8 0x07 SUP_RISE

Table 38: SUP_RISE register details

ADDRESS: 0x07				SUP_RISE					DEFAULT: 0x4967						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I2C_ADDR[3:0]				LP	VDD[4:0]					TI_RISE[5:0]					

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
15:12	I2C_ADDR	0x4	RW	Sets the 4 LSBs of the 7-bit legacy I²C static address, i.e., I²C address = (0x4, I2C_ADDR[3:0]). Also sets the I3C 4-bit Instance ID (i.e., bits [15:12] of the Provisional ID, see Table 13). The value of I2C_ADDR[3:0] can be changed only if GPIODIR is set to 0x1 and GPIO pin is at a logic-level low. The I2C_ADDR[3:0] value is not reset by a software reset (RST set to 0x1) and is preserved when the device goes to SLEEP mode, regardless of the state of the RET bit. A value of 0x0 is returned on a read, regardless of the I2C_ADDR[3:0] value.
11	LP	0x1	RW	Enables lower power when chip is in IDLE mode. Default value should work for most applications. 0x1: Enable low power 0x0: Disable low power
10:6	VDD	0x05	RW	Represents the supply voltage seen at RP/VDD pin and is defined by: $$VDD[4:0] = \frac{\left(\frac{V_{DD}[V]}{0.026}\right) - 128}{2}$$ For VDD[4:0] > 31, use 0x1F. For VDD[4:0] < 0, use 0x00.
5:0	TI_RISE	0x27	RW	Sets the proportional gain for the offset determined by: $$TI_{RISE}[5:0] = \frac{T_{CLK} \times 31.25}{L_1} \times \frac{FB_{ratio}}{R_{sense}}$$ Where TCLK =70 ns and FB_{ratio} is the feedback ratio of the device defined by GAIND.

6.10.9 0x08 INT_ENABLE

Table 39: INT_ENABLE register details

ADDRESS: 0x08				INT_ENABLE		DEFAULT: 0x0000									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									IE_FHE	IE_STCHG	IE_MXERR	IE_SENSF	IE_PLAY	IE_MAXP	IE_ERR

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
6	IE_FHE	0x0	RW	Enables the FIFO Half Empty Interrupt. In FIFO mode (PLAY_MODE[1:0] set to 0x1), the interrupt triggers when the FIFO is at least half empty. 1: interrupt is enabled 0: interrupt is disabled
5	IE_STCHG	0x0	RW	Enables Device State Change Interrupt. The interrupt triggers when the device state indicated by STATE[1:0] changes. 1: interrupt is enabled 0: interrupt is disabled
4	IE_MXERR	0x0	RW	Enables Max Error Interrupt. The interrupt triggers when there is a difference between the waveform played on the output and the setpoint, which typically occurs when the output haptic waveform is too abrupt, or the capacitive load is too high. 1: interrupt is enabled 0: interrupt is disabled
3	IE_SENSF	0x0	RW	Enables Sense Voltage Event Interrupt. The interrupt triggers when a Sense Voltage Event is detected (see section 6.4). 1: interrupt is enabled 0: interrupt is disabled
2	IE_PLAY	0x0	RW	Enables Waveform Playback Status Interrupt. The interrupt triggers when PLAYST is set to 0x1. 1: interrupt is enabled 0: interrupt is disabled
1	IE_MAXP	0x0	RW	Enables Max Power Interrupt. The interrupt triggers when maximum amount of power is used and MXPWR is set to 0x1. 1: interrupt is enabled 0: interrupt is disabled
0	IE_ERR	0x0	RW	Enables Error State Interrupt. The interrupt triggers when the device is in error state and STATE[1:0] is set to 0x3. 1: interrupt is enabled 0: interrupt is disabled

6.10.10 0x09 SENSING (BOS1921 Only)

Table 40: SENSING register details

ADDRESS: 0x09				SENSING					DEFAULT: 0x0000						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN	REP[2:0]			STHRESH[11:0]											

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
15	SIGN	0x0	RW	Defines if voltage feedback value should be above or below the threshold (STHRESH[11:0]) to generate a sense voltage event (ONCOMP must be set to 0x1). 0x1: Below 0x0: Above
14:12	REP	0x0	RW	Amount of time the sense voltage needs to be above or below STHRESH[11:0] to generate a sense voltage event (ONCOMP must be set to 0x1). 0x0: 8 µs 0x1: 16 µs 0x2: 256 µs 0x3: 512 µs 0x4: 1024 µs 0x5: 2048 µs 0x6: 4088 µs 0x7: 8168 µs
11:0	STHRESH	0x000	RW	Sets the differential voltage required at OUT+/OUT- pins to generate a sense voltage event (ONCOMP must be set to 0x1). The amplitude (V) in volts is determined by: $$V = \frac{STHRESH[11:0]}{2^{11}-1} \times V_{ref} \times FB_{ratio}$$ Where V_{ref} = 3.6 V is the internal ADC input range, FB_{ratio} is the feedback ratio of the device defined by GAINS and STHRESH[11:0] is a 12-bit signed number. With GAINS set to 0x1, the following limits apply: • Maximum allowable STHRESH[11:0] value is 0x6CF, corresponding to 13.28 V • Minimum allowable STHRESH[11:0] value is 0xFD0, corresponding to -350 mV

6.10.11 0x0A TRIM

Table 41: TRIM register details

ADDRESS: 0x0A			TRIM			DEFAULT: 0x0000									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRIMRW[1:0]		RSVD				TRIM_OSC[6:0]							TRIM_REG[2:0]		

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
15:14	TRIMRW	0x0	RW	Trim control bits for adjusting the internal clock oscillator frequency (TRIM_OSC[6:0]) and 1.8 V internal regulator voltage (TRIM_REG[2:0]), see Figure 34. Hardware fuses values vary from chip-to-chip. More detail is available in the section 6.2.14. TRIMRW[1:0] bits are automatically reset to 0x0 after each operation. 0x0: Default behaviour where Hardware fuses are latched to the Trim Block at power-up 0x1: Resets the Trim Block with the Hardware Fuses and then transfers Trim Block data to TRIM_OSC[6:0] & TRIM_REG[2:0] for reading (wait for 1 ms before reading) 0x2: Transfers Trim Block data to TRIM_OSC[6:0] & TRIM_REG[2:0] for reading (wait for 1 ms before reading) 0x3: Writes TRIM_OSC[6:0] & TRIM_REG[2:0] to Trim Block and transfers back Trim Block data to TRIM_OSC[6:0] & TRIM_REG[2:0] for reading (wait for 1 ms before reading)
9:3	TRIM_OSC	0x00	RW	Oscillator trimming bits in two's complement. The step size is approximately 150 kHz. Maximum frequency at 0x1F. Minimum frequency at 0x20. Excessive change in oscillator frequency may induce circuit malfunction. This is an advanced feature.
2:0	TRIM_REG	0x0	RW	The internal 1.8 V regulator (REG pin) trimming bits in two's complement. The step size is approximately 22 mV. Maximum voltage at 0x3 Minimum voltage at 0x4

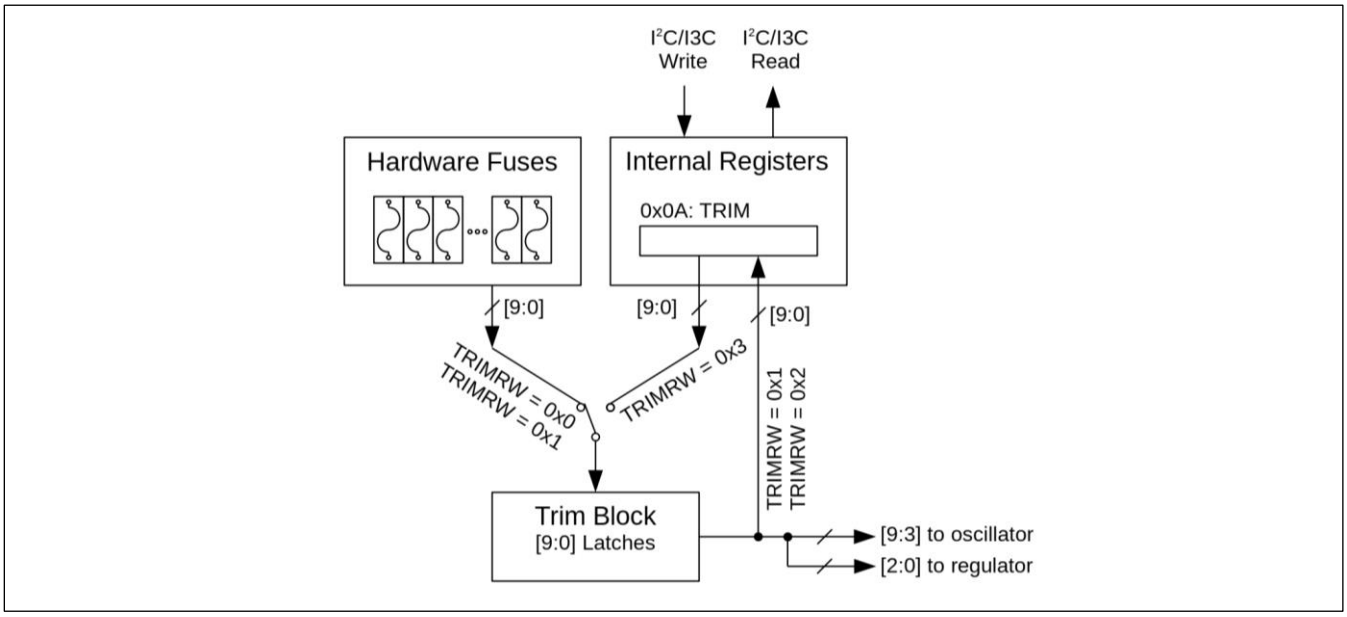


Figure 34: Trim control block diagram

6.10.12 0x0B COMM

Table 42: COMM register details (BOS1921)

ADDRESS: 0x0B			COMM			DEFAULT: 0x001E									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD			RDAI	STR	OD	GPIOSEL[2:0]			GPIODIR	TOUT	RDADDR[4:0]				

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
12	RDAI	0x0	RW	Activates an auto-increment of RDADDR[4:0] bits after a read operation. 0x0: RDADDR[4:0] bits are not modified 0x1: RDADDR[4:0] bits increment after a register read If RDADDR[4:0] bits are 0x1F, the incremented value will be 0x00.
11	STR	0x0	RW	Enables automatic incrementing of the register address during communication. Allows writing several consecutive registers using only the address of the first register (see Figure 20). 0x1: Address auto-increment every two bytes 0x0: No address auto-increment Regardless the STR bit value, an address of 0x00 (REFERENCE register) will not automatically increment to allow more efficient writes to the FIFO or Waveform Synthesizer.
10	OD	0x0	RW	Sets the GPIO output type. 0x0: Open-Drain 0x1: Push-Pull

ADDRESS: 0x0B			COMM			DEFAULT: 0x001E									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD			RDAI	STR	OD	GPIOSEL[2:0]			GPIODIR	TOUT	RDADDR[4:0]				

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
9:7	GPIOSEL	0x0	RW	Selects the active low signal that is output on the GPIO pin when GPIODIR is set to 0x0. 0x0: Device Reset State Indicates if the device is in reset process. 0: Device is in reset state 1: Device is not in reset state and is ready for operation 0x1: Waveform Playback Status Indicates the state of PLAYST bit. 0: PLAYST bit is 0x1 1: PLAYST bit is 0x0 0x2: Error State Indicates if the device is in error state (STATE[1:0] set to 0x3): 0: Error detected 1: No error detected 0x3: Max Power Indicates if maximum amount of power is used (state of MXPWR): 0: Maximum power, distortion likely 1: Amount of power is acceptable 0x4: FIFO Full In FIFO mode (PLAY_MODE[1:0] set to 0x1), indicates if the FIFO is FULL (state of FULL bit): 0: FIFO is full 1: FIFO is not full 0x5: Interrupt Indicates if one of the interrupts of INT_STATUS register is 0x1: 0: Interrupt pending 1: No Interrupt pending 0x6: Sense Trigger Indicates if sensed data met the detection trigger conditions (state of SENS_FLAG bit): 0: Sense detection condition met 1: Sense detection condition not met 0x7: FIFO Half Empty In FIFO mode (PLAY_MODE[1:0] set to 0x1), indicates if the FIFO is at least half empty: 0: At least half of the FIFO locations are available 1: Less than half of the FIFO locations are available
6	GPIODIR	0x0	RW	Sets the direction of the GPIO pin. 0x0: GPIO is an output 0x1: GPIO is an input

ADDRESS: 0x0B			COMM			DEFAULT: 0x001E									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD			RDAI	STR	OD	GPIOSEL[2:0]			GPIODIR	TOUT	RDADDR[4:0]				

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
5	TOUT	0x0	RW	Enables a timeout mechanism which forces the device into SLEEP if it fails to receive the necessary data samples during waveform playback. The conditions for the timeout are the following: • Waveform playback mode is either FIFO or Direct mode (PLAY_MODE[1:0] bits set to 0x0 or 0x1). • The output is enabled (OE bit set to 0x1). • The PLAYST bit has been 0x1 for at least 4 ms. 0x1: Enable 0x0: Disable Note that PLAY_SRATE[2:0] bits are reset to 0x7 when the device enters SLEEP following a timeout event.
4:0	RDADDR	0x1E	RW	Address of the internal register whose content is returned on the communication bus during a read. Reset value is CHIP_ID register address (0x1E).

6.10.13 0x10 IC_STATUS

Table 43: IC_STATUS register details

ADDRESS: 0x10			IC_STATUS			DEFAULT: 0x0001									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD						STATE[1:0]		OVV	OVT	MXPWR	IDAC	UVLO	SC	FULL	PLAYST

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
9:8	STATE	0x0	RO	Indicates the state of the device. STATE[1:0] = 0x3 indicates that one of the following errors occurred: OVV, OVT, IDAC, UVLO or SC. 0x0: IDLE 0x1: CALIBRATION 0x2: RUN. 0x3: ERROR
7	OVV	0x0	RO	Overvoltage fault bit. The voltage level that triggers the fault depends on GAIND value. If GAIND is set to 0x0, the fault is triggered at 100 V and above. If GAIND is set to 0x1, the fault is triggered at 14 V and above. 0x1: Output voltage exceeded the maximum voltage allowed 0x0: Output voltage is OK
6	OVT	0x0	RO	Overtemperature fault bit. 0x1: Overtemperature detected on the device 0x0: Device temperature is OK
5	MXPWR	0x0	RO	Maximum Power warning bit. Indicates that R_{sense} reached the maximum allowed current. 0x1: Maximum power, distortion likely 0x0: Acceptable amount of power

ADDRESS: 0x10				IC_STATUS				DEFAULT: 0x0001							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD						STATE[1:0]		OVV	OVT	MXPWR	IDAC	UVLO	SC	FULL	PLAYST

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
4	IDAC	0x0	RO	IDAC status bit. 0x1: Problem with current detection 0x0: No problem with current detection A problem with the IDAC most likely indicates that R_{sense} or L_1 is disconnected. To recover from an IDAC error, a software reset must be done using CONFIG.RST bit.
3	UVLO	0x0	RO	V_{DD} Under-voltage fault bit. 0x1: V_{DD} under-voltage detected while trying to output a waveform 0x0: V_{DD} voltage is high enough
2	SC	0x0	RO	Piezo load short circuit fault bit. 0x1: Short circuit detected on the piezo load 0x0: No short circuit detected
1	FULL	0x0	RO	Indicates if the FIFO is full when using FIFO mode (PLAY_MODE[1:0] set to 0x1). 0x1: FIFO is full 0x0: FIFO is not full
0	PLAYST	0x1	RO	Waveform playback multi-function status bit. Its function depends on PLAY_MODE[1:0] value. In Direct mode (PLAY_MODE[1:0] set to 0x0), PLAYST bit indicates when new data is needed: 0: No sample required 1: Next sample required In FIFO mode (PLAY_MODE[1:0] set to 0x1), PLAYST bit indicates when FIFO is empty: 0: FIFO is not empty 1: FIFO is empty In RAM Synthesis or RAM playback mode (PLAY_MODE[1:0] set to 0x2 or 0x3), PLAYST bit indicates when the haptic waveform has finished playing: 0: Waveform is not done 1: Waveform is done

6.10.14 0x11 FIFO_STATE

Table 44: FIFO_STATE register details

ADDRESS: 0x11			FIFO_STATE			DEFAULT: 0x4400									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD			ERROR	FULL	EMPTY	FIFO_SPACE[9:0]									

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
12	ERROR	0x0	RO	Indicates if the device is in error state (STATE[1:0] set to 0x3), i.e., any of the following faults has occurred: OVV, OVT, IDAC, UVLO or SC. 0x1: An internal error occurred 0x0: No error
11	FULL	0x0	RO	Same as FULL bit.
10	EMPTY	0x1	RO	Same as PLAYST bit.
9:0	FIFO_SPACE	0x000	RO	Indicates the amount of free space available in FIFO for new data. When FIFO Depth is set to 1024 (using FIFO DEPTH command), a FIFO_SPACE value of 0x000 indicates that either there are 1024 free spaces available (if EMPTY bit is 0x1) or that there is no free space (if EMPTY bit is 0x0).

6.10.15 0x18 SENSE_VALUE (BOS1921 Only)

Table 45: SENSE_VALUE register details

ADDRESS: 0x18			SENSE_VALUE			DEFAULT: 0x06CF									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POL_SENSE	SENSE	GAIN	SENS_FLAG	SENSE_VALUE[11:0]											

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
15	POL_SENSE	0x0	RO	Indicates the polarity of the output when using sensing mode (SENSE is set to 0x1). 0x1: OUT+ pin is connected to V_{DD} 0x0: OUT- pin is connected to V_{DD}
14	SENSE	0x0	RO	Indicates if the device is in sensing mode (SENSE bit is set to 0x1). If the value is not 0x1, then the SENS_FLAG and SENSE_VALUE[11:0] bits should be ignored. 0x0: The device is not in sensing mode 0x1: The device is in sensing mode
13	GAIN	0x0	RO	Gain of the feedback loop (FB_{ratio}) being used by the controller. In normal operation, this value corresponds to GAINS bit when the device is in sensing mode (SENSE bit set to 0x1), otherwise it corresponds to GAIND bit.
12	SENS_FLAG	0x0	RO	Flag indicating when the voltage sensed is above or below the threshold in sense mode. To reset the flag, set ONCOMP to 0x0. 0x1: signal above/below threshold 0x0: Nothing detected

ADDRESS: 0x18			SENSE_VALUE			DEFAULT: 0x06CF									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POL_ SENSE	SENSE	GAIN	SENS_ FLAG	SENSE_VALUE[11:0]											

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
11:0	SENSE_VALUE	0x6CF	RO	Signed representation of the sensed signal. The amplitude in volts is defined by: $$Amplitude[V] = \frac{SENSE\_VALUE[11:0]}{2^{11}-1} \times V_{ref} \times FB_{ratio}$$ Where V_{ref} = 3.6 V is the internal ADC input range and FB_{ratio} is the feedback ratio of the device defined by GAINS.

6.10.16 0x1B RAM_DATA

Table 46: RAM_DATA register details

ADDRESS: 0x1B			RAM_DATA			DEFAULT: 0x0000									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAM_DATA[15:0]															

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
15:0	RAM_DATA	N/A	RO	Value of data read from RAM. To be used in conjunction with the FULL RAM READ or RAM ACCESS WFS commands in read mode.

6.10.17 0x1E CHIP_ID

Table 47: CHIP_ID register details

ADDRESS: 0x1E			CHIP_ID			DEFAULT: 0x3781 (BOS1921), 0x378B (BOS1931)									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHIP_REV[3:0]				CHIP_ID[11:0]											

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
15:12	CHIP_REV	0x3	RO	Indicates the chip revision. 0x3: Revision D 0x2: Revision C 0x1: Revision B
11:0	CHIP_ID	0x781	RO	Indicates the chip ID. 0x781: BOS1921 0x78B: BOS1931

6.10.18 0x1F INT_STATUS

Table 48: INT_STATUS register details

ADDRESS: 0x1F			INT_STATUS			DEFAULT: 0x0000									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									IS_FHE	IS_STCHG	IS_MXERR	IS_SENSF	IS_PLAY	IS_MAXP	IS_ERR

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
6	IS_FHE	0x0	RO	FIFO Half Empty Interrupt Status. Cleared on read. In FIFO mode (PLAY_MODE[1:0] set to 0x1), the interrupt triggers when the FIFO is at least half empty. 1: interrupt is active 0: interrupt is not active
5	IS_STCHG	0x0	RO	State Change Interrupt Status. Cleared on read. The interrupt triggers when the device state indicated with STATE[1:0] has changed. 1: interrupt is active 0: interrupt is not active
4	IS_MXERR	0x0	RO	Max Error Interrupt Status. Cleared on read. The interrupt triggers when there is a difference between the waveform played on the output and the setpoint, which typically occurs when the output haptic waveform is too abrupt, or the capacitive load is too high. 1: interrupt is active 0: interrupt is not active
3	IS_SENSF	0x0	RO	Sense Trigger Interrupt Status. Cleared on read. The interrupt triggers when sensed data meet the detection trigger conditions and SENS_FLAG is set to 0x1. 1: interrupt is active 0: interrupt is not active
2	IS_PLAY	0x0	RO	Waveform Playback Interrupt Status. Cleared on read. The interrupt triggers when PLAYST is set to 0x1. 1: interrupt is active 0: interrupt is not active
1	IS_MAXP	0x0	RO	Max Power Interrupt Status. Cleared on read. The interrupt triggers when maximum amount of power is used and MXPWR is set to 0x1. 1: interrupt is active 0: interrupt is not active
0	IS_ERR	0x0	RO	Error State Interrupt Status. Cleared on read. The interrupt triggers when the device is in error state and STATE[1:0] is set to 0x3. 1: interrupt is active 0: interrupt is not active

7 Implementation

This section presents the following different BOS1921/BOS1931 configurations:

- Typical configuration, using UPI bit set to 0x0.
- UPI configuration, using UPI bit set to 0x1.
- Differential output configuration, driving a bipolar voltage on a single piezo actuator.
- Single-ended output configuration, driving a unipolar voltage on 2 piezo actuators.

Note that shorting the VBUS pin with the RP/VDD pin in the typical configuration is not mandatory but allows for better power efficiency.

7.1 Differential Output Configuration

Differential output configuration is required for applications using both sensing and driving capabilities. In this configuration, piezoelectric actuator is driven with one terminal connected to OUT+ pin and the other terminal connected to OUT- pin. This configuration can achieve a differential output voltage of 190 V_{pk-pk}.

Typical application schematics of the differential output configuration are shown in Figure 35 and Figure 36, without and with Unidirectional Power Input (UPI) configuration. The BOM list is detailed in Table 49.

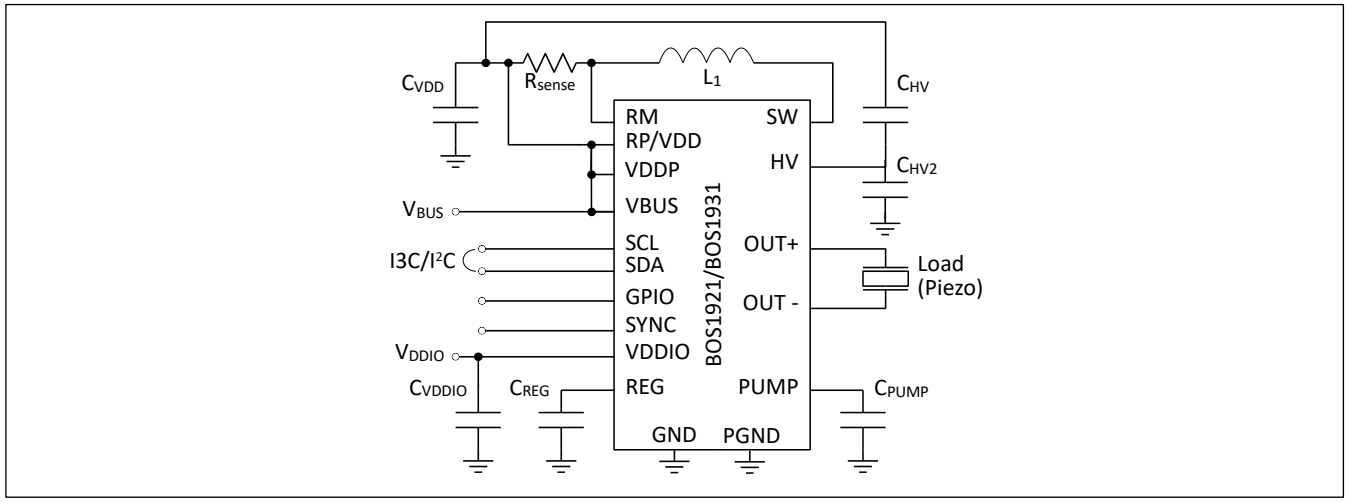


Figure 35: Schematic using differential output and typical configuration (UPI bit set to 0x0)

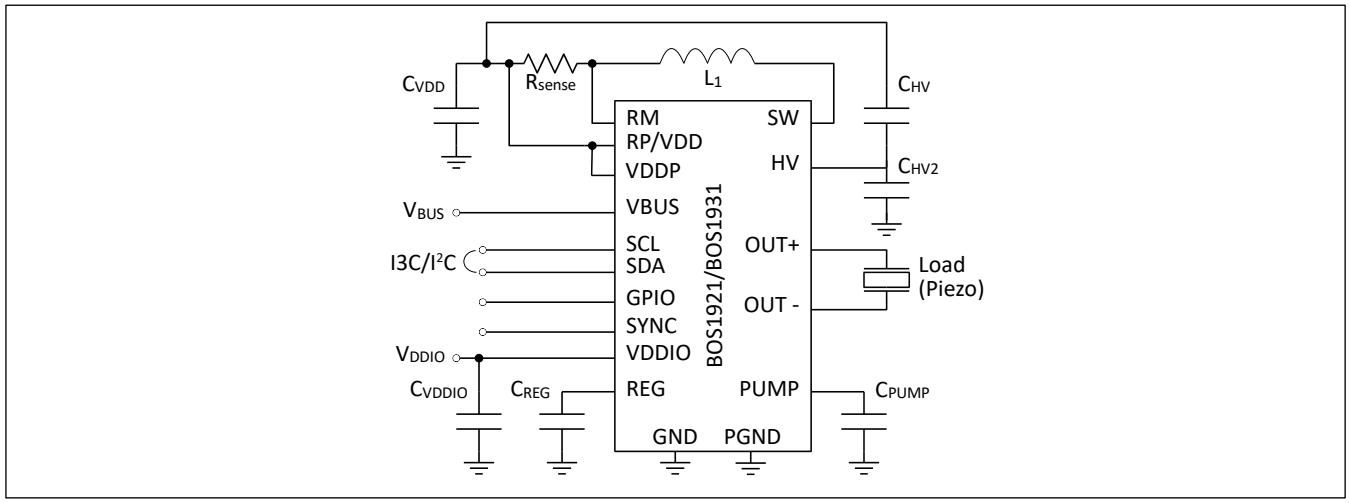


Figure 36: Schematic using differential output and UPI configuration (UPI bit set to 0x1)

7.2 Single-Ended Configuration

When sensing is not needed (BOS1921 and BOS1931), the single-ended output configuration allows driving two actuators independently to reduce the bill-of-material, see Figure 37. With this configuration, the piezo actuators positive terminal must be connected respectively to OUT+ and OUT- while both actuators negative terminals are connected to VDD.

This configuration can output up to 95 V waveform with positive polarity on each actuator. A bipolar waveform must be programmed to output a waveform on 2 actuators. The positive programmed voltage will output on Load 1 while the negative programmed voltage will output on Load 2.

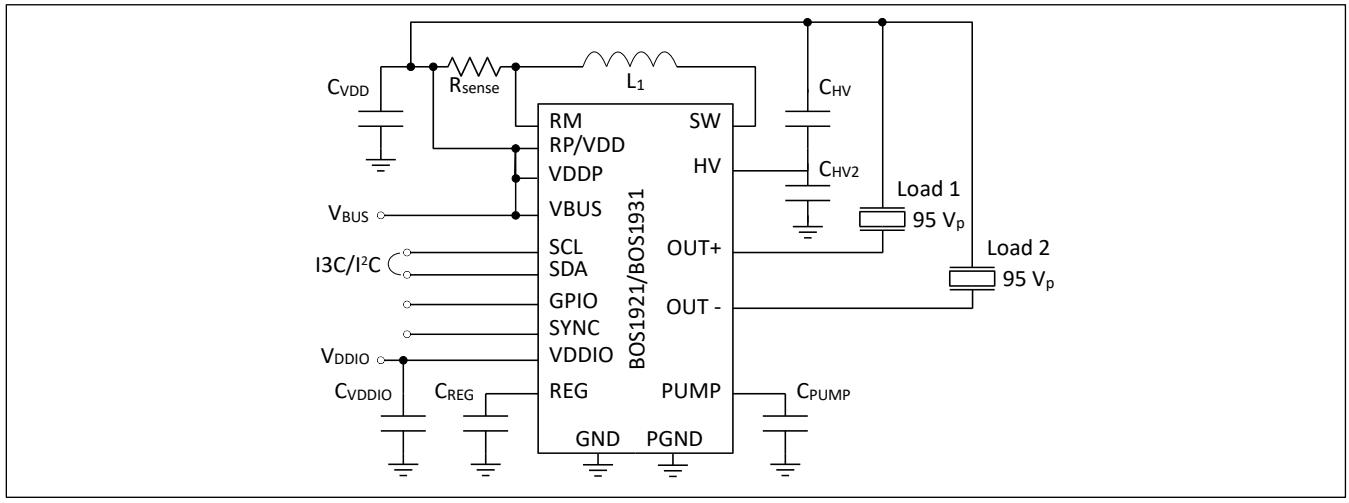


Figure 37: Typical schematic with single-ended output configuration (UPI bit set to 0x0)

7.3 External Components

Typical values of external components are presented in Table 49. See section 7.5 and application notes for details on selecting components.

Table 49: Recommended external components for 190 V_{pk-pk} / 100 nF load

COMPONENT	DESCRIPTION	TYPICAL VALUE FOR MAXMUM LOAD	TYPICAL VALUE FOR 10 nF LOAD
C_L	Load capacitance	100 nF	10 nF
C_{VDD}	V_{DD} capacitor	10 µF (UPI bit set to 0x0) 100 µF (UPI bit set to 0x1)	10 µF
C_{REG}	REG pin capacitor	100 nF	
C_{PUMP}	PUMP pin capacitor		
C_{VDDIO}	V_{DDIO} decoupling capacitor		
C_{HV}	Capacitor on HV pin to VBUS	10 nF	1 nF
C_{HV2}[5]	Capacitor on HV pin to GND	3.9 nF	1.5 nF
R_{sense}	Current sense resistor	0.2 Ω	1 Ω
L_1	Boost inductor	10 µH	68 µH

7.4 Initialization

7.4.1 Power-Up Sequence

1. Apply power to the BOS1921/BOS1931 device with the following criteria:
    a. The V_{BUS} voltage must ramp-up at a minimum rate of 1 V/ms .
    b. The V_{DDIO} pin must be powered up after the V_{BUS} pin or at the same time.
2. Wait for 3 ms during which the BOS1921/BOS1931 starts-up with the following sequence:
    a. Power-up
    b. Initialization
    c. Going to SLEEP mode.

    As shown in Figure 38, V_{BUS}, GPIO & REG pin voltage can be monitored to assess device initialisation.
3. Wake-up from SLEEP by writing on the I^2C/I3C bus (see section 6.3.2.1 for I^2C and 6.3.2.2 for I3C).
4. Wait 50 µs for the BOS1921/BOS1931 to reach IDLE mode.
5. Program the desired internal registers according to your application.
6. BOS1921/BOS1931 is ready for waveform playback.

[5] C_{HV2} is recommended for reduction of high frequency noise.

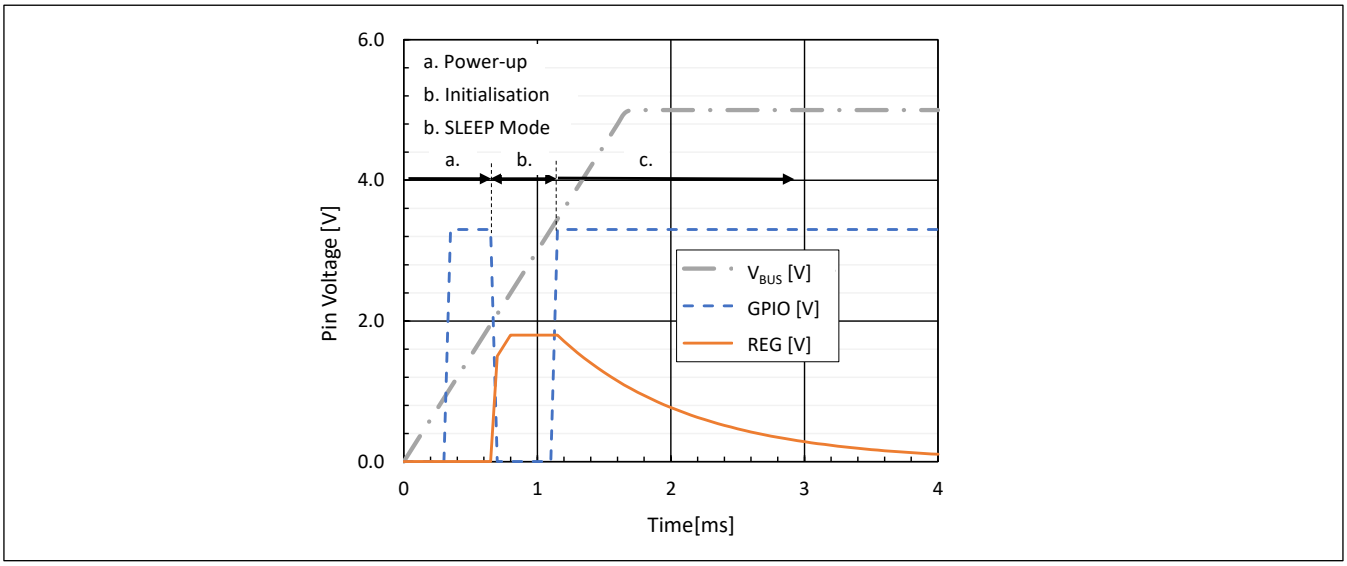


Figure 38: Typical V_{BUS}, GPIO & REG pin voltage during initialisation

7.4.2 Start-Up Sequence

After the initial power-up sequence, the following start-up sequence applies:

- From SLEEP mode, one must perform steps 3 to 6 of the section 7.4.1.
- From IDLE mode, BOS1921/BOS1931 is ready for waveform playback.

7.5 Design Methodology: selection of component

7.5.1 Load Selection

The BOS1921/BOS1931 is designed to drive a capacitive load impedance (Z_L) of up to 5.3 kΩ at 190 V_{pk-pk}, which gives 100 nF at 300 Hz. Larger load capacitances can be driven if the waveform amplitude is reduced (see Figure 14). The conditions must be selected so as not to exceed the maximum peak transient current at SW pin (I_{SW}) of 1.3 A, which is limited by R_{sense} (see section 7.5.3 for R_{sense} selection).

You can use the following procedure to estimate I_{SW} using the desired conditions (I_{SW} could be higher in practice):

1. Set the output signal maximum frequency (f_{OUT}). e.g., 200 Hz.
2. Set the maximum amplitude of the waveform (V_{pk}). e.g., 95 V for a 190 V_{pk-pk} output.
3. Set the minimum supply voltage (V_{BUS}) value during operation. e.g., 3 V.
4. Calculate the I_{SW} and ensure it does not exceed 1.3 A:

Bipolar Waveform	**Unipolar Waveform**	
$V_{out} = V_{pk}\sin(45°) + V_{BUS}$	$V_{out} = \frac{V_{pk}}{2}(1 + \sin(30°)) + V_{BUS}$	(1)
$\overline{I_{out}} = 2\pi f_{OUT} C_L V_{pk} \cos(45°)$	$\overline{I_{out}} = \pi f_{OUT} C_L V_{pk} \cos(30°)$	(2)

5. Calculate the average input current using:

$$\overline{I_{in}} = 1.5 \times \frac{\overline{I_{out}} \times V_{out}}{V_{BUS}} \quad (3)$$

6. Calculate the inductor peak current (current at SW pin):

$$I_{SW} = C \times \overline{I_{in}} \quad (4)$$

With *C* equals to 2 if only DCM mode is used (CCM bit set to 0x0) or equals to 1.5 if CCM or DCM mode is used (CCM bit set to 0x1).

7.5.2 C_{HV} Selection

Load capacitance (C_L) defines the required value of component C_{HV} (up to 10 nF):

$$C_{HV} = 5\% \, C_L \quad (5)$$

The C_{HV} capacitor should have a voltage rating of at least the peak output waveform amplitude. A C_{HV} capacitor with a minimum voltage rating of 95 V is required to output the full-scale output voltage.

7.5.3 R_{sense} Selection

The value of R_{sense} must enable a current range appropriate for the I_{SW} value calculated in equation (4). R_{sense} value is determined using equation (6). The current limit of the power converter is set by R_{sense} components.

$$R_{sense} \leq \frac{0.256 \text{ [V]}}{I_{SW}} \quad (6)$$

$$\text{Current limit} = \frac{0.256 \text{ [V]}}{R_{sense}} \quad (7)$$

7.5.4 L_1 Selection

The BOS1921/BOS1931 can use any COTS inductor. An L_1 inductor greater than 10 µF is recommended but the inductance can be chosen to optimize the power / size / performance trade-off according to the user application as follows:

- Select lower inductance together with a higher switching frequency using FSWMAX[1:0] bits to optimize distortion (i.e., THD+N).
- Select larger inductance to reduce the switching frequency. In general, lower switching frequency corresponds to lower power consumption.

A f_{swmin} value of 300 kHz is recommended.

Use the following procedure to select the first inductor value and then experiment with other values to optimize your application if required:

1. Calculate the ideal duty ratio of the power converter stage:

$$D = 1 - \frac{V_{BUS}}{V_{BUS} + V_{pk}} \quad (8)$$

2. Calculate the maximum L_1 inductor value:

$$L_1 \leq \frac{V_{BUS} D}{I_{pk} f_{swmin}} \quad (9)$$

Select an L_1 inductor with a saturation current higher than I_{SW} and higher than the current limit determined in equation (7).

7.5.5 Input Capacitor (C_{VDD})

An input capacitor (C_{VDD}) must be placed next to the inductor because of the current requirement of the power converter. A low-ESR capacitor of at least 10 µF is recommended.

If the Unidirectional Power Input mode is enabled (UPI bit set to 0x1), the energy recovered from the load in buck conversion accumulates on the C_{VDD}. Energy accumulation on C_{VDD} causes the input voltage to increase. The voltage increase must not make the total voltage on C_{VDD} exceed the maximum absolute 5.5 V limit (V_{DD_max}). Use equation (10) to determine the minimum capacitance value.

$$C_{VDD} = \frac{C_L V_{pk}^2}{V_{DD\_max}^2 - V_{BUS\_max}^2} \quad (10)$$

When selecting the capacitor, make sure to select a capacitor with an effective capacitance close to the capacitance value determined by equation (10).

7.6 Design Methodology: programming

Many operational settings are adjustable through the digital front end. One should program the following parameters according to its specific design. For details, see section 7.5.

7.6.1 Waveform Playback

The readout rate for waveform playback is set using the following parameter:

- Set FIFO readout speed using PLAY_SRATE[2:0] bits.

7.6.2 Power Converter

The internal buck-boost converter can be optimized using the following parameters:

- Set the maximum switching frequency of the power converter using FSWMAX[1:0] bits.
- Set the Power Input mode using UPI bits.

7.6.3 Loop Controller

The BOS1921/BOS1931 implements a proportional-integral (PI) control loop feedback that can be optimized if required with the following parameters:

- Proportional gain is set using KP[10:0]
- Proportional gain term related to waveform amplitude is used with KPA[7:0]
- Integral term is set with KIBASE[3:0]

Table 50 shows the recommended value for a 100 nF load operating at up to 190 V_{pk-pk} at 300 Hz with L_1 = 10 µH and R_{sense} = 0.2 Ω sense resistor.

Table 50: Loop controller parameters

PARAMETER	RECOMMENDED VALUE	COMMENT
KP[10:0]	128 (0x080), default	Reduce value for smaller loads
KPA[7:0]	160 (0xA0), default	Reduce value for smaller loads
KIBASE[3:0]	2 (0x2), default	Increase value up to 4 when using a larger inductor

7.6.4 Power Efficiency

The power efficiency of the BOS1921/BOS1931 and the haptic waveform integrity can be optimized by configuring the internal controller and the switching timing of the internal low-side and high-side switches. This optimization can be done by adjusting the following registers based on selected inductor value (L_1) and current sense limit (set by R_{sense}):

- Optimize Loop Controller (see section 7.6.3).
- Adjust power switch deadtime using DHS[6:0] and DLS[6:0] bits.
- Adjust minimum current required to turn-on HS using IONSCALE[7:0] bits.
- Adjust typical capacitance value on pin SW using PARCAP[7:0] bits.
- Adjust proportional gain for the offset using TI_RISE[5:0] bits.
  Set the nominal supply voltage (VDD) of the design using VDD[4:0] bits.

7.7 Noise Reduction

It may be required to enable continuous conduction mode (CCM) by setting the CCM bit to 0x1 to drive a high capacitance load at high frequencies. In such a situation, the noise level on the supply nodes (i.e., V_{DDIO}, V_{BUS} and V_{DD}) may be higher than what is acceptable for some applications. Electrical noise can be reduced by using one or multiple of the following strategies:

1. Follow the PCB layout recommendations listed in the section 8.
2. Place a Schottky diode as close as possible to the BOS1921/BOS1931 device with a low threshold voltage and fast recovery time in the following locations:
    a. Between the HV and SW pins, as shown in Figure 39.
    b. Between the SW and PGND pins, as shown in Figure 39.

    In the case where only one diode can be used due to cost or space, the Schottky diode between the HV and SW pins will generally have a more significant impact on noise reduction and should be prioritized rather than the diode placed between SW and PGND.

3. Decrease the maximum switching frequency of the BOS1921/BOS1931 by increasing FSWMAX[2:0] to up to 0x3 to increase the input power threshold for entering CCM mode.

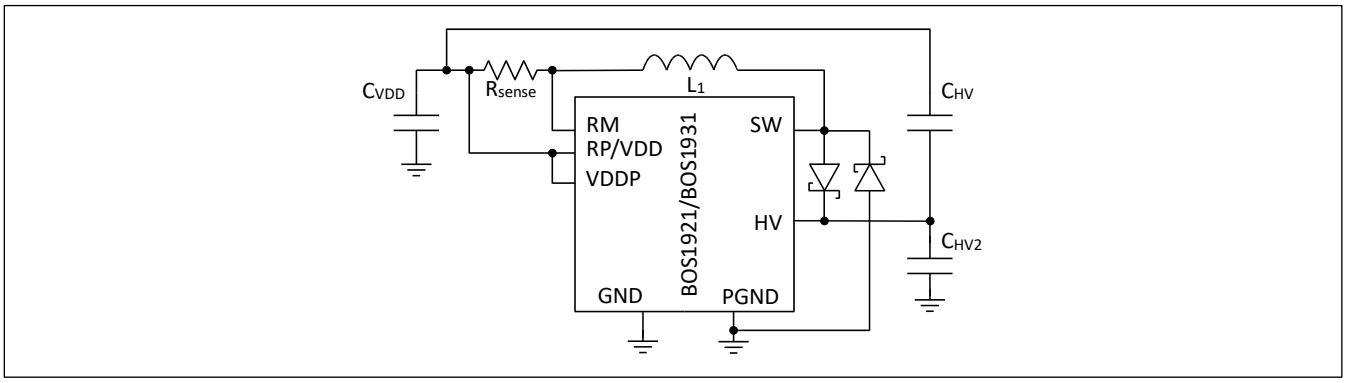


Figure 39: Simplified schematic with a Schottky diode between SW/HV and SW/PGND pins for noise reduction

8 PCB Layout Example

UPI configuration 4-layer PCB layout examples are presented in Figure 40. The recommended layers are as following:

- Top layer: Components and main routing.
- Layer 2: Full ground plane, avoid interruptions/slot as much as possible.
- Layer 3: Power plane split between V_{BUS}, V_{DD} and V_{DDIO}.
- Bottom layer: Routing.

Layout considerations:

1. Keep SW node as small as possible.
2. Place and route components L_1, R_S, C_{VDD}, C_{HV} and C_{HV2} close to each other to minimize area of the high di/dt current loop and reduce high voltage ringing & spikes.
3. Create a GND island on Top layer connecting GND pads of C_{VDD} and C_{HV2} with the following criteria:
    - Connect this copper region to PGND pads of BOS1921/BOS1931.
    - Connect with vias to Layer 2 ground plane.
    - This GND island must not be tied to the Top layer ground polygon/plane (if applicable).
4. Route RP/VDD & RM sensing lines parallel to each other.
5. Create a HV copper region on Top layer connecting VDD pads of C_{HV} and C_{HV2}.
    - Connect this copper region directly to HV pad(s) of BOS1921/BOS1931.
    - Keep this region as close as possible to BOS1921/BOS1931.
    - Keep this region as small as possible.
6. This consideration applies to QFN version only - Create a V_{DD} copper region on Top layer connecting VDD pad of C_{HV}:
    - Connect this copper region directly to VDDP pads (2 and 24 pins) of BOS1921/BOS1931.
    - Connect with vias to Layer 3 V_{DD} plane.

Notes on important components:

- The layout examples are sized for a piezo actuator with a capacitance of 100 nF driven at 190 V_{pk-pk} and 300 Hz.
- Beware of capacitors DC bias, i.e., the decrease in capacitance with increasing DC voltage, which affects the effective value of a capacitor at a given operating voltage. Generally, high capacitance & high-voltage ceramic capacitors are subject to this phenomenon, but C0G/NP0 dielectric and tantalum capacitors do not exhibit any DC bias behavior. Refer to C_{HV2} and C_{VDD} components in Table 51.
- Component requirements must be reevaluated for each application.

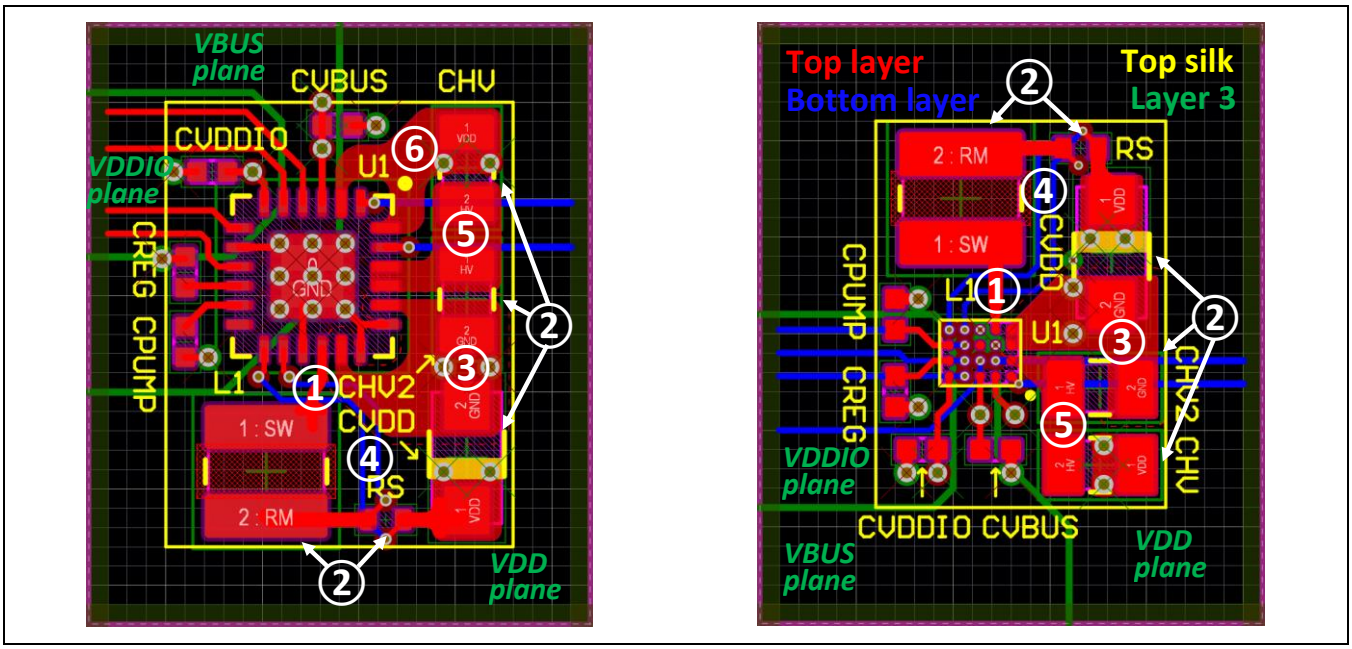


Figure 40: UPI configuration PCB layout examples for QFN 24L 4.0mm × 4.0mm (left) and typical configuration for WLCSP 20B 2.1mm × 1.7mm (right)

Table 51: Bill of Materials for layout examples

DESIGNATOR	QTY	VALUE	DESCRIPTION	MANUFACTURER	PART NUMBER
CHV	1	0.01µF	10000PF 250V X7R 0805	TDK Corporation	CGA4J3X7R2E103K125AA
CHV2	1	3900pF	3900PF 250V C0G/NP0 0805	TDK Corporation	C2012C0G2E392J125AE
CPUMP, CREG, CVBUS, CVDDIO	4	0.1µF	0.1UF 25V X5R 0402	Taiyo Yuden	TMK105BJ104KV-F
CVDD	1	100µF	TANT POLY 100UF 6.3V 1206	KEMET	T527I107M006ATE070
L1	1	10µH	IND 10UH 1.48A 415 MOHM 3×3 mm package	TDK Corporation	VLS3012HBX-100M
RS	1	0.2	0.2 OHM 1% 1/8W 0402	TE Connectivity Passive Product	RLP73N1ER20FTDF

9 Mechanical

9.1 QFN Package Description

9.1.1 Physical Outline Dimension (POD)

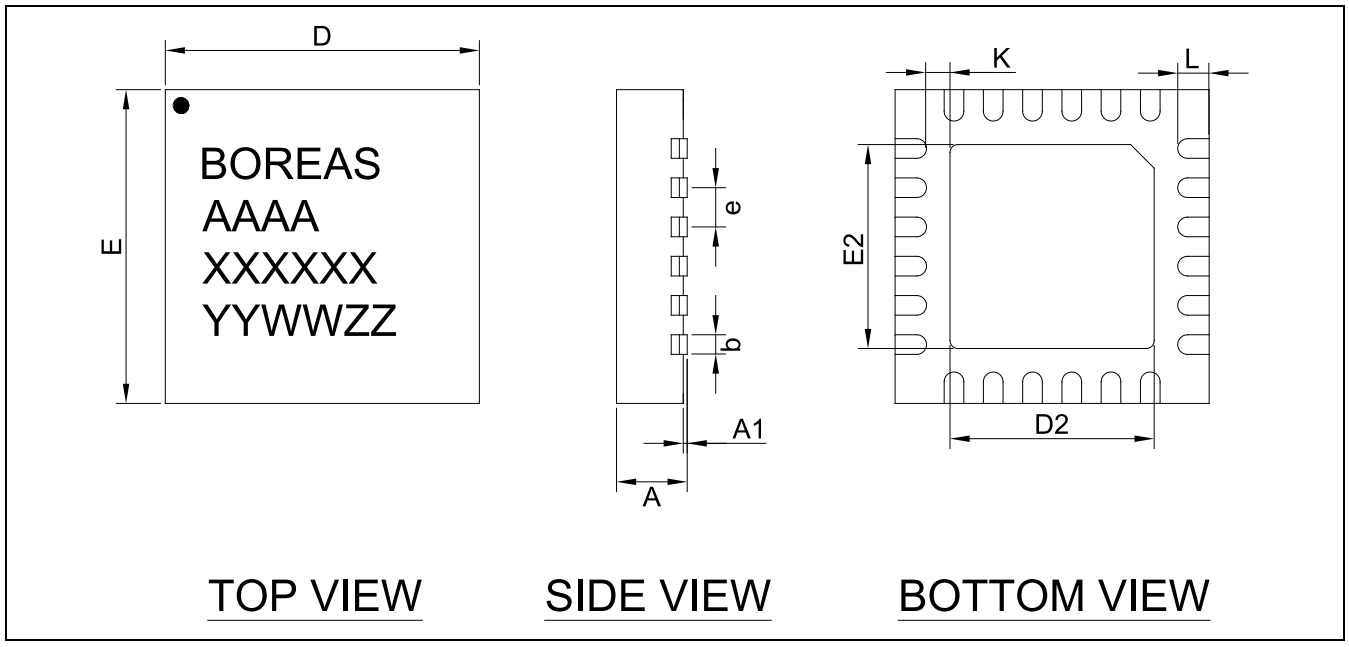


Figure 41: QFN 24L 4.0mm × 4.0mm package outline drawing

Table 52: QFN 24L 4.0mm × 4.0mm package dimensions

SYMBOL	MILLIMETERS		
	MIN	NOM	MAX
A	0.500	0.550	0.600
A1	0.000	-	0.050
b	0.200	0.250	0.300
D	3.950	4.000	4.050
D2	2.350	2.400	2.450
E	3.950	4.000	4.050
E2	2.350	2.400	2.450
e	0.500 BSC		
K	0.325	0.400	0.475
L	0.350	0.400	0.450

‡Reference: JEDEC MO-220-WGGD. BSC: Basic Spacing between Center.

Four lines are branded on the package:

(1) Company Name: BOREAS
(2) Device Marking: AAAA (1921 or 1931)
(3) Wafer Batch Number: XXXXXX
(4) Assembly Date Code: YY (year), WW (week) and ZZ (assembly house code)

9.1.2 QFN Package Soldering Footprint

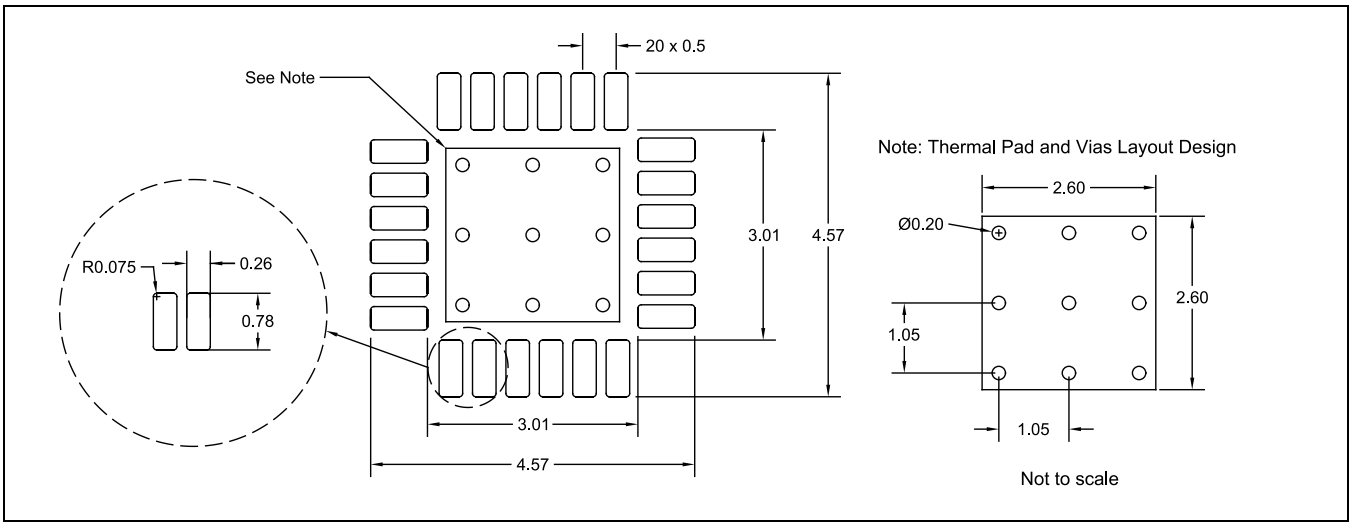


Figure 42: QFN 24L 4.0mm × 4.0mm soldering footprint (NOT TO SCALE)

9.1.3 QFN Reflow

The QFN package soldering reflow profile should be determined based on the recommended reflow profile made by the manufacturer of the solder paste used. Also, it is important to take into consideration that the circuit board dimensions, other board components and the reflow soldering oven may affect the reflow profile.

Finally, please note that the quality of the solder paste plays an important role in board assembly and allows for a reliable and repeatable assembly process.

9.2 WLCSP Package Description

9.2.1 Physical Outline Dimension (POD)

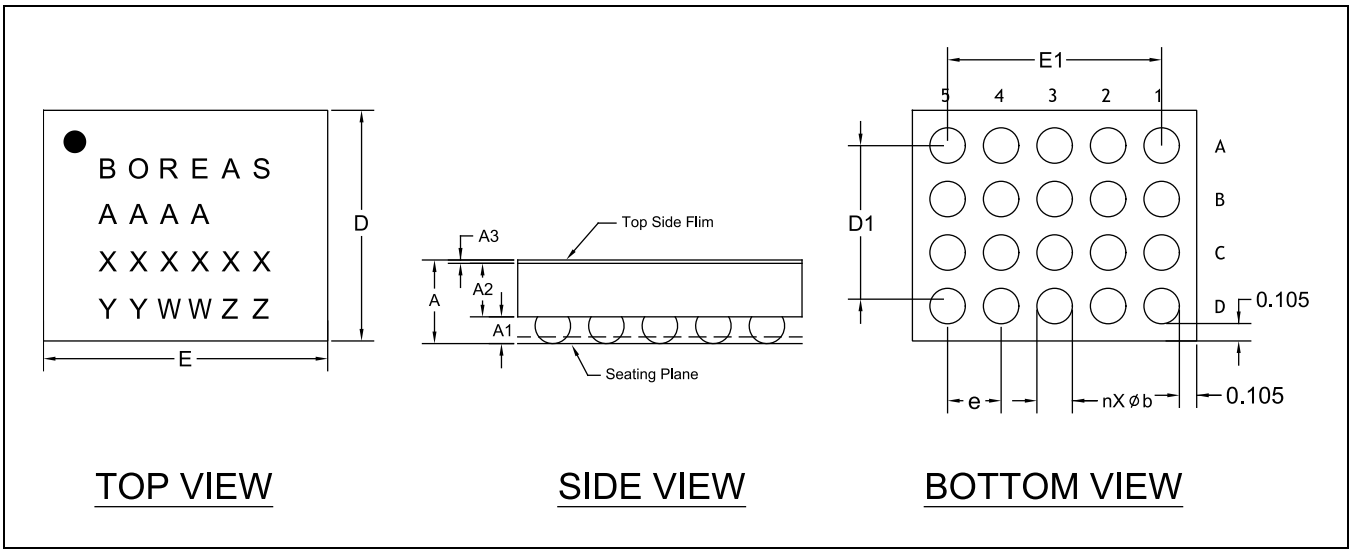


Figure 43: WLCSP 20B 2.1mm × 1.7mm package outline drawing with top, side, and bottom view

Table 53: WLCSP 20B 2.1mm × 1.7mm package dimensions

SYMBOL	MILLIMETERS		
	MIN	NOM	MAX
A	0.585	0.625	0.665
A1	0.180	0.200	0.220
A2	0.380	0.400	0.420
A3	0.022	0.025	0.028
E	2.055	2.075	2.095
D	1.655	1.675	1.695
E1	1.60 BSC		
D1	1.20 BSC		
e	0.40 BSC		
b	0.245	0.265	0.285

BSC: Basic Spacing between Center.

Four lines are branded on the package:

(1) Company Name: BOREAS
(2) Device Marking: AAAA (1921 or 1931)
(3) Wafer Batch Number: XXXXXX
(4) Assembly Date Code: YY (year), WW (week) and ZZ (assembly house code)

9.2.2 WLCSP Package Soldering Footprint

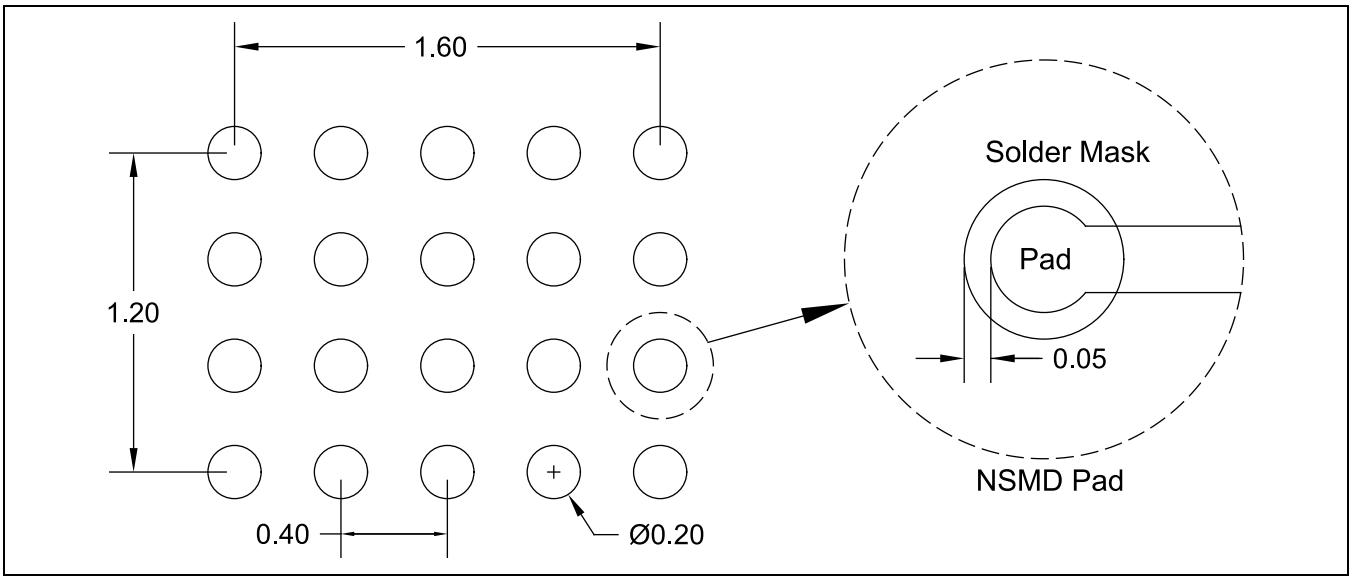


Figure 44: WLCSP 20B 2.1mm × 1.7mm soldering footprint (NOT TO SCALE)

The use of non-solder mask defined (NSMD) pads is recommended, with 0.05 mm solder mask expansion as shown in Figure 44.

9.2.3 WLCSP Reflow

BOS1921CW have SAC405 bumps which supports JEDEC J-STD-020D.1 reflow profile. Figure 45 presents the recommended reflow profile which may be optimized for specific PCB assembly conditions. Note that it is recommended to use solder paste to obtain reliable solders.

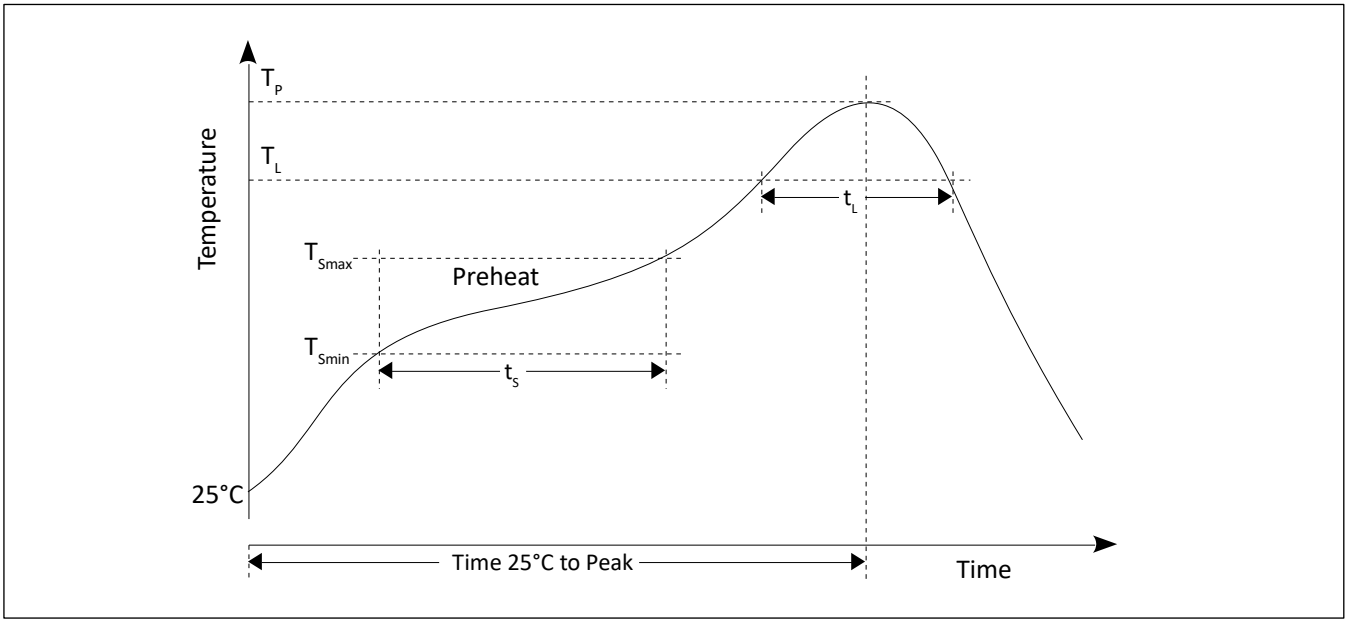


Figure 45: WLCSP reflow profile

Table 54: Reflow profile parameters

PARAMETER	DESCRIPTION	VALUE
T_{Smin}	Preheat minimum temperature	150°C
T_{Smax}	Preheat maximum temperature	200°C
t_S	Time from T_{Smin} to T_{Smax}	60-120 s
	Ramp-up rate from T_L to T_P	3°C/s max
T_L	Liquidous temperature	217°C
T_P	Peak package temperature	260°C
t_L	Time above T_L	60-150 s
	Ramp-down rate from T_P to T_L	6°C/s max
	Time 25 °C to peak temperature	8 min max

9.3 Tape and Reel Specifications

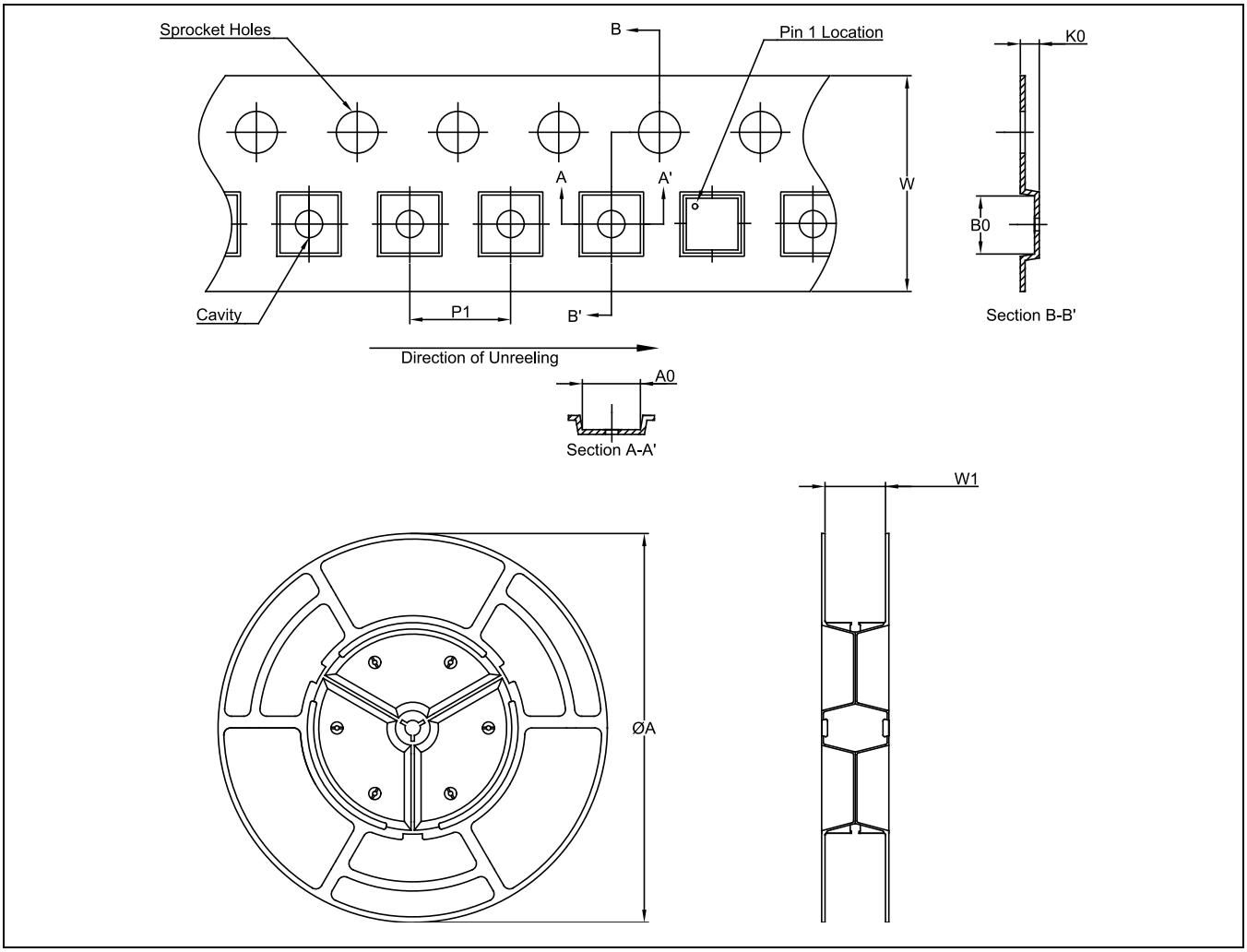


Figure 46: Embossed carrier tape and reel outline drawing

Table 55: Tape and reel dimensions

PART NUMBER	PACKAGE TYPE	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W	⌀A (mm)	W1 (mm)
BOS1921CQ	QFN 24L 4.0mm × 4.0mm	4.250	4.250	0.750	8.00	12.00	330	12.4
BOS1931CQ	QFN 24L 4.0mm × 4.0mm	4.250	4.250	0.750	8.00	12.00	330	12.4
BOS1921CW	WLCSP 20B 2.1mm × 1.7mm	2.275	1.875	0.825	4.00	8.00	178	9
BOS1931CW	WLCSP 20B 2.1mm × 1.7mm	2.275	1.875	0.825	4.00	8.00	178	9

10 Known Issues

10.1 Incorrect Activation of Output Bridge Protection

Affected product revision: B

The output bridge protection (section 6.2.18) is activated under the following conditions:

- Play a positive haptic waveform when a negative voltage smaller than -2.5 V has built up on the piezoelectric ceramic.
- Play a negative haptic waveform when a positive voltage greater than 2.5 V has built up on the piezoelectric ceramic.

In these conditions, the device may output the waveform with the wrong polarity and generate an IDAC fault.

To avoid this issue, one must reset the voltage on the piezoelectric ceramic before starting to play the haptic waveform. This can be achieved by playing one of the following sets of data before the desired haptic waveform:

- Several 0 V data points.
- Voltage data points increasing from -2 V to 0 V if a positive waveform is intended to be played.
- Voltage data points decreasing from 2 V to 0 V if a negative waveform is intended to be played.

10.2 Timeout resets PLAY_SRATE

Affected product revision: All

When using the timeout feature with the TOUT bit set to 0x1, the PLAY_SRATE[2:0] bits are reset to 0x7 when the device enters SLEEP after a timeout event.

10.3 Waveform Amplitude Drift with RELOFF Option

Affected product revision: All

When using RAM Synthesis mode with the RELOFF option enabled, an offset may cumulate when 2 SLICEs of different amplitudes are repeatedly played. This cumulative offset can cause waveform amplitude to drift, potentially leading the device to enter an ERROR state.

To prevent this waveform amplitude drift, avoid repeating SLICE with different amplitudes while using the RELOFF option, ensure that each SLICE has identical amplitude or reduce the number of times the SLICEs are repeated.

10.4 Minimum Slew-Rate of V_{BUS} Supply

Affected product revision: A, B & C

The V_{BUS} voltage must ramp-up at a minimum rate of 3 V/ms to ensure proper device initialisation.

11 Ordering Information

Table 56: Ordering information

ORDERING PART NUMBER	FEATURES	PACKAGE DESCRIPTION	PACKING FORMAT	QUANTITY	MSL LEVEL, PEAK TEMP.	FLOOR LIFE	OPERATING TEMPERATURE	DEVICE MARKING
BOS1921CQR	DRIVE+SENSE	QFN 24L 4.0mm × 4.0mm	Tape & Reel	2500 / Reel	Level 3, 260°C	168Hrs	-40°C to 85°C	1921
BOS1931CQR	DRIVE	QFN 24L 4.0mm × 4.0mm	Tape & Reel	2500 / Reel	Level 3, 260°C	168Hrs	-40°C to 85°C	1931
BOS1921CWR	DRIVE+SENSE	WLCSP 20B 2.1mm × 1.7mm	Tape & Reel	4000 / Reel	Level 1, 260°C	Unlimited	-40°C to 85°C	1921
BOS1931CWR	DRIVE	WLCSP 20B 2.1mm × 1.7mm	Tape & Reel	4000 / Reel	Level 1, 260°C	Unlimited	-40°C to 85°C	1931

NOTE

(1) Ordering Part Number where last letter indicates packing format.
(2) All parts are RoHS compliant and halogen free.
(3) Contact sales@boreas.ca to order.
(4) MSL: Moisture Sensitivity Levels, IPC/JEDEC J-STD-020.

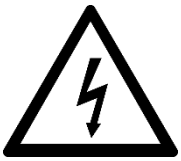
12 Document History

Table 57: Document changes between previous and current versions

ISSUE	DATE	DOCUMENT NUMBER	CHANGES
6	Oct., 2024	BT015DDS01.01	Added BOS1931 device Added $I_{BUS,AVG}$ in sensing (section 5.4) Typo corrected (section 6.2.11) Changed minimum V_{BUS} ramp-up rate (section 7.4.1) Changed known issue name (section 10.1) Added known issue Waveform Amplitude Drift with RELOFF Option (section 10.3) Added known issue Minimum Slew Rate of VBUS Supply (section 10.4) Updated ordering information (section 11) Added C_{HV2} to Figure 35 Corrected wheel width for BOS1921CW (Table 55)
5	April, 2024	BT015CDS01.01	Added a note about Device Reset feature (section 6.2.8) Clarified the Adjustable Internal Clock (section 6.2.14) Updated Current Detection Status Fault description (section 6.2.15.5) Clarified interrupt mechanism (section 6.2.17) Added Output Bridge protection description (section 6.2.18) Updated digital interface terminology (section 6.3) Corrected FIFO descriptions (section 6.6) Clarified SLICE.AMPITUDE[11:0] definition (section 6.8.1) Clarified FSWMAX[1:0] field description (section 6.10.2) Added CHIP_REV[3:0] register field (section 6.10.17) Changed power-up sequence for VDDIO (section 7.4.1) Added guidelines for noise reduction (section 7.7) Modified layout recommendations (section 8) Changed known issue name IDAC fault bit (section 10.1) Added issue Timeout resets PLAY_SRATE (section 10.2) Corrected RAM Playback example (Figure 21) Corrected Figure 23 Corrected examples in Table 20

13 Notice and Warning

Warning High Voltage



For safety, this integrated circuit must be used by qualified and skilled personnel familiar with all applicable safety standards.

ESD Caution

This integrated circuit is ESD (Electrostatic Discharge) sensitive. Therefore, proper ESD precautions and procedures are recommended for handling and installation to avoid damage.

Boréas Technologies Datasheet Status:

Advance Information Datasheet:	Design Data
Preliminary Information Datasheet:	Prototype information
Final Datasheet:	Production information

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BOS1921CQR BOS1921CWR BOS1931CWR