ACS70312

Very High Precision, Programmable Linear Hall-Effect Sensor IC
with Reverse Battery Protection and High-Bandwidth (240 kHz) Analog Output for Core-Based Current Sensing

FEATURES AND BENEFITS

- Factory-programmed segmented linear temperature compensation (TC) provides ultralow thermal drift
  - □ Sensitivity error ±1%
  - □ Offset error ±5 mV
- On-board supply regulator with reverse-battery protection provides high immunity to electrical overstress (EOS)
- Very fast response time (2 µs)
- High operating bandwidth: DC to 240 kHz
- AEC-Q100 Grade 0, automotive qualified
- Customer-programmable, high-resolution offset, and sensitivity trim
- Extremely low noise and high resolution achieved via proprietary Hall element and low-noise amplifier circuits

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DESCRIPTION

The Allegro ACS70312 IC incorporates a Hall element with BiCMOS integrated circuitry to provide a fully monolithic linear current sensor IC. The IC is sensitive to magnetic flux density orthogonal to the IC package surface and the output is an analog voltage proportional to the applied flux density. The ACS70312 is designed to be used in conjunction with a ferromagnetic core to provide highly accurate current sensing. The gain and offset drift over temperature is factory-programmed at Allegro and delivers a solution with ±1% sensitivity error and ±5 mV offset error from 25°C to 150°C.

The ACS70312 is customer programmable. The absolute value of gain and offset can be programmed after manufacturing to

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PACKAGE: 4-pin SIP (suffix KT)

TN Leadform

KT Package

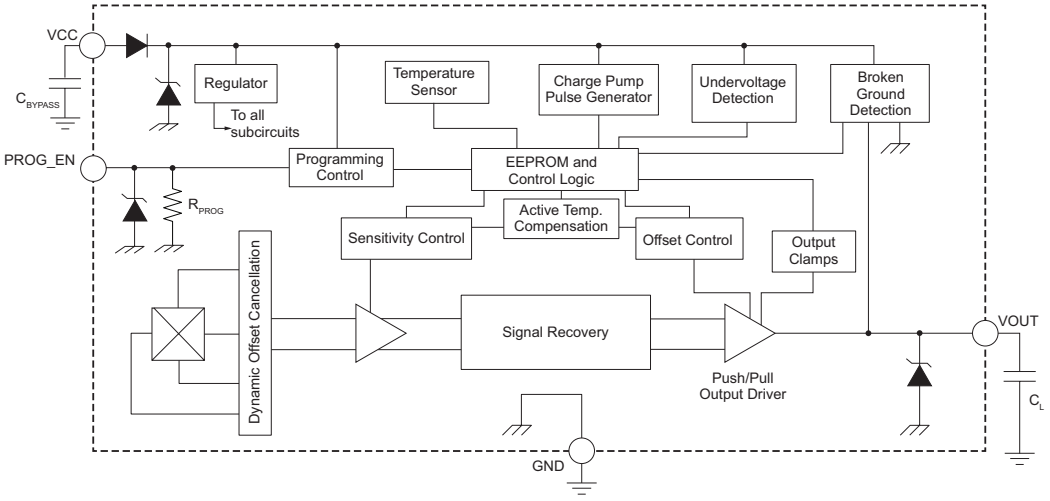

Figure 1: Functional Block Diagram

FEATURES AND BENEFITS (continued)

- Patented circuits suppress IC output spiking during fast current step inputs
- Wide selectable sensitivity range between 0.5 and 8 mV/G
- User-selectable ratiometric behavior of sensitivity, quiescent voltage, and clamps (ratiometry can be disabled), for simple interface with application analog-to-digital converter (ADC)
- Open-circuit detection on the GND pin (broken wire)
- Customer-programmable output voltage clamps provide short-circuit diagnostic capabilities
- Undervoltage detection (UVD)
- Low-voltage programming
- Wide ambient temperature range: –40°C to 150°C
- Immune to mechanical stress
- Extremely thin package: 1 mm case thickness

DESCRIPTION (continued)

provide customers with industry-leading current sensing accuracy. The sensor has a high operating bandwidth from DC to 240 kHz and a fast 2 µs response time. The ACS70312 is ideal for use in high-frequency automotive inverters and DC/DC converters where fast switching is required.

The ACS70312 offers undervoltage detection (UVD) as well as low-voltage programming that eliminates the need for voltages greater than V_{CC} during user programming.

Broken-ground-wire detection, clamps, power-on-reset, and under/overvoltage detection provide the required diagnostics for automotive applications.

The on-board supply regulator enables the VCC pin to survive voltages of ±18 V and the VOUT pin to survive voltages of +16 to –6 V for added robustness in the harsh automotive environment.

Device parameters are specified across an extended ambient automotive temperature range: –40°C to 150°C. The ACS70312 sensor IC is provided in an extremely thin case (1 mm thick), 4-pin SIP (single in-line package, suffix KT). Packages are lead (Pb) free, with 100% matte tin leadframe plating.

Table of Contents

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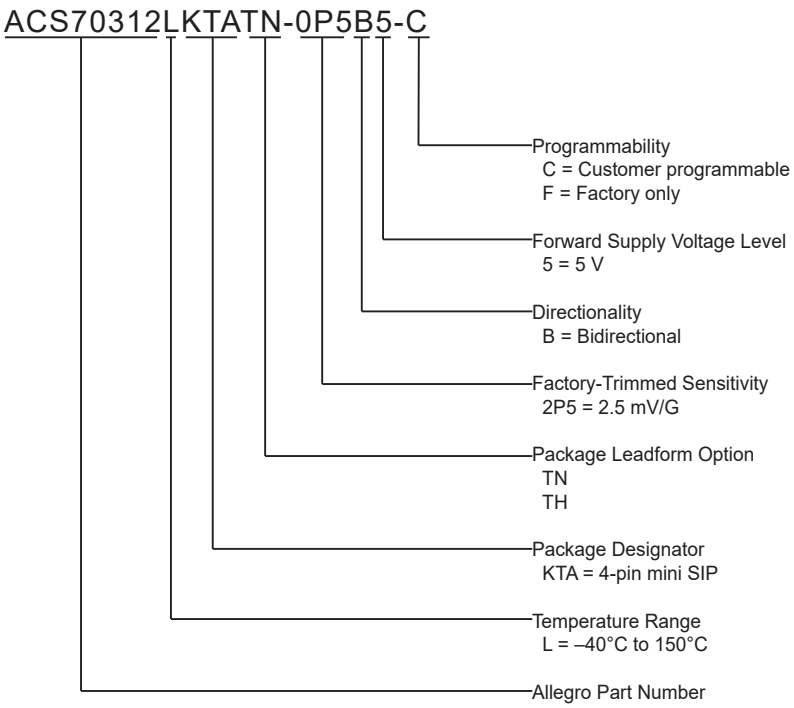
SELECTION GUIDE

Part Number [1]	Factory-Programmed Sensitivity (mV/G)	Programmable Sens Range (mV/G)	Package	T_A (°C)	Packing
ACS70312LKTATN-0P5B5-C	0.57	0.5 to 0.8	4-pin SIP (suffix KT) TN leadform	–40 to 150	4000 pieces per 13-inch reel
ACS70312LKTATN-001B5-C	1	0.8 to 1.8			

[1] Characteristics are guaranteed within the sense programmable range of the corresponding part number.



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ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		18	V
Reverse Supply Voltage	V_{RCC}	$T_{J(max)}$ should not be exceeded	–18	V
Forward Output Voltage	V_{OUT}	$V_{OUT} < V_{CC} + 2$ V	16	V
Reverse Output Voltage	V_{ROUT}	Difference between V_{CC} and output should not exceed 20 V	–6	V
Output Current	I_{OUT}	Maximum survivable sink or source current on the output	±10	mA
Forward Program Enable Voltage	V_{PROG}	$V_{PROG} < V_{CC} + 2$ V	6	V
Reverse Program Enable Voltage	V_{RPROG}		–0.5	V
Operating Ambient Temperature	T_A	L temperature range	–40 to 150	°C
Storage Temperature	T_{stg}		–65 to 165	°C
Maximum Junction Temperature	$T_{J(max)}$		165	°C

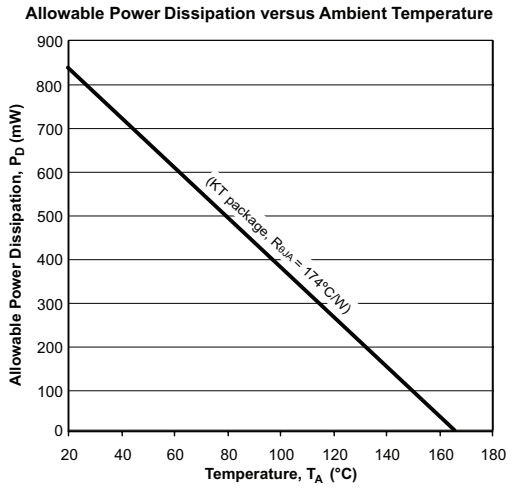
ESD RATINGS

Characteristic	Symbol	Test Conditions	Value	Unit
Human Body Model	V_{HBM}	Per JEDEC JS-001, ACS70312 devices	±8	kV
Charged Device Model	V_{CDM}	Per JEDEC JS-002	±1	kV

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions [1]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On one-layer PCB with exposed copper limited to solder pads	174	°C/W

[1] Additional thermal information available on the Allegro website



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PINOUT DIAGRAM AND TERMINAL LIST TABLES

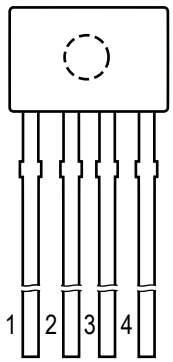

Figure 2: KT Package Pinout Diagram

(Ejector pin mark on opposite side)

ACS70312 Terminal List Table

Number	Name	Function
1	VCC	Input power supply; also used for programming
2	VOUT	Output signal; also used for programming
3	PROG_EN	Low-voltage programming enable pin; connect to GND for optimal ESD performance
4	GND	Ground

TYPICAL APPLICATION DRAWING

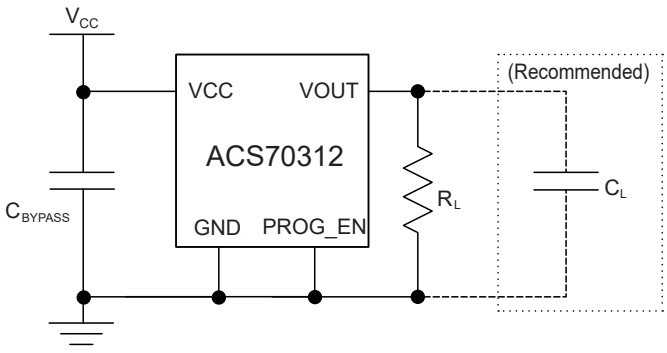

Figure 3: ACS70312 Typical Application Drawing

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OPERATING CHARACTERISTICS: Valid over full operating temperature range of T_A, C_{BYPASS} = 0.1 µF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}		4.5	5	5.5	V
Supply Current	I_{CC}	No load on VOUT; V_{CC} at 4.5, 5, and 5.5 V	–	13	15	mA
Power-On Reset Voltage	V_{POR_H}	T_A = 25°C, V_{CC} rising	3.4	3.65	3.8	V
	V_{POR_L}	T_A = 25°C, V_{CC} falling	3	3.3	3.4	V
Power-On Reset Hysteresis	V_{POR_HYS}	T_A = 25°C	200	350	600	mV
Power-On Reset Release Time	t_{POR_R}	T_A = 25°C, V_{CC} rising	–	32	–	µs
Power-On Delay Time	t_{PO}	T_A = 25°C, C_{BYPASS} = open, C_L = 1 nF	–	72	–	µs
Overvoltage Detection [1]	V_{OVD_H}	T_A = 25°C	7.3	7.6	7.9	V
	V_{OVD_L}	T_A = 25°C	6.3	6.6	6.9	V
Undervoltage Detection [1]	V_{UVD_H}	T_A = 25°C	4	4.2	4.4	V
	V_{UVD_L}	T_A = 25°C	3.6	3.8	4	V
UVD Hysteresis [1]	V_{UVD_HYS}	T_A = 25°C	300	400	500	mV
UVD Enable/Disable Delay Time [1]	t_{UVD_EN}	T_A = 25°C	60	72	84	µs
	t_{UVD_DIS}	T_A = 25°C	10	16	30	µs
Temperature Compensation Power-On Time	t_{TC}	T_A = 150°C, C_{BYPASS} = open, C_L = 1 nF, Sens = 0.57 mV/G	140	170	200	µs
Supply Zener Clamp Voltage	V_z	T_A = 25°C, I_{CC} = 30 mA	18	20	25	V
OUTPUT CHARACTERISTICS						
DC Output Resistance	R_{OUT}	T_A = 25°C	2	4	8	Ω
Output Load Resistance [2]	R_L	VOUT to GND or VCC	4.7	10	–	kΩ
Output Load Capacitance	C_L	VOUT to GND	–	–	5	nF
Output Voltage Saturation	V_{SAT_H}	T_A = 25°C, R_L = 10 kΩ to GND, bias = 400 G	4.75	4.8	V_{CC}	V
	V_{SAT_L}	T_A = 25°C, R_L = 10 kΩ to VCC, bias = 400 G	0.05	0.2	0.25	V
Output Voltage Clamp	V_{CLP_H}	T_A = 25°C, R_L = 10 kΩ to GND, bias = 400 G	4.65	4.7	4.75	V
	V_{CLP_L}	T_A = 25°C, R_L = 10 kΩ to VCC, bias = 400 G	0.25	0.3	0.36	V
Output Voltage with Broken GND	V_{BRK_L}	T_A = 25°C, R_L = 10 kΩ to GND, pin 3 = open	0	100	200	mV
	V_{BRK_H}	T_A = 25°C, R_L = 10 kΩ to VCC, pin 3 = open	4.8	4.9	5	V
Noise	V_{IN}	T_A = 25°C, C_L = 1 nF, Sens = 5 mV/G	–	1.5	–	mG/√(Hz)
	V_{ON}	T_A = 25°C, Sens = 5 mV/G	–	3.5	–	mV_{RMS}
Propagation Delay Time	t_{pd}	T_A = 25°C, C_L = 1 nF, R_L= 10 kΩ	–	1.2	1.65	µs
Response Time	$t_{RESPONSE}$	T_A = 25°C, C_L = 1 nF, R_L= 10 kΩ	–	2.1	3	µs
Rise Time	t_r	T_A = 25°C, C_L = 1 nF, R_L= 10 kΩ	–	1.9	–	µs
Output Slew Rate	SR	T_A = 25°C, C_L = 1 nF, R_L= 10 kΩ	410	480	550	V/ms
Bandwidth	BW	Small signal –3 dB, C_L = 1 nF, T_A = 25°C; Sens = 5 mV/G	–	240	–	kHz
Chopping Frequency	f_c	T_A = 25°C	–	1.14	–	MHz

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OPERATING CHARACTERISTICS (continued): Valid over full operating temperature range of T_A, C_{BYPASS} = 0.1 µF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
QUIESCENT OUTPUT VOLTAGE ($V_{OUT(Q)}$)							
Number of Fine QVO Programming Bits	QVO_FINE			–	9	–	bit
Quiescent Voltage Output [3]	$V_{OUT(Q)}$	T_A = 25°C		2.495	2.5	2.505	V
Average Quiescent Voltage Output Programming Step Size [4]	$V_{OUT(Q)Step}$	T_A = 25°C		–	1.18	–	mV
Average Quiescent Voltage Output Temperature Compensation Step Size	$V_{OUT(Q)TCStep}$			–	$V_{OUT(Q)Step}$	–	mV
SENSITIVITY (Sens)							
Coarse Sensitivity Programming Bits [5]	SENS_COARSE			–	2	–	bit
Fine Sensitivity Programming Bits	SENS_FINE			–	9	–	bit
Sensitivity Programming Range [6]	$Sens_{PR}$	SENS_COARSE = 0		0.5	0.57	0.8	mV/G
		SENS_COARSE = 1		0.8	1.0	1.8	mV/G
		SENS_COARSE = 2		1.8	2.5	4.1	mV/G
		SENS_COARSE = 3		4.1	5	8.6	mV/G
Average Sensitivity Programming Step Size	$Step_{SENS}$	SENS_COARSE = 0		–	2.1	–	µV/G
		SENS_COARSE = 1		–	4.5	–	µV/G
		SENS_COARSE = 2		–	9.8	–	µV/G
		SENS_COARSE = 3		–	20.3	–	µV/G
Average Sensitivity Temperature Compensation Step Size	$Step_{SENSTC}$	T_A = –40°C to 150°C		–	$Step_{SENS}$	–	µV/G
SENSITIVITY ERROR							
Sensitivity Error	$Sens_{ERR}$	T_A = 25°C		–	0.7	–	%
Sensitivity Drift Over Temperature	$\Delta Sens_{TC}$	T_A = 25°C to 150°C		–1	–	1	%
		T_A = –40°C to 25°C		–1.2	–	1.2	%
Sensitivity Linearity Error [7]	Lin_{ERR}	Characterized with 1000G, 2000G, 3000G, 4000G, 4500G	±3 kG	–	0.3	–	%
			±4 kG	–	0.5	–	%
			±4.5 kG	–	1	–	%
Sensitivity Ratiometry Error	$Rat_{ERRSENS}$	V_{CC} = 4.85 to 5.15 V		–0.55	–	0.55	%
QUIESCENT VOLTAGE OUTPUT ERROR							
Quiescent Voltage Output Error	$V_{OUT(Q)ERR}$	T_A = 25°C		–5	–	5	mV
Quiescent Voltage Output Drift Over Temperature	$\Delta V_{OUT(Q)TC}$	T_A = 25°C to 150°C		–5	–	5	mV
		T_A = –40°C to 25°C		–5	–	5	mV
Quiescent Voltage Output Ratiometry Error	$V_{RatERRVOUT(Q)}$	V_{CC} = 4.85 to 5.15 V		–5	–	5	mV

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OPERATING CHARACTERISTICS (continued): Valid over full operating temperature range of T_A, C_{BYPASS} = 0.1 µF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
LIFETIME [8]						
Quiescent Voltage Output Lifetime Drift	$V_{OUT(Q)\_LIFE}$	T_A = 25°C	–	0.4	–	mV
Sensitivity Lifetime Drift	$Sens_{ERR\_LIFE}$	T_A = 25°C	–	0.5	–	%
MAGNETIC CHARACTERISTICS						
Maximum Field Range	B	Input field range to which the part responds	–4500	–	4500	G

[1] OVD/UVD was characterized on the bench. V_{CC} ramp rate of 0.5 V/ms and 1 V/µs for thresholds and timing respectively.
[2] Using a small R_L increases output error; this error scales with output, causing offset and symmetry error; i.e., using R_L = 4.7 kΩ causes a 4 mV error due to the resistor divider between the $R_{L(pulldown)}$ and the internal resistance of 4 Ω at 5 V output. Keep this in mind when sizing R_L.
[3] Devices programmed to the typical values are guaranteed to meet the $\Delta V_{OUT(Q)TC}$ specification.
[4] This is an average, and the actual step can vary. For best results, check $V_{OUT(Q)}$ after every retrim. Refer to the quiescent voltage output programming resolution information in the Response Characteristics, Definitions, and Performance Data section.
[5] Allegro guarantees limits of devices that remain within their factory-programmed SEN_COARSE and the corresponding $SENS_{PR}$ during customer programming.
[6] Device performance is guaranteed within these ranges. Typical value is the factory-programmed sensitivity.
[7] Validated by characterization and design. Specification valid from V_{OUT} = 0.4 V to 4.6 V.
[8] Lifetime drift numbers represent the average parameter drift observed during qualification.

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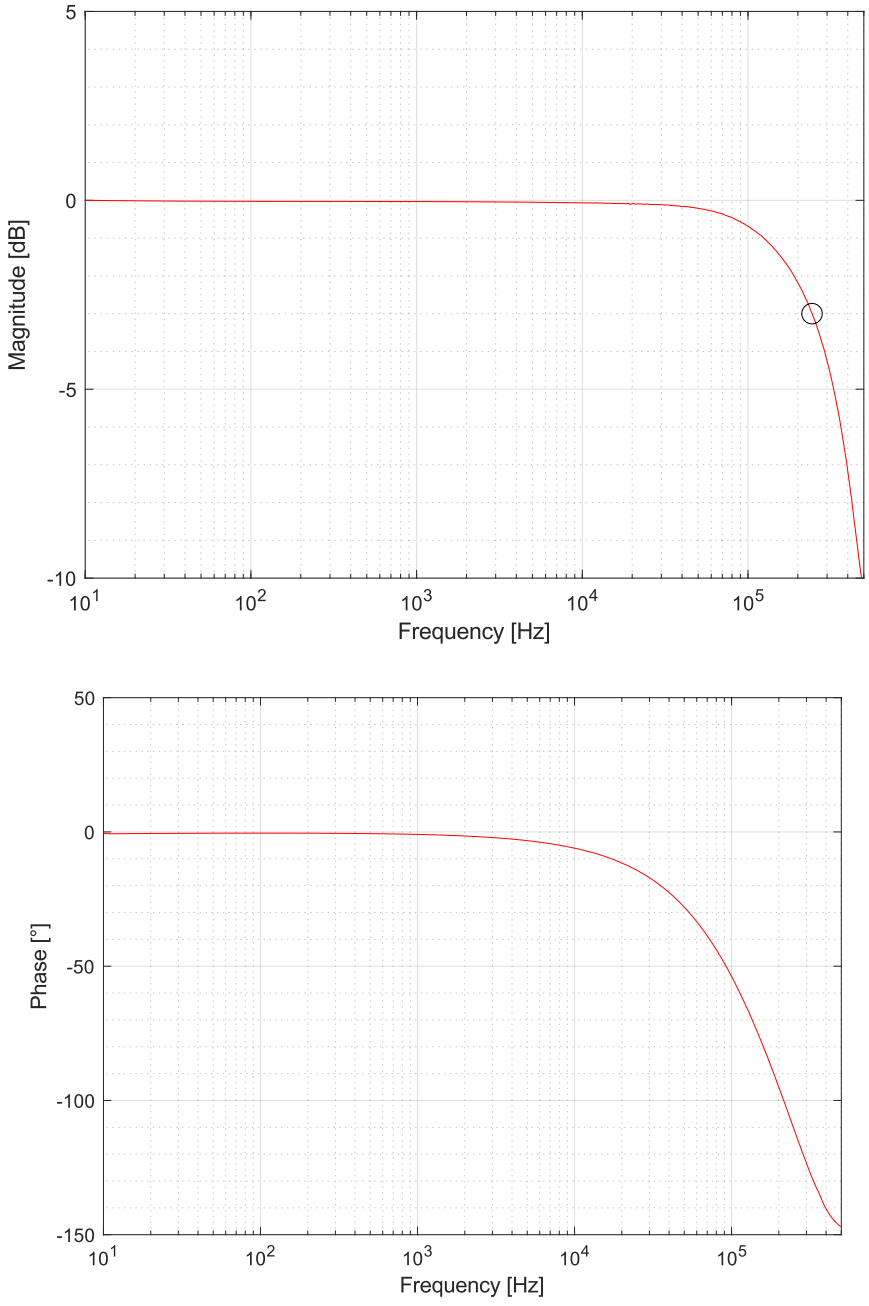
CHARACTERISTIC PERFORMANCE
ACS70312 TYPICAL FREQUENCY RESPONSE



For information regarding bandwidth characterization methods used for the ACS70312, see the “Characterizing System Bandwidth” application note (https://www.allegromicro.com/en/insights-and-innovations/technical-documents/hall-effect-sensor-ic-publications/an-effective-method-for-characterizing-system-bandwidth-an296169) on the Allegro website.

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RESPONSE CHARACTERISTICS, DEFINITIONS, AND PERFORMANCE DATA

Response Time ($t_{RESPONSE}$)

The time interval between a) when the applied magnetic field reaches 90% of its final value, and b) when the sensor output reaches 90% of its full-scale value.

Propagation Delay (t_{pd})

The time interval between a) when the applied magnetic field reaches 20% of its full-scale value, and b) when the sensor output reaches 20% of its full-scale value.

Rise Time (t_r)

The time interval between a) when the sensor reaches 10% of its full-scale value, and b) when it reaches 90% of its full-scale value.

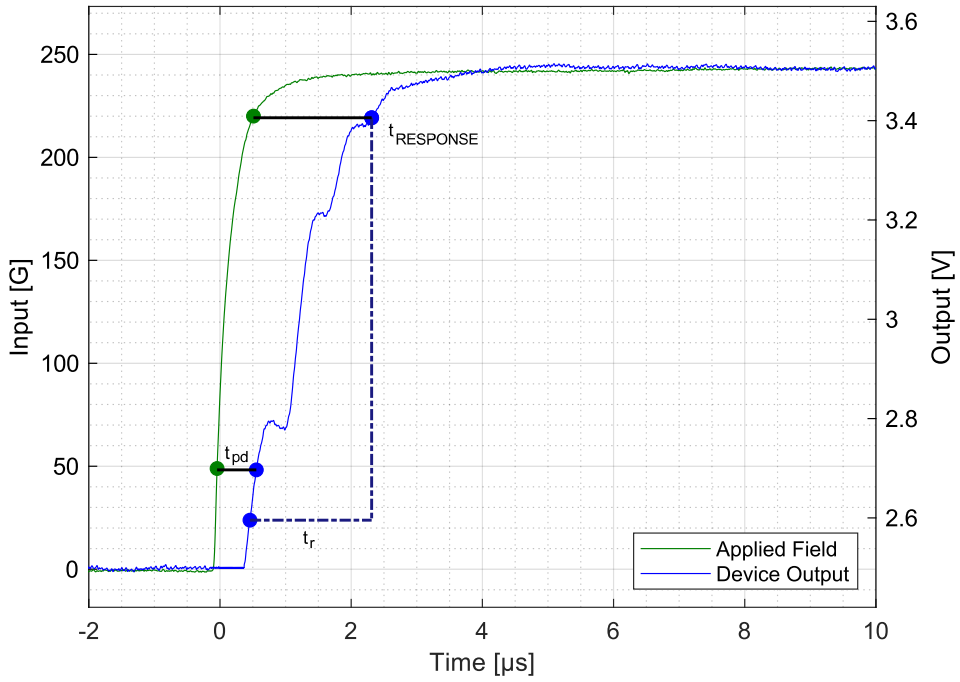
Output Slew Rate (SR)

The rate of change (V/µs) in the output voltage between a) when the sensor reaches 10% of its full-scale value, and b) when it reaches 90% of its full-scale value.

Response Time, Propagation Delay, Rise Time, and Output Slew Rate

Applied step with 10% to 90% rise time = 1 µs

Test Conditions: T_A = 25°C, C_{BYPASS} = 0.1 µF, C_L = 1 nF, R_L = 10 kΩ, 1 V output swing



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Quiescent Voltage Output ($V_{OUT(Q)}$)

In the quiescent state (no significant magnetic field: B = 0 G), the output ($V_{OUT(Q)}$) has a constant ratio to the supply voltage (V_{CC}) throughout the entire operating ranges of V_{CC} and ambient temperature (T_A).

Before any programming, the quiescent voltage output ($V_{OUT(Q)}$) has a nominal value of $V_{CC}/2$ for a bidirectional device and 0.5 V for unidirectional parts with a V_{CC} of 5 V.

Quiescent Voltage Output Programming Range

The quiescent voltage output ($V_{OUT(Q)}$) can be programmed within the quiescent voltage output programming range limits. Exceeding the specified quiescent voltage output programming range limits causes the quiescent voltage output drift over temperature ($\Delta V_{OUT(Q)TC}$) to deteriorate beyond the specified values.

Average Quiescent Voltage Output Programming Step Size ($V_{OUT(Q)Step}$)

The average quiescent voltage output programming step size ($V_{OUT(Q)Step}$) is determined using the following calculation:

$$V_{OUT(Q)Step} = \frac{V_{OUT(Q)maxcode} - V_{OUT(Q)mincode}}{2^n - 1}, \quad (1)$$

where n is the number of available programming bits in the trim range, 9 bits, $V_{OUT(Q)maxcode}$ is at decimal code 255, and $V_{OUT(Q)mincode}$ is at decimal code 256.

Quiescent Voltage Output Programming Resolution

The programming resolution for any device is half of its programming step size.

The step size of each bit can vary. For best accuracy, check $V_{OUT(Q)}$ after every trim. The DAC performance of the device is screened and accounted for in the factory-standard trim, but becomes a possible source of error if the devices is reprogrammed beyond the quiescent voltage output; programming beyond this range causes $\Delta V_{OUT(Q)TC}$ to be invalid.

Quiescent Voltage Output Drift Over Temperature ($\Delta V_{OUT(Q)TC}$)

The quiescent voltage output ($V_{OUT(Q)}$) may drift from its nominal value through the operating ambient temperature (T_A). The quiescent voltage output drift over temperature ($\Delta_{VOUT(Q)TC}$) is defined as:

$$\Delta V_{OUT(Q)TC} = V_{OUT(Q)(TA)} - V_{OUT(Q)(25°C)} \quad (2)$$

$\Delta V_{OUT(Q)TC}$ should be calculated using the measured value of $V_{OUT(Q)}$ at the current temperature and at 25°C.

Sensitivity (Sens) and Sensitivity Error ($Sens_{ERR}$)

The presence of a south-polarity magnetic field, perpendicular to the branded surface of the package face, increases the output voltage from its quiescent value toward the supply voltage rail. The amount of the output voltage increase is proportional to the magnitude of the magnetic field applied.

Conversely, application of a north-polarity field decreases the output voltage from its quiescent value. This proportionality is specified as the magnetic sensitivity, Sens (mV/G), of the device, defined as:

$$Sens = \frac{V_{OUT(BPOS)} - V_{OUT(BNEG)}}{BPOS - BNEG}, \quad (3)$$

where BPOS and BNEG are two magnetic fields with opposite polarities.

Sensitivity error is the error in percent between the factory-programmed sensitivity and the measured sensitivity value.

Factory-Programmed Sensitivity

Before any programming, sensitivity has a nominal value that depends on the SENS_COARSE bits setting. Each ACS70312 variant has a different SENS_COARSE setting. The TC performance is guaranteed if the SENS_COARSE bit is in its default factory value and within the sensitivity programming range corresponding to the SENS_COARSE bit.

Sensitivity Programming Range ($Sens_{PR}$)

The magnetic sensitivity (Sens) can be programmed around its initial value within the sensitivity range limits: $Sens_{PR}$(min) and $Sens_{PR}$(max). Exceeding the specified sensitivity range causes sensitivity drift over temperature ($\Delta Sens_{TC}$) to deteriorate beyond the specified values.

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Average Fine Sensitivity Programming Step Size ($Step_{SENS}$)

This is the change in the fine sensitivity parameter, per the code of the SENSF digital-to-analog converter (DAC). This value changes depending on SENS_COARSE. The over-temperature performance of the device is guaranteed only for the factory-programmed SENS_COARSE bit and its associated $Sens_{PR}$.

Sensitivity Programming Resolution

This resolution is equal to or less than 1/2 × $Step_{SENS}$. If the device is more than 1/2 × $Step_{SENS}$ but less than one $Step_{SENS}$ away from a desired trim, an additional step in the correct direction yields a resolution of less than 1/2 × $Step_{SENS}$.

Sensitivity Drift Over Temperature ($\Delta Sens_{TC}$)

Sensitivity (Sens) may drift from its expected value (SENS_EXPECTED) over the operating ambient temperature range (T_A). The sensitivity drift over temperature ($\Delta Sens_{TC}$) is defined as:

$$\Delta Sens_{TC} = \frac{Sens_{(TA)} - Sens_{(25°C)}}{Sens_{(25°C)}} \times 100\% \quad . \qquad (4)$$

Output Voltage Operating Range

The functional output voltage for optimal performance of the device is 0.5 V to 4.5 V output voltage, where V_{CC} = 5 V. The device can respond to magnetic fields that cause the output to go beyond these voltages, but parameters may not meet datasheet limits.

Sensitivity Linearity Error (Lin_{ERR})

The ACS70312 is designed to provide a linear output in response to a ramping applied magnetic field. Lin_{ERR} is valid from 0 G to ±2000 G input field while within the output voltage operating range. Consider two magnetic fields, B1 and B2. Ideally, the sensitivity of a device is the same for both fields, for a given supply voltage and temperature. Linearity error is present when there is a difference between the sensitivities measured at B1 and B2.

Linearity error (%) is measured and defined as:

$$Lin_{ERR} = \left(1 - \frac{Sens_{B2}}{Sens_{B1}}\right) \times 100\% \qquad (6)$$

where:

$$Sens_{Bx} = \frac{|V_{OUT(Bx)} - V_{OUT(Q)}|}{B_x} \quad . \qquad (7)$$

Ratiometry Error (Rat_{ERR})

The ACS70312 device features a ratiometric output. This means that the quiescent voltage output ($V_{OUT(Q)}$), sensitivity (Sens), and output voltage clamp (V_{CLP}) are proportional to the supply voltage (V_{CC}).When the supply voltage increases or decreases by a certain percentage, each characteristic also increases or decreases by the same percentage. Ratiometry error is the difference between the measured change in the supply voltage relative to 5 V and the measured change in each characteristic.

The quiescent voltage output ratiometry error, $Rat_{ERRVOUT(Q)}$ (%), for a given supply voltage (V_{CC}) is defined as:

$$Rat_{ERRVOUT(QBI)} = \left[1 - \frac{\left(\frac{V_{OUT(Q)(VCC)}}{V_{OUT(Q)(5V)}}\right)}{\frac{V_{CC}}{5\ V}}\right] \times 100\% \qquad (8)$$

The quiescent voltage output ratiometry error, $V_{RatERRVOUT(Q)}$ (mV), for a given supply voltage (V_{CC}) is defined as:

$$V_{RATERRVOUT(Q)} = \left[\left(V_{OUT(5V)} \times \frac{Vcc}{5V}\right) - V_{OUT(VCC)}\right] \qquad (9)$$

The sensitivity ratiometry error, $Rat_{ERRSens}$ (%), for a given supply voltage (V_{CC}) is defined as:

$$Rat_{ERRSens} = \left(1 - \frac{Sens_{(VCC)} / Sens_{(5V)}}{V_{CC} / 5\ V}\right) \times 100\% \quad . \qquad (10)$$

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Power-On-Reset Voltage (V_{POR})

On power-up, the ACS70312 is held in a reset state. The reset signal is disabled when V_{CC} reaches V_{POR_H} and time t_{PORR} has elapsed, allowing the output voltage to go from a high-impedance state into typical operation. During power-down, the reset signal is enabled when V_{CC} reaches V_{POR_L}, causing the output voltage to go into a high-impedance state.

Power-On Reset Release Time (t_{POR_R})

When V_{CC} rises to V_{POR_H}, the power-on-reset counter starts. The ACS70312 output voltage transitions from a high-impedance state to typical operation only when the power-on-reset counter has reached t_{PORR} and V_{CC} has been maintained above V_{POR_H}.

Output Saturation Voltage (V_{SAT})

When output voltage clamps are disabled, the output voltage can swing to a maximum of V_{SAT_H} and to a minimum of V_{SAT_L}.

Broken-Wire Voltage (V_{BRK})

If the GND pin is disconnected (broken-wire event), the output voltage goes to V_{BRK_H} (if a load resistor is connected to VCC) or to V_{BRK_L} (if a load resistor is connected to GND).

Power-On Time (t_{PO})

When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field.

Power-on time (t_{PO}) is defined as the time it takes for the output voltage to settle within ±10% of its steady-state value under an applied magnetic field, after the power supply has reached its minimum specified operating voltage ($V_{CC(min)}$) as shown in Figure 5.

Temperature Compensation Power-On Time (t_{TC})

After the power-on time (t_{PO}) has elapsed, t_{TC} is required before a valid temperature-compensated output.

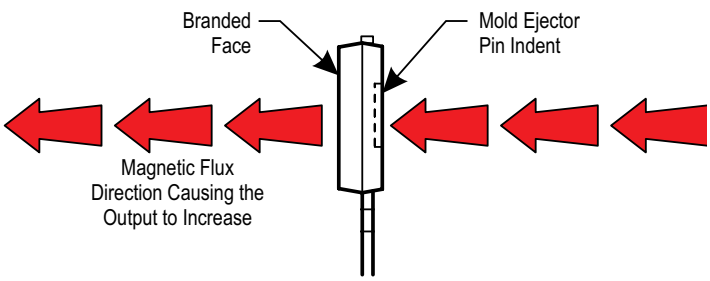

Figure 4: Magnetic Flux Polarity

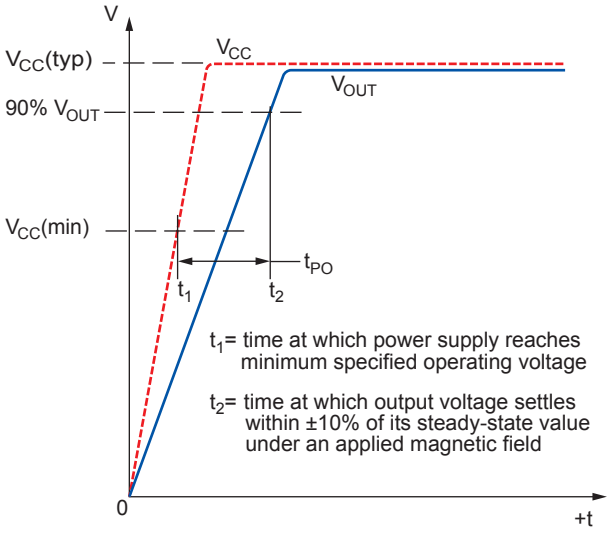

Figure 5: Power-On Time Definition

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FUNCTIONAL DESCRIPTIONS

The descriptions in this section assume: temperature = 25°C, no output load (R_L, C_L), and no magnetic field is present.

Power-On Reset (POR)

When the device is off, the output is in a high-impedance state.

Power-On

As V_{CC} ramps up, the device output is in high-impedance until V_{CC} reaches V_{POR_H}. As V_{CC} rises above V_{POR_H}, the device output leaves the high-impedance state and enters the typical operating mode.

Overvoltage Detection (V_{OVD})

When V_{CC} is raised above the overvoltage-detection-enable voltage (V_{OVD_H}), the ACS70312 output stage enters a high-impedance state. V_{OUT} is either pulled to V_{CC} with a pull-up R_L or pulled to GND with a pull-down R_L when V_{OVD_H} is reached. When programming the ACS70312, overvoltage detection must be active for communication. The ACS70312 output resumes typical operation after V_{CC} is below the overvoltage detection disable voltage, V_{OVD_L}.

NOTE: The supply voltage limits still apply for all operating characteristics.

Undervoltage Detection (V_{UVD})

When V_{CC} drops below the undervoltage-detection-enable voltage (V_{UVD_H}), the ACS70312 output stage drops close to GND, beyond the clamp or saturation voltage. The ACS70312 output resumes typical operation after V_{CC} is above the undervoltage-detection-disable voltage, V_{UVD_H}.

NOTE: The supply voltage limits still apply for all operating characteristics.

Power-Down

As V_{CC} ramps down, the device output is active until V_{CC} falls below V_{POR_L}. As V_{CC} falls below V_{POR_L}, the device output enters a high-impedance state.

Power On/Off Profile

ACS70312 power-on with a pull-down resistor is shown in Figure 6. The output follows VCC ratiometrically after exiting POR and is pulled to ground after entering UVD.

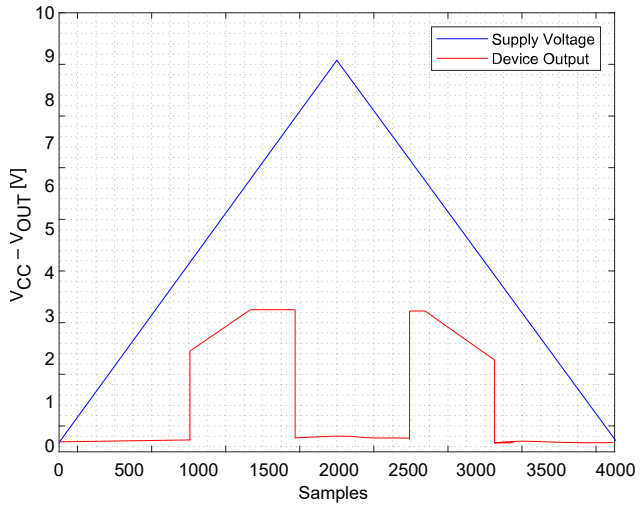

Figure 6: ACS70312 Power On/Off and UVD, R_L = 10 kΩ

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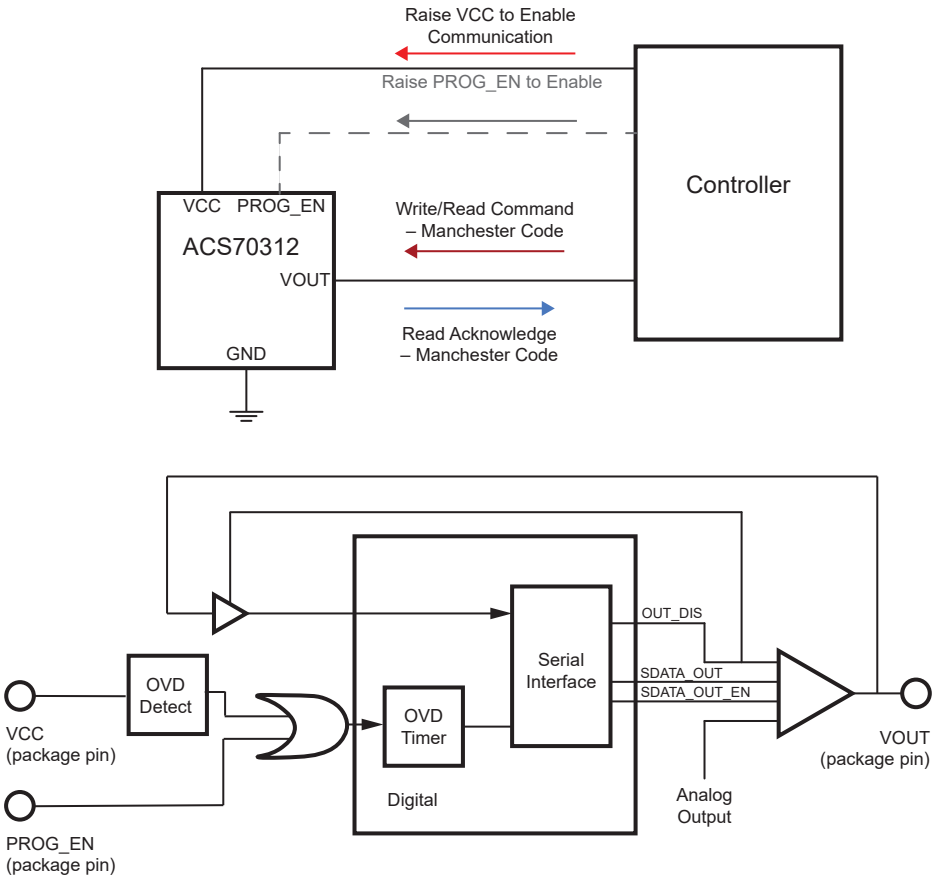
PROGRAMMING GUIDELINES

The serial interface uses a bidirectional communication on VOUT. The ACS70312 enters programming mode when V_{CC} increases beyond V_{prgH}(VCC). The ACS70312 also enters programming-enable mode if voltage on PROG_EN exceeds V_{prgH} (PROG_EN). The PROG_EN pin allows for low-voltage programming on the ACS70312 without the need to raise the supply voltage above 5 V.

The device has an internal charge pump to generate the EEPROM pulses.

Recommended programming kits/subkits and software can be found under the Technical Documents on the ACS70312 product page on the www.allegromicro.com website.



SDATA_OUT_EN	OUT_DIS	VOUT
0	0	Analog output
0	1	High-Z
1	X	SDATA_OUT

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Memory-Locking Mechanisms

The ACS70312 is equipped with two distinct memory-locking mechanisms:

- ***Default Lock:*** At power-up, all registers of the ACS70312 are locked by default. EEPROM and volatile memory cannot be written. To disable the default lock, a specific 32-bit customer access code must be written to address 0x36 within the access code timeout period (t_{ACC}) from power-up. After doing so, registers can be accessed. If VCC is power-cycled, the default lock is automatically re-enabled. This ensures that, during typical operation, memory content is altered due to unwanted glitches on VCC or the VOUT pin.
- ***Lock Bit:*** After EEPROM has been programmed by the user, the DEV_LOCK bit can be set high and VCC power-cycled to permanently disable the ability to read or write any register. This prevents the ability to disable the default lock using the previously described method.
- NOTE: After the DEV_LOCK bit has been set high and the VCC pin has been power-cycled, the DEV_LOCK bit can no longer be cleared and registers can no longer be written to.

Serial Communication

The serial interface allows an external controller to read from and write to registers, including EEPROM, in the ACS70312 using a point-to-point command/acknowledge protocol. The ACS70312 does not initiate communication; it only responds to commands from the external controller. Each transaction consists of a command from the controller. If the command is a write, there is no acknowledgment from the ACS70312. If the command is a read, the ACS70312 responds by transmitting the requested data.

Serial interface timing parameters are provided in Table 1.

NOTE: The external controller must avoid sending a command frame that overlaps a read acknowledge frame.

The serial interface uses a Manchester-encoding-based protocol (0 = rising edge, 1 = falling edge), with address and data transmitted MSB first. Four commands are recognized by the ACS70312: write access code, write to volatile memory, write to nonvolatile memory (EEPROM), and read. One frame type, read acknowledge, is sent by the ACS70312 in response to a read command.

The ACS70312 device uses a three-wire programming interface,

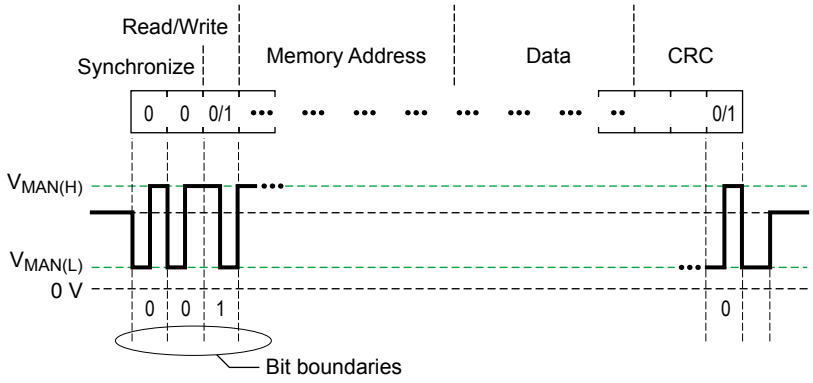

Figure 7: General Format for Serial Interface Commands

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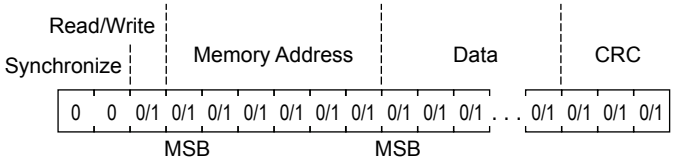
where VCC or PROG_EN is used to control the program-enable signal, data is transmitted on VOUT, and all signals are referenced to GND. This three-wire interface makes it possible to communicate with multiple devices with shared VCC and GND lines.

The four transactions (write access, write to EEPROM, write to volatile memory, and read) are shown in the figures on the following pages. To initialize any communication, VCC or PROG_EN should be increased to a level above V_{prgH} without exceeding the pin maximum voltage. At this time, VOUT is disabled and acts as an input.

After program-enable is asserted, the external controller must drive the output low in a time less than the program time delay, t_d. This prevents the device from interpreting any false transients on VOUT as data pulses. After the command is completed, VCC or PROG_EN is reduced below V_{prgL}, back to the typical operating level. Also, the output is enabled and responds to magnetic input.

When performing a write-to-EEPROM transaction, the ACS70312 requires a delay of t_w to store the data in EEPROM. The device responds with a high-to-low transition on VOUT to indicate the write-to-EEPROM sequence is complete.

When sending multiple command frames, it is not necessary to toggle the program-enable signal on VCC or PROG_EN. After the first command frame has completed and VCC or PROG_EN has remained at V_{prgH}, the device ignores any subsequent pulses on the output. When the program-enable signal is brought below V_{prgL}, the output responds to the magnetic input.



Quantity of Bits	Name	Values	Description
2	Synchronization	00	Used to identify the beginning of a serial interface command
1	Read/Write	0	[As required] Write operation
		1	[As required] Read operation
6	Address	0/1	[Read/Write] Register address (volatile memory or EEPROM)
32	Data	0/1	26 data bits and 6 ECC bits For a read command frame, the data consists of 32 bits: [31:28] not relevant, [27:26] ECC pass/fail, and [25:0] data, where bit 0 is the LSB For a write command frame, the data consists of 32 bits: [31:26] not relevant, and [25:0] data, where bit 0 is the LSB
3	CRC	0/1	Bits to check the validity of the frame

Figure 8: Command Frame General Format

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Table 1: Programming Parameters, C_{BYPASS} = 0.1 µF, V_{CC} = 5 V

Characteristics	Symbol	Note	Min.	Typ.	Max.	Unit
V_{CC} Program Enable Voltage High	V_{prgH}(VCC)	Program-enable signal high level on VCC	7.3	7.6	7.9	V
V_{CC} Program Enable Voltage Low	V_{prgL} (VCC)	Program-enable signal low level on VCC	6.3	6.6	6.9	V
PROG_EN Program Enable Voltage High	V_{prgH} (PROG_EN)	Program-enable signal high level on PROG_EN	2.4	–	–	V
PROG_EN Program Enable Voltage Low	V_{prgL} (PROG_EN)	Program-enable signal low level on PROG_EN	–	–	1.3	V
PROG_EN Internal Pull-Down Resistor	R_{PROG}		65	100	135	kΩ
Output Enable Delay	t_e	External capacitance (C_{LX}) on VOUT may increase the output enable delay	100	125	150	µs
Program Time Delay	t_d		84	88	93	µs
Program Write Delay	t_w		23	24	25	ms
Manchester High Voltage	$V_{MAN(H)}$	Data pulses on VOUT	4	5	VCC	V
Manchester Low Voltage	$V_{MAN(L)}$	Data pulses on VOUT	0	–	1	V
Bit Rate	t_{BITR}	Communication rate	1	30	100	kbps
Bit Time	t_{BIT}	Data-bit pulse width at 30 kbps	37	39	42	µs
Access Code Timeout	t_{ACC}		–	50	–	ms

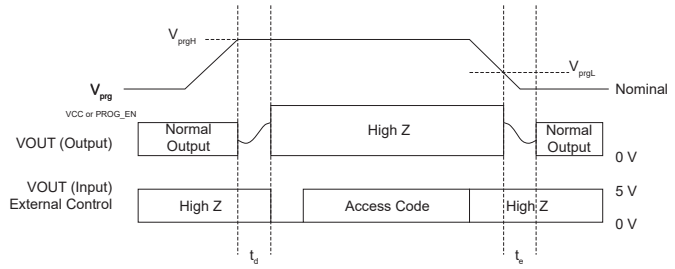

Figure 9: Write Access Code

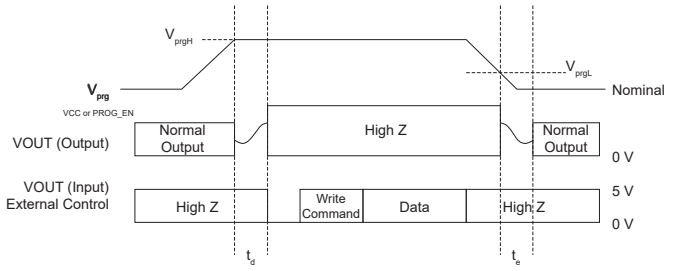

Figure 10: Write Nonvolatile Memory

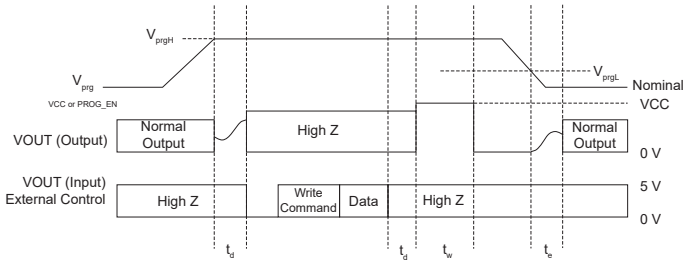

Figure 11: Write Volatile Memory

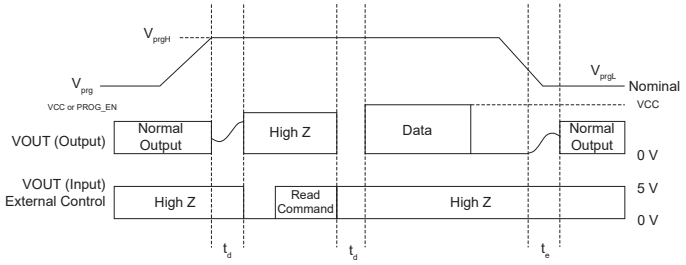

Figure 12: Read

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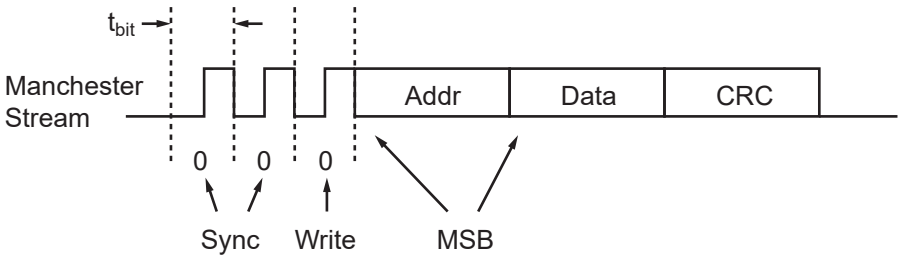
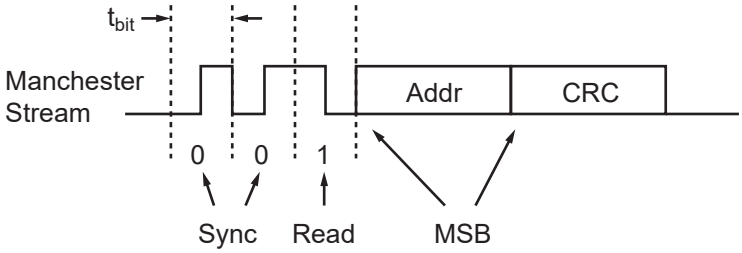
MANCHESTER COMMUNICATION

Command Format

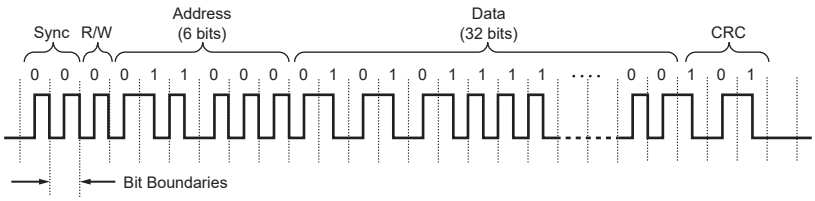


Manchester Write Command

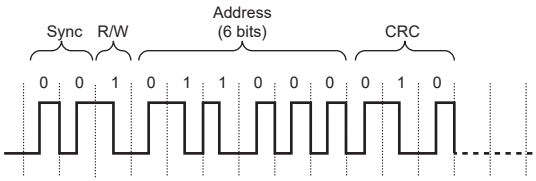


Manchester Read Command

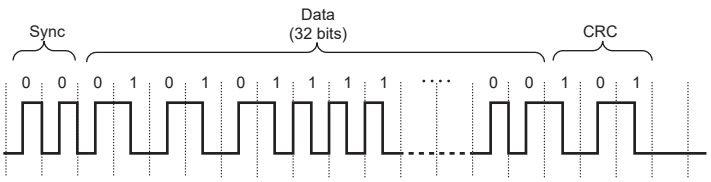
Write Command



Read Command



Read Acknowledge



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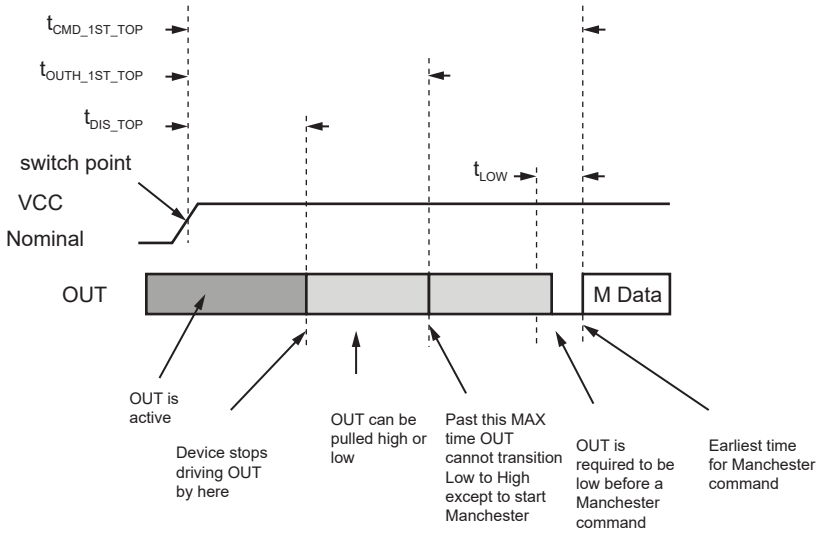
Generic Timing

For initial portion of Manchester command



Parameter	Description	Min.	Max.
t_{sclk}	System clock period after trimming	133 ns (7.5 MHz)	167 ns (6 MHz)
t_{bit}	Bit time	1 µs (1 MBd)	1 ms (1 kBd)
t_{DIS_TOP}	OUT pin is disabled after raising VCC	56 µs (512 × t_{sclk})	73.5 µs (514 × t_{sclk})
$t_{OUTH\_1ST\_TOP}$	The OUT pin is either pulled high or low Low-to-high transitions are not allowed after this maximum time has elapsed, except to start the Manchester command This is for the first Manchester command after raising VCC	73.5 µs	123 µs
$t_{CMD\_1ST\_TOP}$	Time required before the first Manchester command can be sent after raising VCC	144 µs	n/a
t_{LOW}	Time required to hold output low before the first Manchester edge	1 µs	n/a

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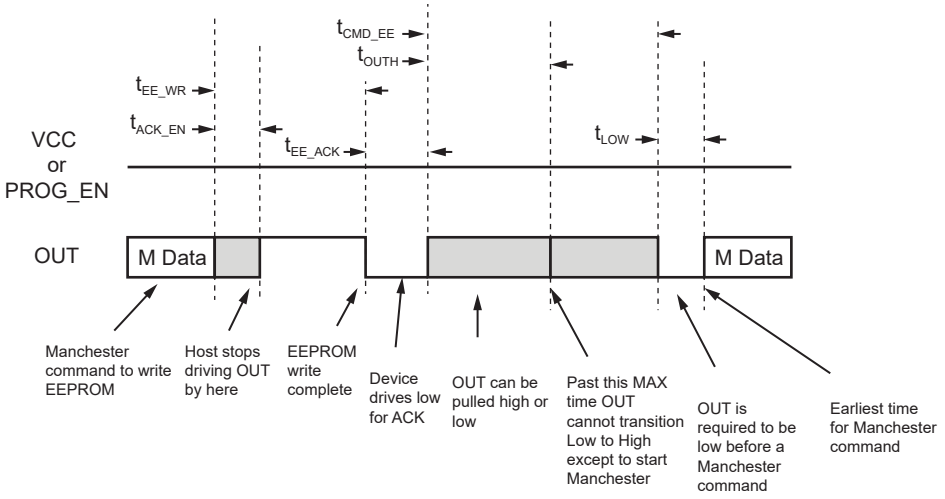
Write to EEPROM

If VCC or PROG_EN is held high at the programming voltage, multiple Manchester commands can be executed.



Parameter	Description	Min.	Max.
t_{sclk}	System clock period after trimming	133 ns (7.5 MHz)	167 ns (6 MHz)
t_{bit}	Bit time	1 µs (1 MBd)	1 ms (1 kBd)
t_{ACK_EN}	Time for the device to drive OUT after Manchester command: Host must stop driving OUT within this time	2 × t_{bit}	2 × t_{bit}
t_{EE_WR}	The device writes to EEPROM during this time	–	–
t_{EE_ACK}	Device drives OUT low during this time	1 × t_{bit}	1 × t_{bit}
t_{OUTH}	The OUT pin is either pulled high or low Low-to-high transitions are not allowed after this maximum time has elapsed, except to start the next Manchester command	0	1.8 × t_{bit}
t_{CMD_EE}	Time before the next Manchester command may be given following a write to EEPROM	2.2 × t_{bit}	–
t_{LOW}	Time required to hold output low before the first Manchester edge	1 µs	–

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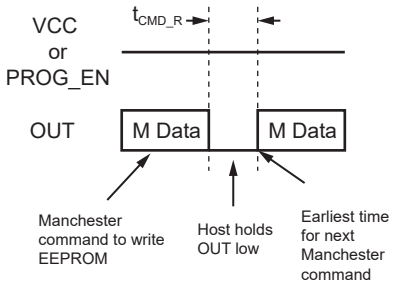
Write to Register (Not EEPROM)



Parameter	Description	Min.	Max.
t_{sclk}	System clock period after trimming	133 ns (7.5 MHz)	167 ns (6 MHz)
t_{bit}	Bit time	1 µs (1 MBd)	1 ms (1 kBd)
t_{CMD_R}	Time before the next Manchester command may be given following a write to a register	2 µs	n/a

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Read (Controller to ACS70312)

The fields for the read command are:

- Sync (2 bits, both with a value of zero)
- Read/Write (1 bit, must be 1 for read)
- CRC (3 bits)

The sequence for a read command is shown in Figure 13.

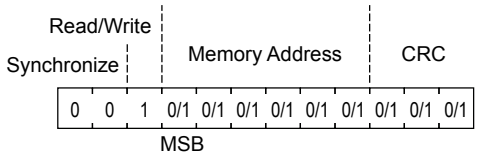

Figure 13: Read Sequence

Read Acknowledge (ACS70312 to Controller)

The fields for the data return frame are:

- Sync (2 bits, both with a value of zero)
- Data (32 bits):
  - □ [31:28] Not relevant
  - □ [27:26] ECC pass/fail
  - □ [25:0] Data

The sequence for a read acknowledge is shown in Figure 14. For instructions about how to detect read/write synchronize memory address data (32 bits) and ECC failure, refer to the Detecting ECC Error section.

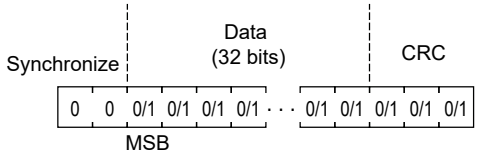

Figure 14: Read Acknowledgement Sequence

Write (Controller to ACS70312)

The fields for the write command are:

- Sync (2 bits, both with a value of zero)
- Read/Write (1 bit, must be 0 for write)
- Address (6 bits)
- Data (32 bits):
  - □ [31:26] Not relevant
  - □ [25:0] Data
- CRC (3 bits)

The sequence for a write command is shown in Figure 15. Bits [31:26] are not relevant because the ACS70312 automatically generates 6 ECC bits based on the content of bits [25:0]. These ECC bits are stored in EEPROM at locations [31:26].

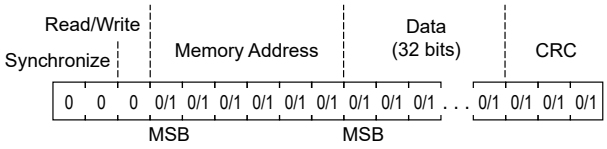

Figure 15: Write Sequence

Write Access Code (Controller to ACS70312)

The fields for the access code command are:

- Sync (2 bits, both with a value of zero)
- Read/Write (1 bit, must be 0 for write)
- Address (6 bits, address 0x36 for customer access)
- Data (32 bits, 0xC4136737 for customer access)
- CRC (3 bits)

The sequence for an access code command is shown in Figure 16.

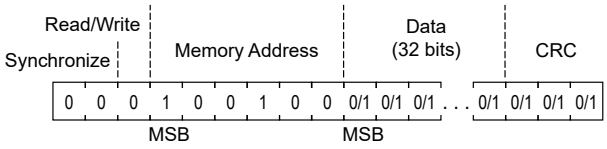

Figure 16: Write Access Code

The controller must open the serial communication with the ACS70312 device by sending an access code. It must be sent within access code timeout period, t_{ACC}, from power-up, or the device becomes disabled for read and write access.

Access Codes Information

Name	Serial Interface Format	
	Register Address (Hex)	Data (Hex)
Customer	0x36	0xC4136737

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EEPROM Error Checking and Correction (ECC)

Hamming code methodology is implemented for EEPROM checking and correction. The device has ECC enabled after power-up.

The device always returns 32 bits.

The message received from the controller is analyzed by the device EEPROM driver and ECC bits are added. The first 6 received bits from device to controller are dedicated to ECC.

The Manchester serial interface uses a 3-bit cyclic redundancy check (CRC) for data-bit error checking (synchronized bits are ignored during the check). The CRC algorithm is based on the polynomial $g(x) = x^3 + x + 1$ and is initialized to 111 when first powered up. Write commands written to the peripheral are checked against the embedded CRC field.

Detecting ECC Error

If an uncorrectable error has occurred, bits 27:26 are set to 10, the VOUT pin goes to a high-impedance state, and the device does not respond to the applied magnetic field.

EEPROM ECC Errors

Bits	Name	Description
31:28	–	No meaning
27:26	ECC	00 = No Error 01 = Error detected and message corrected 10 = Uncorrectable error 11 = No meaning
25:0	D[25:0]	EEPROM data

Table 2: Customer Memory Map

Address	Register Name	Parameter Name	Description	r/w	Bits	Location
0x4	SCRATCH_C	CUSTOMER_SCRATCH	Unused register that can be written to, as needed, for customer data storage	RW	26	25:0
0x5	CUST0_C	SENSF	Sensitivity, fine adjustment, 2's-complement register	RW	9	8:0
		QVOF	Quiescent output voltage (QVO), fine adjustment, 2's-complement register	RW	9	17:9
		SENSC [1]	Coarse sensitivity	RW	2	19:18
0x6	CUST1_C	RAT_DIS	Ratiometry disable; Sens and $V_{OUT(Q)}$ are not guaranteed if ratiometry is disabled	RW	1	2
		UNI_EN [1]	Enables unidirectional output	RW	1	4
		CLAMP_EN	Clamp enable	RW	1	5
		POL [1]	Reverses output polarity	RW	1	6
		DEV_LOCK	Bit to lock the serial interface from receiving data	RW	1	7
0x28	STATUS_C	CUSTOMER_ACCESS	Customer write access enabled	RO	1	0
0x36	UNLOCK_C	CUSTOMER_UNLOCK	Write 0xC4136737 to address 0x36 within t_{ACC} to unlock the device	WO	32	31:0

[1] If this register is changed from the factory default, overtemperature performance is no longer valid.

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PACKAGE OUTLINE DRAWINGS

For Reference Only - Not for Tooling Use

(Reference DWG-0000426, Rev. 1)
Dimensions in millimeters - NOT TO SCALE
Dimensions exclusive of mold flash, gate burs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

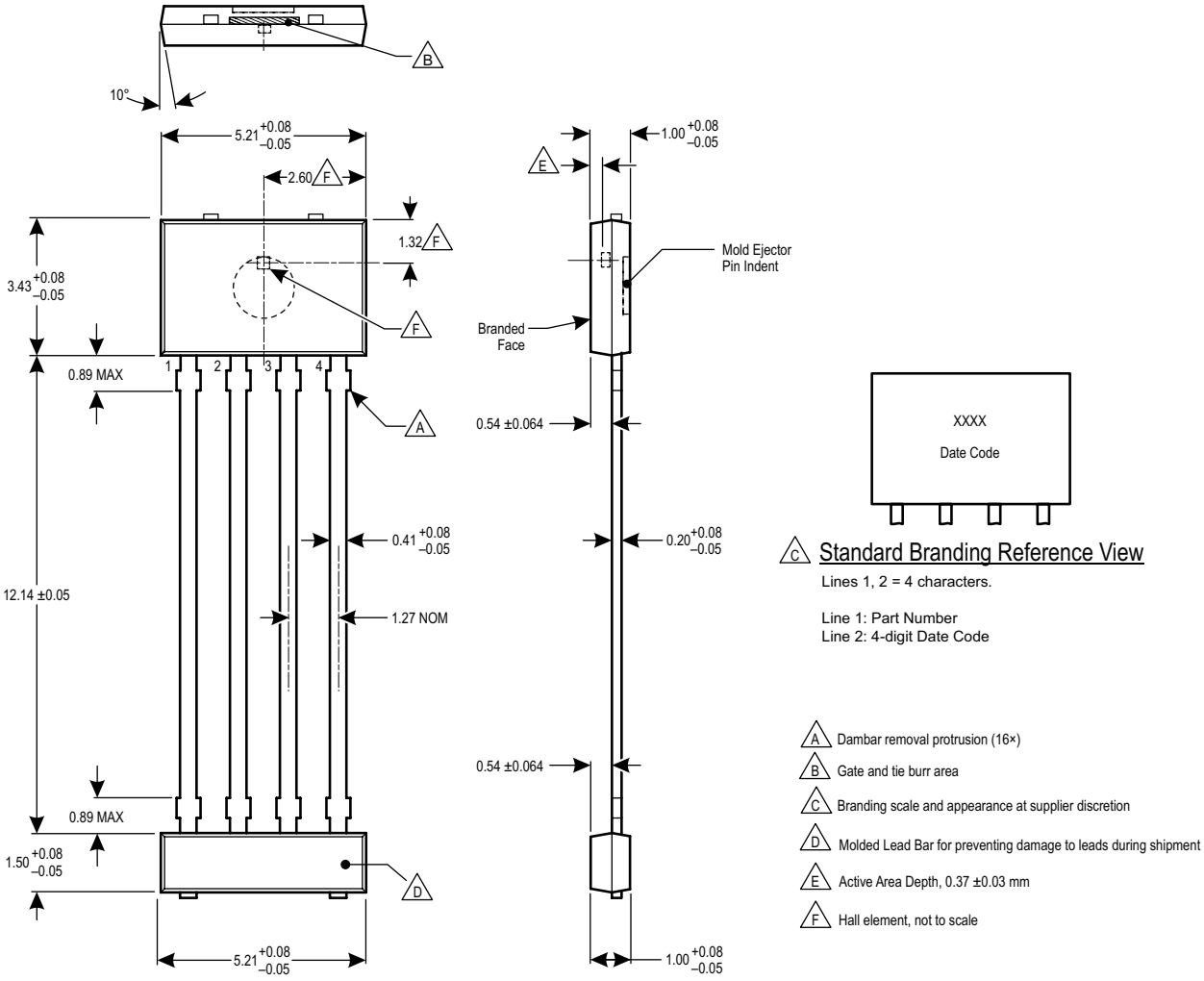

Figure 17: Package KT, 4-Pin SIP, TN Leadform

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Revision History

Number	Date	Description
–	October 30, 2023	Preliminary
1	March 4, 2024	Initial release: Updated sensitivity error, sensitivity range, and sensitivity linearity error (page 7); moved maximum field range to a magnetic characteristics section (page 8); aligned symbol for average quiescent voltage output programming step size throughout by changing $Step_{VOUT(Q)}$ to $V_{OUT(Q)Step}$ (page 11); corrected plot of on/off behavior (page 14); corrected address for STATUS_C register and added notes to QVOF and SENSF registers (page 24); corrected Hall-element location (page 25); and made minor editorial corrections throughout (all pages)
2	March 14, 2024	Released for publication (no content changes; headings only)
3	April 3, 2024	Updated Selection Guide Sensitivity Programming Range values (page 3) and Sensitivity Programming Range values (page 7).
4	October 15, 2024	Modified footnote for sensitivity linearity error operating characteristic (page 8), modified default lock description (page 16), t_{ACC} characteristic (pages 16 and 18), and overtemperature performance notes in customer memory map table (page 24)

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