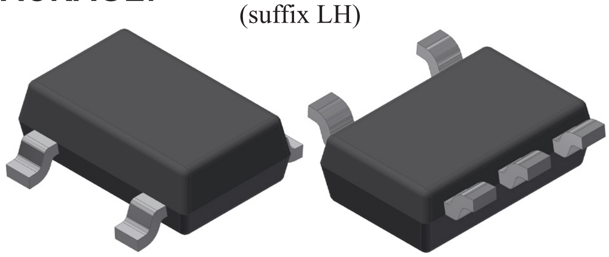
ACS37041 and ACS37042

Integrated Hall Effect Current Sensor in SOT23-W 5-Pin

FEATURES AND BENEFITS

- Self contained shuntless current sensing with no external sense resistor required; single package solution
- Low ohmic loss with 1.6 mΩ conductor resistance on the LH package
- Differential sensing robust against external magnetic fields
- Small footprint, SOT23-W 5-pin LH package
- 150 kHz analog output for fast response time
- Inherent galvanic isolation
  - □ 100 V_{RMS} functional isolation (ACS37041 only)
  - □ UL certified 285 V_{RMS} basic working voltage (ACS37042 only, pending)
- Total error less than ±5% over temperature
- 3.3 V and 5 V supply voltage options
- Bidirectional current sensing up to 30 A
- Wide operating temperature range, –40ºC to 125ºC
- AEC-Q100 Grade 1, automotive qualified (ACS37041 only, ACS37042 qualification pending)

PACKAGE: 5-pin SOT23-W (suffix LH)



DESCRIPTION

The ACS37041/2 is a small, integrated current sensor for cost-optimized applications. It features a voltage output that is galvanically isolated from the measured current. The current conductor has a low 1.6 mΩ resistance, ideal for low power dissipation constraints.

The ACS37041 features a 100 V_{RMS} functional working voltage while the ACS37042 features a 285 V_{RMS} basic working voltage

The ACS37041/2 has 5 V and 3.3 V variants, allowing it to function in a variety of applications. The ACS37041/2 has a sensitivity error that is less than ±3.5% over temperature and can sense up to 30 A bidirectionally, all with the same footprint as a SOT23-W 5-pin current sense amplifier without the need for a shunt resistor.

The ACS37041/2 is a lead (Pb) free device plated with 100% matte tin, compatible with standard lead-free printed circuit board assembly processes.

APPLICATIONS

- Industrial motor drivers (<100 V)
- Clean energy string inverter (optimizer)
- Clean energy micro inverter
- Personal mobility (e-bikes and e-scooters)

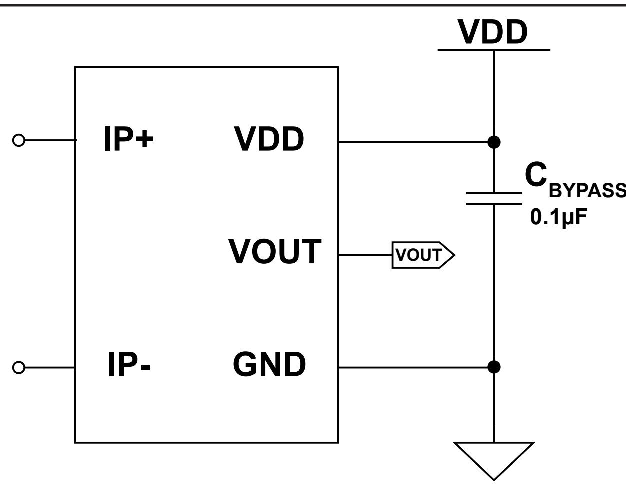


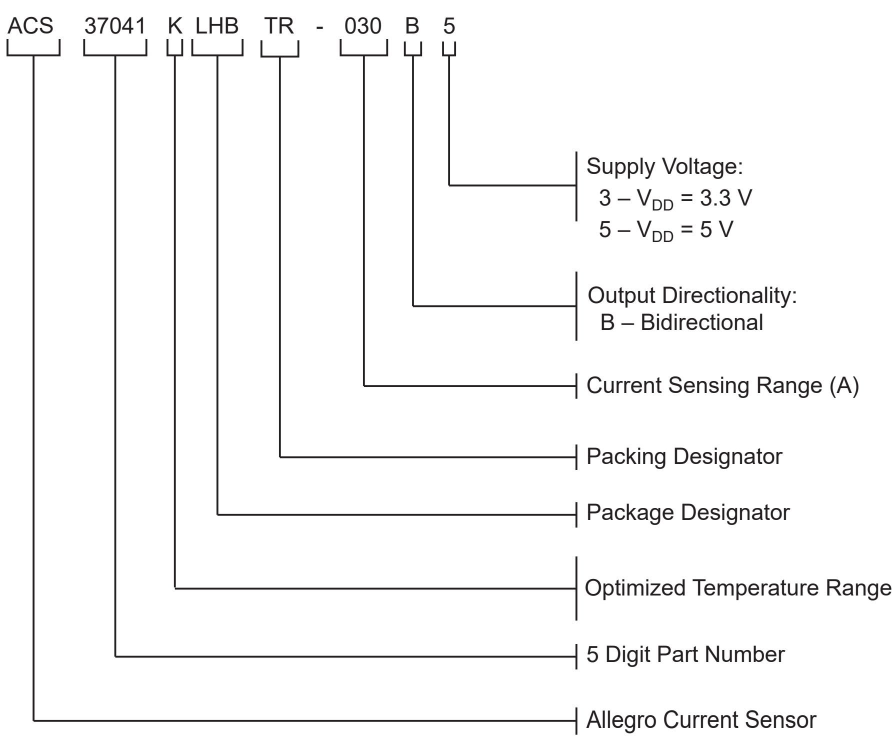
Figure 1: Typical Application Circuit

The ACS37041 outputs an analog signal at VOUT that varies linearly with the primary current, I_P, within the specified ranges.

SELECTION GUIDE

Part Number	Current Sensing Range, I_{PR} (A)	Sensitivity (mV/A)	V_{DD} (V)	V_{QVO} (V)	Optimized Temperature Range T_A (°C)	Packing
ACS37041KLHBLT-010B3	±10	132	3.3	1.65	–40 to 125	Tape and Reel, 3000 pieces per reel
ACS37041KLHBLT-030B3	±30	44				
ACS37041KLHBLT-010B5	±10	200	5	2.5		
ACS37041KLHBLT-030B5	±30	66.7				
ACS37042KLHBLT-010B3	±10	132	3.3	1.65	–40 to 125	Tape and Reel, 3000 pieces per reel
ACS37042KLHBLT-030B3	±30	44				
ACS37042KLHBLT-010B5	±10	200	5	2.5		
ACS37042KLHBLT-030B5	±30	66.7				

NAMING SPECIFICATION



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ABSOLUTE MAXIMUM RATINGS[1]

Characteristic	Symbol	Notes	Min	Max	Unit
Supply Voltage	V_{DD}	Applies to VDD	–0.5	6	V
Output Voltage	V_O	Applies to VOUT	–0.5	V_{DD} + 0.5	V
Operating Ambient Temperature	T_A		–40	125	°C
Storage Temperature	T_{STG}		–65	165	°C
Maximum Junction Temperature	T_J		–	165	°C

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ISOLATION CHARACTERISTICS

Characteristic	Symbol	Notes	Rating	Unit
ACS37041 Only				
Working Voltage for Functional Isolation	V_{WVFI}	Allegro approved working voltage for functional insulation	100	V_{RMS}
ACS37042 Only				
Withstand Voltage[1][2]	V_{ISO}	Agency rated for 60 seconds per UL 62368-1 (edition 3)	1767	V_{RMS}
Working Voltage for Basic Isolation[2]	V_{WVBI}	Maximum approved working voltage for basic insulation according to UL 62368-1 (edition 3)	403	V_{PK} or V_{DC}
			285	V_{RMS}
Impulse Withstand Voltage	$V_{IMPULSE}$	Tested ±5 pulses at 2/minute in compliance to IEC 61000-4-5, 1.2 µs (rise) / 50 µs (width)	2500	V_{PK}
ACS37041/ACS37042				
Clearance	D_{CL}	Minimum distance through air from IP leads to signal leads	1.9	mm
Creepage	D_{CR}	Minimum distance along package body from IP leads to signal leads	2	mm
Distance Through Insulation	DTI	Minimum internal distance through insulation	25	µm
Comparative Tracking Index	CTI	Material Group II	400 to 599	V

[1] 100% Production-tested in accordance with UL 62368-1 (edition 3)
[2] Certification pending. Advanced information.

PACKAGE CHARACTERISTICS

Characteristic	Symbol	Notes	Min.	Typ.	Max.	Unit
Internal Conductor Resistance	R_{IC}	T_A = 25°C	–	1.6	–	mΩ
Internal Conductor Inductance	L_{IC}	T_A = 25°C	–	2	–	nH
Moisture Sensitivity Level	MSL	Per IPC/JEDEC J-STD-020	–	2	–	–

THERMAL CHARACTERISTICS

Characteristic	Symbol	Notes	Value	Unit
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	Mounted on the Allegro LH Current Sensor Evaluation Board (ACSEVB-LH5)	32	°C/W
Package Thermal Metric (Junction to Top)	Ψ_{JT}		3	°C/W

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

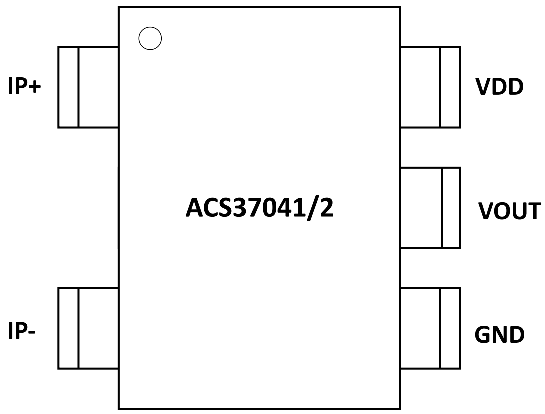


Figure 2: LH Package Pinout Diagram

Terminal List Table

Number	Name	Function
1, 2	IP	Integrated current sensing path
3	GND	Device ground
4	VOUT	Voltage output
5	VDD	Device supply voltage

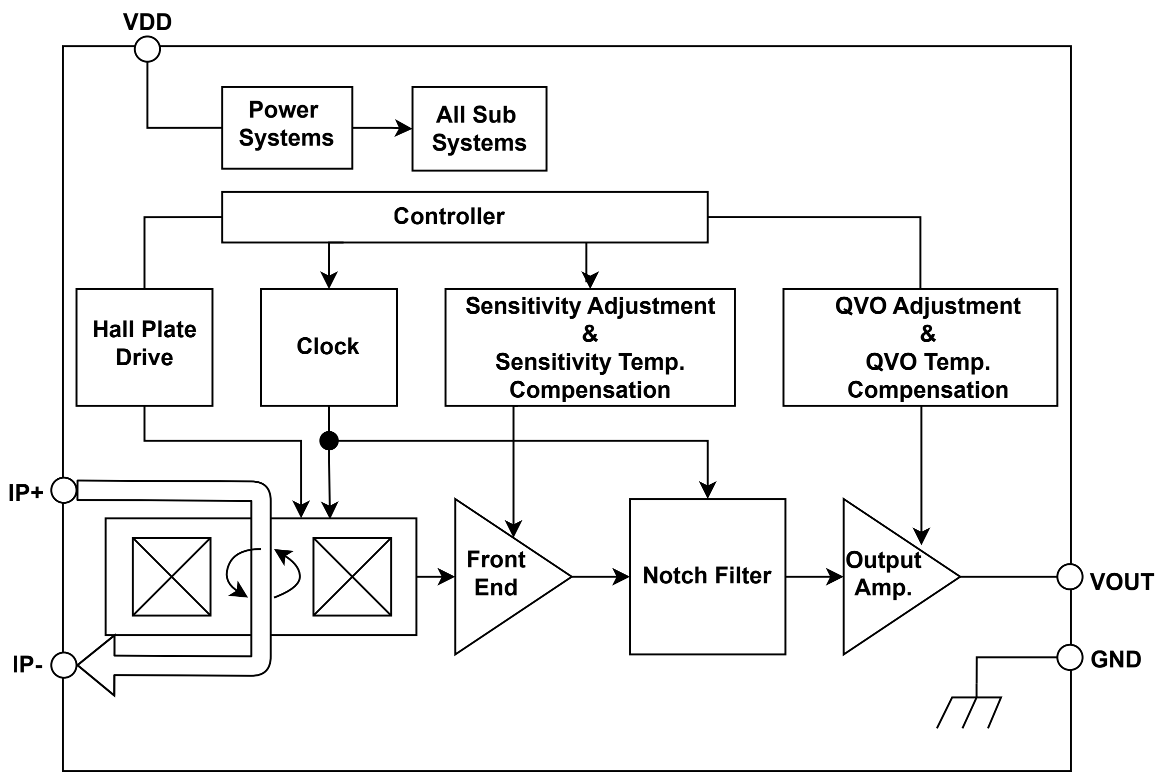


Figure 3: Functional Block Diagram

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

COMMON ELECTRICAL CHARACTERISTICS: Valid through full operating temperature range, T_A = – 40°C to 125°C, C_{BYPASS} = 0.1 µF, and typical VDD, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{DD}	5 V variant	4.5	5	5.5	V
		3.3 V variant	3.0	3.3	3.6	V
Supply Current	I_{DD}	5 V variant, no load on VOUT	–	9	12	mA
		3.3 V variant, no load on VOUT	–	8	10	mA
VOUT Capacitive Load	C_{L_VOUT}	VOUT to GND	–	–	1	nF
VOUT Resistive Load	R_{L_VOUT}	VOUT to GND, VOUT to VDD	10	–	–	kΩ
Power-On Reset Voltage	V_{POR}	VDD rising 1 V/ms	–	–	2.9	V
POR Hysteresis	V_{POR_HYS}		100	–	–	mV
Power-On Time	t_{PO}	T_A = 25°C, VDD rising 1 V/ms	–	84	–	µs
Rise Time	t_R	T_A = 25°C, C_L = 1 nF	–	2.8	4.8	µs
Response Time	t_{RESP}	T_A = 25°C, C_L = 1 nF	–	3	5	µs
Propagation Delay	t_{PD}	T_A = 25°C, C_L = 1 nF	–	1.8	3	µs
Bandwidth	BW	Small signal –3 dB, C_L = 1 nF	–	125	–	kHz
Noise Density	N_D	5 V variant, T_A = 25°C, CL = 1 nF	–	139	–	µA/√Hz
		3.3 V variant, T_A = 25°C, CL = 1 nF	–	205	–	µA/√Hz
Output Saturation Voltage	V_{SAT_H}	R_L = 10 kΩ to GND	V_{DD} – 0.25	–	–	V
	V_{SAT_L}	R_L = 10 kΩ to VDD	–	–	0.25	V
Common-Mode Field Sensitivity	CMFS	Input-referred error due to a 40 G common-mode field	–	0.45	–	mA/G

ALLEGRO microsystems

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

xKLHB-010B3 PERFORMANCE CHARACTERISTICS: Valid through full operating temperature range, T_A = – 40°C to 125°C, C_{BYPASS} = 0.1 µF, and V_{DD} = 3.3 V unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
NOMINAL PERFORMANCE						
Current Sensing Range	I_{PR}		–10	–	10	A
Sensitivity	Sens	$I_{PR(min)} < I_P < I_{PR(max)}$	–	132	–	mV/A
Quiescent Voltage Output	V_{QVO}	I_P = 0 A	–	1.65	–	V
ERROR COMPONENTS[1]						
Noise	N	T_A = 25°C, C_L = 1nF, BW = 125 kHz	–	±13	–	mV_{RMS}
Power Supply Sensitivity Error	E_{SENS_PS}	$V_{DD(MIN)}$ to $V_{DD(MAX)}$, T_A = –40°C to 125°C	–1.8	–	1.8	%
Power Supply Quiescent Voltage Output Error	V_{QVO_PS}	$V_{DD(MIN)}$ to $V_{DD(MAX)}$, T_A = –40°C to 125°C	–11	–	11	mV
ERROR COMPONENTS INCLUDING LIFETIME DRIFT[2]						
Sensitivity Error	E_{SENS}	I_P = 3 A, T_A = 25°C	–2.3	±1.2	2.3	%
		I_P = 3 A, T_A = 25°C to 125°C	–2.8	±1.2	2.8	%
		I_P = 3 A, T_A = –40°C to 25°C	–3.1	±1.2	3.1	%
Quiescent Voltage Output Error	V_{QVO_E}	I_P = 0 A, T_A = 25°C	–20	±7	20	mV
		I_P = 0 A, T_A = 25°C to 125°C	–27	±11	27	mV
		I_P = 0 A, T_A = –40°C to 25°C	–21	±10	21	mV

[1] "Min." and "Max." interval for performance characteristics is determined such that 99.99% of devices lie within the interval during initial characterization. The worst case of µ±6σ was calculated and applied symmetrically. "Min" and "Max" limits include a calculation buffer for additional margining.
[2] "Min." and "Max." interval is determined such that 99.7% of devices lie within the interval derived from 2 lots of characterization and the worst case drift observed in AEC-Q100 qualification stresses with additional margin. The worst case of µ±3σ was calculated and applied symmetrically. "Typ." is determined such that 68% of devices lie within the interval during initial characterization. The worst case of µ±1σ was calculated and recorded.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

xKLHB-030B3 PERFORMANCE CHARACTERISTICS: Valid through full operating temperature range, T_A = – 40°C to 125°C, C_{BYPASS} = 0.1 µF, and V_{DD} = 3.3 V unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
NOMINAL PERFORMANCE						
Current Sensing Range[1]	I_{PR}		–30	–	30	A
Sensitivity	Sens	$I_{PR(min)} < I_P < I_{PR(max)}$	–	44	–	mV/A
Quiescent Voltage Output	V_{QVO}	I_P = 0 A	–	1.65	–	V
ERROR COMPONENTS[2]						
Noise	N	T_A = 25°C, C_L = 1nF, BW = 125 kHz	–	±4	–	mV_{RMS}
Power Supply Sensitivity Error	E_{SENS_PS}	$V_{DD(MIN)}$ to $V_{DD(MAX)}$, T_A = –40°C to 125°C	–1.8	–	1.8	%
Power Supply Quiescent Voltage Output Error	V_{QVO_PS}	$V_{DD(MIN)}$ to $V_{DD(MAX)}$, T_A = –40°C to 125°C	–5	–	5	mV
ERROR COMPONENTS INCLUDING LIFETIME DRIFT[3]						
Sensitivity Error	E_{SENS}	I_P = 3 A, T_A = 25°C	–2.4	±1.4	2.4	%
		I_P = 3 A, T_A = 25°C to 125°C	–2.6	±1.4	2.6	%
		I_P = 3 A, T_A = –40°C to 25°C	–2.9	±1.4	2.9	%
Quiescent Voltage Output Error	V_{QVO_E}	I_P = 0 A, T_A = 25°C	–11	±4	11	mV
		I_P = 0 A, T_A = 25°C to 125°C	–12	±4	12	mV
		I_P = 0 A, T_A = –40°C to 25°C	–16	±9	16	mV

[1] For accuracy considerations with current greater than 15 A, refer to the “IP Power Dissipation Output Drift” on page 16.
[2] “Min.” and “Max.” interval for performance characteristics is determined such that 99.99% of devices lie within the interval during initial characterization. The worst case of µ±6σ was calculated and applied symmetrically. “Min” and ”Max” limits include a calculation buffer for additional margining.
[3] “Min.” and “Max.” interval is determined such that 99.7% of devices lie within the interval derived from 2 lots of characterization and the worst case drift observed in AEC-Q100 qualification stresses with additional margin. The worst case of µ±3σ was calculated and applied symmetrically. “Typ.” is determined such that 68% of devices lie within the interval during initial characterization. The worst case of µ±1σ was calculated and recorded.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

xKLHB-010B5 PERFORMANCE CHARACTERISTICS: Valid through full operating temperature range, T_A = – 40°C to 125°C, C_{BYPASS} = 0.1 µF, and V_{DD} = 5 V unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
NOMINAL PERFORMANCE						
Current Sensing Range	I_{PR}		–10	–	10	A
Sensitivity	Sens	$I_{PR(min)} < I_P < I_{PR(max)}$	–	200	–	mV/A
Quiescent Voltage Output	V_{QVO}	I_P = 0 A	–	2.5	–	V
ERROR COMPONENTS[1]						
Noise	N	T_A = 25°C, C_L = 1nF, BW = 125 kHz	–	±13	–	mV_{RMS}
Power Supply Sensitivity Error	E_{SENS_PS}	$V_{DD(MIN)}$ to $V_{DD(MAX)}$, T_A = –40°C to 125°C	–1.3	–	1.3	%
Power Supply Quiescent Voltage Output Error	V_{QVO_PS}	$V_{DD(MIN)}$ to $V_{DD(MAX)}$, T_A = –40°C to 125°C	–16	–	16	mV
ERROR COMPONENTS INCLUDING LIFETIME DRIFT[2]						
Sensitivity Error	E_{SENS}	I_P = 3 A, T_A = 25°C	–2.1	±1.2	2.1	%
		I_P = 3 A, T_A = 25°C to 125°C	–3.1	±1.6	3.1	%
		I_P = 3 A, T_A = –40°C to 25°C	–2.9	±1.2	2.9	%
Quiescent Voltage Output Error	V_{QVO_E}	I_P = 0 A, T_A = 25°C	–26	±6	26	mV
		I_P = 0 A, T_A = 25°C to 125°C	–45	±11	45	mV
		I_P = 0 A, T_A = –40°C to 25°C	–31	±8	31	mV

[1] "Min." and "Max." interval for performance characteristics is determined such that 99.99% of devices lie within the interval during initial characterization. The worst case of µ±6σ was calculated and applied symmetrically. "Min" and "Max" limits include a calculation buffer for additional margining.
[2] "Min." and "Max." interval is determined such that 99.7% of devices lie within the interval derived from 2 lots of characterization and the worst case drift observed in AEC-Q100 qualification stresses with additional margin. The worst case of µ±3σ was calculated and applied symmetrically. "Typ." is determined such that 68% of devices lie within the interval during initial characterization. The worst case of µ±1σ was calculated and recorded.

ALLEGRO microsystems
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

xKLHB-030B5 PERFORMANCE CHARACTERISTICS: Valid through full operating temperature range, T_A = – 40°C to 125°C, C_{BYPASS} = 0.1 µF, and V_{DD} = 5 V unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
NOMINAL PERFORMANCE						
Current Sensing Range[1]	I_{PR}		–30	–	30	A
Sensitivity	Sens	$I_{PR(min)} < I_P < I_{PR(max)}$	–	66.7	–	mV/A
Quiescent Voltage Output	V_{QVO}	I_P = 0 A	–	2.5	–	V
ERROR COMPONENTS[2]						
Noise	N	T_A = 25°C, C_L = 1nF, BW = 125 kHz	–	±4	–	mV_{RMS}
Power Supply Sensitivity Error	E_{SENS_PS}	$V_{DD(MIN)}$ to $V_{DD(MAX)}$, T_A = –40°C to 125°C	–1.3	–	1.3	%
Power Supply Quiescent Voltage Output Error	V_{QVO_PS}	$V_{DD(MIN)}$ to $V_{DD(MAX)}$, T_A = –40°C to 125°C	–8	–	8	mV
ERROR COMPONENTS INCLUDING LIFETIME DRIFT[3]						
Sensitivity Error	E_{SENS}	I_P = 3 A, T_A = 25°C	–2.7	±1.1	2.7	%
		I_P = 3 A, T_A = 25°C to 125°C	–3.3	±1.6	3.3	%
		I_P = 3 A, T_A = –40°C to 25°C	–2.8	±1.1	2.8	%
Quiescent Voltage Output Error	V_{QVO_E}	I_P = 0 A, T_A = 25°C	–13	±4	13	mV
		I_P = 0 A, T_A = 25°C to 125°C	–19	±6	19	mV
		I_P = 0 A, T_A = –40°C to 25°C	–19	±8	19	mV

[1] For accuracy considerations with current greater than 15 A, refer to the “IP Power Dissipation Output Drift” on page 16.
[2] “Min.” and “Max.” interval for performance characteristics is determined such that 99.99% of devices lie within the interval during initial characterization. The worst case of µ±6σ was calculated and applied symmetrically. “Min” and ”Max” limits include a calculation buffer for additional margining.
[3] “Min.” and “Max.” interval is determined such that 99.7% of devices lie within the interval derived from 2 lots of characterization and the worst case drift observed in AEC-Q100 qualification stresses with additional margin. The worst case of µ±3σ was calculated and applied symmetrically. “Typ.” is determined such that 68% of devices lie within the interval during initial characterization. The worst case of µ±1σ was calculated and recorded.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

RESPONSE CHARACTERISTICS DEFINITIONS AND PERFORMANCE DATA

Response Time (t_{RESP})

The time interval between a) when the sensed input current reaches 90% of its full-scale value, and b) when the sensor output, V_{OUT}, reaches 90% of its full-scale output value.

Propagation Delay (t_{PD})

The time interval between a) when the sensed input current reaches 20% of its full-scale value, and b) when the sensor output, V_{OUT}, reaches 20% of its full-scale output value.

Rise Time (t_R)

The time interval between a) when the sensor output, V_{OUT}, reaches 10% of its full-scale value, and b) when the sensor output, V_{OUT}, reaches 90% of its full-scale value.

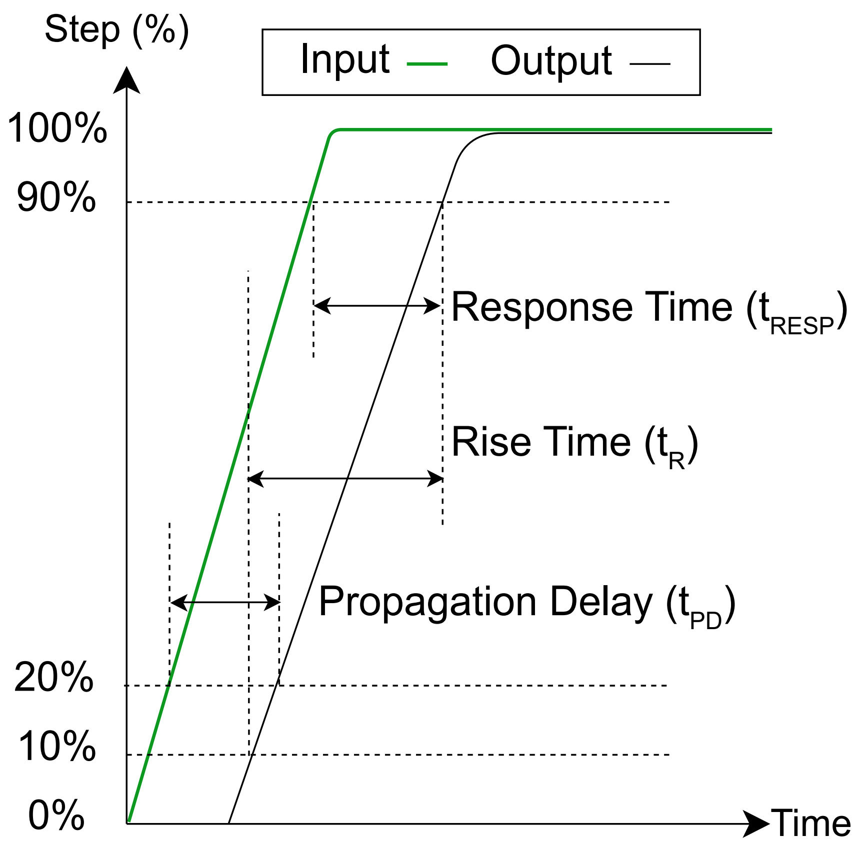


Figure 4: Step Response Characteristics

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

FUNCTIONAL DESCRIPTION OF POWER ON/OFF OPERATION

Introduction

The graphs in this section show the behavior of V_{OUT} as V_{DD} reaches or falls below the required power-on voltage. Figure 5 and ***Figure*** 6 use the same labeling convention for different voltage thresholds. References in brackets "[ ]" are valid for each of these graphs.

POWER-ON OPERATION

As V_{DD} ramps up, the VOUT pin is in a high-impedance (high-Z) state until V_{DD} reaches and passes V_{POR} [1]. Once V_{DD} has passed V_{POR} [1], V_{OUT} enters normal operation and starts responding to applied current, I_P.

POWER-OFF OPERATION

As V_{DD} drops below $V_{POR} – V_{POR\_HYS}$ the outputs enters a high-Z state. The hysteresis on the power-on voltage prevents noise on the supply line from causing V_{OUT} to repeatedly enter and exit the high-Z state around the V_{POR} level.

NOTE: Because the device is entering a high-Z state and not driving the output, the time it takes the output to reach a steady state depends on the external circuitry.

Voltage Thresholds

POWER-ON RESET RELEASE VOLTAGE (V_{POR})

If V_{DD} falls below $V_{POR} – V_{POR\_HYS}$ [2] while the sensor is in operation, the digital circuitry turns off and the output re-enters a high-Z state. After V_{DD} recovers and exceeds V_{POR} [1], the output enters normal operation after a delay of t_{PO}.

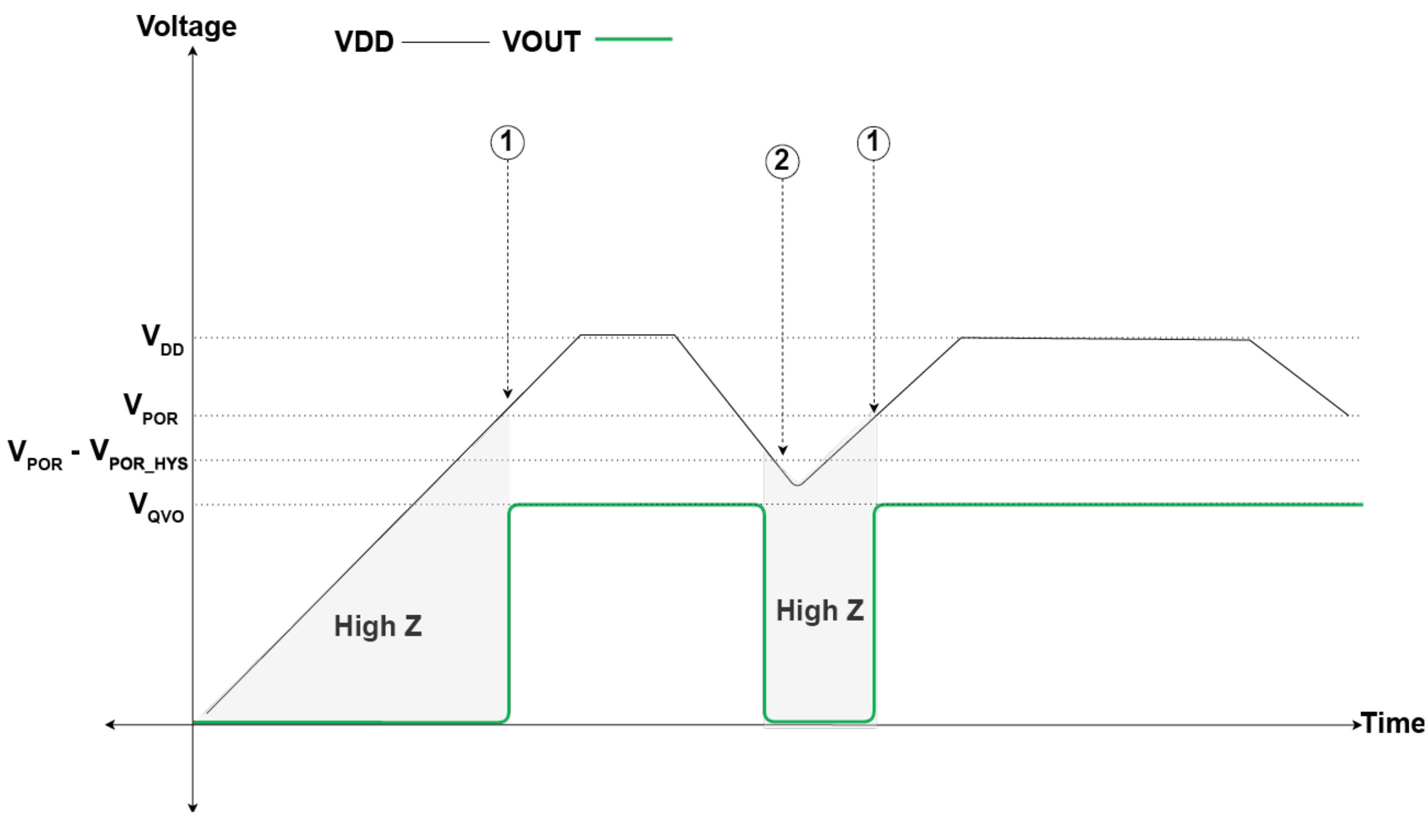


Figure 5: Power-On And Power-Off Operation

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Timing Thresholds

POWER-ON DELAY (t_{PO})

When the supply voltage reaches V_{POR} [1], the device requires a finite time to power its internal components before the outputs are released from the high-impedance state and start responding to the measured current, I_P. Power-On Time, t_{PO}, is defined as the time it takes for the output voltage to settle within ±10% of its steady-state value under an applied current, I_P, which can be seen as the time from [1] to [A] in Figure 6.

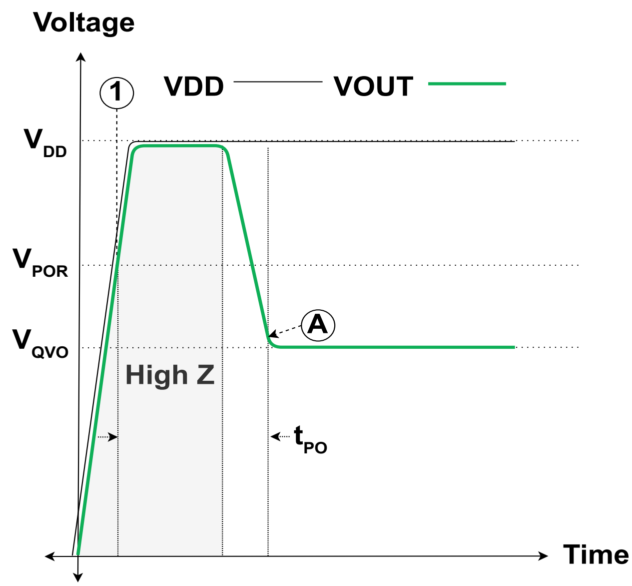


Figure 6: Power-On Delay, t_{PO}

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

DEFINITIONS OF OPERATING AND PERFORMANCE CHARACTERISTICS

Quiescent Voltage Output (V_{QVO})

Quiescent Voltage Output, V_{QVO}, is defined as the voltage on the output, V_{OUT}, when no current is applied, $I_P = 0$.

Quiescent Voltage Output Error (V_{QVO_E})

Quiescent Voltage Output Error, V_{QVO_E}, is defined as the deviation of V_{QVO} from the nominal target value in production testing.

Quiescent Voltage Output Temperature Drift (V_{QVO_T})

Quiescent Voltage Output Temperature Drift, V_{QVO_T}, is defined as the expected deviation of V_{QVO} from its value at T_A= 25°C over the temperature range T_A= –40 to 25°C and T_A= 25 to 125°C, based on observed three-sigma temperature drifts.

Output Saturation Voltage (V_{SAT_H} and V_{SAT_L})

Output Saturation Voltage, V_{SAT}, is defined as the low or high voltage that V_{OUT} does not exceed. V_{SAT_H} is the highest voltage the output can reach, while V_{SAT_L} is the lowest. Note that changing the sensitivity does not change the V_{SAT} points.

Sensitivity (Sens)

Sensitivity, or Sens, is defined as the ratio of the V_{OUT} swing and the current through the primary conductor, I_P. The current causes a voltage change on V_{OUT} away from V_{QVO} until V_{SAT}. The magnitude and direction of the output voltage is proportional to the magnitude and direction of the current, I_P. The proportional relationship between output voltage and current is Sensitivity, defined as:

$$Sens = \frac{V_{OUT(IP_1)} - V_{OUT(IP_2)}}{IP_1 - IP_2}$$

where I_{P1} and I_{P2} are two different currents, and $V_{OUT}(I_{P1})$ and $V_{OUT}(I_{P2})$ are the respective output voltages, at VOUT, at those currents.

Sensitivity Error (E_{SENS})

Sensitivity Error, E_{SENS}, is the deviation of Sensitivity from the nominal sensitivity target value in production testing.

Sensitivity Temperature Drift (E_{SENS_T})

Sensitivity Temperature Drift, E_{SENS_T}, is defined as the expected deviation of Sens from its value at T_A= 25°C over the temperature range T_A= –40 to 25°C and T_A= 25 to 125°C, based on observed three-sigma temperature drifts.

Power Supply Sensitivity Error (E_{SENS_PS})

Power Supply Sensitivity Error, E_{SENS_PS}, is defined as the percent change in Sens when V_{DD} varies within the specified test voltages.

Power Supply Offset Error (V_{OE_PS})

Power Supply Offset Error, V_{OE_PS}, is defined as the change in V_{QVO} when V_{DD} varies within the specified test voltages.

Noise Density (N_D)

Noise density, N_D, is the spectral density of noise, or the square root of noise power per square root hertz.

To calculate the A_{RMS} assuming a brick wall filter approximation, take the provided input noise density, N_D, and multiply it by the square root of the device or system bandwidth. Input-referred noise density helps to evaluate the sensor performance independent of its sensitivity. Refer to Figure 7 below for the average noise density of the ACS37041/2 device variants.

$$A_{RMS} = N_D * \sqrt{BW}$$

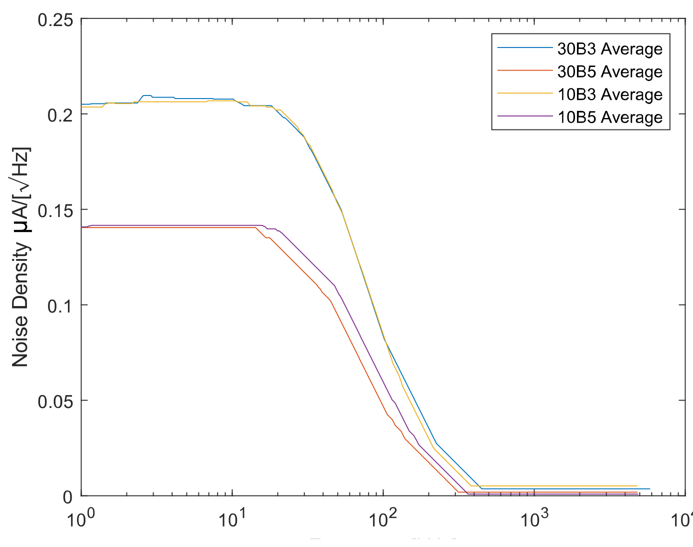


Figure 7: Average Noise Density

Noise (N)

Noise, N, is the output referred noise of the ACS37041/2. This is the total noise at the output of the sensor, and it includes noise sources within the sensor itself.

ALLEGRO microsystems
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

THERMAL PERFORMANCE

Thermal Rise vs. Primary Current

Resistive heating due to the flow of electrical current in the package should be considered during the thermal design of the application. The sensor, printed circuit board (PCB), and contacts to the PCB will generate heat and act as a heat sink.

The thermal response is highly dependent on PCB layout, copper thickness, cooling methods, and the profile of the injected current, including peak current, current on-time, and duty cycle.

Vias-in-pad help improve thermal performance. Placing vias under the copper pads of the current sensor reduces electrical resistance and improves heat conduction to the PCB, while vias outside of the pads limit the current path to the top of the PCB trace and have worse heatsinking under the part (see Figure 8 and Figure 9).

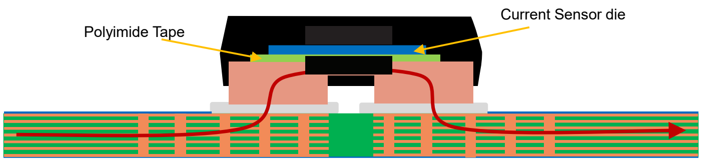


Figure 8: Via-In-Pad

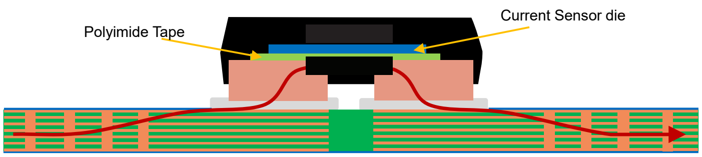


Figure 9: No Vias-In-Pad

Figure 10 shows the measured rise in steady-state die temperature of the ACS37041/2 versus DC continuous current at an ambient temperature, T_A, of 25°C for two board designs: filled vias under copper pads and no vias under copper pads.

Figure 11 shows the measured rise in steady-state die temperature of the ACS37041/2 versus DC continuous current at an ambient temperature of 25°C and 125°C.

The thermal capacity of the ACS37041/2 should be verified by the end user in the application specific conditions. The maximum junction temperature, $T_{J(max)}$ (165°C), should not be exceeded. Measuring the temperature of the top of the package is a close approximation of the die temperature.

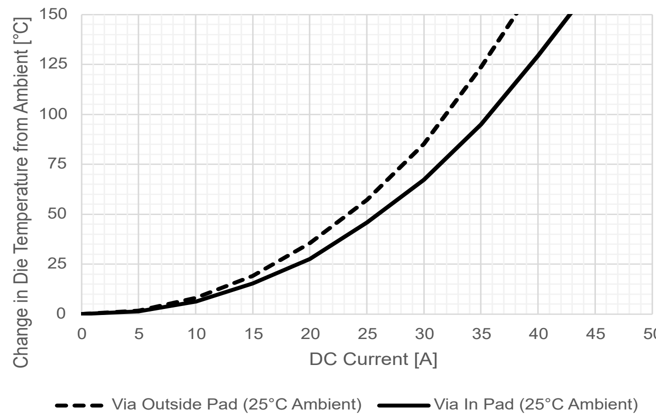


Figure 10: Comparison of die-temperature increase with and without in-pad vias at T_A = 25°C

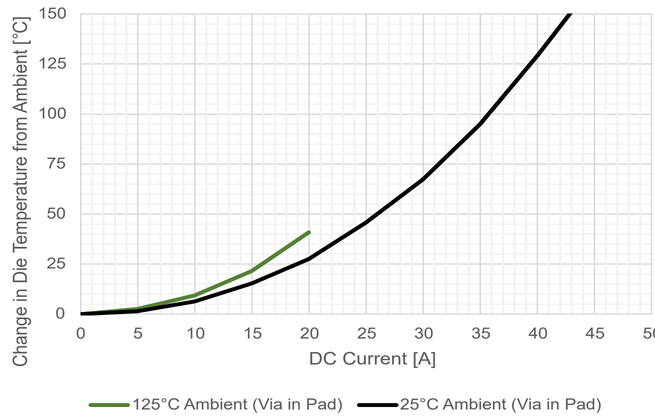


Figure 11: Comparison of die-temperature increase at T_A = 25°C and T_A = 125°C with vias-in-pad

Evaluation Board Layout

Thermal data was collected using the LH Current Sensor Evaluation Board (ACSEVB-LH5, TED-0004112) in Figure 12.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

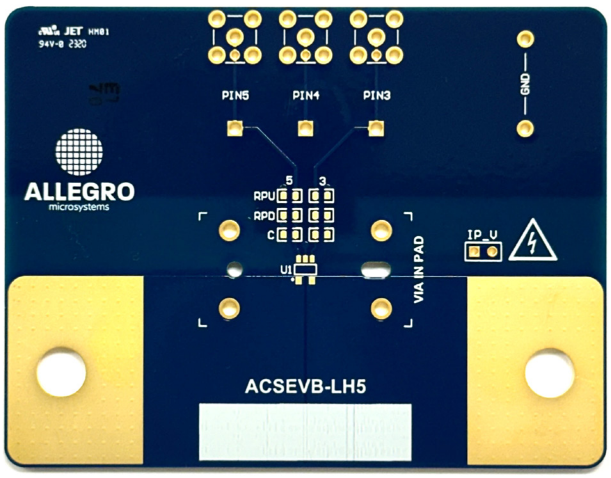


Figure 12: LH Package Allegro Evaluation Board

Design support files for the ACSEVB-LH5 evaluation board are available for download from the Allegro website. See the technical documents section of the ACS37041/2 website for more information.

CURRENT RANGE VS. TEMPERATURE

From –40°C to 25°C, there is a rating of up to 60 A for up to 200 ms, and from 25°C to 125°C, there is a rating of up to 60 A to 40 A for up to 200 ms with a derating slope of –0.2 A/°C. This range is a statement of allowable current excursions and on times during transient events such as over current events.

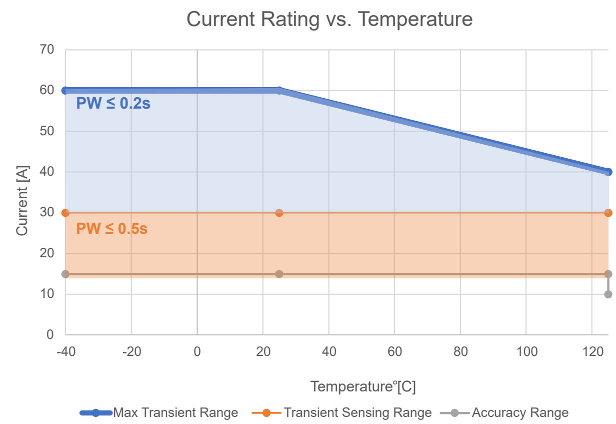


Figure 13: Current Ratings vs. Temperature

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

I_P POWER DISSIPATION OUTPUT DRIFT

Introduction

Power dissipation in very small packages creates challenges for integrated conductor current sensing devices. The ACS37041/2 is in a small, custom SOT23 package designed to minimize the effect of heating due to applied current on the accuracy of the measurement. However, higher applied currents can cause small thermal gradients across the die, which can create a small offset shift. It is important for the system integrator to understand this effect when designing a system using the ACS37041/2.

I_P power-dissipation is the heat generated by the ohmic loss in the integrated primary conductor (I_P) when current is applied. The heat generated by the internal conductor spreads through the package unevenly, and induces a thermal gradient across the die. A gradient of temperature across the circuitry creates mismatch resulting in a change in the signal path performance. The generation of the thermal gradient is not instantaneous. The offset error of the device due to IP power dissipation will both depend on the time the current is applied and the square of the current applied. The effect is independent of the direction of the applied current.

Characteristics of the I_P Power Dissipation Output Drift

POSITIVE APPLIED CURRENT

Figure 17 to Figure 19 shows the ACS37041/2 I_P power dissipation output drift during and after a positive current step is applied to the device.

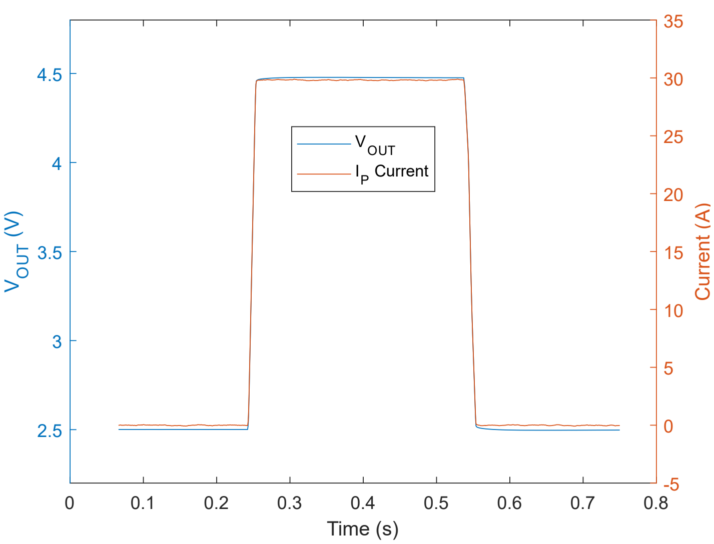


Figure 17: Positive I_P Pulse, I_P Power Dissipation Output Drift

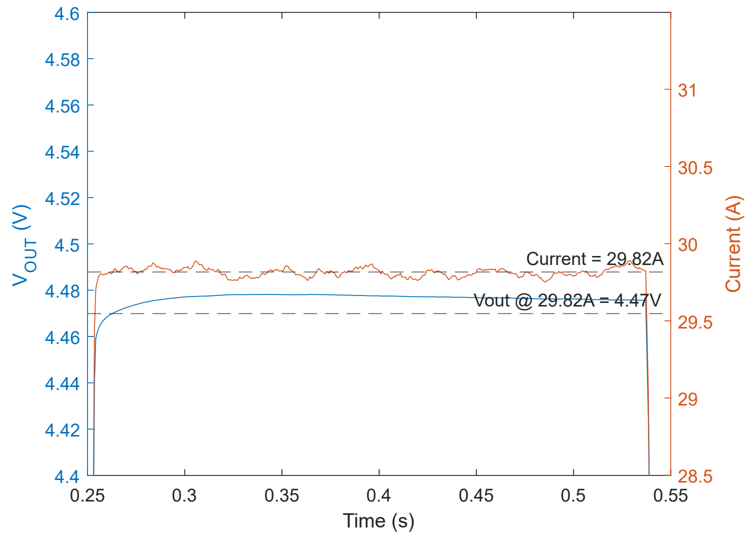


Figure 18: Positive I_P Pulse, I_P Power Dissipation Output Drift During Applied Step

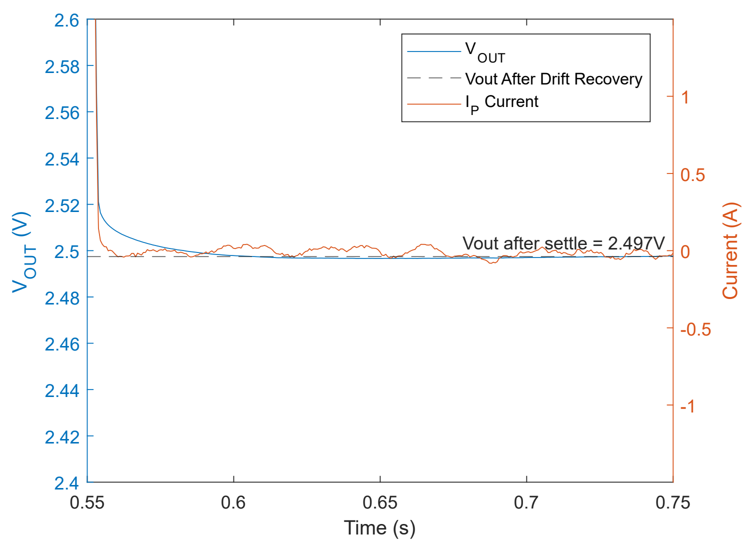


Figure 19: Positive I_P Pulse, I_P Power Dissipation Output Drift After Applied Step

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

IP POWER DISSIPATION OUTPUT DRIFT

NEGATIVE APPLIED CURRENT

Figure 20 to Figure 22 shows the ACS37041/2 I_P power dissipation output drift during and after a positive current step is applied to the device.

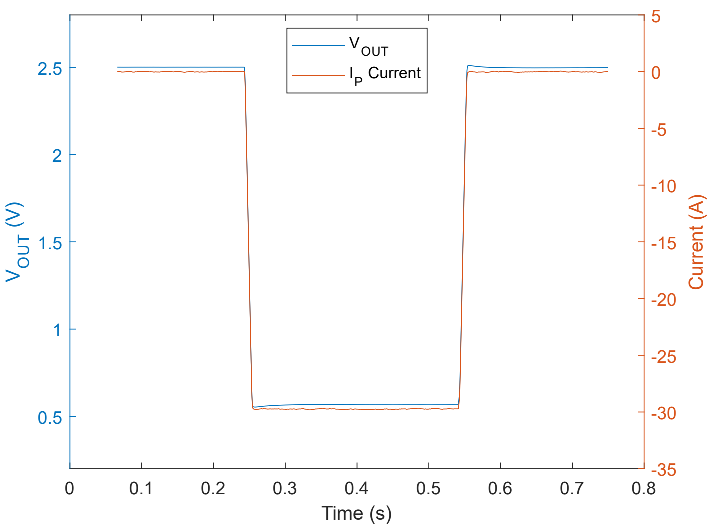


Figure 20: Negative I_P Pulse, I_P Power Dissipation Output Drift

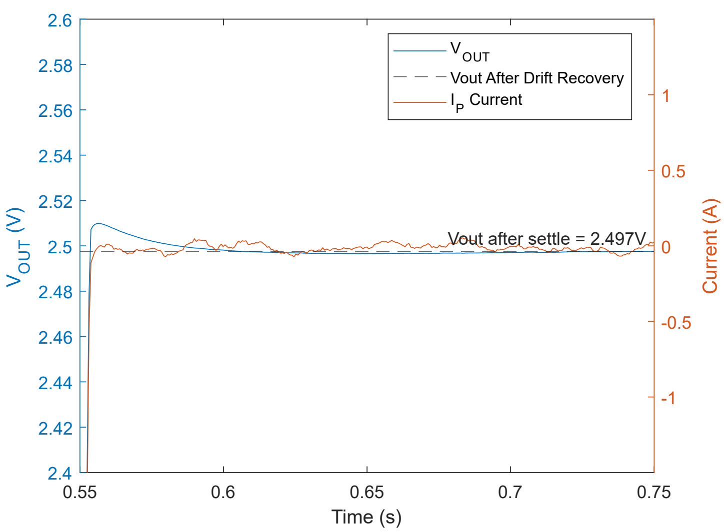


Figure 21: Negative I_P Pulse, I_P Power Dissipation Output Drift During Applied Step

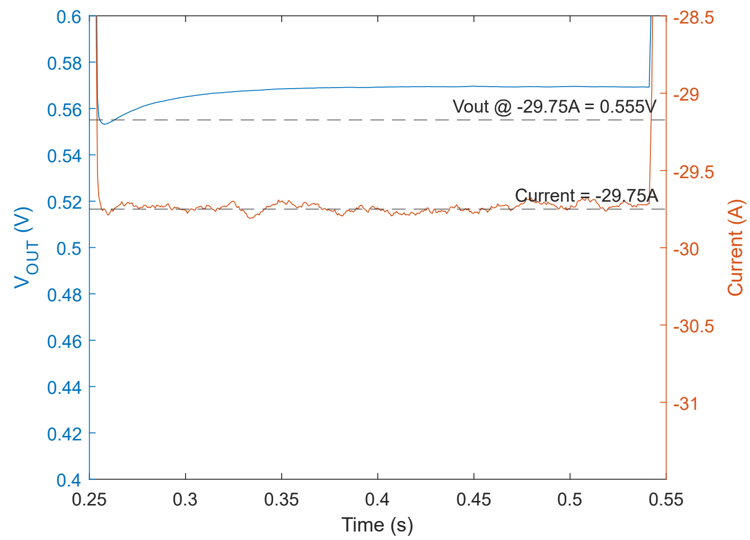


Figure 22: Negative I_P Pulse, I_P Power Dissipation Output Drift After Applied Step

I_P Power Dissipation Output Drift Description

The impact of the thermal gradient on the circuit is to create an offset in the front-end amplifier. Because the drift occurs before any amplification, the signal path gain affects the amount of mV of error seen at the output due to this heating effect, but it is consistent in mA error when input referred. Values in this document are input referred. To determine the effect on a specific ACS37041/2 variant, adjust the error reported by the gain of the sensor.

As the ambient temperature increases, the I_P power dissipation drift also increases. This is due to the fact that the internal conductor is copper and changes resistance over temperature. Additionally, the thermal transmissivity of the integrated conductor, solder, and PCB pads decrease over temperature so the system takes more time to reach a steady state at higher temperatures.

Recommended Use Cases

For the accuracy specifications in the performance characteristics table, it is recommended to use the ACS3704/2 for systems with steady state current operation below 15 A. While the ACS37041/2 can measure currents up to 30 A, it is recommended to keep currents over 15 A to short transients of < 1 second.

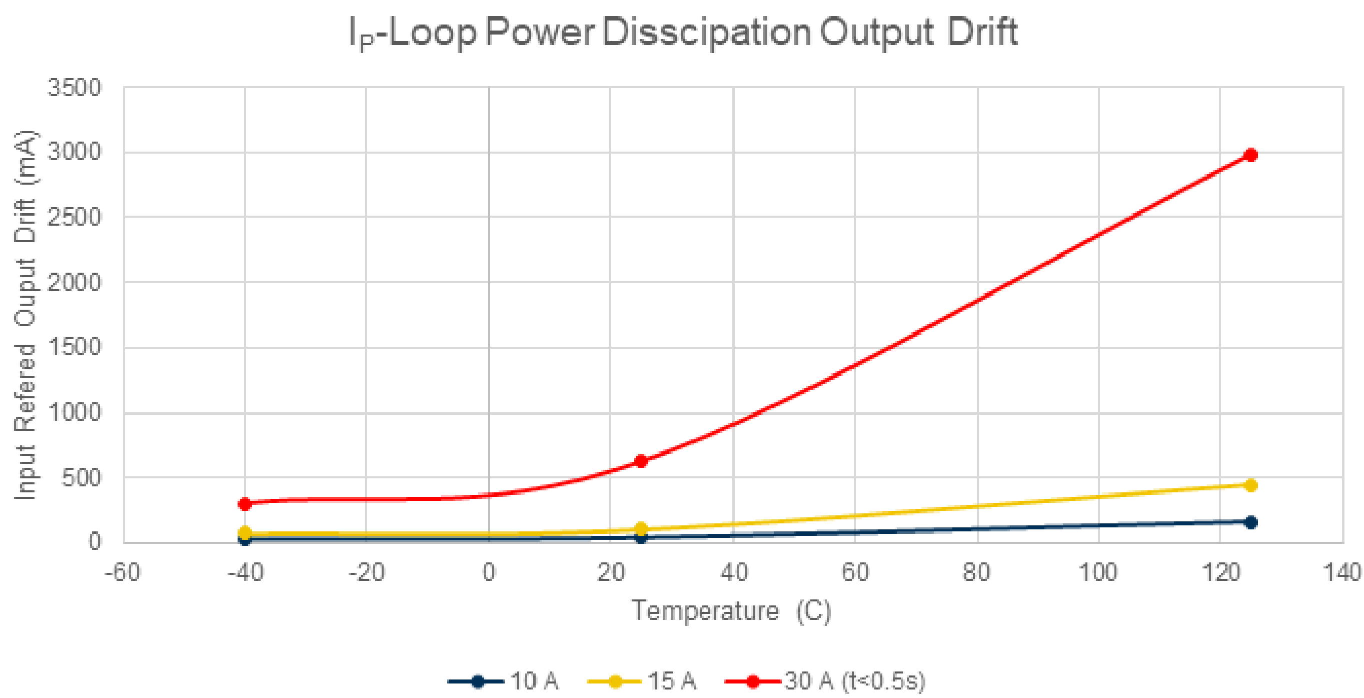


Figure 23: Power Dissipation Output Drift Over Temperature

I_P Power Dissipation Output Drift Specifications

The power loss, $P = I^2R$, generates the heat and aligns with exponential relationship between output drift dependance of applied current at a specific temperature. The numbers provided in Table 1 are the worst case measurements taken on 10 devices during bench characterization; the drift behavior was isolated from other sources of error. The ambient temperature affects the integrated current loop resistance aligning with this data showing a scaling effect over temperature (refer to Figure 23). The systems ability to manage this heat is critical to the outcome of these results and includes the device and PCB design. In the case of 10 and 15 A of applied current the system is able to reach a thermal equilibrium across all temperatures, keeping this behavior contained below 3% of the input signal. The 30 A case however, is beyond they systems capability to contain the behavior especially at higher temperatures leading to output drift nearly 10% of the input signal even with a shorter on time.

PCB layout will affect the overall system performance in terms of magnitude and time scales of the I_P power dissipation output drift. Please refer to the "Thermal Performance" on page 14 for more information.

Note: Any thermal gradient across the device can create similar behavior to I_P power dissipation output drift with the direction being dependant on the direction of temperature gradient across the die.

Table 1: I_P Power Dissipation Output Drift Summary

Current [A]	Step Duration [s]	Temperature			Offset (Input Referred)
		–40°C	25°C	125°C	
10	1.5	35	45	165	mA
15	1.5	80	115	450	mA
30	0.5	310	650	2990	mA

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PACKAGE OUTLINE DRAWING

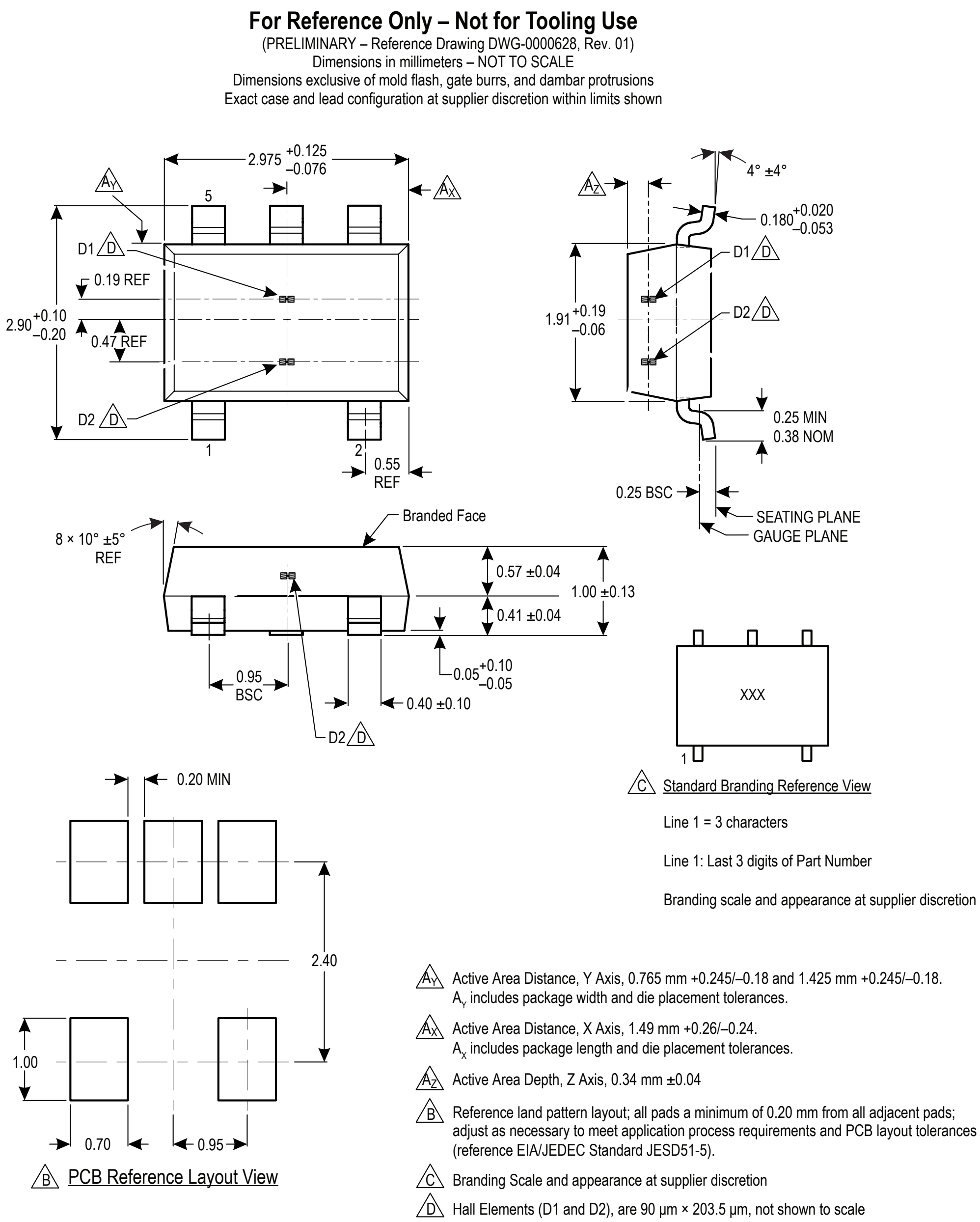


Figure 24: ACS37041 LH 5-Pin SOT23W Package Drawing

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Revision History

Number	Date	Description
–	November 1, 2024	Initial release

For the latest version of this document, visit our website:

www.allegromicro.com

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com