A8509

Wide Input Voltage Range, High Efficiency 4-Channel Fault Tolerant LED Driver

Discontinued Product

These parts are no longer in production The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: September 30, 2024

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, refer to the A80604KESJSR.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

A8509

Wide Input Voltage Range, High Efficiency 4-Channel Fault Tolerant LED Driver

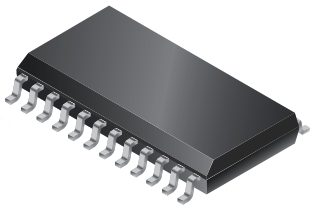
FEATURES AND BENEFITS

- Four integrated high current sinks for LED strings; can be tied together for even higher currents
- Fixed frequency current mode control with integrated gate driver / boost controller; powerful gate driver to drive an external N-channel MOSFET allows significant scaling capability on the number of LEDs per string
- Parallel operation with one boost controller (master) and up to three additional slave controllers; can run up to 16 strings of LEDs while populating only a single master boost regulator
- Active current sharing between LED strings for 0.7% accuracy and 0.8% matching
- Wide input voltage range: 9 to 40 V
- Internal bias supply for single-supply operation (typically V_{IN} = 12 or 24 V)
- Separate Enable and PWM pins as interface for Enable and PWM Dimming functions
- FSET / SYNC function to either set the boost converter switching frequency or synchronize at up to 800 kHz
- Protection Features
  - Open or shorted LED pin protection
  - Open Schottky protection
  - Pulse-by-pulse current limit
  - Overtemperature protection (OTP)

PACKAGES

(Not to scale)

24-pin TSSOP with Exposed Thermal Pad (LP package)



24-pin SOICW with Four Internally-Fused Pins (LB package)

DESCRIPTION

The A8509 is a multi-output white LED driver for backlighting LCD panels. It integrates a current-mode boost controller and four individual current sinks.

The boost controller architecture allows for significant scaling of boost voltage to optimize the solution for the required number of LEDs per string. The FSET/SYNC pin either sets the required boost switching frequency or synchronizes the value in the range of 300 to 800 kHz.

The LED sink current value is set by an external ISET resistor (see figure 1). The four LED sinks can also be combined to achieve even higher current per LED string.

The A8509 provides protection against output shorts and overvoltage, open or shorted LED pins, and overtemperature. A dual-level, pulse-by-pulse current limit function provides soft-start and protects the external current switch against high current overloads. As an option, the A8509 can drive an external P-FET interfaced to the $\overline{\text{FAULT}}$ pin to disconnect the input supply from the system in the event of short-to-ground in the boost converter.

Package options are 24-pin TSSOP (suffix LP) and SOICW (LB) packages. The TSSOP has an exposed thermal pad, and the SOICW has four internally fused pins, for enhanced thermal dissipation. Both packages are lead (Pb) free, with 100% matte tin leadframe plating.

Typical Application

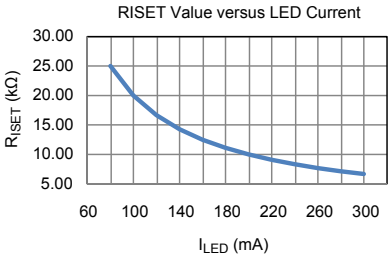
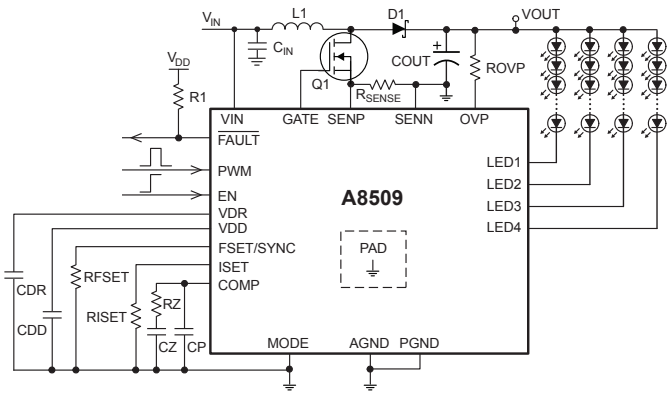


Figure 1. Typical application circuit showing 4 channels of LEDs; RZ-CZ optional (component list shown in the Typical Applications section)



SELECTION GUIDE

Part Number	Package	Packing [1]
A8509GLPTR-T	24-pin TSSOP with exposed thermal pad	4000 pieces per 13-in. reel
A8509GLBTR-T [2]	24-pin SOICW with internally fused leads	Contact Allegro

[1] Contact Allegro for additional packing options.
[2] Contact Allegro for availability.

ABSOLUTE MAXIMUM RATINGS*

Characteristic	Symbol	Notes	Rating	Unit
LEDx Pin Voltage	V_{LEDx}		–0.3 to 55	V
OVP Pin Voltage	V_{OVP}		–0.3 to 60	V
VIN Pin Voltage	V_{IN}		–0.3 to 40	V
$\overline{FAULT}$ Pin Voltage	V_{FAULT}		–0.3 to 40	V
COMP, EN, FSET/SYNC, ISET, MODE, PWM, SENN, SENP, and VDD Pin Voltage	–		–0.3 to 5.5	V
GATE, VDR Pin Voltage	–		–0.3 to 8	V
Operating Ambient Temperature	T_A	G temperature range	–40 to 105	°C
Maximum Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

*Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Package LP, on 4-layer PCB based on JEDEC standard	28	°C/W
		Package LB, on 4-layer PCB based on JEDEC standard	35	°C/W

*Additional thermal information available on the Allegro website.

Table of Contents

Specifications 2
Functional Block Diagram 3
Pin-out Diagram and Terminal List 4
Electrical Characteristics Table 5
Functional Description 8
Enabling the IC 8
Powering up: LED pin short-to-GND check 8
Soft-start function 9
Frequency selection 10
Synchronization 10
LED current setting and LED dimming 11
PWM dimming 12
Analog dimming 12
Boost switch overcurrent protection 13
Setting the current sense resistor 13
Current sense resistor routing 13
Pulse-by-pulse current limit 14
Secondary boost switch limit 14
Output overvoltage and undervoltage protection 14
LED Open Detect 15
Undervoltage Protection (UVP) 15
LED short detect 16
Input UVLO 16
VDD and VDR 16
Shutdown 17
Fault protection during operation 17
Application Information 19
Paralleling more than one A8509 19
Design Example 21
Typical Applications 24
Typical Applications 25
Package Drawings 27

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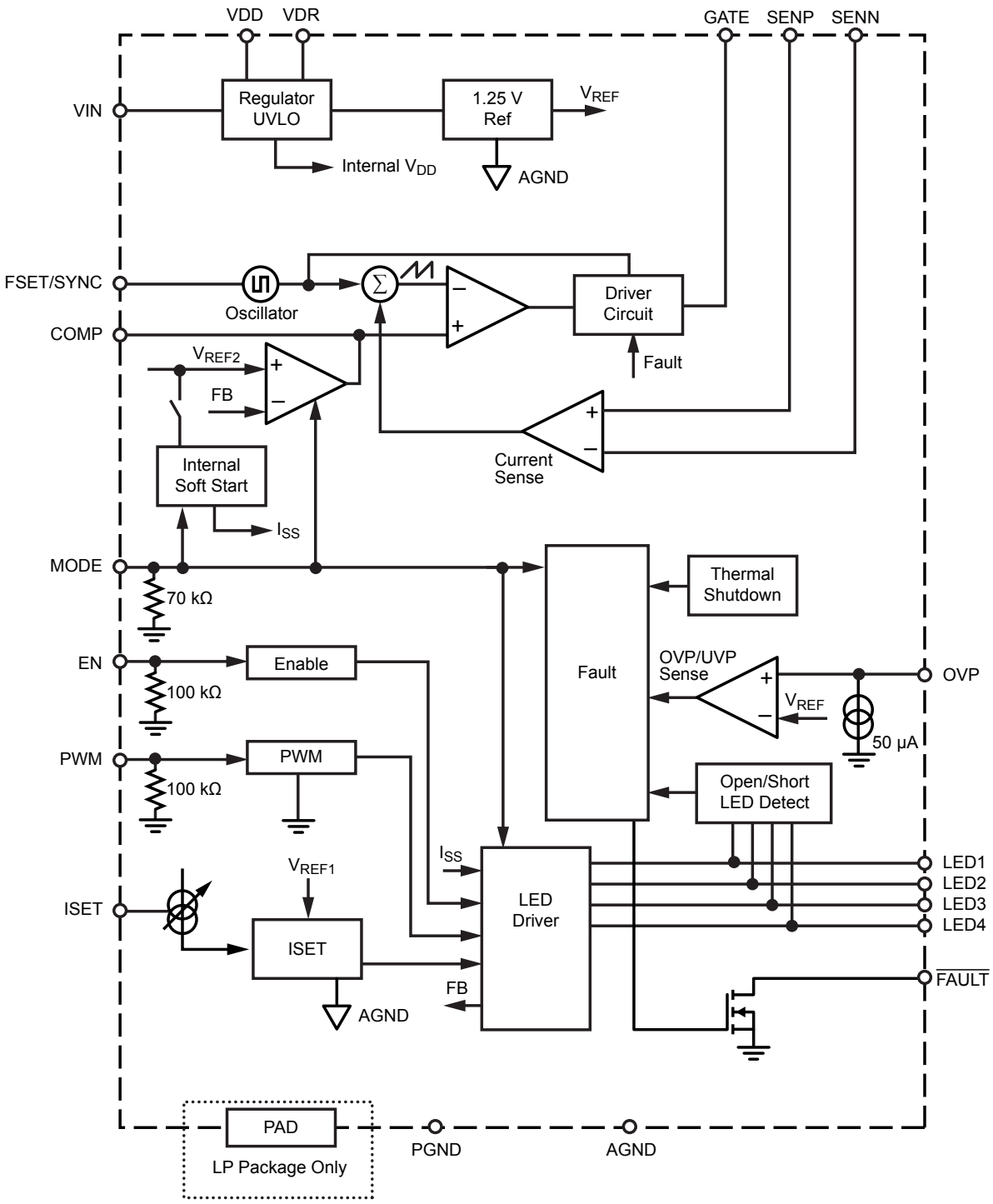
FUNCTIONAL BLOCK DIAGRAM



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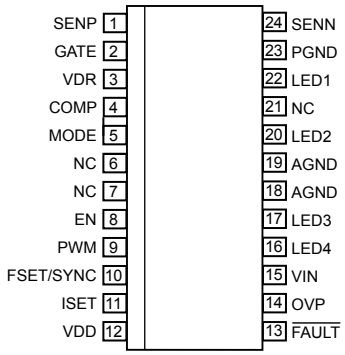
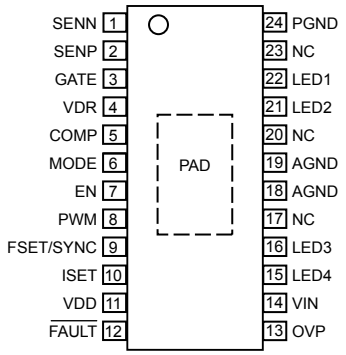
Pinout Diagrams



LB Package



LP Package

Terminal List Table

Name	Number		Function
	LB	LP	
AGND	18, 19	18, 19	LED ground.
COMP	4	5	Output of the error amplifier and compensation node. Connect a compensation network from this pin to ground.
EN	8	7	Enable for the A8509.
$\overline{\text{FAULT}}$	13	12	This pin is used to indicate a fault condition. Connect a pull-up resistor between this pin and the required logic level voltage. The pin is an open drain type configuration that will be pulled low when a fault occurs.
FSET/SYNC	10	9	Frequency/synchronization pin. A resistor RFSET from this pin to ground sets the switching frequency. This pin can also be used to synchronize two or more converters in the system.
GATE	2	3	Gate pin for driving external N-channel FET.
ISET	11	10	Connect the RISET resistor between this pin and ground to set the 100% LED current.
LED1 LED2 LED3 LED4	22 20 17 16	22 21 16 15	Connect the cathode of each LED string to these pins.
MODE	5	6	This pin is used to determine the mode of operation. MODE high tied to VDD allows parallel operation, and MODE low is used for single IC operation.
NC	6, 7, 21	17, 20, 23	No connection.
OVP	14	13	This pin is used to sense an Overvoltage (OVP) condition. Connect the ROVP resistor from VOUT to this pin to adjust the overvoltage protection.
PAD	n/a	–	For TSSOP package, this exposed pad provides enhanced thermal dissipation. This pad must be connected to the ground plane(s) of the PCB with at least 8 vias, directly in the PAD solder pad.
PGND	23	24	Power ground for the internal gate driver circuit.
PWM	9	8	PWM dimming pin. Used to control the LED intensity by using pulse width modulation. The typical PWM dimming frequency is in the range of 100 to 1000 Hz.
SENN	24	1	Negative sense line for boost switch current sensing.
SENP	1	2	Positive sense line for boost switch current sensing.
VDD	12	11	Output of internal LDO regulator. Connect a 0.1 µF decoupling capacitor between this pin and ground.
VDR	3	4	Output of the gate driver bias voltage regulator. Connect a 1 µF decoupling capacitor between this pin and ground.
VIN	15	14	Input power to the A8509.

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ELECTRICAL CHARACTERISTICS [1]: Valid at V_{IN} = 12 V, T_A = 25°C, • indicates specifications guaranteed by design and characterization over the full operating temperature range with $T_A = T_J$ = –40°C to 105°C; unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
INPUT VOLTAGE SPECIFICATIONS							
Operating Input Voltage Range	V_{IN}		•	9	–	40	V
UVLO Start Threshold	$V_{UVLO(th)}$	V_{IN} rising	•	–	–	8.5	V
UVLO Hysteresis	$V_{UVLO(hys)}$	V_{IN} falling		–	400	–	mV
INPUT CURRENTS							
Input Quiescent Current	I_Q	EN = V_{IH}; f_{SW} = 800 kHz, no load		–	7	–	mA
Input Sleep Supply Current	I_{QSLEEP}	V_{IN} = 12 V, EN = FSET/SYNC = 0 V	•	–	0.5	10.0	µA
INPUT LOGIC LEVELS (EN, PWM, MODE, FSET/SYNC)							
Input Logic Level – Low	V_{IL}	9 V < V_{IN} < 40 V	•	–	–	400	mV
Input Logic Level – High	V_{IH}	9 V < V_{IN} < 40 V	•	1.5	–	–	V
EN, PWM Pins Pull-Down Resistor	$R_{pulldown}$	EN, PWM = 5 V		–	100	–	kΩ
MODE Pin Pull-Down Resistor	R_{MODE}	MODE=2.5 V		–	70	–	kΩ
ERROR AMPLIFIER							
Open Loop Voltage Gain	A_{VOL}			–	47	–	dB
Transconductance	g_m	ΔI_{COMP} = ±10 µA		–	990	–	µA/V
Source Current	$I_{EA(SRC)}$	V_{COMP} = 1.5 V		–	–360	–	µA
Sink Current MODE High	$I_{EA(SINK)H}$	V_{COMP} = 1.5 V, MODE = V_{IH}		–	80	–	µA
Sink Current MODE Low	$I_{EA(SINK)L}$	V_{COMP} = 1.5 V, MODE = V_{IL}		–	360	–	µA
COMP Pin Pull-Down Resistor	R_{COMP}	$\overline{FAULT}$ = 0		–	1.5	–	kΩ
Soft-Start COMP Level	V_{COMPSS}			–	200	–	mV
OVERVOLTAGE PROTECTION							
Overvoltage Threshold	$V_{OVP(th)}$	OVP connected to VOUT	•	1.11	1.25	1.4	V
OVP Sense Current	I_{OVPH}		•	45	49	53	µA
Output Undervoltage Threshold	$V_{UVP(LOW)}$	Falling		–	100	–	mV
	$V_{UVP(HIGH)}$	Rising		–	120	–	mV
BOOST SWITCH GATE DRIVER							
Gate Driver Voltage	V_{DRV}	Measured at GATE pin		–	7	–	V
Driver Pull-Up and Pull-Down Resistance	R_{GATEUD}	Measured at V_{GATE} =V_{DRV} / 2		–	4.5	–	Ω
Driver to Ground Resistance	R_{GATEG}	EN = 0, VIN = 0		–	200	–	kΩ
Sense Positive	V_{SENSEP}		•	85	100	115	mV
Secondary Sense Positive	$V_{SENSESEC}$			–	165	–	mV

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Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
BOOST SWITCH GATE DRIVER (continued)							
Soft-Start Boost Current Limit Reference Voltage	$V_{SWSS(LIM)}$	Reference voltage for boost switch current limit during soft-start		–	39	–	mV
Minimum Switch On-Time	$t_{SWONTIME}$			–	–	110	ns
Minimum Switch Off-Time	$t_{SWOFFTIME}$			–	–	85	ns
OSCILLATOR FREQUENCY							
Oscillator Frequency	f_{SW}	R_{FSET} = 7.5 kΩ	•	725	800	875	kHz
		R_{FSET} = 10 kΩ	•	540	600	660	kHz
		R_{FSET} = 20 kΩ		–	300	–	kHz
FSET/SYNC Pin Voltage	V_{FSET}	R_{FSET} = 8.25 kΩ		–	1.00	–	V
SYNCHRONIZATION							
Synchronized PWM Frequency	f_{SWSYNC}		•	300	–	800	kHz
Synchronization Input Minimum Off-Time	$t_{PWSYNCOFF}$		•	150	–	–	ns
Synchronization Input Minimum On-Time	$t_{PWSYNCON}$		•	150	–	–	ns
LED CURRENT SINKS							
LEDx Accuracy	Err_{LED}	I_{SET} = 80 µA		–	0.7	–	%
LEDx Matching	ΔLEDx	I_{SET} = 80 µA		–	0.8	2.5	%
LEDx Regulation Voltage	V_{LED}	V_{LED1} through V_{LED4} all equal, I_{SET} = 80 µA		–	650	–	mV
I_{SET} to I_{LEDx} Current Gain	A_{ISET}	I_{SET} = 80 µA		–	2320	–	A/A
ISET Pin Voltage	V_{ISET}			–	1.000	–	V
Allowable ISET Current	I_{SET}		•	34	–	130	µA
LEDx Pin Short Detect	V_{LEDSC}	While LED sinks are in regulation, sensed from LEDx pin to GND	•	4.6	–	–	V
Soft-Start LEDx Current Gain	I_{LEDSS}	Current through each enabled LEDx pin during soft-start, R_{ISET} = 12.4 kΩ		–	88	–	A/A
PWM High to LED-On Delay	$t_{dPWM(on)}$	Time between PWM enable and LEDx current reaching 90% of maximum	•	–	0.5	1.1	µs
PWM Low to LED-Off Delay	$t_{dPWM(off)}$	Time between PWM enable going low and LEDx current reaching 10% of maximum	•	–	–	500	ns

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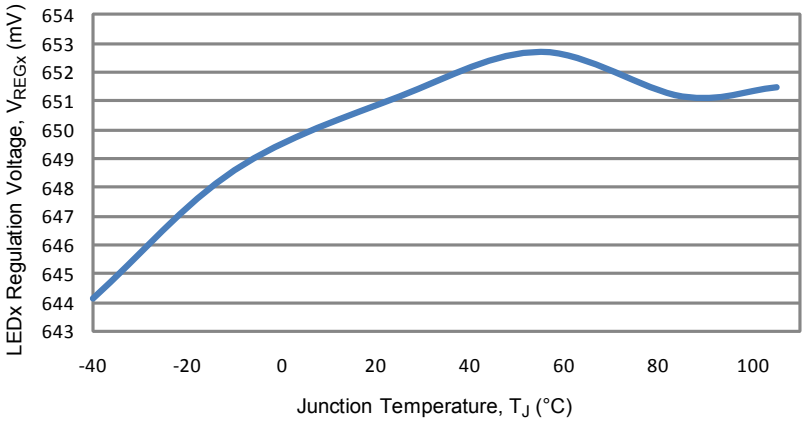
Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
$\overline{\text{FAULT}}$ PIN							
$\overline{\text{FAULT}}$ Pin Pull-Down Voltage	V_{FAULT}	I_{FAULT} = 1 mA (400 Ω internal switch resistance)		–	0.4	–	V
$\overline{\text{FAULT}}$ Pin Leakage Current	$I_{FAULTLKG}$	V_{FAULT} = 5 V	•	–	–	1	µA
THERMAL PROTECTION (TSD)							
Thermal Shutdown Threshold [2]	T_{SD}	Temperature rising		–	165	–	°C
Thermal Shutdown Hysteresis [2]	T_{SDHYS}			–	20	–	°C

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).

[2] Ensured by design and characterization, not production tested.



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FUNCTIONAL DESCRIPTION

Enabling the IC

The IC turns on when a logic high signal is applied on the EN pin, and the input voltage present on the VIN pin is greater than the 8.5 V necessary to clear the UVLO ($V_{UVLOrise}$) threshold. Before the LEDs are enabled, the A8509 driver goes through a system check to determine if there are any possible fault conditions that might prevent the system from functioning correctly.

Powering Op: LED Pin short-to-GND Check

After the VIN pin goes above the UVLO threshold, and a high signal is present on the EN pin, the IC proceeds to check if any LEDx pins are shorted to GND and/or are not used. Each unused pin should be connected to GND with a 2.4 kΩ pull-down resistor.

After the voltage threshold on the LEDx pins exceeds 120 mV, a timer of 1536 clock cycles (2 ms at 800 kHz switching frequency, see figure 2) is applied during which the A8509 determines the status of the pins. Any unused pin connected to GND with the pull-down resistor will be taken out of regulation at this point and will not contribute to the boost regulation loop (see figure 3). A typical example is shown in figure 4. When a pin is connected to GND through a 2.4 kΩ resistor, the voltage on that LEDx pin during the LED detection period is about 200 mV. This is shown in figure 2.

If an LEDx pin is shorted to ground such that LEDx pin voltage is < 100 mV, the A8509 will not proceed with soft-start until the short is removed from the LEDx pin. This prevents the A8509

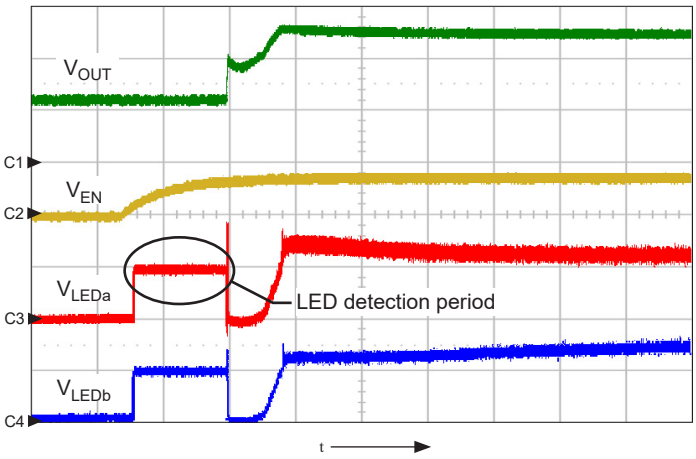

Figure 2. LED detect circuit operation for two connected LEDs at f_{SW} = 800 kHz; shows V_{OUT} (ch1, 10 V/div.), V_{EN} (ch2, 5 V/div.), an LEDx, V_{LEDa} (ch3, 500 mV/div.), another LEDx, V_{LEDb} (ch4, 500 mV/div.), t = 2 ms/div.

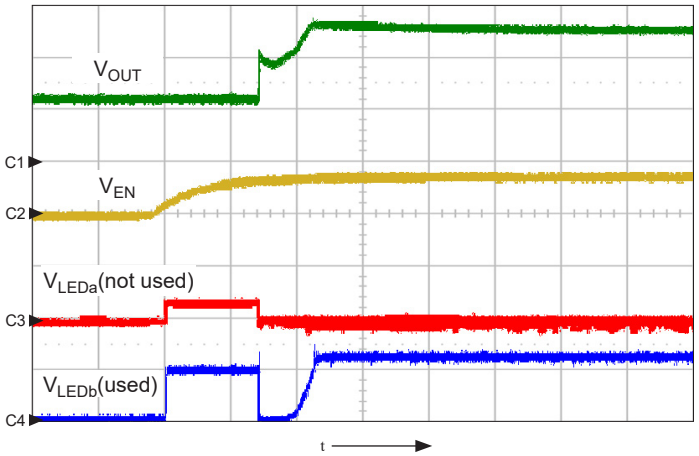

Figure 3. LED detect circuit operation for an LED pin that is not being used; shows V_{OUT} (ch1, 10 V/div.), V_{EN} (ch2, 5 V/div.), an unused LEDx with a 2.4 kΩ resistor from this pin to GND, V_{LEDa} (ch3, 500 mV/div.), and a used LEDx, V_{LEDb} (ch4, 500 mV/div.), t = 2 ms/div.

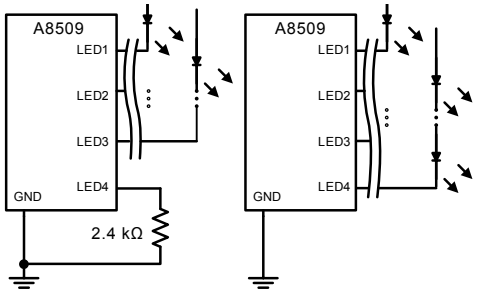

Figure 4. Channel select setup: (left) channel LED4 not used, (right) using all channels.

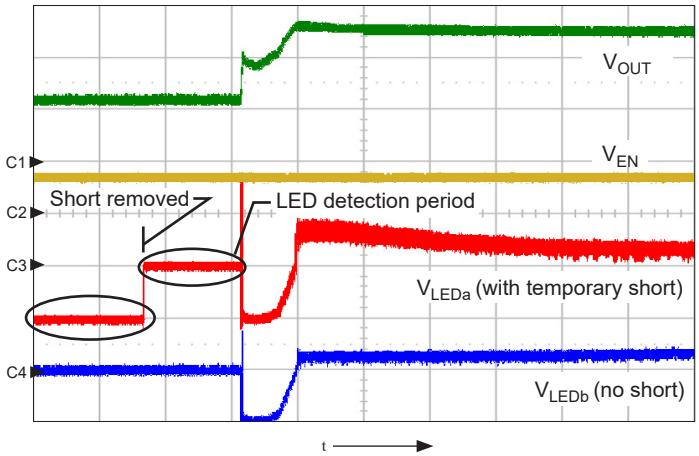

Figure 5. LED detect circuit operation: device powers-up after the short is removed from the LED pin; shows V_{OUT} (ch1, 10 V/div.), V_{EN} (ch2, 5 V/ div.), an LEDx with short, V_{LEDa} (ch3, 500 mV/div.), and an LEDx without short, V_{LEDb} (ch4, 500 mV/div.), t = 2 ms/div.

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from powering-up and putting an uncontrolled amount of current through the LEDs. After the short is removed the affected LEDx pin will rise up to the 500 mV level. When the LEDx pin voltage exceeds the 260 mV threshold, the IC detects connected LEDs and proceeds with LED detection and soft-start. Figure 2 shows a case when two LED channels are enabled. During the LED detection period, voltage on both LEDx pins > 260 mV. Figure 5 shows a case with LEDa temporarily shorted to ground and LEDb in normal operation.

Soft-Start Function

During soft-start, the LED current gain is reduced to (I_{LEDSS}). As an example, for a 240 mA output current, the soft-start LED current would be set to about 9 mA (see figure 7). Also during soft-start the boost switch sense voltage is reduced to the $V_{SWSS(LIM)}$ level, to limit the initial inrush current generated by the charging of the output capacitors. The actual current limit (I_{LIM}) is equal to:

$$I_{LIM} = V_{SWSS(LIM)} / R_{SENSE} \quad (1)$$

where $V_{SWSS(LIM)}$ is found in the Electrical Characteristics table, and R_{SENSE} is the current sense resistor value.

When the converter senses that there is enough voltage on the LEDx pins, the converter proceeds to increase the LED current to the preset regulation current and the boost switch current sense voltage limit is switched to the $I_{SW(LIM)}$ level to allow the A8509 to deliver the necessary output power to the LEDs (figure 8).

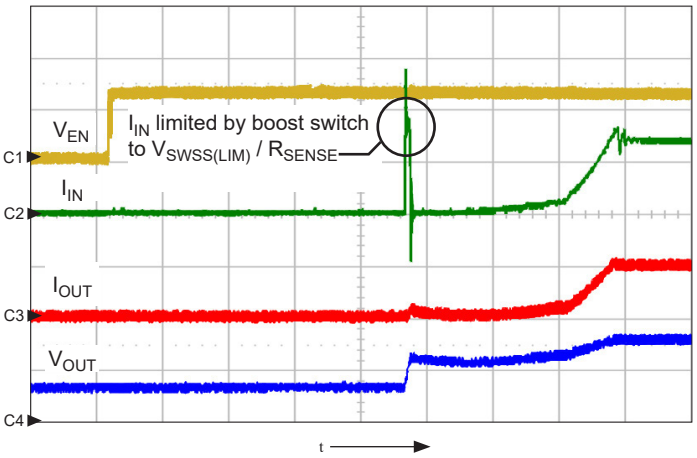

Figure 7. Start-up operation, individual LEDx current = 240 mA, boost sense resistor = 0.010 Ω; shows V_{EN} (ch1, 2 V/div.), I_{IN} (ch2, 2 A/div.), I_{OUT} (ch3, 1 A/div.), and V_{OUT} (ch4, 20 V/div.), t = 500 µs/div.

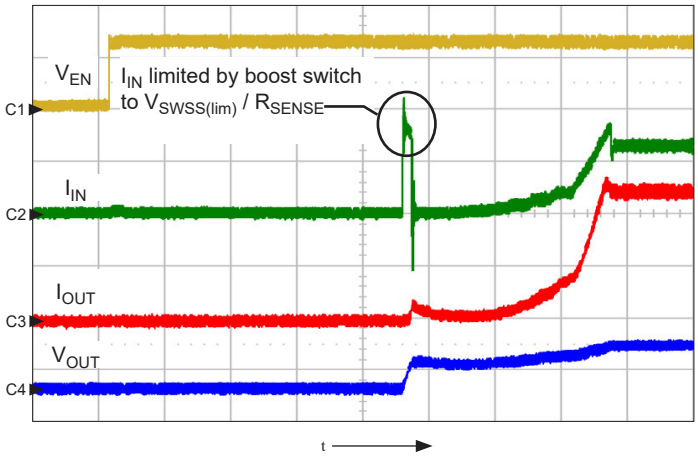

Figure 6. Start-up operation, individual LEDx current = 120 mA, boost sense resistor = 0.020 Ω; shows V_{EN} (ch1, 2 V/div.), I_{IN} (ch2, 1 A/div.), I_{OUT} (ch3, 200 mA/div.), and V_{OUT} (ch4, 20 V/div.), t = 500 µs/div.

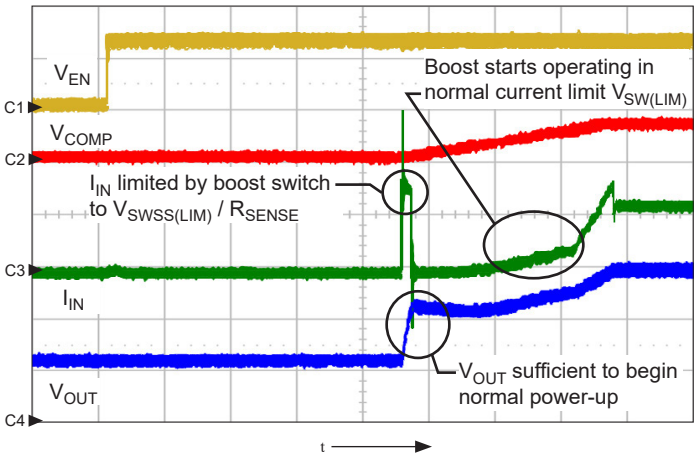

Figure 8. Normal start-up behavior; shows VEN (ch1, 2 V/div.), V_{COMP} (ch2, 2 V/div.), I_{IN} (ch3, 1 V/div.), and V_{OUT} (ch4, 10 V/div.), t = 500 µs/div.

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Frequency Selection

The switching frequency on the boost regulator is set by connecting a resistor between the FSET/SYNC pin and ground. The switching frequency range is 300 to 800 kHz, with example values of:

R_{FSET} Value (kΩ)	Switching Frequency, f_{SW} (kHz)
7.5	800
10	600

The relationship of R_{FSET} and f_{SW} is shown in figure 9.

The FSET/SYNC pin has short-to-ground protection. If the FSET/SYNC pin is held low for more than 4 µs typical, the A8509 will stop switching and disable the LEDx pins (see figures 10 and 11). If the FSET/SYNC pin is released at any time after 7 µs, the A8509 will proceed to soft-start but will not perform the LED detection phase.

Synchronization

The A8509 can also be synchronized by using an external clock connected to the FSET/SYNC pin. The synchronization function of IC was designed to work with a push-pull type of clock driver. The amplitude of the clock signal should be between 1.5 and 3.3 V. The synchronization clock should have duty cycles that meet the minimum on/off times. Figure 12 shows the timing for a synchronization clock into the A8509 at 800 kHz. The 150 ns minimum on-time and 150 ns minimum off-time are

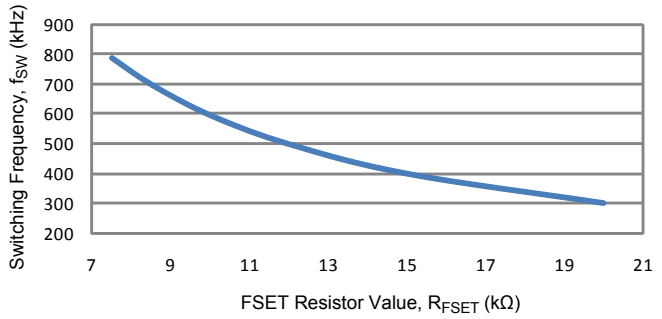

Figure 9. Switching Frequency as determined by R_{FSET} value.

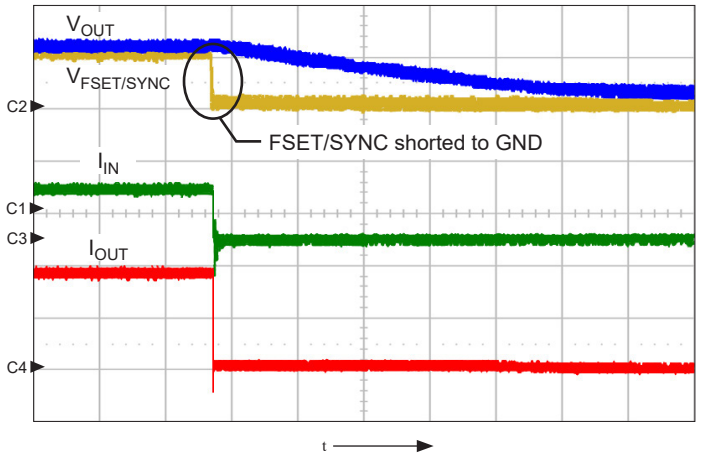

Figure 10. Shutdown when the FSET/SYNC pin is shorted to ground; shows V_{OUT} (ch1, 10 V/div.), $V_{FSET/SYNC}$ (ch2, 1 V/div.), I_{IN} (ch3, 2 A/div.), and I_{OUT} (ch4, 500 mA/div.), t = 200 µs/div.

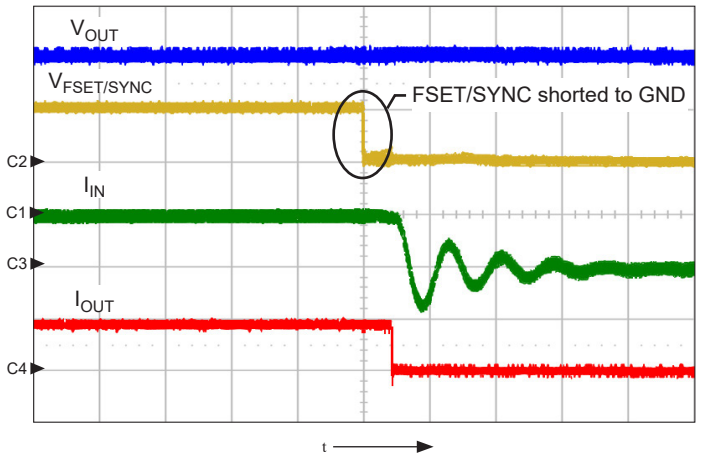

Figure 11. Zoomed-in view of figure 9, showing quick shutdown when FSET/SYNC shorted to ground, preventing IC running at very high frequency; shows V_{OUT} (ch1, 10 V/div.), $V_{FSET/SYNC}$ (ch2, 1 V/div.), I_{IN} (ch3, 2 A/div.), and I_{OUT} (ch4, 1 A/div.), t = 10 µs/div.

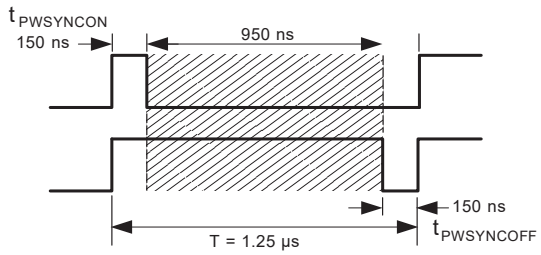

Figure 12. SYNC pulse minimum on and off time requirements, for an 800-kHz clock.

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indicated by the specifications for $t_{PWSYNCON}$ and $t_{PWSYNCOFF}$. Thus any pulse with a duty cycle of 19% to 85% at 800 kHz will synchronize the IC.

It is recommended to also use the RFSET resistor with the external clock signal. If a synchronization clock is lost during operation, the IC will revert to the preset switching frequency that is set by the RFSET resistor. In this configuration the preset frequency does not have any restrictions other than the normal operating range of 300 to 800 kHz. During the changeover period the IC stops switching for an approximately 5 µs period to allow for the synchronization detection circuitry to switch over to external preset switching frequency.

Although examples shown in figures 13 and 14 are extreme cases of clock-to-resistor frequency changes, it is recommended that actual applications do not have such large switching frequency changes. In most applications the RFSET resistor and clock frequency should be very close to each other in terms of frequency. Setting the frequencies close together will prevent the system from experiencing large changes on frequency-dependent signals and components, such as the inductor ripple current and the compensation resistor and capacitor.

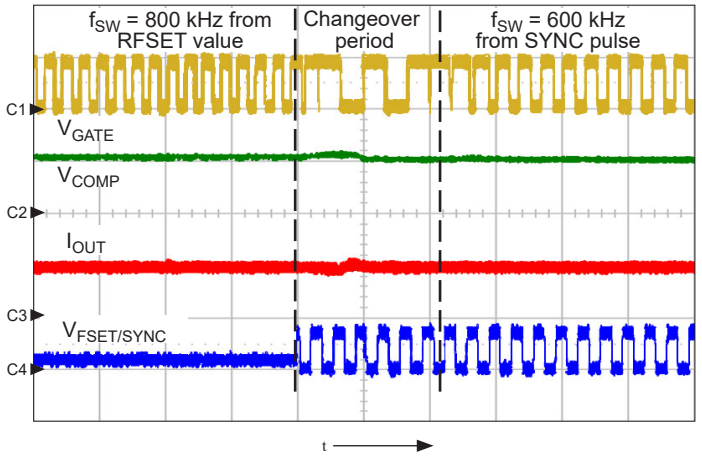

Figure 13. Synchronization feature with 200 kHz difference between R_{FSET} and external clock signal. The synchronization frequency is 600 kHz, and the resistor preset frequency is 800 kHz. Note that there is very little disturbance in the LED current at the time of changeover; shows V_{GATE} (ch1, 5 V/div.), V_{COMP} (ch2, 1 V/div.), I_{OUT} (ch3, 1 A/div.), and $V_{FSET/SYNC}$ (ch4, 5 V/div.), t = 5 µs/div.

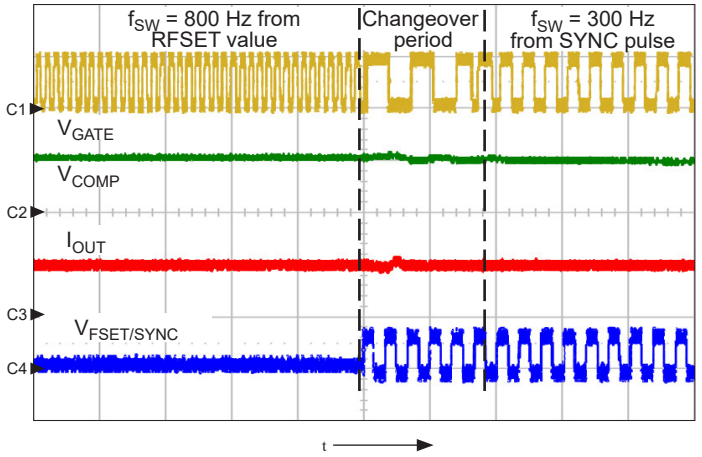

Figure 14. Synchronization feature with 500 kHz difference between R_{FSET} and external clock signal, illustrating the flexibility of the RFSET/SYNC pin; synchronization frequency is 300 kHz, and the resistor preset frequency is 800 kHz; shows V_{GATE} (ch1, 5 V/div.), V_{COMP} (ch2, 1 V/div.), I_{OUT} (ch3, 1 A/div.), and $V_{FSET/SYNC}$ (ch4, 5 V/div.), t = 10 µs/div.

LED Current Setting and LED Dimming

The maximum LED current can be up to 300 mA per channel. The LED current is set through the RISET resistor connected between the ISET pin and ground. The I_{LED} current is set according to the following formula:

$$R_{ISET} = (1.000 / I_{LED}) \times 2320 \quad (2)$$

where R_{ISET} is in Ω, and I_{LED} is in A. This sets the maximum current through the LEDs, referred to as the *100% current*. Standard R_{ISET} values are as follows:

Standard Resistor Value Closest to R_{ISET} (kΩ)	LED current per LED, I_{LED} (mA)
7.87	300
9.53	240
11.5	200
14.3	160
19.1	120

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The cited values are for 1% tolerance resistors. If the calculated value was not present, the next lowest value of 1% resistor was chosen.

PWM Dimming

Applying an external PWM signal on the PWM pin performs PWM dimming. When the PWM pin is pulled high, the A8509 enables the LEDx pins to sink 100% current. When PWM is pulled low, the boost converter and LEDx sinks are turned off. The compensation (COMP) pin is floated, and critical internal circuits are kept active.

The typical PWM dimming frequencies fall between 100 and 1000 Hz. Figures 15 and 16 show examples of dimming at 50% and 0.5% duty cycles.

Analog Dimming

The A8509 can also be dimmed by using an external DAC or other voltage source applied either directly to the ground side of the RISET resistor or through an external resistor to the ISET pin (see figure 17). The ISET current can be varied in the range between 34 µA and 130 µA.

• For a single-resistor configuration (panel A of figure 17), the ISET current is controlled by the following formula:

$$I_{SET} = \frac{V_{ISET} - V_{DAC}}{R_{ISET}} \quad (3)$$

where V_{ISET} is the ISET pin voltage and V_{DAC} is the DAC output voltage.

• For a dual-resistor configuration (panel B of figure 17), the ISET current is controlled by the following formula:

$$I_{SET} = \frac{V_{ISET}}{R_{ISET}} - \frac{V_{DAC} - V_{ISET}}{R_1} \quad (4)$$

The advantage of this circuit is that the DAC voltage can be higher or lower, thus adjusting the LED current to a higher or lower value of the preset LED current set by the R_{ISET} resistor:

- V_{DAC} = 1.00 V: output is strictly controlled by R_{ISET}
- V_{DAC} > 1.00 V: LED current is reduced
- V_{DAC} < 1.00 V: LED current is increased

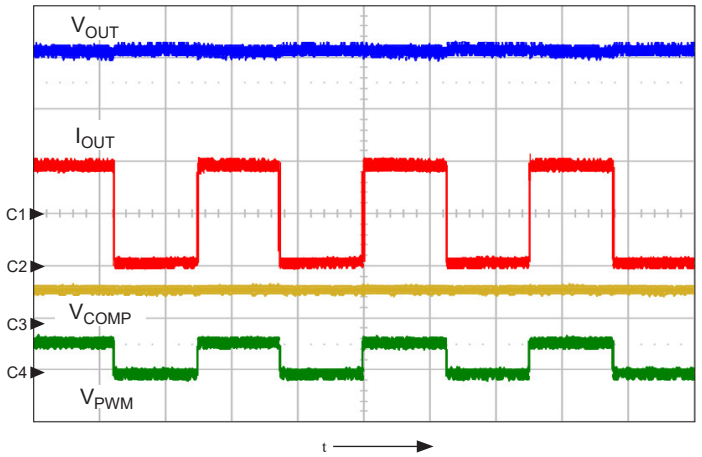

Figure 15. PWM dimming: f_{SW} = 200 Hz, 50% duty cycle, V_{OUT} = 30 V, V_{IN} = 12 V, and I_{LED} = 240 mA per LED string; shows V_{OUT} (ch1, 10 V/div.), I_{OUT} (ch2, 500 mA/div.), V_{COMP} (ch3, 2 V/div.), and PWM (ch4, 5 V/div.), t = 2 ms/div.

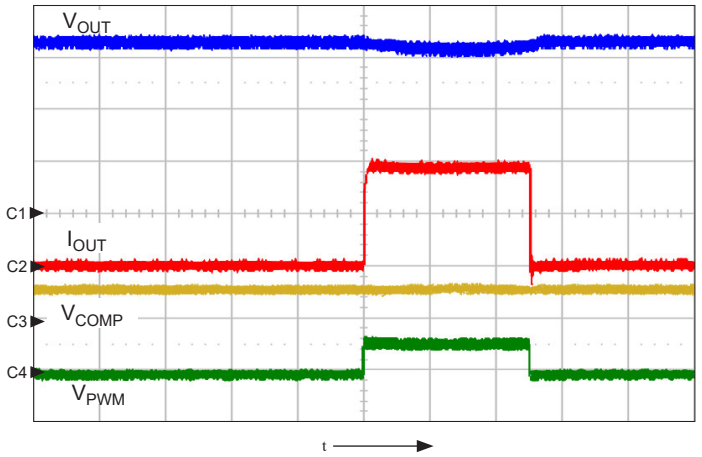

Figure 16. PWM dimming: f_{SW} = 200 Hz, 0.5% duty cycle, V_{OUT} = 30 V, V_{IN} = 15 V, I_{LED} = 240 mA per LED string; shows V_{OUT} (ch1, 10 V/div.), I_{OUT} (ch2, 500 mA/div.), V_{COMP} (ch3, 2 V/div.), and V_{PWM} (ch4, 5 V/div.), t = 10 µs/div.

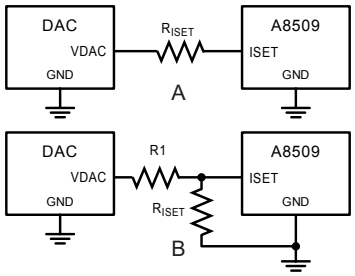

Figure 17. Typical application simplified diagram of voltage LED current control using a DAC to control LED current.

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Boost Switch Overcurrent Protection

The boost switch is protected with pulse-by-pulse current limiting set by the external RSENSE resistor. There also is a secondary current limit that is sensed on the boost switch.

Setting the Current Sense Resistor

The current sense resistor (see figure 18) is set according to the following formula:

$$I_{LIM} = \frac{V_{SENP}}{R_{SENSE}} \quad (5)$$

where V_{SENP} is found in the Electrical Characteristics table, and R_{SENSE} is the current sense resistor value.

The current limit is calculated by the following formula:

$$I_{LIM} = I_{IN}(max) + \frac{\Delta I_L}{2} \quad (6)$$

where $I_{IN}(max)$ is the maximum input current, and ΔI_L is the inductor current ripple.

Current Sense Resistor Routing

The current sense resistor must be routed as a differential pair to minimize measurement accuracy errors. For most current sense resistors, the resistance is measured between the inside edges of the mounting pads of the RSENSE resistor.

Figure 19 shows correct differential current sensing connections to the A8509. The individual current sense traces are kept short and side-by-side to get proper signal voltage levels. The trace for the positive sense pin (SENP) must be routed to the inside edge of the mounting pad on the high side of RSENSE. The trace for the negative sense pin (SENN) must be routed to the inside edge of the mounting pad on the ground side of RSENSE.

It should be noted that when designing the PCB layout, the trace for the negative sense pin (SENN) is often automatically merged with the ground flood fill and with the mounting pad on the ground side of RSENSE (shown in figure 20). However, the trace must be kept separate and dedicated, and careful attention must be given when routing the PCB.

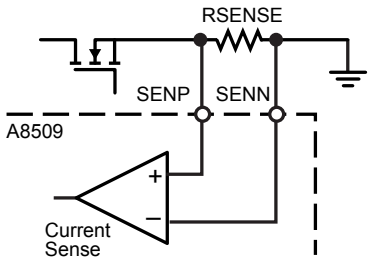

Figure 18. Simplified schematic of the current sense resistor connections to the current sense amplifier.

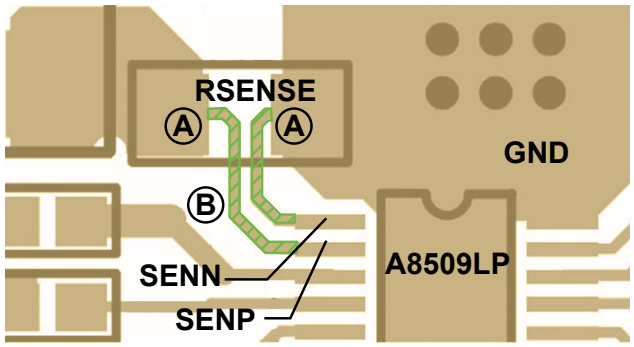

Figure 19. Correct layout of current sense resistor traces: (A) connect to inside edges of pads, (B) parallel and dedicated

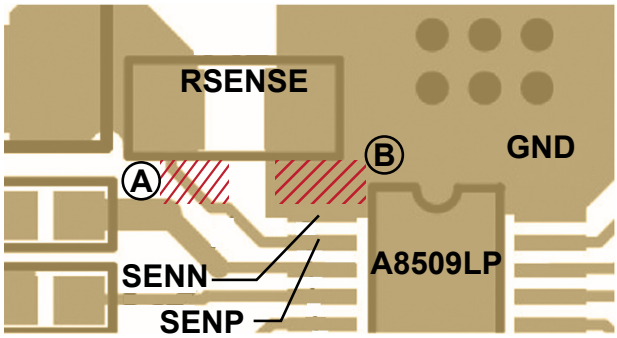

Figure 20. Incorrect layout of current sense resistor traces: (A) do not connect to outside edge of pad, (B) do not merge trace into ground

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Pulse-By-Pulse Current Limit

Figure 21 illustrates the normal waveform for the current sense signal. The pulse-by-pulse current limit is designed to limit the current through the external MOSFET to prevent failure. When the V_{SENSEP} threshold is reached, the IC stops switching to allow the inductor current to fall. Operation of pulse-by-pulse current limiting is shown in figure 22.

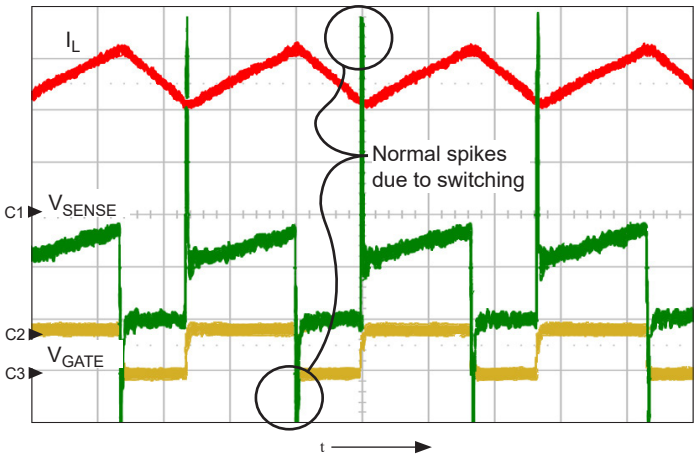

Figure 21. Current sense signal (V_{SENSE}) during normal operation, showing large spikes that are filtered out by a blanking period to avoid false overcurrent tripping; R_{SENSE} = 10 mΩ; shows inductor current I_L (ch1, 1 A/div.), V_{SENSE} (ch2, 20 mV/div.), and gate voltage of the main boost switch V_{GATE} (ch3), t = 500 ns/div.

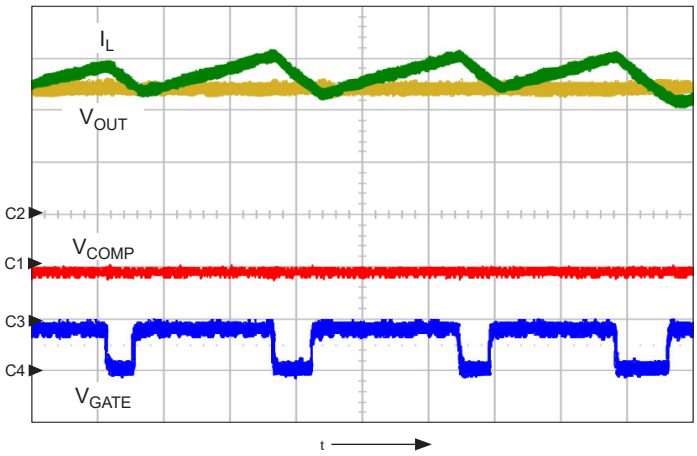

Figure 22. Typical pulse-by-pulse current limit; shows I_L (ch1, 2 A/div.), V_{OUT} (ch2, 10 V/div.), V_{COMP} (ch3, 2 V/div.), and V_{GATE} (ch4), t = 500 ns/div.

Secondary Boost Switch Limit

In case there is an inductor short during operation ,the A8509 has a secondary switch current limit. When this threshold is reached, the IC immediately shuts down. The level of this current limit is set above the pulse-by-pulse current limit to protect the switch from destructive currents when the boost inductor is shorted.

Output Overvoltage And Undervoltage Protection

The OVP pin on the A8509 controls both the overvoltage (OVP) and undervoltage (UVP) protection features. The pin circuit is shown in figure 23. The OVP protection protects the boost converter from excessive voltage levels when the feedback control loop is broken, usually caused by an open connection from output voltage to the LEDs. The UVP function provides output voltage-to-ground short protection when an external disconnect switch is used. For more detailed information on disconnect switch application, see the Undervoltage Protection (UVP) section.

For proper operation of this pin, due to the relatively low voltage level, special care has to be taken during PCB layout. Figure 24 is an example of a proper PCB layout.

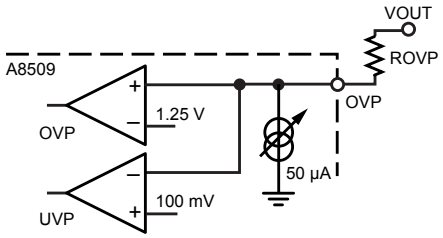

Figure 23. Simplified schematic of the Overvoltage Protection section.

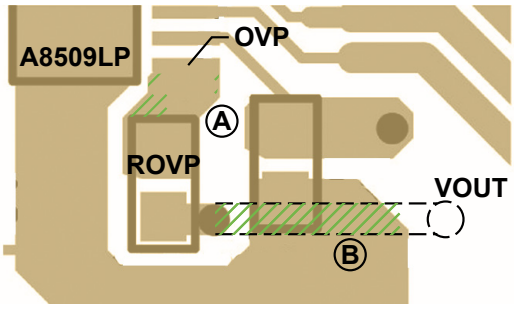

Figure 24. Simplified schematic of the OVP resistor connections; (A) connection should be short, (B) connection to VOUT can be long, and ROVP should be as close to the OVP pin as possible.

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LED Open Detect

When any LED string opens, the boost control circuit increases the output voltage until it reaches the overvoltage protection level. The OVP event causes any LED string that is below regulation level to be disabled. After disabling the open string, the output voltage returns to normal operating voltage. An EN low signal will reset the LED string regulation lock.

Figure 25 shows a typical overvoltage condition when the output voltage is disconnected from the LED load. Figure 26 shows an extended view of the same situation. Figure 27 shows an OVP condition created by a single open LED string.

Undervoltage Protection (UVP)

If the output voltage is shorted to ground the OVP pin will sense an undervoltage condition (UVP). When UVP is sensed, the IC sets the Fault flag low which, if used to interface to the output-disconnect switch, will shut off the P-FET device. Figure 28 is a schematic showing the input disconnect switch implementation.

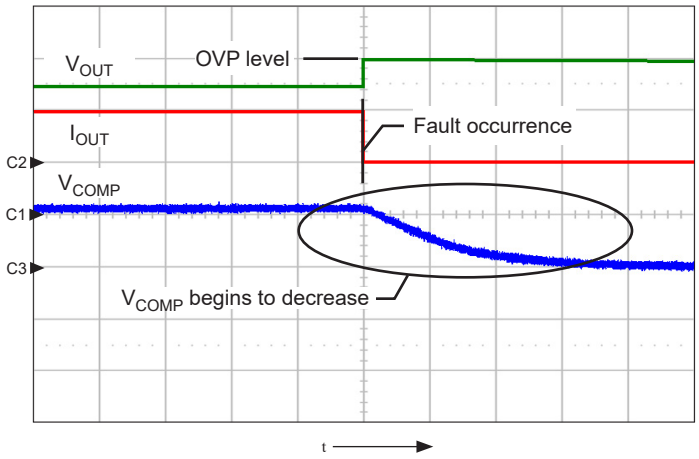

Figure 25. OVP operation with all LEDx pins open. V_{OUT} rises to the overvoltage level and stays there until the IC is shut down; shows V_{OUT} (ch1, 20 V/div.), I_{OUT} (ch2, 1 A/div.), and V_{COMP} (ch3, 2 V/div.), t = 2 ms/div.

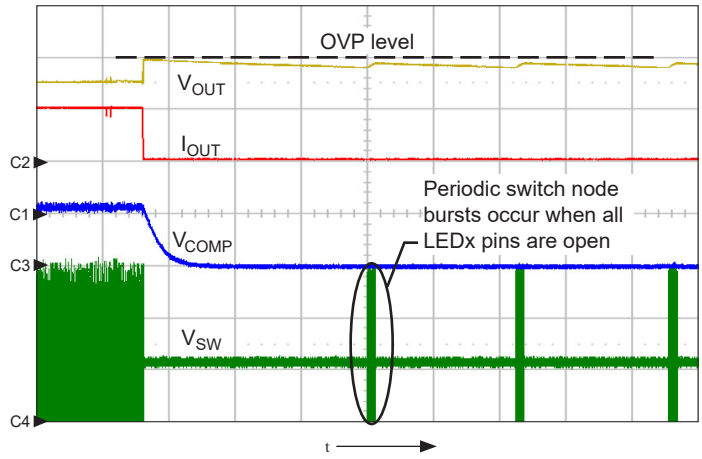

Figure 26. Extended view of the OVP condition in figure 25; shows V_{OUT} (ch1, 20 V/div.), I_{OUT} (ch2, 1 A/div.), V_{COMP} (ch3, 1 V/div.), and switch node (V_{SW}) (ch4, 20 V/div.), t = 10 ms/div.

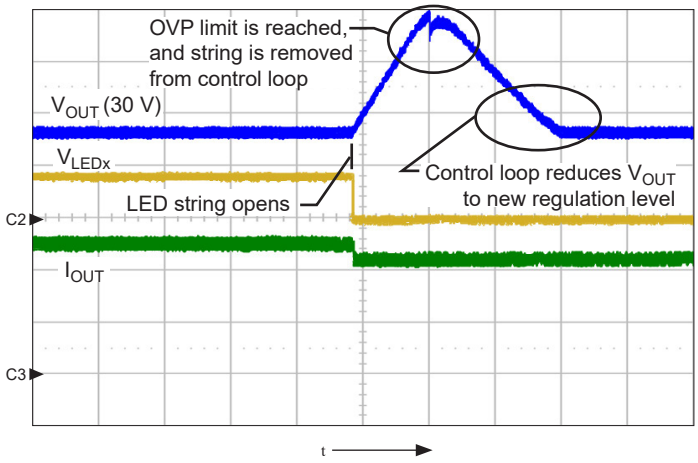

Figure 27. OVP condition created by an open LED string; shows V_{OUT} (ch1, 2 V/div.), pin voltage V_{LEDx} (ch2, 5 V/div.), and I_{OUT} (ch3, 200 mA/div.), t = 2 ms/div.

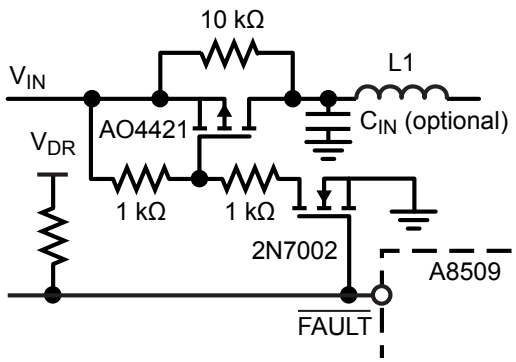

Figure 28. Simplified schematic of an external disconnect switch implementation.

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The waveforms in figure 29 show the operation of the disconnect feature.

LED Short Detect

All LEDx pins are rated for 55 V, thus allowing LEDx pin-to-VOUT short protection in case of a connector short. Any LEDx pin that has a voltage exceeding V_{LEDSC} will be removed from operation. This is to prevent the IC dissipating too much power by having a large voltage present on the LEDx pins.

Input UVLO

When V_{IN} rises above the UVLO threshold ($V_{UVLO(th)}$), the A8509 is enabled. It is disabled when V_{IN} falls below $V_{UVLO(th)} - V_{UVLO(hys)}$ for more than 2 µs. This lag is to avoid shutdown because of momentary glitches in the power supply.

VDD and VDR

The VDD pin provides the regulated bias supply for the internal circuits. A capacitor with a value in the range 0.1 to 1 µF should be used to decouple the internal analog and digital circuitry.

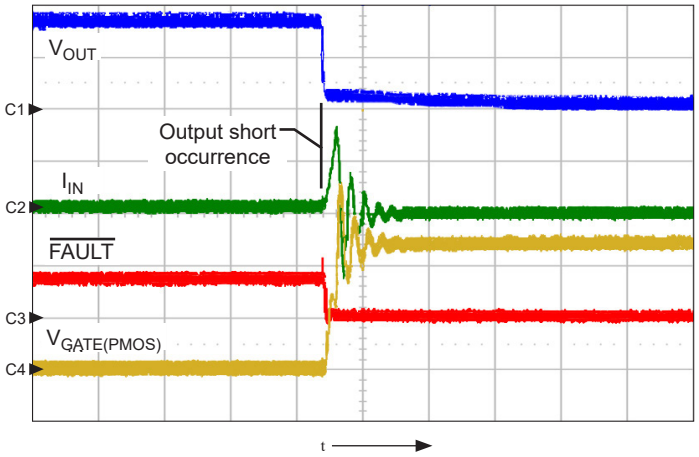

Figure 29. Input disconnect switch shutdown during an output short condition; shows V_{OUT} (ch1, 20 V/div.), I_{IN} (ch2, 10 A/div.), $\overline{FAULT}$ (ch3, 5 V/div.), and PMOS device V_{GATE} (ch4, 5 V/div.), t = 50 µs/div.

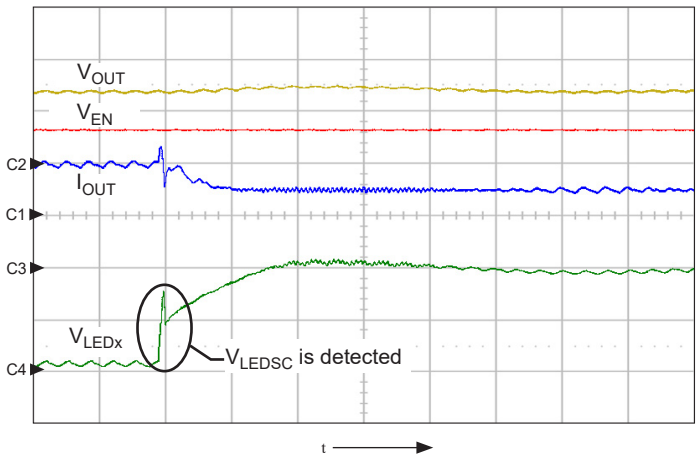

Figure 30. Typical shorted LED: when voltage exceeds V_{LEDSC}, the LED is disabled and remains disables until either the EN pin is toggled or the power cycled; shows V_{OUT} (ch1, 20 V/div.), V_{EN} (ch2, 5 V/div.), I_{OUT} (ch3, 0.5 A/div.), and V_{LEDx} (ch4, 10 V/div.), t = 10 µs/div.

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The VDR circuit provides power to the gate driver of the A8509. For VDR the decoupling capacitor value should fall in the range 0.47 to 1 µF. A 1 µF capacitor is recommended.

Shutdown

If the EN pin is pulled low, the IC will shut down immediately.

Fault Protection During Operation

The A8509 device constantly monitors the state of the system to determine if any fault conditions occur during normal operation. The response to a triggered fault condition is summarized in table 1. The possible fault conditions that the part can detect are:

- Open LED pin
- Shorted inductor with second level switch current protection
- VOUT short-to-ground
- ISET pin short-to-ground
- FSET pin short-to-ground
- Shorted LED
- Open Schottky diode
- Short Schottky diode protection with second level switch current protection
- Thermal shutdown (TSD)
- Overvoltage protection (OVP)

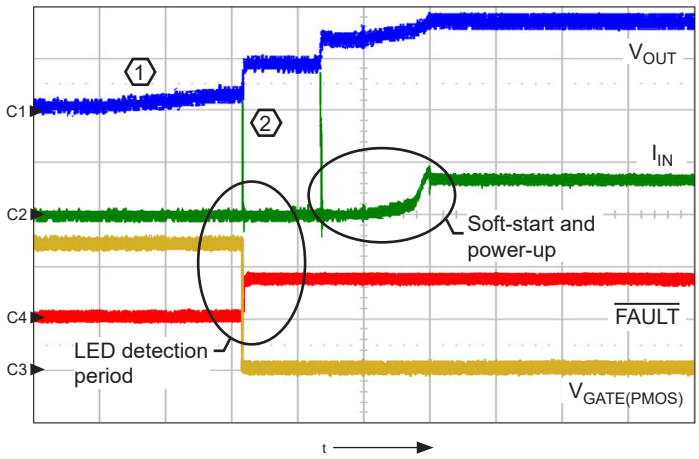

Figure 31. Input disconnect switch power-up: (1) V_{OUT} charges via 10 kΩ resistor, (2) I_{IN} current spike from charging COUT when the PMOS is enabled; shows V_{OUT} (ch1, 20 V/div.), I_{IN} (ch2, 2 A/div.), $\overline{FAULT}$ (ch3, 5 V/div.), and PMOS device V_{GATE} (ch4, 5 V/div.), t = 2 ms/div.

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Table 1. Fault Modes

Fault Name	Type	Active	Fault Flag Set	Description	Boost	Sink driver
Primary switch current protection (pulse-by-pulse current limit)	Auto-restart	Always	No	This fault condition is triggered by the pulse-by-pulse current limit when the SENSP pin voltage exceeds V_{SENSEP}.	Off for a single cycle	On
Secondary switch current limit	Latched	Always	Yes	When the current through the boost switch exceeds the secondary current limit ($V_{SENSESEC}$) the IC immediately shuts down the LED drivers and the boost. To re-enable the A8509 the EN pin must be toggled.	Off	Off
LEDx pin short to GND protection	Auto-restart	Startup	Yes	This fault prevents the IC from starting-up if any of the LEDx pins are shorted. The IC stops soft-start from starting while any of the LEDx pins are determined to be shorted. After the short is removed, soft-start is allowed to start.	Off	Off
LEDx pin open	Auto-restart	Normal operation	No	When an LEDx pin is open the device will determine which LEDx pin is open by increasing the output voltage until OVP is reached. Any LED string below regulation will be turned off. The device then goes back to normal operation by reducing the output voltage to the appropriate voltage level.	On	Off for open pins. On for all others
LED short protection	Auto-restart	Always	No	This fault occurs when the LED pin voltage exceeds V_{LEDSC}. When the LED short protection is detected, the LED string that is above the threshold will be removed from operation.	On	Off for shorted pins. On for all others
FSET pin short protection	Auto-restart	Always	No	This fault occurs when the FSET pin current goes above 150% of the maximum current. The boost stops switching, and the IC disables the LED sinks until the fault is removed. When the fault is removed the IC tries to restart with soft-start.	Off	On in soft-start current
ISET pin short protection	Auto-restart	Always	No	This fault occurs when the ISET pin current goes above 150% of the maximum current. The boost stops switching and the IC disables the LED sinks until the fault is removed. When the fault is removed the IC tries to regulate to the preset LED current.	Off	Off
Overvoltage protection	Auto-restart	Always	No	The fault occurs when the OVP pin voltage exceeds the $V_{OVP(th)}$ threshold. The A8509 immediately stops switching to try to reduce the output voltage. If the output voltage decreases then the A8509 restarts switching to regulate the output voltage.	Stop during OVP event	On
Output undervoltage protection	Auto-restart	Always	Yes	This fault occurs when the OVP pin senses less than 100 mV on the pin. The IC disables the external P-FET switch, if one is used.	Off	Off
Overtemperature protection	Auto-restart	Always	Yes	The fault occurs when the die temperature exceeds the overtemperature threshold, typically 165°C.	Off	Off
VIN UVLO	Auto-restart	Always	No	This fault occurs when V_{IN} drops below $V_{UVLO(th)}$(max), 8.5 V. This fault resets all latched faults.	Off	Off

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APPLICATION INFORMATION

Paralleling More Than One A8509

The A8509 can be paralleled together by using a single boost converter (master) to provide output power for up to a total of four A8509s (slaves). The MODE pin of each device must be tied to the VDD pin of the same device for proper mode selection. In this mode, the $\overline{\text{FAULT}}$ pins and the COMP pins become a bi-direction signal bus for the system to communicate.

At initial power-up, each IC will release a pull-down resistor on the COMP pin and start in soft-start mode. When 200 mV is detected on the COMP pin, the master will then switch to normal mode. Also, for proper operation all of the $\overline{\text{FAULT}}$ pins must be tied together to prevent the parallel ICs from powering-up into a shorted LEDx pin situation. While the $\overline{\text{FAULT}}$ pins are pulled low, the system will not proceed with start-up.

Below is a simple list of necessary connections for the master, to ensure proper parallel operation (refer to Application C in the Typical Applications section):

- COMP pin
- VOUT node
- $\overline{\text{FAULT}}$ pin
- EN pin
- PWM pin

Each one of these must be connected to the corresponding signal on the slave devices.

OVP setting for parallel operation

A notable exception to the list is the OVP pin. In this system, each OVP pin must be set with a dedicated resistor. To make sure that the system will operate properly, the overvoltage protection on the master IC should be set higher than on the slave IC. The A8509 checks open LED condition upon hitting the OVP voltage. If the master OVP voltage is set lower than the slave OVP, the slave OVP pin will not trip to permit the open LED check. This in turn will not remove the corresponding LEDx pins from regulation. Therfore, the output voltage will stay at the master OVP limit and never decrease the output voltage to the lower regulation level.

The required slave OVP resistor value can be calculated using the following formula:

$$R_{OVP(slave)} = \frac{V_{OUT(OVP)} - 1.25\ V}{I_{OVPH}(min)} \quad (7)$$

where $V_{OUT(OVP)}$ is the required OVP voltage level, and $I_{OVPH}(min)$ is the current into the OVP pin found in the Electrical Characteristics table. The minimum value should be used in this calculation.

The required master OVP voltage level can be calculated using the following formula:

$$V_{OVP(master)} = R_{OVP(slave)} \times I_{OVPH}(max) + 1.25\ V \quad (8)$$

where $V_{OVP(master)}$ is the minimum OVP voltage level of the master IC, $I_{OVPH}(max)$ is current into the OVP pin found in the Electrical Characteristics table. The maximum value should be used in this calculation.

The required master OVP resistor value can be calculated using the following formula:

$$R_{OVP(master)} = \frac{V_{OVP(master)} - 1.25\ V}{I_{OVPH}(min)} \quad (9)$$

where $V_{OVP(master)}$ is the minimum required master OVP voltage level, and $I_{OVPH}(min)$ is the current into the OVP pin found in the Electrical Characteristics table. The minimum value should be used in this calculation.

Following the above formulas will guarantee that there is no overlap in OVP voltage levels in the system. All slave A8509s in the system can have the same OVP voltage setting. Figure 32 shows a proper master-slave OVP setting, and figure 33 shows the result of setting the master OVP too low.

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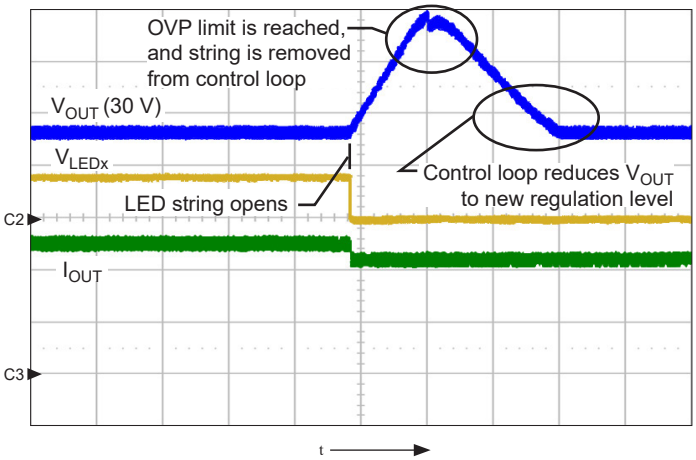

Figure 32. Proper OVP setting for the master and slave configuration. The master OVP is set higher than the slave, shows V_{OUT} (ch1, 2 V/div.), pin voltage V_{LEDx} (ch2, 2 V/div.), and I_{OUT} (ch3, 200 mA/div.), t = 2 ms/div.

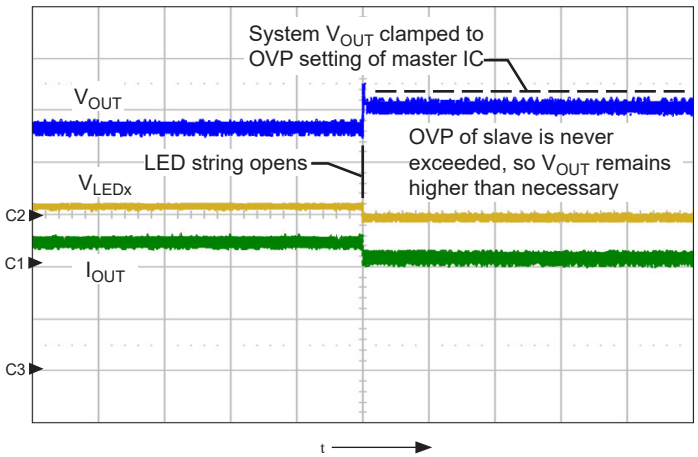

Figure 33. OVP on the master IC is set too low and the IC does not respond properly to the open LED condition on the slave IC; shows V_{OUT} (ch1, 10 V/div.), V_{LEDx} (ch2, 5 V/div.), and I_{OUT} (ch3, 200 mA/div.), t = 100 ms/div.

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Design Example

This section provides a method for selecting component values when designing an application using the A8509.

Assumptions: For the purposes of this example, the following are given as the application requirements:

- V_{IN}: 10 to 16 V
- Quantity of LED channels, #CHANNELS: 4
- Quantity of series LEDs per channel, #SERIESLEDS : 10
- LED current per channel, I_{LED}: 240 mA
- $V_{f(240)}$ at 240 mA: 3.2 V (max)
- f_{SW} : 600 kHz
- T_A(max): 65°C
- PWM dimming frequency: 200 Hz, 1% duty cycle

Step 1: Connect LEDs to pins LED1 through LED4.

Step 2: Determine the LED current by setting resistor R_{ISET}. To do so, apply equation 2:

$$\begin{aligned} R_{ISET} &= (1.000 / I_{LED}) \times 2320 \\ &= (1.000\ \text{V} / 0.240\ \text{A}) \times 2320 \\ &= 9.67\ \text{k}\Omega \end{aligned}$$

Choose a 9.53 kΩ resistor.

STEP 3: Determine the OVP resistor. The OVP resistor is connected between the OVP pin and the output voltage of the converter. The first step is to determine the maximum voltage based on the LED requirements. Then the regulation voltage of 650 mV should be added, along with 2 V for noise and regulation. Given the regulation voltage (V_{LED}) of the A8509 is 650 mV, the minimum required voltage can be determined as follows:

$$\begin{aligned} V_{OUT(OVP)} &= \#\text{SERIESLEDS} \times V_{f(240)} + V_{LED} + 2\ \text{V} \\ &= 10 \times 3.2\ \text{V} + 0.650\ \text{V} + 2\ \text{V} \\ V_{OUT(OVP)(min)} &= 34.65\ \text{V} \end{aligned} \quad (10)$$

The OVP resistor (ROVP) value can be calculated as:

$$\begin{aligned} R_{OVP} &= \frac{V_{OUT(OVP)(min)} - V_{OVP(th)}(\text{min})}{I_{OVPH}(\text{min})} \\ &= \frac{34.65\ \text{V} - 1.11\ \text{V}}{45\ \mu\text{A}} \\ &= 745\ \text{k}\Omega \end{aligned} \quad (11)$$

where both $I_{OVP(th)}$(min) and $V_{OVP(th)}$(min) are found in the Electrical Characteristics table. Choose a value of resistor that is the closest value higher than the calculated R_{OVP}. In this design example, a value of 750 kΩ is selected.

Below is the actual value of the minimum OVP trip level with the selected resistor, applying equation 8:

$$\begin{aligned} V_{OVP(master)} &= R_{OVP} \times I_{OVPH} + 1.25\ \text{V} \\ &= 750\ \text{k}\Omega \times 49\ \mu\text{A} + 1.25\ \text{V} \\ &= 38.75\ \text{V} \end{aligned}$$

STEP 4: Determine the inductor. The inductor must be chosen such that it can handle the necessary input current. In most applications, due to stringent EMI requirements, the inductor must operate in continuous conduction mode throughout the whole input voltage range.

STEP4a: Determine the maximum duty cycle of the system:

$$\begin{aligned} D(\text{max}) &= 1 - \frac{V_{IN}(\text{min}) \times \eta}{V_{OUT(OVP)} + V_{f(boost)}} \\ &= 1 - \frac{10\ \text{V} \times 0.9}{34.65\ \text{V} + 0.4\ \text{V}} \\ &= 74.5\% \end{aligned} \quad (12)$$

A good approximation of efficiency (η) is 90%. The voltage drop of the boost diode can be approximated to be about 0.4 V.

STEP 4b: Determine the maximum and minimum input current to the system. The minimum input current dictates the inductor value. The maximum current rating dictates the current rating of the inductor.

To calculate the maximum input current, first determine the required output current:

$$\begin{aligned} I_{OUT} &= \#\text{CHANNELS} \times I_{LED} \\ &= 4 \times 240\ \text{mA} \\ &= 0.960\ \text{A} \end{aligned} \quad (13)$$

Then substitute into the formula for maximum input current:

$$\begin{aligned} I_{IN}(\text{max}) &= \frac{V_{OUT} \times I_{OUT}}{V_{IN}(\text{min}) \times \eta} \\ &= \frac{34.65\ \text{V} \times 0.960\ \text{A}}{10\ \text{V} \times 0.90} \\ &= 3.7\ \text{A} \end{aligned} \quad (14)$$

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The minimum input current can be calculated as:

$$I_{IN}(min) = \frac{V_{OUT} \times I_{OUT}}{V_{IN}(max) \times \eta} \quad (15)$$
$$= \frac{34.65\ V \times 0.960\ A}{16\ V \times 0.90}$$
$$= 2.31\ A$$

STEP 4c: Determining the inductor value. To assure that the inductor operates in continuous conduction mode, the value of inductor must be set such that $^1/_2$ of the inductor ripple current is not greater than the average minimum input current.

As a first pass, take I_{ripple} to be 30% of the maximum inductor current:

$$\Delta I_L = I_{IN}(max) \times (I_{ripple} / I_{IN}(max)) \quad (16)$$
$$= 3.72\ A \times 0.30$$
$$= 1.1\ A$$

Check to make sure that $^1/_2$ of the inductor ripple current is less than $I_{IN}(min)$:

$$I_{IN}(min) > \frac{1}{2} \times \Delta I_L$$
$$2.31\ A > 0.56\ A$$

The inductor value can be calculated as:

$$L = \frac{V_{IN}(min)}{\Delta I_L \times f_{SW}} \times D(max) \quad (17)$$
$$= \frac{10\ V}{1.1\ A \times 600\ kHz} \times 0.745$$
$$= 10.62\ \mu H$$

A good inductor value to use would be $L_{used} = 10\ \mu H$.

STEP 4d: Determining the inductor current rating. The inductor current rating must be greater than the $I_{IN}(max)$ value plus the ripple current ΔI_L, calculated as:

$$I_L(min) = I_{IN}(max) + \frac{1}{2} \times \Delta I_{Lused} \quad (18)$$
$$= 3.72\ A + 0.56\ A$$
$$= 4.28\ A$$

STEP 4e: Choosing the RSENSE resistor. The sense resistor value can be calculated as follows:

$$R_{SENSE} = \frac{V_{SENSEP}}{I_L(min)} \quad (19)$$
$$= \frac{0.086\ V}{4.28\ A}$$
$$= 0.02\ \Omega$$

0.018 Ω is a good value to use for the resistor.

STEP 4f: This step is used to verify that there is sufficient slope compensation for the inductor chosen. The internal slope compensation value is determined by the following formula:

$$\text{Slope Compensation} = 2.81 \times 10^{-7} \times f_{SW} \quad (20)$$

where f_{SW} is in Hz. Substituting:

$$= 0.168\ V/\mu s$$

With $R_{SENSE} = 0.02\ \Omega$ this translates to:

$$0.168 / 0.02 = 8.4\ A/\mu s$$

Next invert equation 17 and insert the inductor value used in the design:

$$\Delta I_{Lused} = \frac{V_{IN}(min)}{L_{used} \times f_{SW}} \times D(max) \quad (21)$$

where f_{SW} is in MHz. Substituting:

$$= \frac{10\ V}{10\ \mu H \times 600\ kHz} \times 0.745$$
$$= 1.24\ A$$

$$\text{Inductor Current Slope} = \frac{\Delta I_{Lused} \times 1 \times 10^{-6}}{\frac{1}{f_{SW}} \times (1 - D(max))} \quad (22)$$
$$= \frac{1.24\ A \times 1 \times 10^{-6}}{\frac{1}{600\ kHz} \times (1 - 0.745)}$$
$$= 2.91\ A/\mu s$$

Note: that the 1×10^{-6} is a constant multiplier. This slope should be smaller than the internal slope compensation.

STEP 5: To determine the resistor values for a switching frequency use figure 9.

STEP 6: Choosing the proper switching diode. The switching diode must be chosen for three characteristics when it is used in LED lighting circuitry: reverse voltage rating, current rating, and reverse current characteristic of the diode.

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The reverse voltage rating should be such that, during any operation condition, the voltage rating of the device is larger than the maximum output voltage. In this case, the maximum output voltage is $V_{OUT(OVP)}$.

The peak current through the diode is:

$$I_{d(peak)} = I_{IN}(max) + \Delta I_{Lused} \quad (23)$$
$$= 3.72\ A + 0.56\ A$$
$$= 4.28\ A$$

The other major component in determining the switching diode is the reverse current characteristic of the diode. This characteristic is especially important when PWM dimming is implemented. During PWM off-time the boost converter is not switching. This results in a slow bleeding-off of the output voltage due to leakage currents (I_R). I_R, or reverse current, can be a huge contributor especially at high temperatures. On the diode that was selected in this design, the current varies between 1 and 100 µA.

STEP 7: Choosing the output capacitors. The output capacitors must be chosen such that they can provide filtering for both the boost converter and for the PWM dimming function. The biggest factor that contributes to the size of the output capacitor is PWM dimming frequency and the PWM duty cycle. Another major contributor is leakage current (I_{LK}). This current is the combination of the OVP current sense as well as the reverse current of the switching diode.

In this design the PWM dimming frequency is 200 Hz and the minimum duty cycle is 1%. Typically, the voltage variation on the output during PWM dimming must be less than 250 mV (V_{COUT}) so that no audible hum can be heard:

$$C_{OUT} = I_{LK} \times \frac{1 - D_{PWM(min)}}{f_{PWM} \times V_{COUT}} \quad (24)$$
$$= 300\,\mu A \times \frac{1 - 0.01}{200\ Hz \times 0.250\ V}$$
$$= 5.94\,\mu F$$

A capacitor larger than 5.94 µF should be selected due to degradation of capacitance at high voltages on the capacitor. Two ceramic 4.7 µF 50 V capacitors are a good choice to fulfill this requirement.

The rms current through the capacitor is given by:

$$I_{COUTrms} = I_{OUT} \sqrt{\frac{D(max) + \frac{\Delta I_{Lused}}{I_{IN}(max) \times 12}}{1 - D(max)}} \quad (25)$$
$$= 0.960\ A \sqrt{\frac{0.745 + \frac{1.24\ A}{3.72\ A \quad \times 12}}{1 - 0.745}}$$
$$= 1.67\ A$$

The output capacitor must have a current rating of at least 1.67 A. The output capacitors selected in this design have a combined rms current rating of 2 A.

STEP 8: Selection of input capacitor. The input capacitor must be selected such that it provides a good filtering of the input voltage waveform. A good rule of thumb is to set the input voltage ripple (ΔV_{IN}) to be 1% of the minimum input voltage. The minimum input capacitor requirements are as follows:

$$C_{IN} = \frac{\Delta I_{Lused}}{8 \times f_{SW} \times \Delta V_{IN}} \quad (26)$$
$$= \frac{1.24\ A}{8 \times 600\ kHz \times 0.1\ V}$$
$$= 2.65\ \mu F$$

The rms current through the capacitor is given by:

$$I_{INrms} = \frac{I_{OUT} \times \frac{\Delta I_{Lused}}{I_{IN}(max)}}{(1 - D(max))\sqrt{12}} \quad (27)$$
$$= \frac{0.960\ A \times \frac{1.24\ A}{3.72\ A}}{(1 - 0.765)\sqrt{12}}$$
$$= 0.363\ A$$

A good ceramic input capacitor with ratings of 50 V, 4.7 µF will suffice for this application.

Corresponding capacitors include:

Vendor	Value	Part number
Murata	4.7 µF 50 V	GRM32ER71H475KA88L
Murata	2.2 µF 50 V	GRM31CR71H225KA88L

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Typical Applications

The following is the component list for the typical application circuit shown in figure 1.

Designator	Description	Part Number	Manufacturer
CDD	0.1 µF / 10 V	GRM2195C1H104JA01D	Murata
CDR	1 µF / 16 V	DRM188R61A105K	Murata
C_{IN}	4.7 µF / 50 V	GRM32ER71H475KA88L	Murata
COUT	10 µF / 50 V	GRM32ER71H475KA88L	Murata
CP	1 µF / 16V	GRM188R61A474K	Murata
CZ	DNP		
D1	60 V / 5 A Schottky	CMSH5-60-AMI	Central Semi
L1	10 µH / 5 A	74477110	Wurth Electronics
Q1	NMOS	FQD13N06LTM	Faichild
R1	100 kΩ		DigiKey
RFSET	8.45 kΩ 1%		
RISET	12.4 kΩ 1%		
ROVP	732 kΩ 1%		
R_{SENSE}	0.015 Ω		
RZ	DNP		
U1	A8509	A8509	Allegro

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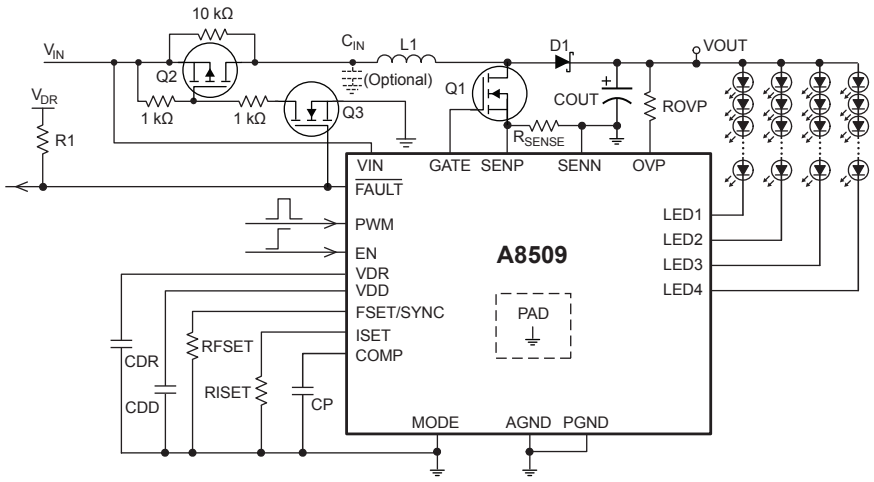
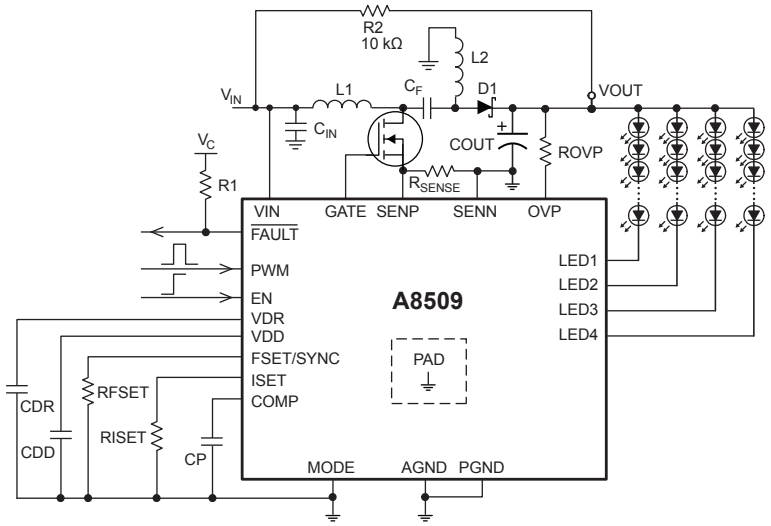
Typical Applications



Application A. Typical schematic for boost application with disconnect switch application



Application B. Typical application showing SEPIC configuration

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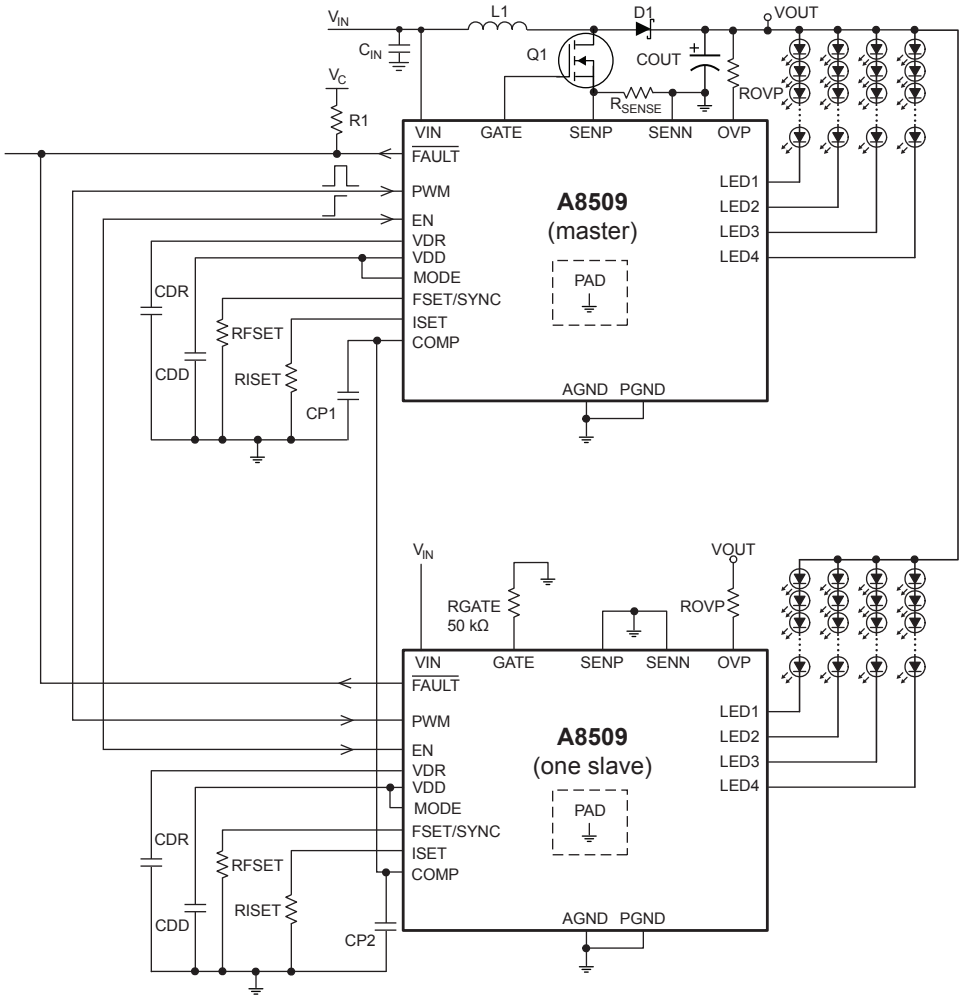

Application C. Parallel operation of two A8509s; overvoltage protection on master must be set higher than the OVP on the slave

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Package LP, 24-Pin TSSOP with Exposed Thermal Pad

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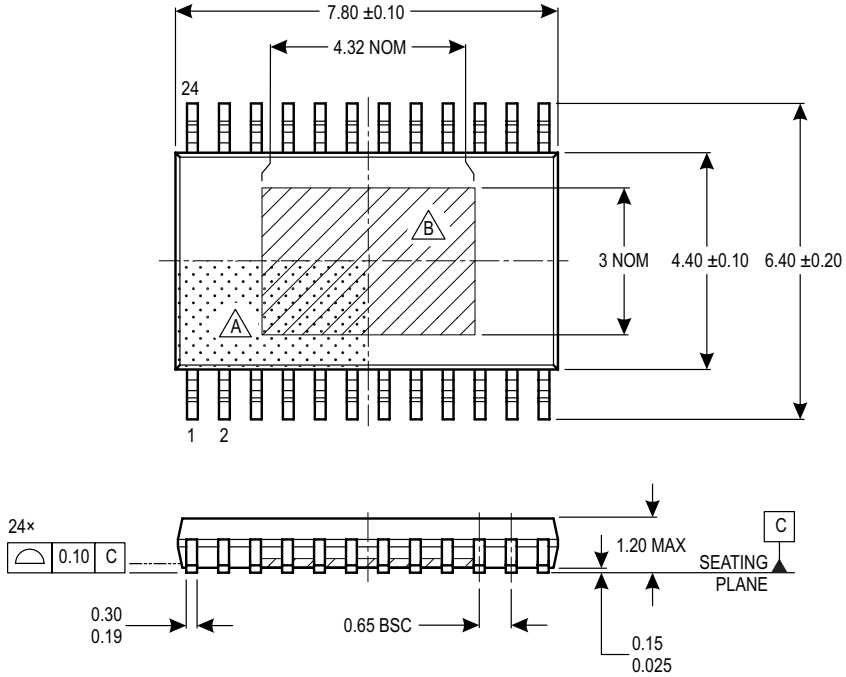
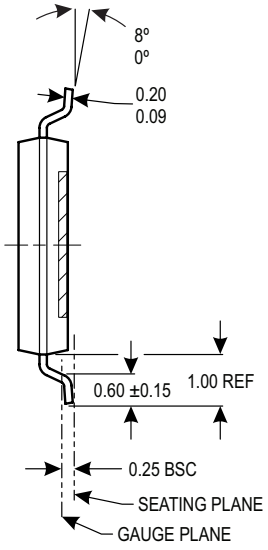
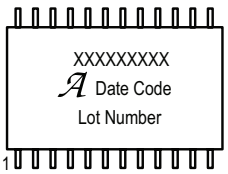
(Reference Allegro DWG-0000379, Rev. 3 and JEDEC MO-153ADT)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



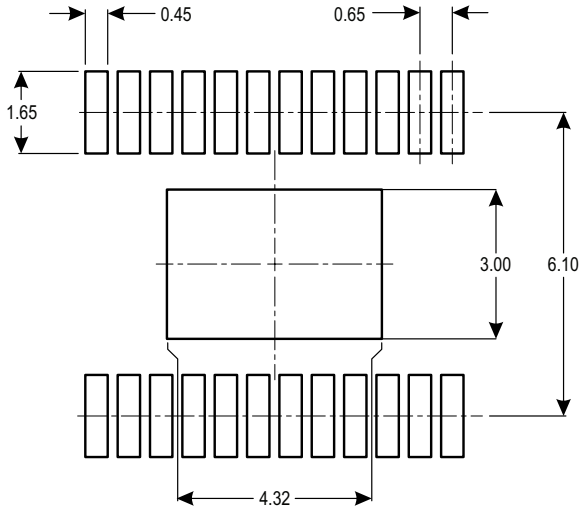




△D Standard Branding Reference View

Lines 1, 2, 3: Maximum 9 characters per line

Line 1: Part number
Line 2: Logo A, 4-digit date code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number



△C PCB Layout Reference View

△A Terminal #1 mark area.

△B Exposed thermal pad (bottom surface); dimensions may vary with device.

△C Reference land pattern layout (reference IPC7351 TSOP65P640X120-25M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5).

△D Branding scale and appearance at supplier discretion.

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Package LB, 24-Pin SOICW with Exposed Thermal Pad

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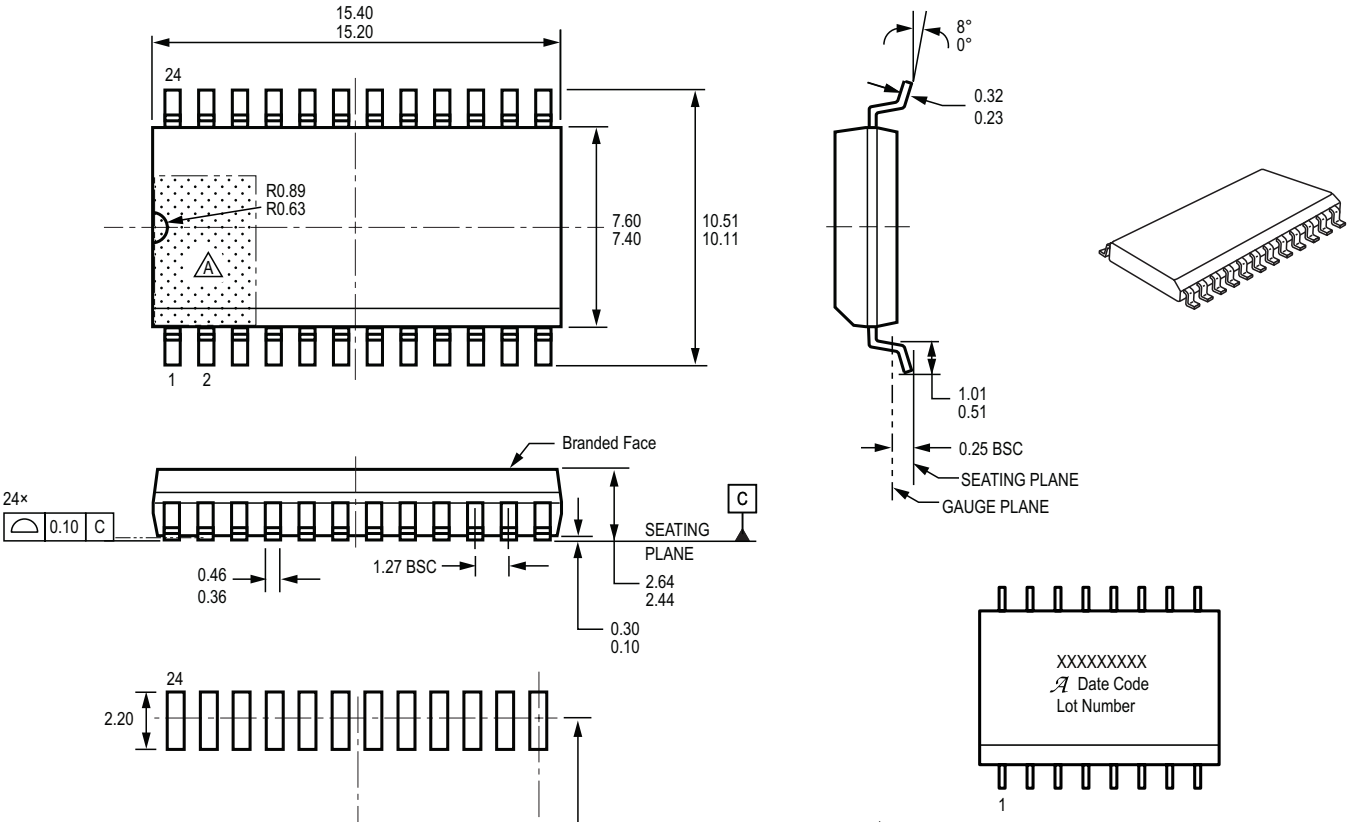
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown
Internal configuration of fused pins is device-dependent



B PCB Layout Reference View

C Standard Branding Reference View

Line 1, 2, 3 = 15 Characters

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Assembly Lot Number

A Terminal #1 mark area

B Reference pad layout (reference IPC SOIC127P1030X265-24M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

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Revision History

Number	Date	Description
–	June 19, 2011	Initial release
1	May 14, 2020	Minor editorial updates
2	May 11, 2022	Updated LP package drawing (page 27); added LB package drawing (page 28); minor editorial updates
3	March 19, 2024	Updated product status to Last-Time Buy
4	September 12, 2024	Updated product status to Discontinued

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