A1333

Precision, High Speed, Hall-Effect Angle Sensor IC with Integrated Diagnostics for Safety-Critical Applications

FEATURES AND BENEFITS

- Contactless 0° to 360° angle sensor IC, for angular position, rotational speed, and direction measurement
  - Capable of sensing magnet rotational speeds targeting 12-bit effective resolution with 900 G field
  - Circular vertical Hall (CVH) technology provides a single-channel sensor system supporting operation across a wide range of air gaps
- Developed in accordance with ISO 26262 requirements for hardware product development for use in safety-critical applications
  - Single die version designed to meet ASIL B requirements when integrated and used in conjunction with the appropriate system-level control, in the manner prescribed in the A1333 Safety Manual
  - Dual-die version designed to meet ASIL D requirements when integrated and used in conjunction with the appropriate system-level control, in the manner prescribed in the A1333 Safety Manual
- High diagnostic coverage
  - On-chip diagnostics include logic built-in self-test (LBIST), signal path diagnostics, and watchdogs to support safety-critical (ASIL) applications
  - 4-bit CRC on SPI
- On-chip EEPROM for storing factory and customer calibration parameters
  - Single-bit error correction, dual-bit error detection through the use of error correction control (ECC)

Continued on next page...

DESCRIPTION

The A1333 is a 360° angle sensor IC that provides contactless high-resolution angular position data based on magnetic circular vertical Hall (CVH) technology. It has a system-on-chip (SoC) architecture that includes: a CVH front end, digital signal processing, and motor commutation (UVW) or encoder outputs (A, B, I). It also includes on-chip EEPROM technology, capable of supporting up to 100 read/write cycles, for flexible end-of-line programming of calibration parameters. The A1333 is ideal for automotive applications requiring 0° to 360° angle measurements, such as electronic power steering (EPS), rotary PRNDLs, and throttle systems.

The A1333 supports customer integration into safety-critical applications.

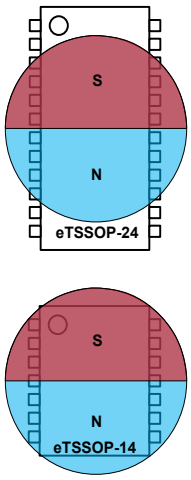
The A1333 is available in a dual-die 24-pin eTSSOP and a single-die 14-pin TSSOP package. The packages are lead (Pb) free with 100% matte tin leadframe plating.

PACKAGES:

24-pin eTSSOP (Suffix LP) 14-pin TSSOP (Suffix LE)

Not to scale

Dual Independent SoCs Single SoC



Magnet oriented for 0° output

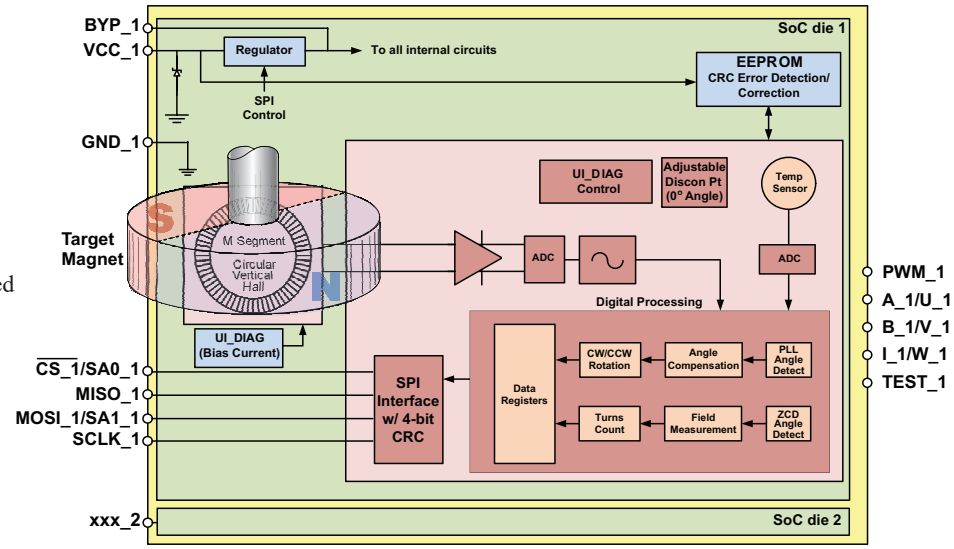


Figure 1: A1333 Magnetic Circuit and IC Diagram

FEATURES AND BENEFITS (continued)

- Supports harsh operating conditions required for automotive and industrial applications, including direct connection to 12 V battery
  - □ Operating temperature range from –40°C to 150°C
  - □ Operating supply voltage range from 4.0 to 16.5 V
    - ♦ Can support ISO 7637-2 Pulse 5b up to 39 V
- Multiple output formats supported for ease of system integration
  - □ ABI/UVW output provides high resolution, low latency, and PWM for initial position
  - □ 10 MHz SPI for low-latency angle and diagnostic data; enables multiple independent ICs to be connected to the same bus
  - □ Output resolution on ABI and UVW are selectable
- Multiple programming/configuration formats supported
  - □ The system can be completely controlled and programmed over SPI, including EEPROM writes
  - □ For system with limited pins available, writing and reading can be performed over VCC and PWM pins. This allows configuring the EEPROM in production line for a device with only ABI/UVW and PWM pins connected.
- Stacked dual-die construction to improve die-to-die matching for systems that require redundant sensors
- Reduces magnet misalignment impact on die-to-die matching for a given magnet diameter, relative to side-by-side dual-die orientation

SELECTION GUIDE

Part Number	System Die	Package	Packing	Interface Voltage
A1333LLPTR-DD-T	Dual	24-pin eTSSOP	4000 pieces per 13-in. reel	3.3 V
A1333LLETR-T	Single	14-pin TSSOP	4000 pieces per 13-in. reel	3.3 V
A1333LLPTR-5-DD-T	Dual	24-pin eTSSOP	4000 pieces per 13-in. reel	5 V
A1333LLETR-5-T	Single	14-pin TSSOP	4000 pieces per 13-in. reel	5 V

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}	Not sampling angles	26.5	V
Reverse Supply Voltage	V_{RCC}	Not sampling angles	–18	V
All Other Pins Forward Voltage	V_{IN}		5.5	V
All Other Pins Reverse Voltage	V_R		–0.5	V
Operating Ambient Temperature [1]	T_A	L range	–40 to 150	°C
Maximum Junction Temperature	T_J(max)		170	°C
Storage Temperature	T_{stg}		–65 to 170	°C

[1] Maximum operational voltage is reduced at high ambient temperatures (T_A). See Operating Characteristics, footnote 2.

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [2]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	LP-24 package	69	°C/W
		LE-14 package	82	°C/W

[2] Additional thermal information available on the Allegro website.

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Table of Contents

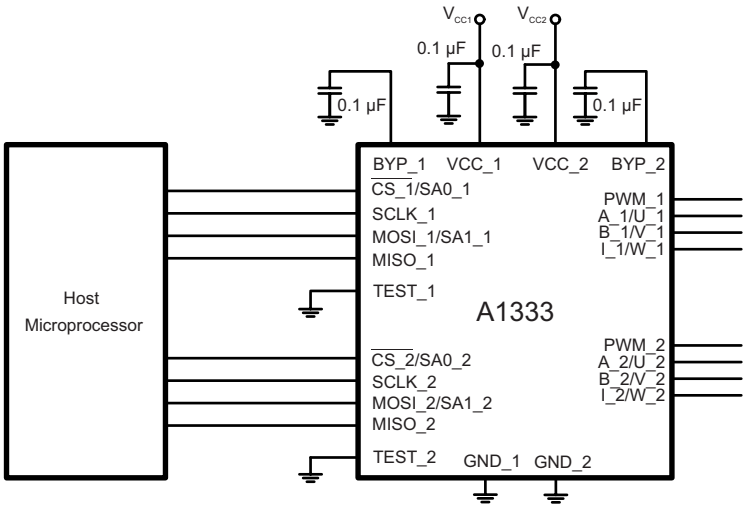

Figure 2: Typical Application Circuit

Both die are electrically separate and can be operated simultaneously using different power/GND sources.

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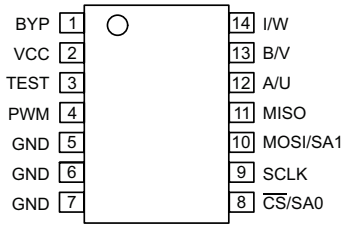
PINOUT DIAGRAMS AND TERMINAL LIST TABLES

Pinout Diagram

LE 14-Pin TSSOP



LE 14-Pin TSSOP Terminal List Table

Pin Name	Pin Number	Function
BYP	1	External bypass capacitor terminal for internal regulator
VCC	2	Power supply/Manchester input
TEST	3	Test pin; bring to GND
PWM	4	PWM angle output/Manchester output
GND	5, 6, 7	Device ground terminal
$\overline{CS}$ /SA0	8	SPI: Chip-select terminal, active low input Manchester: LSB of ID value. Tie to BYP for 1, GND for 0
SCLK	9	SPI: Clock terminal input
MOSI/SA1	10	SPI: Controller output, peripheral input Manchester: MSB of ID value. Tie to BYP for 1, GND for 0
MISO	11	SPI: Controller input, peripheral output
A/U	12	Option 1: Quadrature A output signal Option 2: U (phase 1) output signal
B/V	13	Option 1: Quadrature B output signal Option 2: V (phase 2) output signal
I/W	14	Option 1: Quadrature I (index) output signal Option 2: W (phase 3) output signal

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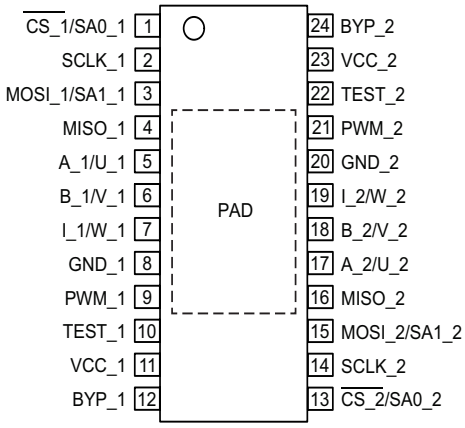
Pinout Diagram

LP 24-Pin eTSSOP



LP 24-Pin eTSSOP Terminal List Table

Pin Name	Pin Number	Function
CS_1 /SA0_1	1	SPI: Chip-select terminal, active low input (die 1) Manchester: LSB of ID value for die 1. Tie to BYP_1 for 1, GND_1 for 0
SCLK_1	2	SPI: Clock terminal input (die 1)
MOSI_1/SA1_1	3	SPI: Controller output, peripheral input (die 1) Manchester: MSB of ID value for die 1. Tie to BYP_1 for 1, GND_1 for 0
MISO_1	4	SPI: Controller input, peripheral output (die 1)
A_1/U_1	5	Option 1: Quadrature A output signal signal (die 1) Option 2: U (phase 1) output signal (die 1)
B_1/V_1	6	Option 1: Quadrature B output signal (die 1) Option 2: V (phase 2) output signal (die 1)
I_1/W_1	7	Option 1: Quadrature I (index) output signal (die 1) Option 2: W (phase 3) output signal (die 1)
GND_1	8	Device ground terminal (die 1)
PWM_1	9	PWM angle output/Manchester output (die 1)
TEST_1	10	Test pin; bring to GND (die 1)
VCC_1	11	Power supply/Manchester input (die 1)
BYP_1	12	External bypass capacitor terminal for internal regulator (die 1)
CS_2/SA0_2	13	SPI: Chip-select terminal, active low input (die 2) Manchester: LSB of ID value for die 2. Tie to BYP_2 for 1, GND_2 for 0
SCLK_2	14	SPI: Clock terminal input (die 2)
MOSI_2/SA1_2	15	SPI: Controller output, peripheral input (die 2) Manchester: MSB of ID value for die 2. Tie to BYP_2 for 1, GND_2 for 0
MISO_2	16	SPI: Controller input, peripheral output (die 2)
A_2/U_2	17	Option 1: Quadrature A output signal (die 2) Option 2: U (phase 1) output signal (die 2)
B_2/V_2	18	Option 1: Quadrature B output signal (die 2) Option 2: V (phase 2) output signal (die 2)
I_2/W_2	19	Option 1: Quadrature I (index) output signal (die 2) Option 2: W (phase 3) output signal (die 2)
GND_2	20	Device ground terminal (die 2)
PWM_2	21	PWM angle output/Manchester output (die 2)
TEST_2	22	Test pin; bring to GND (die 2)
VCC_2	23	Power supply/Manchester input (die 2)
BYP_2	24	External bypass capacitor terminal for internal regulator (die 2)
PAD	PAD	Exposed pad for thermal dissipation

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OPERATING CHARACTERISTICS: Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
ELECTRICAL CHARACTERISTICS						
Supply Voltage [2]	V_{CC}	Customer supply	4	–	16.5	V
Supply Current	I_{CC}	One die, sampling angles	–	17	19	mA
Undervoltage Flag Threshold [3]	V_{UVD}	dV/dt = 1 V/ms, A1333 sampling enabled, T_A = 25°C	3.6	–	3.9	V
Supply Zener Clamp Voltage	V_{ZSUP}	I_{CC} = I_{CC} + 3 mA, T_A = 25°C	26.5	–	–	V
Reverse Battery Current	I_{RCC}	V_{RCC} = 18 V, T_A = 25°C	–	–	5	mA
Power-On Time [4][6]	t_{PO}	Power-on diagnostics disabled	–	15	20	ms
	t_{PO_D}	Power-on time; CVH self-test and LBIST enabled	–	45	50	ms
Bypass Pin Output Voltage [5]	V_{BYP}	T_A = 25°C, C_{BYP} = 0.1 µF, 3.3 V interface	2.97	3.3	3.63	V
		T_A = 25°C, C_{BYP} = 0.1 µF, 5 V interface enabled and V_{CC} ≥ 5 V	4	5	5.5	V
SPI AND ABI (UVW) ELECTRICAL SPECIFICATIONS (3.3 V INTERFACE)						
Digital Input High Voltage	V_{IH}	MOSI, SCLK, $\overline{CS}$ pins	2.8	–	3.63	V
Digital Input Low Voltage	V_{IL}	MOSI, SCLK, $\overline{CS}$ pins	–	–	0.5	V
Output High Voltage	V_{OH}	MISO, ABI/UVW pins, C_L = 20 pF	2.93	3.3	3.63	V
Output Low Voltage	V_{OL}	MISO, ABI/UVW pins, C_L = 20 pF	–	0.3	–	V
SPI AND ABI (UVW) ELECTRICAL SPECIFICATIONS (5.0 V INTERFACE)						
Digital Input High Voltage	V_{IH}	MOSI, SCLK, $\overline{CS}$ pins	3.75	–	5.5	V
Digital Input Low Voltage	V_{IL}	MOSI, SCLK, $\overline{CS}$ pins	–	–	0.5	V
Output High Voltage	V_{OH}	MISO, ABI/UVW pins, C_L = 20 pF, V_{CC} ≥ 5 V	4	5	5.5	V
Output Low Voltage	V_{OL}	MISO, ABI/UVW pins, C_L = 20 pF	–	0.3	–	V
SPI INTERFACE SPECIFICATIONS						
SPI Clock Frequency [6]	f_{SCLK}	MISO pins, C_L = 20 pF	0.1	–	10	MHz
SPI Clock Duty Cycle [6]	D_{fSCLK}	SPI_{CLKDC}	40	–	60	%
SPI Frame Rate [6]	t_{SPI}	16-bit SPI packet	5.8	–	588	kHz
Chip Select to First SCLK Edge [6]	t_{CS}	Time from $\overline{CS}$ going low to SCLK falling edge	50	–	–	ns
Chip Select Idle Time [6]	t_{CS_IDLE}	Time $\overline{CS}$ must be high between SPI message frames	200	–	–	ns
Data Output Valid Time [6]	t_{DAV}	Data output valid after SCLK falling edge	–	30	–	ns
MOSI Setup Time [6]	t_{SU}	Input setup time before SCLK rising edge	25	–	–	ns
MOSI Hold Time [6]	t_{HD}	Input hold time after SCLK rising edge	50	–	–	ns
SCLK to CS Hold Time [6]	t_{CHD}	Hold SCLK high time before $\overline{CS}$ rising edge	5	–	–	ns
Load Capacitance [6]	C_L	Loading on digital output (MISO) pin	–	–	20	pF

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OPERATING CHARACTERISTICS (continued): Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
PWM INTERFACE SPECIFICATIONS						
PWM Carrier Frequency	f_{PWM}	PWM frequency minimum setting	–	98	–	Hz
		PWM programmable options (7 bits)	–	128	–	options
		PWM frequency maximum setting	–	3.125	–	kHz
PWM Output Low Clamp	$D_{PWM(min)}$	Corresponding to digital angle of 0x000	–	5	–	%
PWM Output High Clamp	$D_{PWM(max)}$	Corresponding to digital angle of 0xFFF	–	95	–	%
INCREMENTAL OUTPUT, ABI (UVW) SPECIFICATIONS						
ABI and UVW Output Angular Hysteresis [6]	hys_{ANG}	Programmable via EEPROM (6 bits)	0	–	1.38	degrees
AB Channel Resolution [6]	RES_{AB}	Programmable via EEPROM, 4-bit field Specified in pulses per revolution, PPR	1	–	2048	PPR
AB Quadrature Resolution [6]	RES_{AB_INT}	Equal to 4 × RES_{AB}, specified in counts per revolution, CPR	4	–	8192	CPR
UVW Pole Pairs [6]	N_{pole}	DC commutation signals Programmable via EEPROM, 4-bit field	1	–	16	pole pairs
Maximum Sourcing Current	I_{SOURCE}	Output voltage ≥ 2.5 V	–	1.5	–	mA
Maximum Sinking Current	I_{SINK}	5 V IO setting; output voltage ≈ 0.35 V	–	4.5	–	mA
MANCHESTER INTERFACE SPECIFICATIONS						
Manchester High Voltage	$V_{MAN(H)}$	Applied to VCC line	7.3	8	$V_{CC(max)}$	V
Manchester Low Voltage	$V_{MAN(L)}$	Applied to VCC line	$V_{CC(min)}$	5	5.7	V
Manchester Bit Rate	f_{MAN}	Line state changes once or twice per bit Maximum speed is usually limited by VCC line capacitance	2.2	–	100	kbit/s
BUILT-IN SELF-TEST						
Logic BIST Time	t_{LBIST}	Configurable to run on power-up or on user request Runs in parallel with CVH self-test (if enabled)	–	30	–	ms
Circular Vertical Hall Self-Test Time	t_{CVHST}	Configurable to run on power-up or on user request Runs in parallel with LBIST (if enabled)	–	30	–	ms
MAGNETIC CHARACTERISTICS						
Magnetic Field	B	Range of input field	–	–	1200	G

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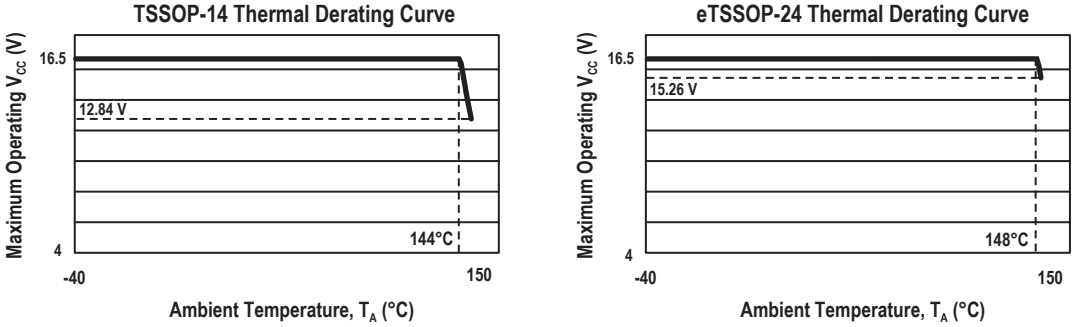
OPERATING CHARACTERISTICS (continued): Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
ANGLE CHARACTERISTICS						
Output [7]	RES_{ANGLE}	Both 12- and 15-bit angle values are available via SPI	–	12/15	–	bit
Angle Refresh Rate [8]	t_{ANG}	ORATE = 0	–	1	–	µs
Response Time [6]	$t_{RESPONSE}$	Angular latency; valid for ABI or UVW interface; ORATE = 0	–	7	–	µs
Angle Error	ERR_{ANG}	T_A = 25°C, ideal magnet alignment, B = 300 G, target rpm = 0	–1	±0.4	+1	degrees
		T_A = 150°C, ideal magnet alignment, B = 300 G, target rpm = 0	–1.3	±0.6	+1.3	degrees
Temperature Drift	$ANGLE_{DRIFT}$	T_A = 150°C, B = 300 G, angle change from 25°C	–1.4	–	1.4	degrees
		T_A = –40°C, B = 300 G, angle change from 25°C	–	0.9	–	degrees
Angle Noise [9]	N_{ANG}	T_A = 25°C, B = 300 G, no internal filtering, target rpm = 0, 3-sigma noise	–	±0.19	–	degrees
		T_A = 150°C, no internal filtering, B = 300 G, target rpm = 0, 3-sigma noise	–	±0.25	–	degrees
Effective Resolution [10]		B = 300 G, T_A = 25°C	–	12.5	–	bits
Angle Drift Over Lifetime [11]	$ANGLE_{Drift\_Life}$	B = 300 G, average maximum drift observed following AEC-Q100 qualification testing	–	0.5	–	degrees

[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] Maximum operational voltage is reduced at high ambient temperatures (T_A). See plots below.



[3] Undervoltage flag indicates V_{CC} level below expected operational range. Degraded sensor accuracy may result.
[4] During the power-on phase, the A1333 SPI transactions are valid within ≈ 300 µs of power on (with no self-tests). Angle reading requires full t_{PO} to stabilize.
[5] The output voltage specification is to aid in PCB design. The pin is not intended to drive any external circuitry. The specifications indicate the peak capacitor charging and discharging currents to be expected during typical operation.
[6] Parameter is not guaranteed at final test. Determined by design.
[7] RES_{ANGLE} represents the number of bits of data available for reading from the die registers.
[8] The rate at which a new angle reading becomes ready.
[9] This value represents 3-sigma or three times the standard deviation of the measured samples.
[10] Effective resolution is calculated using:

$$log_2(360) - log_2\left(\frac{1}{n}\sum_{i=1}^{n}\sigma_i\right)$$

where σ is the standard deviation based on 30 averaged measurements taken at each of the 32 angular positions, I = 11.25, 22.5, … 360.
[11] Maximum observed angle drift following AEC-Q100 stress is 1.37 degrees.

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TYPICAL PERFORMANCE CHARACTERISTICS

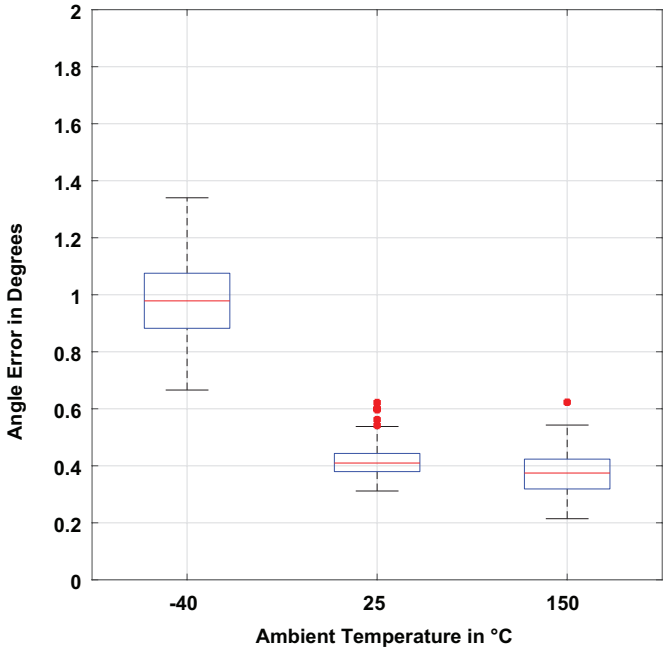

Figure 3: Peak Angle Error over Temperature [1] (300 G)

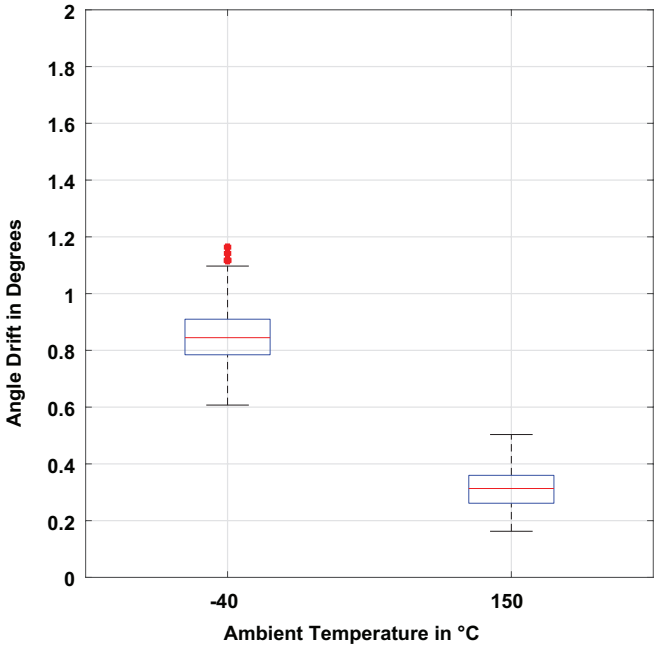

Figure 4: Maximum Absolute Drift from 25°C Reading [1] (300 G)

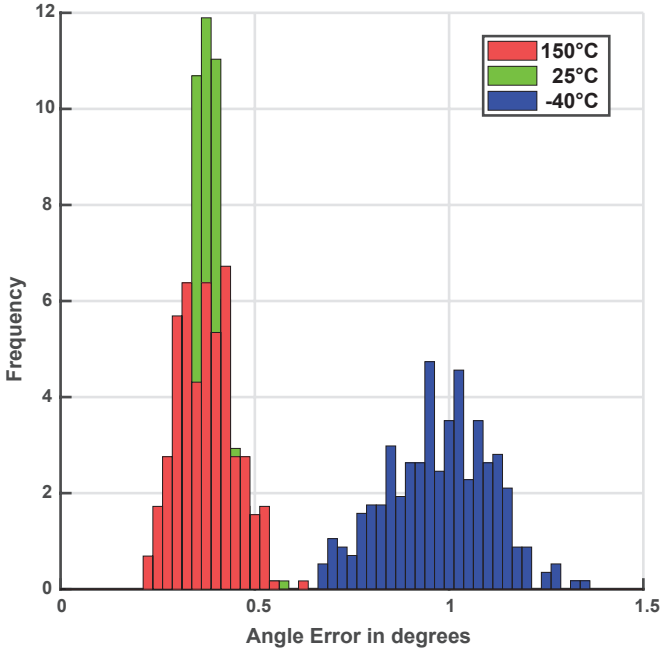

Figure 5: Peak Angle Error Distributions over Temperature (300 G)

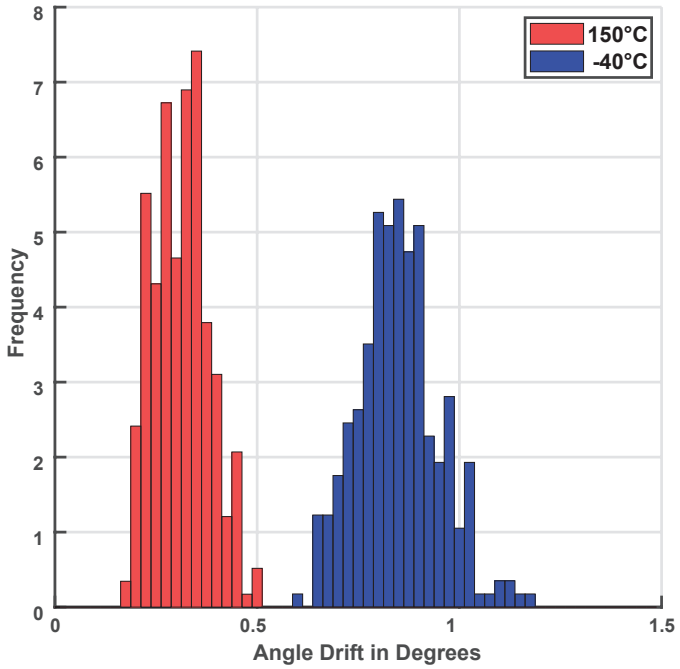

Figure 6: Angle Drift from 25°C (300 G)

[1] Central mark indicates median value. Bottom and top edges of the box indicate the 25th and 75th percentiles. Whiskers extend to the most extreme data points not defined as outliers. Outliers are shown in red. Outliers are defined as those points outside Q1 or Q3 by more than 1.5 times the inter-quartile range (≈ 2.7 σ away from the center of the distribution).

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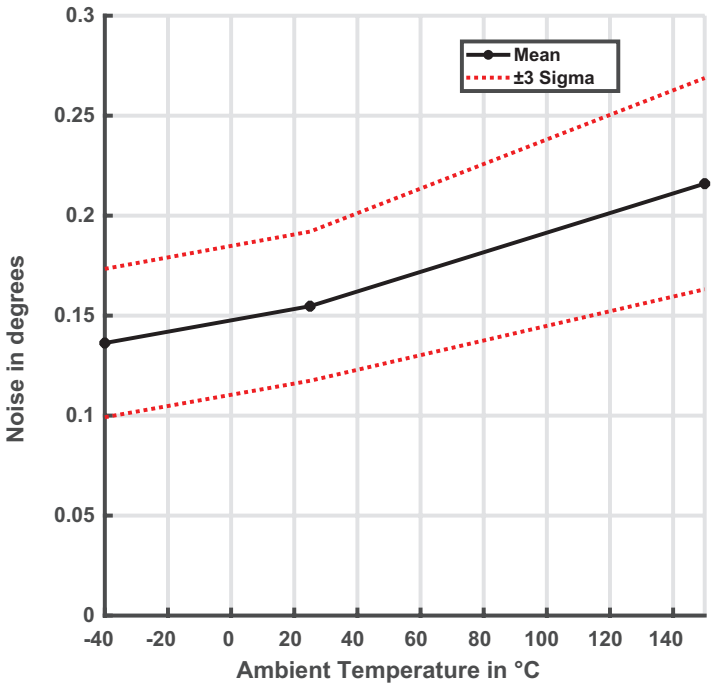

Figure 7: Noise Performance over Temperature (3 Sigma, 300 G)

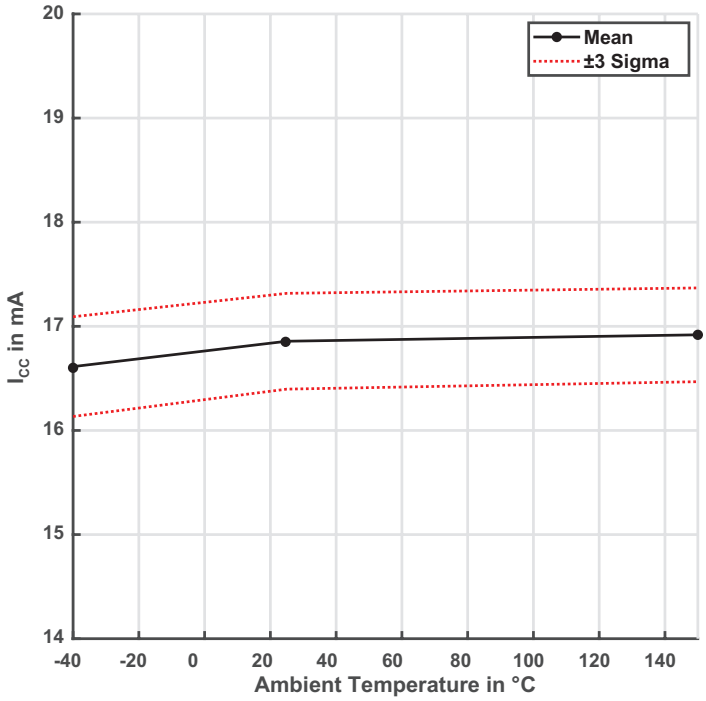

Figure 8: I_{CC} over Temperature (V_{CC} = 16.0 V)

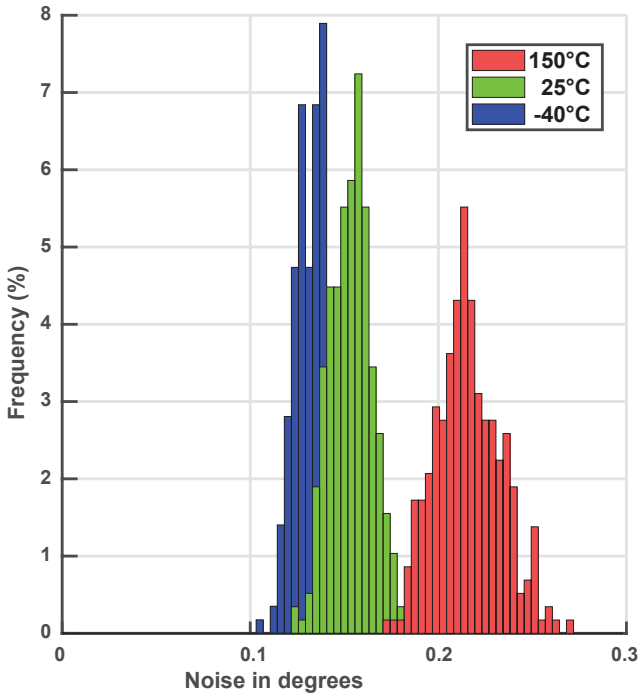

Figure 9: Noise Distribution over Temperature (3 Sigma, 300 G)

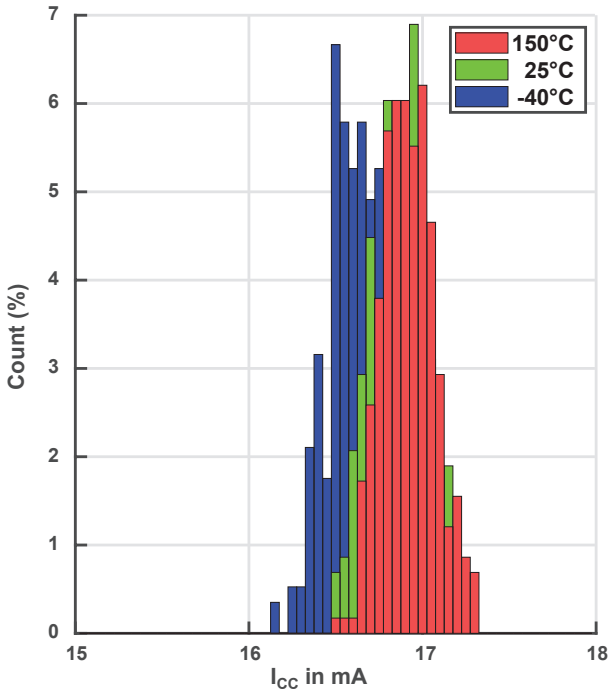

Figure 10: I_{CC} Distribution over Temperature (V_{CC} = 16.0 V)

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TYPICAL PERFORMANCE OF FIELD AND TEMPERATURE

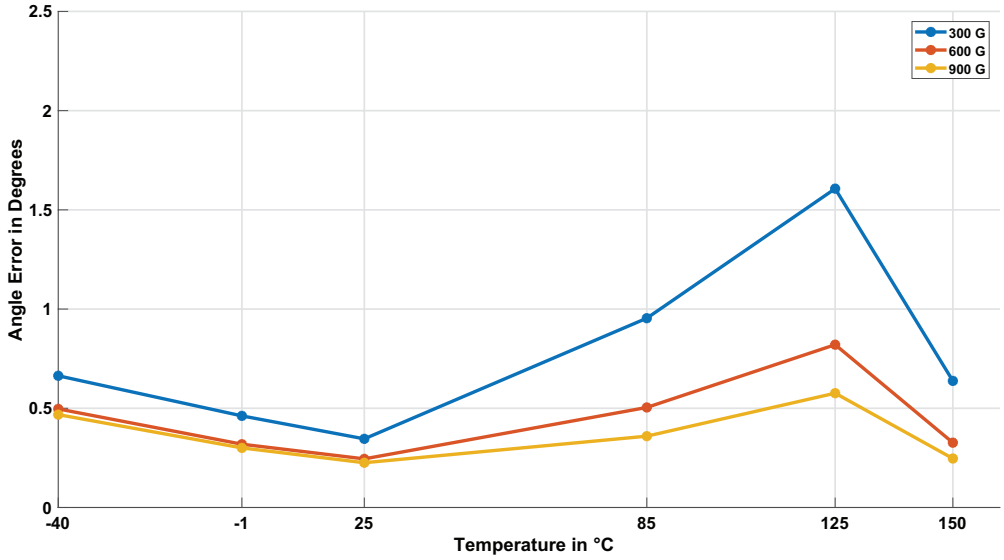

Figure 11: Average Angle Error over Temperature Across 10 Devices

Recommended operating range: 300 G and above

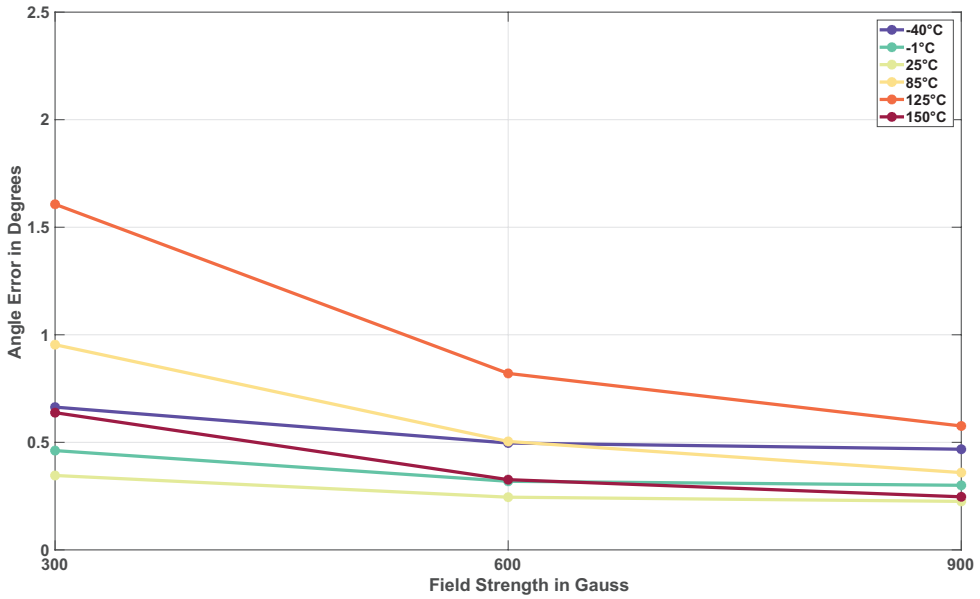

Figure 12: Average Angle Error over Field

Recommended operating range: 300 G and above

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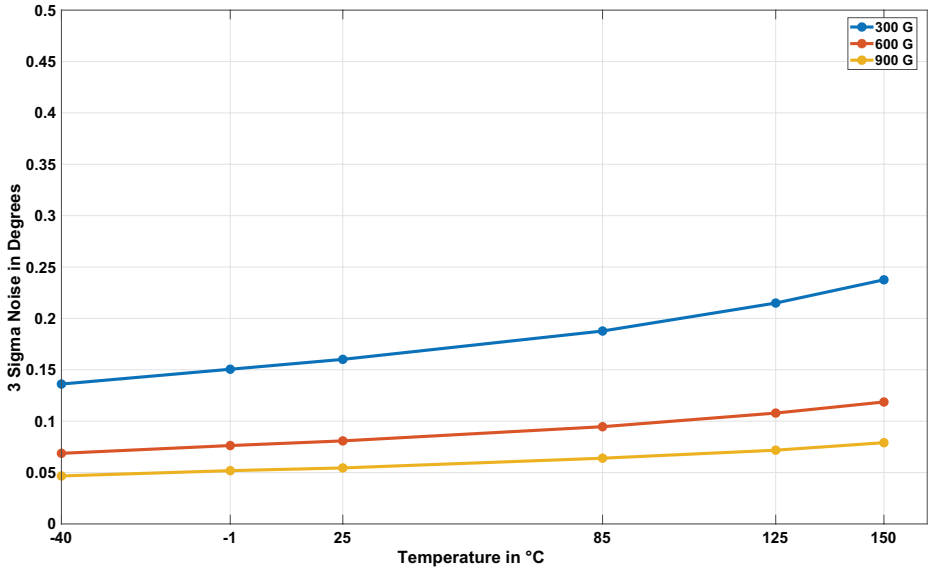

Figure 13: Average 3-Sigma Angle Noise over Temperature

Recommended operating range: 300 G and above

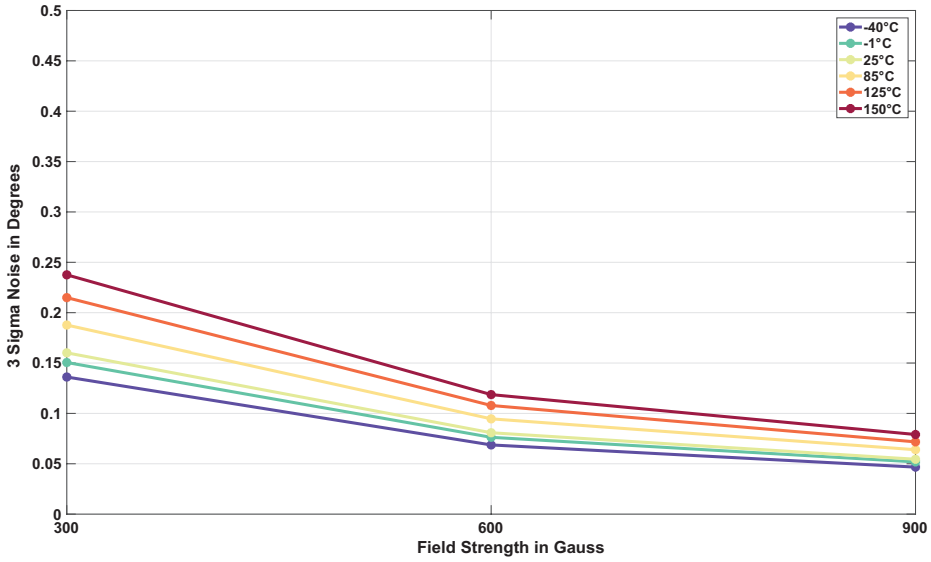

Figure 14: Average 3-Sigma Angle Noise over Field

Recommended operating range: 300 G and above

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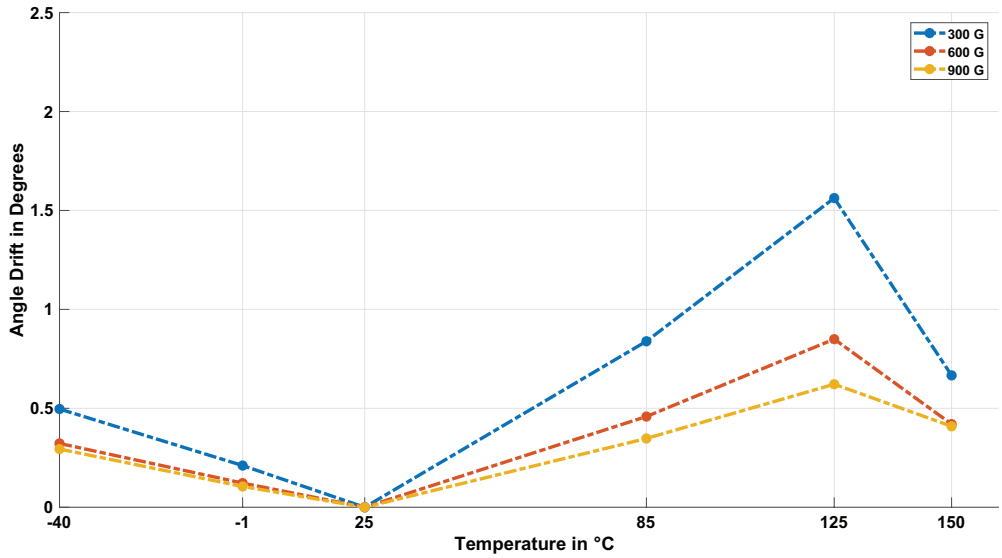

Figure 15: Average Angle Drift over Temperature Across 10 Devices

Recommended operating range: 300 G and above

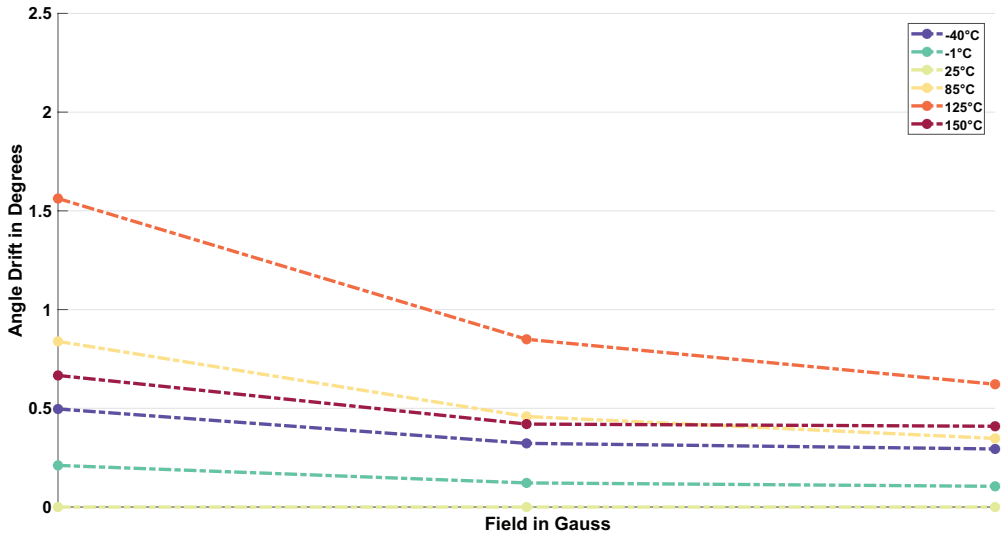

Figure 16: Average Angle Drift over Field Across 10 Devices

Recommended operating range: 300 G and above

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FUNCTIONAL DESCRIPTION

Overview

The A1333 is a rotary position Hall-sensor-based device in a surface-mount package, providing solid-state consistency, reliability, and supporting a wide variety of automotive applications. The Hall-sensor-based device measures the direction of the magnetic field vector through 360° in the x-y plane (parallel to the branded face of the device) and computes an angle measurement based on the actual physical reading, as well as any internal parameters that have been set by the user. The output is used by the host microcontroller to provide a single channel of target data.

This device is an advanced, programmable system-on-chip (SoC). Each integrated circuit includes a circular vertical Hall (CVH) analog front end, a high-speed sampling analog-to-digital converter (ADC), digital filtering, digital signal processing (which includes two separate signal paths), SPI, PWM, motor commutation outputs (UVW), and encoder outputs (A, B, I).

Offset, filtering, and diagnostic adjustment options are available in the A1333. These options can be configured in onboard EEPROM, providing a wide range of sensing solutions in the same device. Device performance can be optimized by enabling individual functions or disabling them in EEPROM to minimize latency.

Angle Measurement

The IC features two digital signal paths. The main signal path uses a PLL to generate high-resolution, low-latency angle readings. A secondary, lower-power signal path (referred to as the ZCD path) is used for turns-counting, magnetic-field measurement, and diagnostic comparison.

The A1333 is capable of tracking magnet position at high speed. Performance up to 12,000 rpm has been verified by testing. Operation up to 30,000 rpm has been verified via design simulation.

The A1333 has a typical refresh rate of 1 MHz.

Angle is represented as either a 12- or 15-bit value, based on the register address accessed.

12-Bit Angle Value; Serial Register 0x20

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	EF	UV	P	ANGLE [11:0]											

15-Bit Angle Value; Serial Register 0x32

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	ANGLE [14:0]														

When reading the 12-bit angle value, 3 additional status bits are provided with each packet: a general error flag (EF), undervoltage flag (UV), and a parity bit (P).

PWM output is always resolved to a 12-bit angle value. ABI/UVW operates on a 15-bit angle representation.

The zero-degree position may be adjusted by writing to EEPROM.

The sensor readout is processed in various steps. These are detailed in Figure 21.

System-Level Timing

Internal registers are updated with a new angle value every t_{ANG}. Due to signal-path delay, the angle is $t_{RESPONSE}$ old at each update. In other words, $t_{RESPONSE}$ is the delay from time of magnet sampling until generation of a processed angle value. SPI, which is asynchronously clocked, results in a varying latency depending on sampling frequency and SCLK speed. The values presented to the user are latched on the first SCLK edge of the SPI response frame. This results in a variable age of the angle data, ranging from $t_{RESPONSE} + t_{SPI}$ to $t_{RESPONSE} + t_{ANG} + t_{SPI}$, where t_{SPI} is the length of a read response packet, and t_{ANG} is the update rate of the angle register.

Similar to SPI, when using the PWM output, the output packet is not synchronized with the internal update rate of the sensor. The angle is latched at the beginning of the carrier frequency period (effectively at the rising edge of the PWM output). Because of this, the age of the angle value, once read by the system microcontroller, may be up to $t_{RESPONSE} + t_{ANG} + 1/f_{PWM}$.

The update rate and the signal delay of the different angle output paths depending on sensor settings are shown in Figure 20.

The value of the ANGLE_ZCD (ZCD signal path) register is updated approximately every 32 µs. The field strength reading (register 0x2A) is updated approximately every 128 µs.

Impact of High-Speed Sensing

Due to signal-path latency, the angle data is delayed by $t_{RESPONSE}$. This delay equates to a greater angle value as the rotational velocity increases (i.e., a magnet rotating at 20,000 rpm traverses twice as much angular distance in a fixed time period as a magnet rotating at 10,000 rpm), and is referred to as angular lag.

The lag is directly proportional to rpm, and compensation for this lag can be made externally if the velocity is known.

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Angular lag can be expressed using the following equation:

$$Ang\_Lag = \frac{rpm \times 6}{1{,}000{,}000} \times t_{RESPONSE}$$

where *rpm* represents the rotational velocity of the magnet, *Angle_Lag* is expressed in degrees, and $t_{RESPONSE}$ is in µs.

The expected angular lag over rpm is shown in Figure 17.

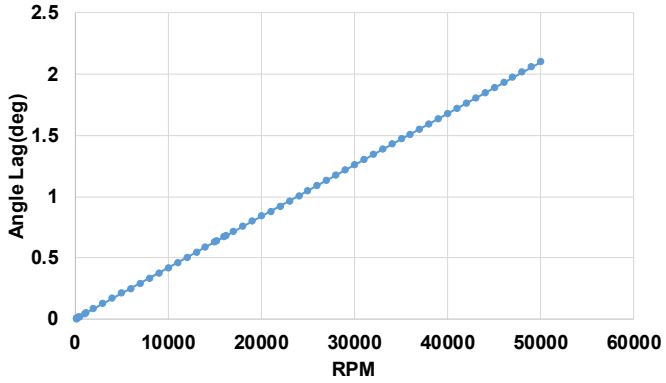

Figure 17: Expected Angle Lag vs. RPM

Measured Performance Over RPM

The measured performance of the A1333 at speeds up to 12,000 rpm is shown in Figure 18 and Figure 19, where data was taken with no internal averaging (ORATE = 0).

The measured angle lag over increasing rpm is shown in Figure 18. Data was collected by triggering SPI angle reads from a high-precision encoder. To present data independent of output protocol, the delay due to SPI packet transmission has been removed from the plot. As such, the plot shows the angle lag due to signal-path delays only.

Figure 19 depicts the equivalent response time (in µs), derived from the slope of Figure 18. The measured response times range between 6.5 and 7.6 µs.

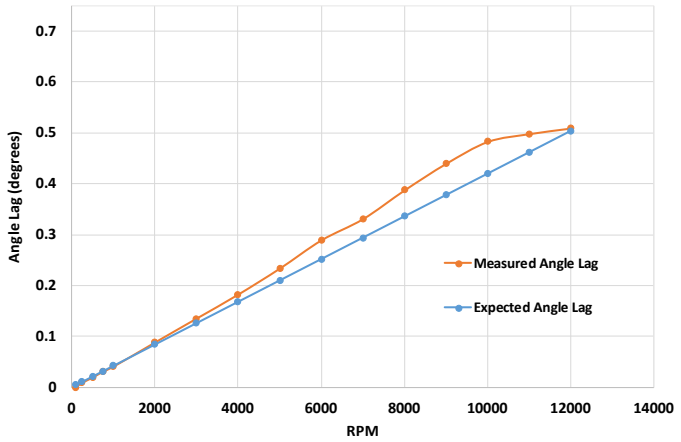

Figure 18: Measured Angle Lag vs. RPM

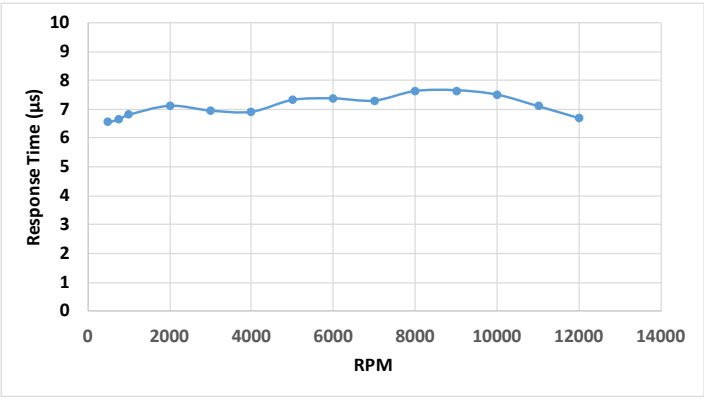

Figure 19: Measured Response Time Over RPM

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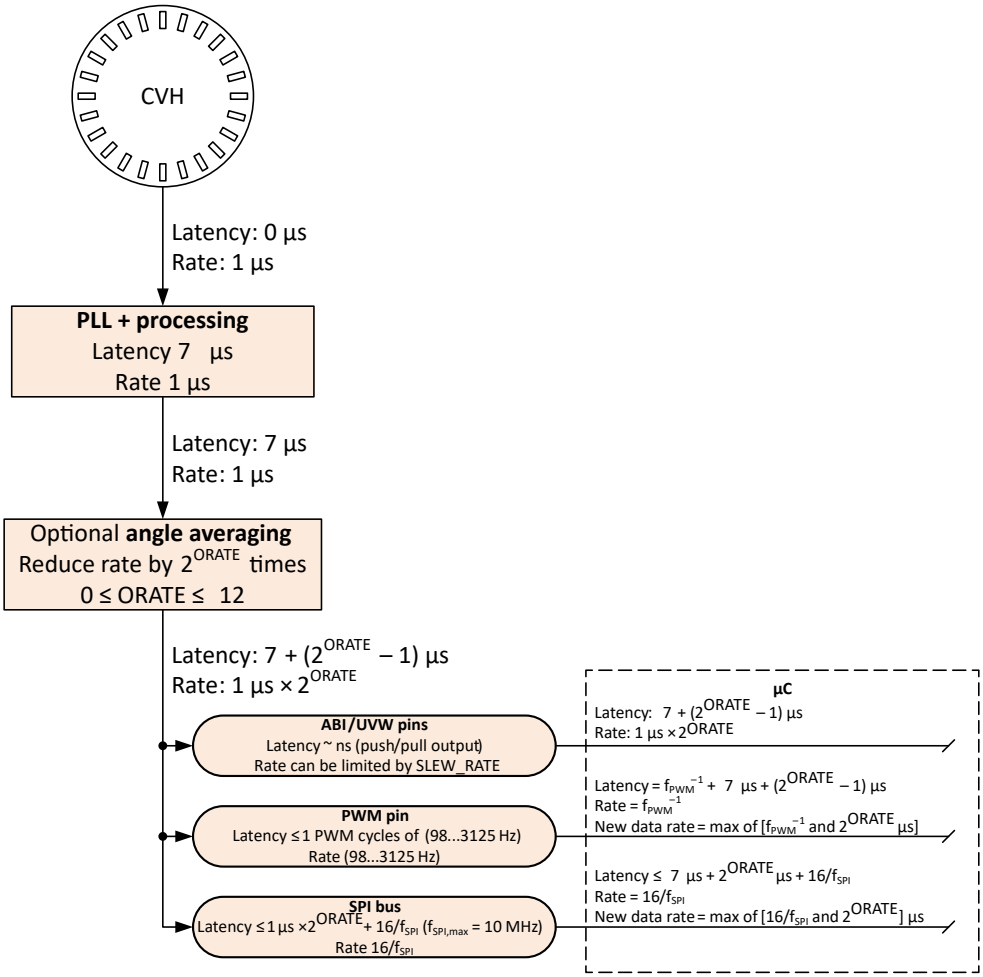

Figure 20: Update Rate and Signal Delay

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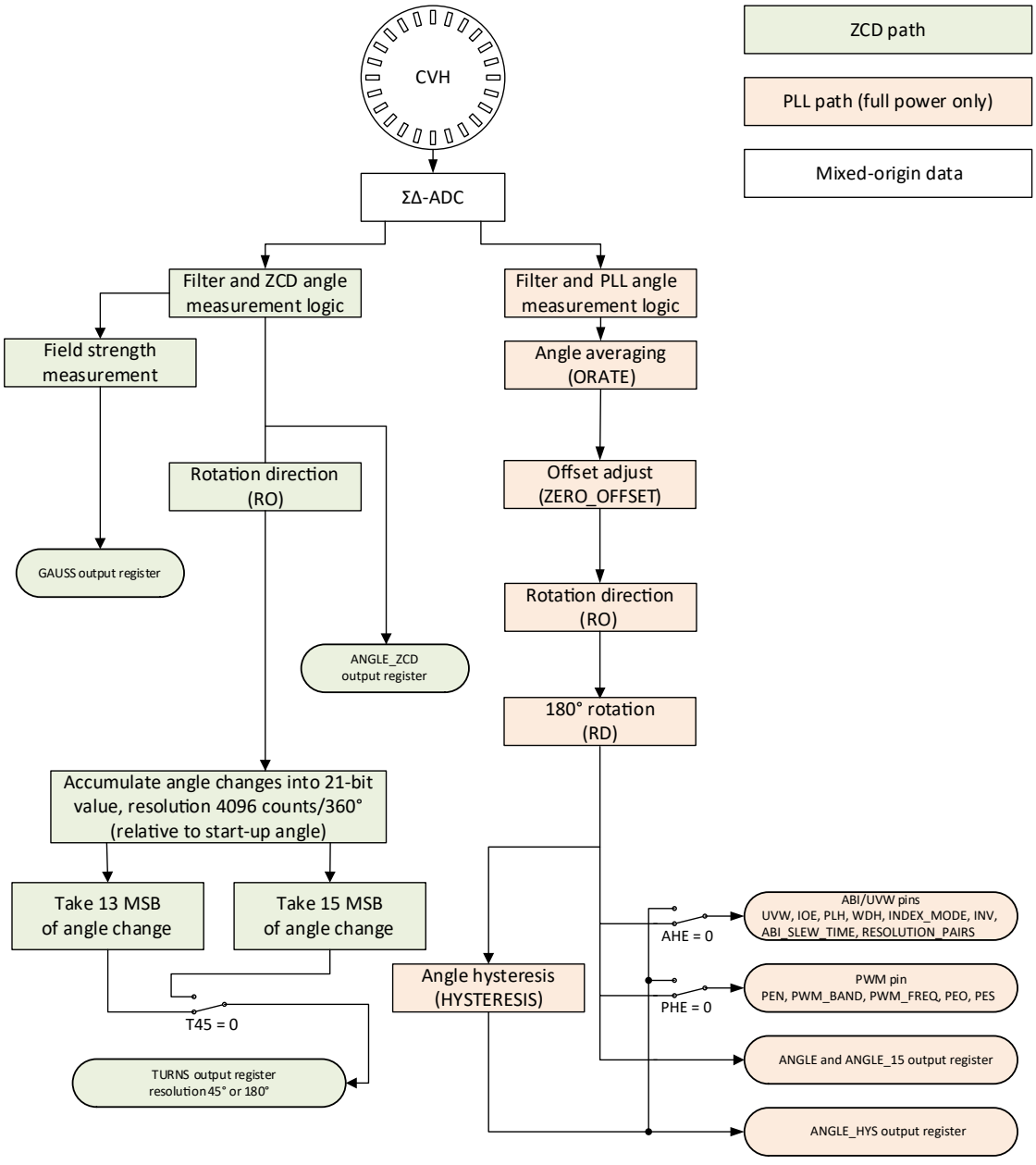

Figure 21: Angle Measurement—Sensor Readout Steps

Names in all capitals correspond to EEPROM or serial register fields.

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Power-Up

Upon applying power to the A1333, the device automatically runs through an initialization routine. The purpose of this initialization is to ensure that the device comes up in the same predictable operating condition every power cycle. This initialization routine takes time to complete, which is referred to as power-on time, t_{PO}. Regardless of the state of the device before a power cycle, the device repowers with the shadow memory contents copied from the EEPROM anew, and serial registers in their default states. For example, on every power-up, the device powers with the ZERO_OFFSET that was stored in the EEPROM. The extended write access field, WRITE_ADR, is set back to its default value, zero.

PWM Output

The A1333 provides a pulse-width-modulated open-drain output, with the duty cycle (DC) proportional to measured angle. The PWM duty cycle is clamped at 5% and 95% for diagnostics purposes. A 5% DC corresponds to 0°; a 95% DC corresponds to 360°.

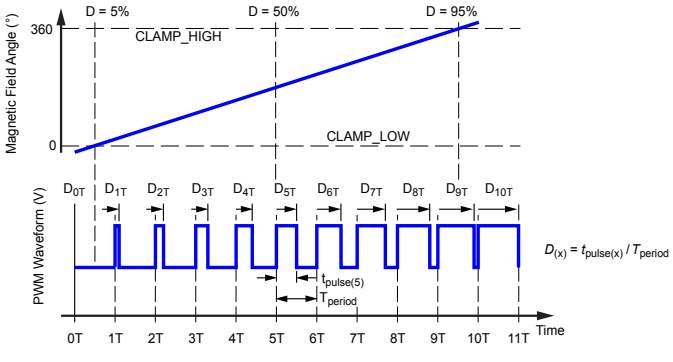

Figure 22: PWM Mode Outputs a Duty-Cycle Proportional To Sensed Angle

Within each cycle, the output is high for the first 5% and low for the last 5% of the period. The middle 90% of the period is a linear interpolation of the angle as sampled at the start of the PWM period.

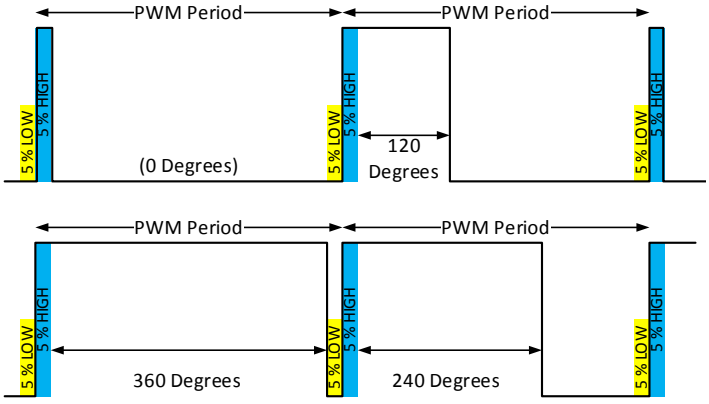

Figure 23: Pulse-Width Modulation (PWM) Examples

The angle is represented in 12-bit resolution and can never reach 360°. The maximum duty cycle high period is:

$$\text{DutyCycleMax (\%)} = (4095 / 4096) \times 90 + 5 .$$

PWM CARRIER FREQUENCY

The PWM carrier frequency is controlled via two EEPROM fields, both of which are found in the PWS row.

- PWM_FREQ
- PWM_BAND

Together, these two fields allow 128 different PWM carrier frequencies to be selected.

Table 1: PWM Carrier Frequencies in Hz

		PWM_BAND							
		0	1	2	3	4	5	6	7
PWM_FREQ	0	3125	2778	2273	1667	1087	641	352	185
	1	3101	2740	2222	1613	1042	610	333	175
	2	3077	2703	2174	1563	1000	581	316	166
	3	3053	2667	2128	1515	962	556	301	157
	4	3030	2632	2083	1471	926	532	287	150
	5	3008	2597	2041	1429	893	510	275	143
	6	2985	2564	2000	1389	862	490	263	137
	7	2963	2532	1961	1351	833	472	253	131
	8	2941	2500	1923	1316	806	455	243	126
	9	2920	2469	1887	1282	781	439	234	121
	10	2899	2439	1852	1250	758	424	225	116
	11	2878	2410	1818	1220	735	410	217	112
	12	2857	2381	1786	1190	714	397	210	108
	13	2837	2353	1754	1163	694	385	203	105
	14	2817	2326	1724	1136	676	373	197	101
	15	2797	2299	1695	1111	658	362	191	98

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Incremental Output Interface (ABI)

The A1333 offers an incremental output mode in the form of quadrature A/B and index outputs to emulate an optical or mechanical encoder. The A and B signals toggle with a 50% duty cycle (relative to angular distance, not necessarily time) at a frequency of 2^N cycles per magnetic revolution, giving a cycle resolution of $(360 / 2^N)$ degrees per cycle, where N is set by the RESOLUTION_PAIRS field in EEPROM; see Table 2. B is offset from A by ¼ of the cycle period. The "I" signal is an index pulse that occurs once per revolution to mark the zero (0) angle position. One revolution is shown in Figure 24.

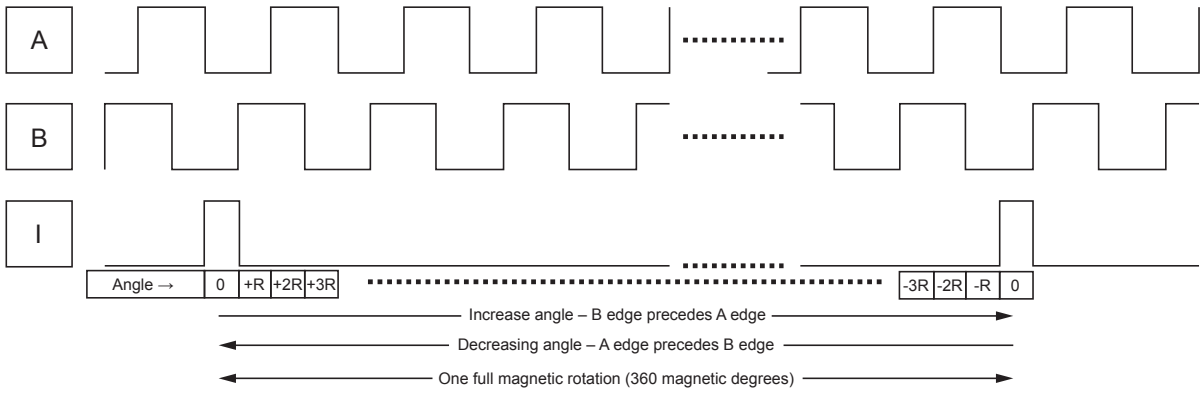

Figure 24: One Full Magnetic Revolution

Because A and B are offset by ¼ of a cycle, they are in *quadrature* and together have four unique states per cycle. Each state represents $R = [360 \div (4 \times 2^N)]$ degrees of the full revolution. This angular distance is the quadrature resolution of the encoder. The order in which the states change, or the order of the edge transitions from A to B, allow the direction of rotation to be determined. If a given B edge (rising/falling) precedes the following A edge, the angle is increasing from the perspective of the electrical (sensor) angle, and the angle position should be incremented by the quadrature resolution (R) at each state transition. Conversely, if a given A edge precedes the following B edge, the angle is decreasing from the perspective of the electrical (sensor) angle, and the angle position should be decremented by the quadrature resolution (R) at each state transition. The angle position accumulator wraps each revolution back to 0.

The quadrature states are designated as Q1 through Q4 in the following diagrams, and are defined as follows:

State Name	A	B
Q1	0	0
Q2	0	1
Q3	1	1
Q4	1	0

Note that the A/B progression is a grey coding sequence where only one signal transitions at a time. The state progression must be as follows to be valid:

Increasing angle: Q1 → Q2 → Q3 → Q4 → Q1 → Q2 → Q3 → Q4

Decreasing angle: Q4 → Q3 → Q2 → Q1 → Q4 → Q3 → Q2 → Q1

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The duration of one cycle is referred to as 360 *electrical degrees*, or 360e. One half of a cycle is therefore 180e and one quarter of a cycle (one quadrature state, or R degrees) is 90e. This is the terminology used to express variance from perfect signal behavior. Ideally, the A and B cycle are as shown in Figure 25 for a constant velocity.

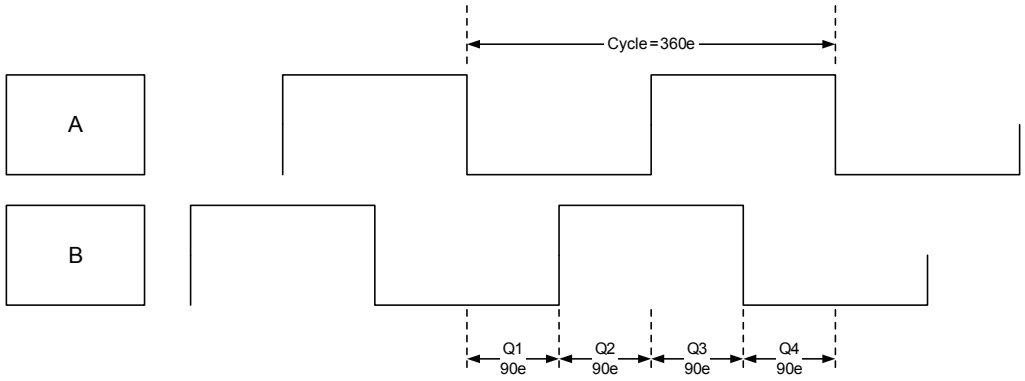

Figure 25: Electrical Cycle

In reality, the edge rate of the A and B signals, and the switching threshold of the receiver inputs/outputs (I/Os) affect the quadrature periods as shown in Figure 26.

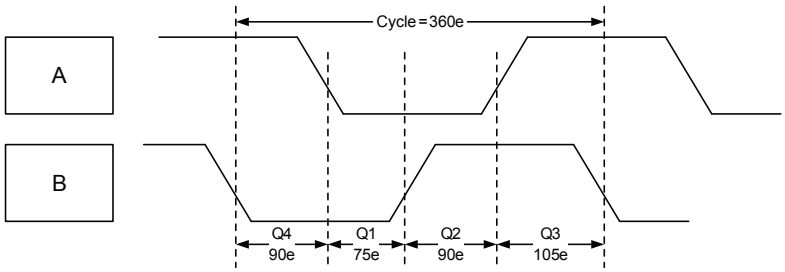

Figure 26: Electrical Cycle

Here, an exaggeration of the switching thresholds shows that Q4 and Q2, which are fall-fall and rise-rise, have the expected 90e period, whereas Q1 is less than expected and Q3 is greater than expected due to imbalance in switching thresholds.

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ABI RESOLUTION

The A1333 supports the ABI output resolutions shown in Table 2. This is set via the RESOLUTION_PAIRS field in EEPROM and shadow (EEPROM 0x19, bits 3:0).

ABI INVERSION

The logic levels of the ABI pins may inverted by setting the ABI.INV bit within EEPROM. This also applies if using the UVW output logic.

Table 2: ABI Output Resolution

EEPROM Resolution Field	Cycle Resolution (Bits = N)	Quadrature Resolution (Bits = 4 × N)	Cycles per Revolution (A or B)	Quadrature States per Revolution	Cycle Resolution (Degrees)	Quadrature Resolution (R) (Degrees)
0	Factory Use Only					
1	Factory Use Only					
2	Factory Use Only					
3	11	13	2048	8192	0.176	0.044
4	10	12	1024	4096	0.352	0.088
5	9	11	512	2048	0.703	0.176
6	8	10	256	1024	1.406	0.352
7	7	9	128	512	2.813	0.703
8	6	8	64	256	5.625	1.406
9	5	7	32	128	11.25	2.813
10	4	6	16	64	22.5	5.625
11	3	5	8	32	45	11.25
12	2	4	4	16	90	22.5
13	1	3	2	8	180	45
14	0	2	1	4	360	90
15	–	–	–	–	–	–

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INDEX PULSE

The index pulse, I (or Z in some descriptions), marks the absolute zero (0) position of the encoder. Under rotation, this allows the receiver to synchronize to a known mechanical/magnetic position, and then use the incremental A/B signals to keep track of the absolute position. To support a range of ABI receivers, the I pulse has four widths, defined by the INDEX_MODE EEPROM field, as shown in Figure 27.

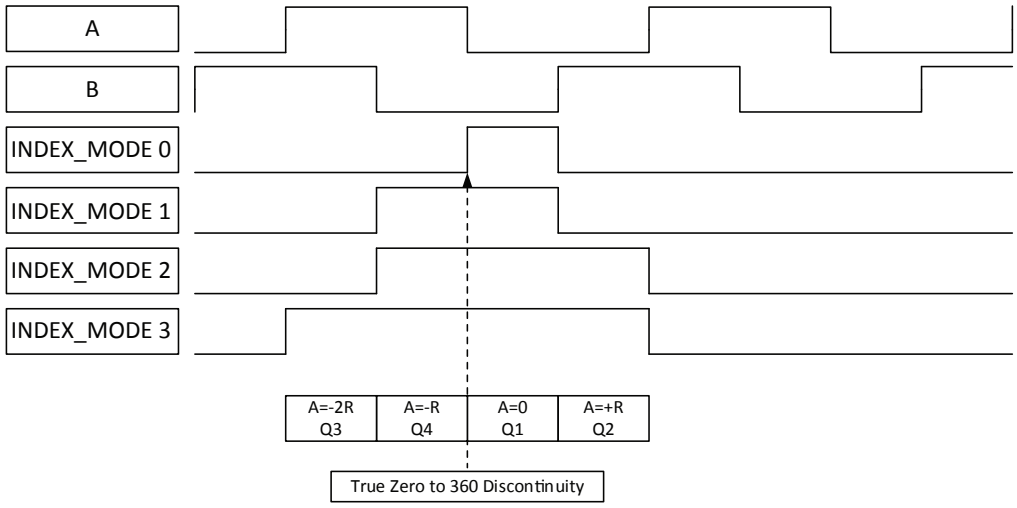

Figure 27: Index Pulse

ABI BEHAVIOR AT POWER-UP

At power-up, the A1333 requires time to acquire a stable angle value; this is quantified by t_{PO} (or t_{PO_D}, if power-on diagnostics are used). Because the angle value is not guaranteed to be stable between power-on and t_{PO}, the output of the ABI should be ignored until at least t_{PO} after power-on.

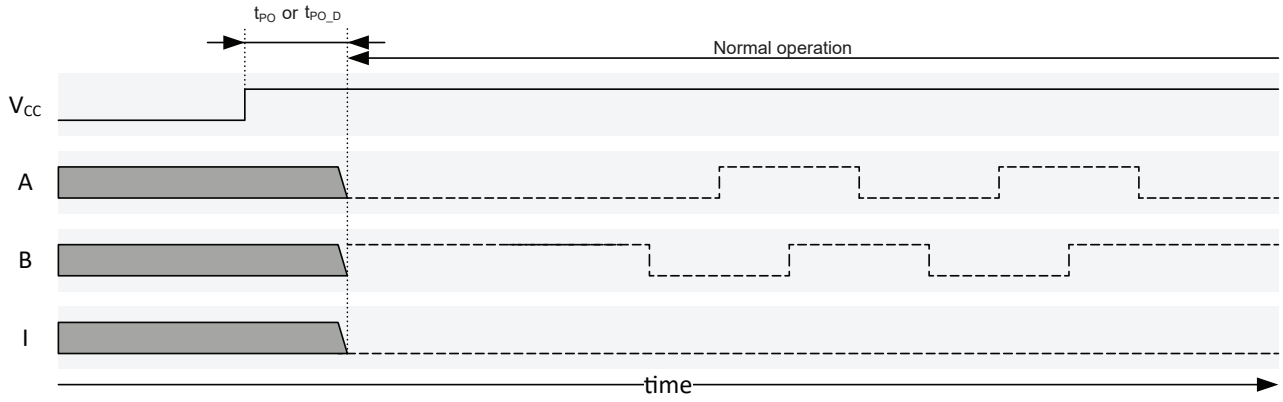

Figure 28: ABI Startup Behavior

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ZERO-DEGREE POSITION INDICATION

The edge of the index pulse corresponding to the “zero” position, as observed by the sensor, changes based on rotation direction, as shown in Figure 29.

With the magnet rotating such that the observed angle is increasing, the 0° position is indicated by the rising edge of the index pulse. If the magnet is rotated in the opposite direction (or the RO bit is changed in EEPROM) to produce a decreasing angle value, the 0° position is represented by the falling edge of the index pulse.

The ABI resolution and I pulse-mode selection (described above) determine the width of the index pulse and the corresponding shift in the zero-position indication.

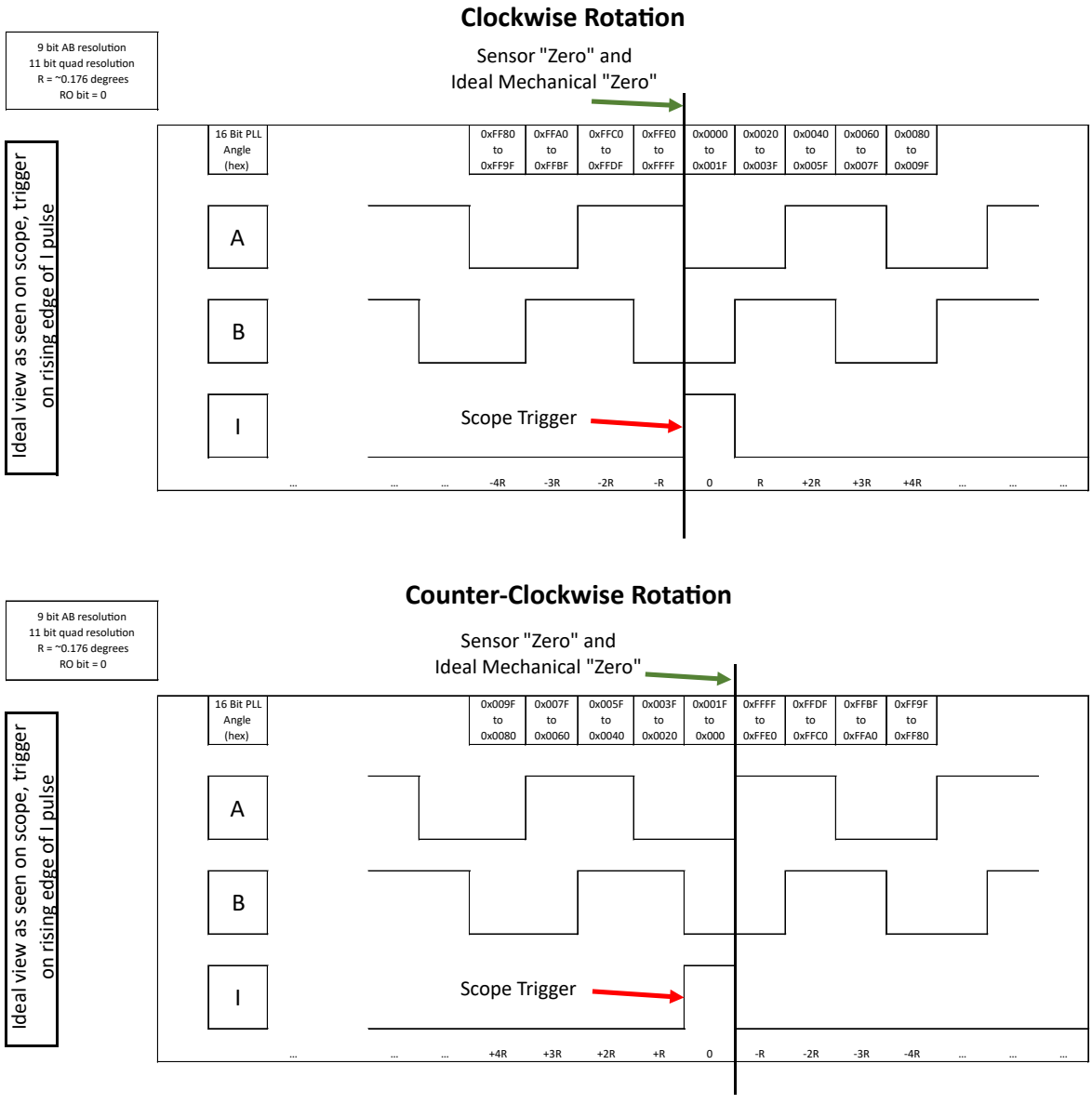

Figure 29: Index Pulse Corresponding to “Zero” Position

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SLEW-RATE LIMITING FOR ABI

Slew-rate limiting is enabled when the ABI_SLEW_TIME field is non-zero. This option separates the sensor's observed angle change from the ABI output rate, and can be used to control two circumstances:

- The angle sample does not monotonically increase or decrease at the quadrature resolution, thereby "skipping" one or more quadrature states. In this case, the slew-rate limiting logic transitions the ABI signals in the required valid sequence, at the slew rate, until the ABI output "catches up" with the angle samples, at which point the typical sample-rate output resumes. This skipping most likely occurs either at very low velocities, if the noise is high, or at very high velocities when the angle changes more than the quadrature resolution in one angle sample period.
- The ABI receiver at the host end cannot reliably detect edge transitions that are spaced at the sample rate of 1 µs. The slew limit time can be set greater than the nominal angle sample update period, providing the velocity of the angle rotation does not, on average, require ABI transitions greater than the angle sample rate.

In both cases, the ABI output correctly tracks the rotation position; however, the speed of the ABI edges are accomplished at the slew-rate limit set in EEPROM. Whenever slew-rate limiting occurs, the SRW flag in the WARN serial register asserts, informing the system of the occurrence.

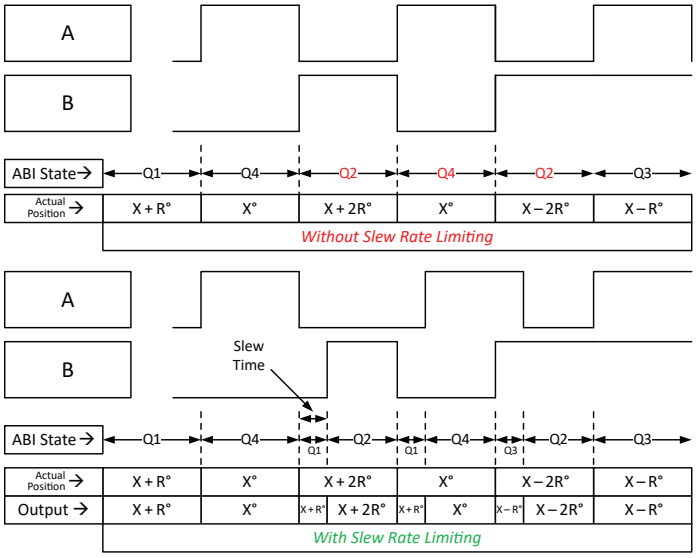

Figure 30: Slew-Rate Limiting

EFFECTIVE SPEED OF SLEW TIME

When slew-rate limiting occurs, the ABI update rate is no longer dependent on the observed rotation rate, but instead occurs at a period set via EEPROM. This change in the edge rate is observed as a change in the target velocity. This perceived velocity depends on:

- Configured ABI_SLEW_TIME (EEPROM 0x19, bits 21:16)
- ABI resolution (resolution pairs, EEPROM 0x19, bits 3:0)

The equivalent rpm for select combinations of slew time and ABI resolution is shown in Table 3.

When designing a system, it is important to note the listed rpm occurs for any change in rotation direction (i.e., motor transitioning from clockwise, CW, to counterclockwise, CCW, rotation), when both hysteresis and ABI slew-rate limiting are enabled, as the IC "back fills" the ABI edges for the programmed hysteresis window (EEPROM 0x17, bits 17:12).

Table 3

EEPROM Setting		Equivalent RPM Based on ABI Resolution		
ABI_SLEW_TIME (Decimal)	Slew Time (µs)	12-Bit Quadrature	11-Bit Quadrature	10-Bit Quadrature
1	0.25	58,593.8	117,187.5	234,375.0
2	0.375	39,062.5	78,125.0	156,250.0
3	0.5	29,296.9	58,593.8	117,187.5
4	0.625	23,437.5	46,875.0	93,750.0
5	0.75	19,531.3	39,062.5	78,125.0
6	0.875	16,741.1	33,482.1	66,964.3
7	1	14,648.4	29,296.9	58,593.8
8 (default)	1.125	13,020.8	26,041.7	52,083.3
…	…	…	…	…
62	7.875	1,860.1	3,720.2	7,440.5
63	8	1,831.1	3,662.1	7,324.2

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Brushless DC Motor Output (UVW)

The A1333 offers U, V, and W (UVW) signals for stator commutation of brushless DC (BLDC) motors. If hysteresis is enabled (set via AHE, bit 12 of EEPROM address 0x19), the UVW edges update based on the rotation direction and hysteresis window. For greater detail, refer to the Angle Hysteresis section. The UVW outputs switch when the measured mechanical angle crosses the value where a change should occur. By default, the UVW signals are 180° duty cycle waveforms (complete one cycle every 360°), spaced 120° apart. Options are provided for 1 to 16 pole-pairs, which control how many times the UVW waveforms are repeated for an observed mechanical rotation. This emulates the typical Hall-switch output, from a multi pole-pair motor. The UVW waveforms for one-, three-, and five-pole-pair BLDC motors are shown in Figure 31, Figure 32, and Figure 33.

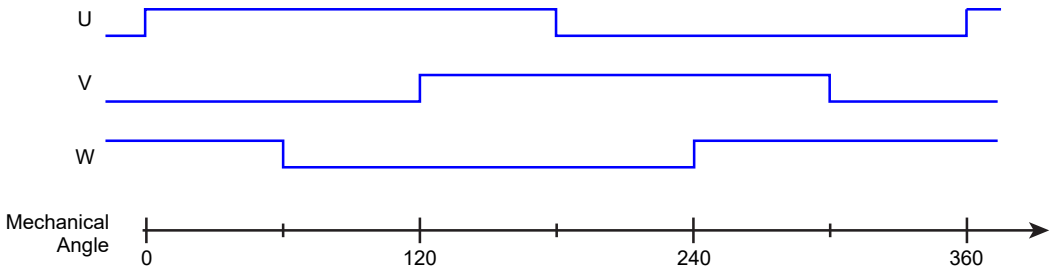

Figure 31: UVW Outputs for One-Pole-Pair BLDC Motor

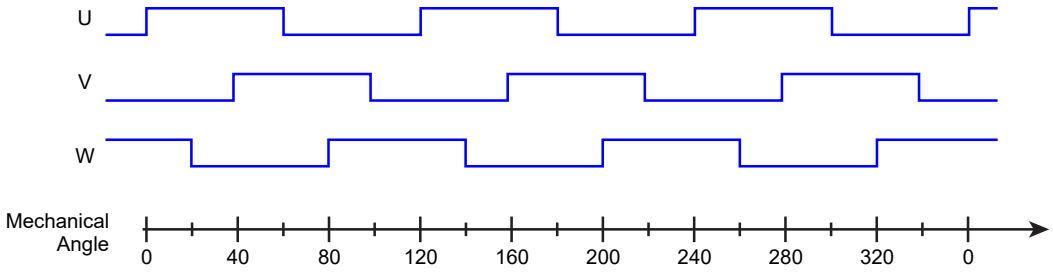

Figure 32: UVW Outputs for Three-Pole-Pair BLDC Motor

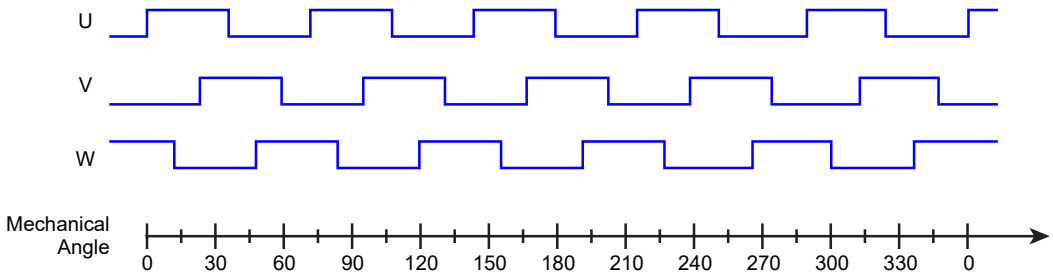

Figure 33: UVW Outputs for Five-Pole-Pair BLDC Motor

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Table 4: UVW Pole-Pair Settings

RESOLUTION_PAIRS (Hex)	Quantity of Pole-Pairs	Cycle Width (Mechanical Degrees)
0x0	1	360
0x1	2	180
0x2	3	120
0x3	4	90
0x4	5	72
0x5	6	60
0x6	7	51.43
0x7	8	45
0x8	9	40
0x9	10	36
0xA	11	32.73
0xB	12	30
0xC	13	27.69
0xD	14	25.71
0xE	15	24
0xF	16	22.5

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Angle Hysteresis

Hysteresis can be applied to the compensated angle to moderate jitter in the angle output due to noise or mechanical vibration. In the A1333, the hysteresis field (ANG.HYSTERESIS) defines the width of an angle window at 14-bit resolution. Mathematically, the width of this window is:

$$HYSTERESIS \times (360 / 16384) \text{ degrees} \quad ,$$

HYSTERESIS is a 6-bit wide EEPROM field, allowing a range of 0 to 1.384 degrees of hysteresis to be applied.

The hysteresis-compensated angle can be routed to the ABI or UVW interface by setting the AHE bit in EEPROM to a 1 (bit 12 of address 0x19). On the SPI or Manchester interface, the hysteresis-compensated angle can be read via an alternate register (HANG.ANGLE_HYS) at 12-bit resolution.

The effect of the hysteresis is shown in Figure 34. The current angle position as measured by the sensor is at the "head" of the hysteresis window. As long as the sensor (electrical) angle advances in the same direction of rotation, the output angle is the sensor angle, minimizing latency. If the sensor angle reverses direction, the output angle is held static until the sensor angle exits the hysteresis window in either direction. If the exit is in the opposite direction of rotation where the "head" was, the head flips to the opposite end of the hysteresis window and that becomes the new reference direction. The current direction of rotation, or "head" for the purposes of hysteresis, is viewable via the STA.ROT bit, where 0 is in the increasing-angle direction and 1 is in the decreasing-angle direction.

This behavior has the following consequences:

1. If the hysteresis window is greater than the output resolution, the output angle skips consecutive resolution steps.
2. If there is jitter due to noise or mechanical vibration, especially at a static angle position or very slow rotation, the angle tends to bias to one side of the window, depending on the direction of rotation as the angular velocity approaches zero (i.e., towards the current "head") rather than to the average position of the jitter.

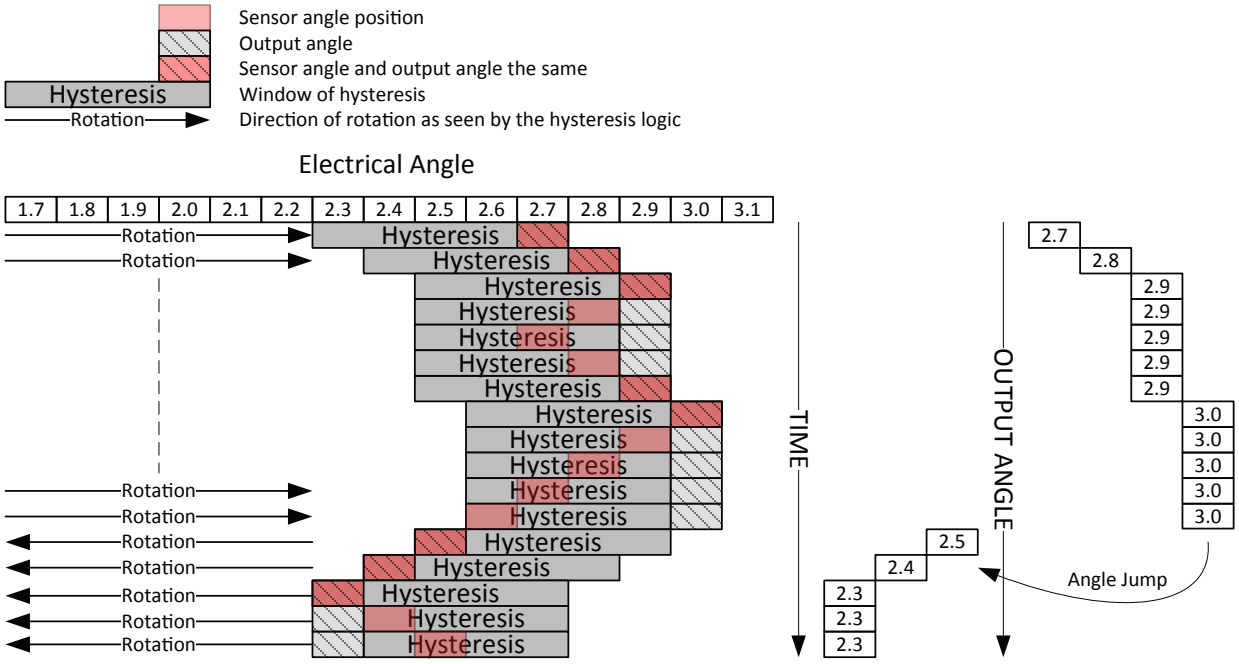

Figure 34: Effect of Hysteresis

Note: The rotation direction resets to 0, or increasing angle direction. At power-up or after LBIST, the hysteresis window always lags behind the initial angle position; therefore, if hysteresis is enabled, a decreasing angle direction of rotation does not register until the hysteresis window has passed.

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Turns-Counting

The A1333 uses a secondary, lower-power signal path (called the ZCD path) to track rotation turns. The turns-counter logic tracks the turns in either 45-degree or 180-degree increments, based on the T45 register field. The signal path, which tracks total turns, does not implement the same angle compensation as the primary signal path. Because of this, the turns -count value does not precisely match the primary angle output.

The turns-counter saturates at 2047 and –2048 in the 45-degree mode and at 511 and –512 in the 180-degree mode. If this happens, the turns-count warning flag (bit 0 of serial register 0x26) asserts and remains asserted until the turns-counter is reset via the control register (serial register 0x1E). (See the Primary Serial Interface Register Reference section).

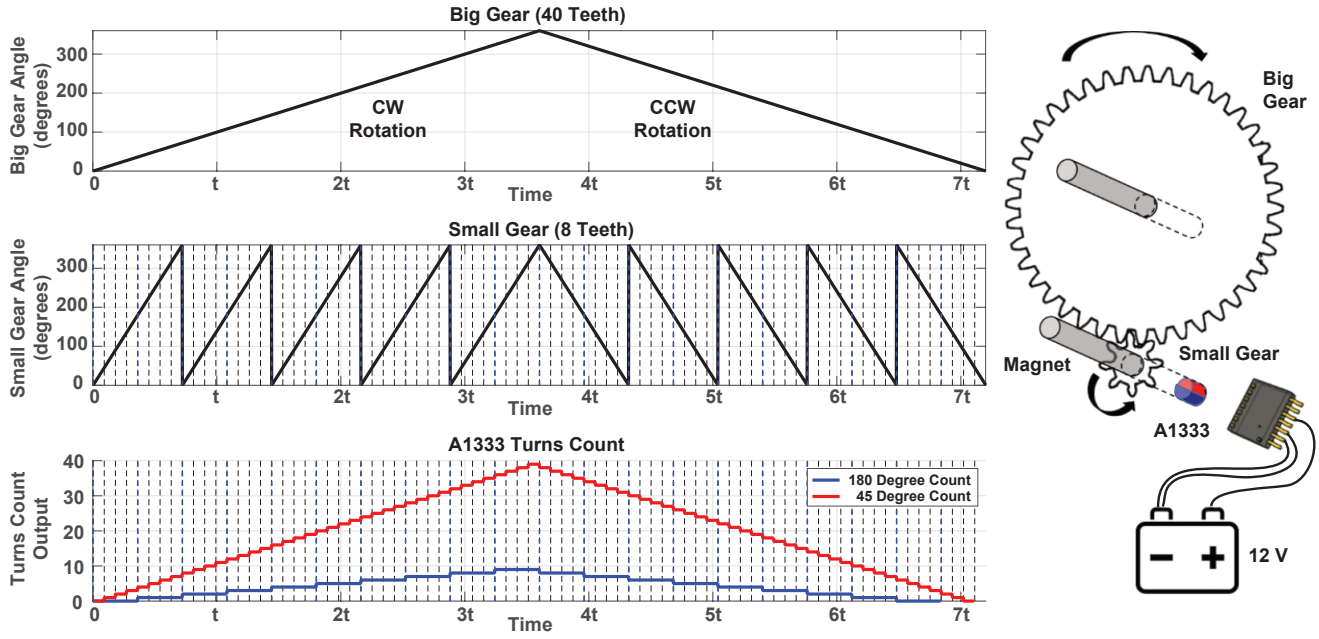

Figure 35: Example of a Turns-Counting Application

INVOKING A TURNS-COUNTER RESET

Resetting the turns-counter is a command invoked using the SPECIAL field of the CTRL register (register address 0x1E; see the Primary Serial Interface Register Reference section). Following a reset, turns are tracked relative to that point, as measured by the signal path (ZCD).

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DEVICE PROGRAMMING INTERFACES

The A1333 can be programmed in two ways:

- Using the *SPI interface* for input and output, while supplying the VCC pin with typical operating voltage
- Using a *Manchester protocol* on the supply pin for input and the PWM pin for output.

The A1333 does not require special supply voltages to write to the EEPROM.

All setting fields and all data fields of the sensor can be read and written using both protocols. If EEPROM locking is used (detailed in the EEPROM Write Lock section), write access using either of the protocols is prevented.

A separate setting to completely disable the Manchester interface is available in the DM field of the EEPROM. Using this setting causes the sensor to ignore any commands entered using Manchester protocol. The SPI interface does not become disabled by disabling the Manchester interface.

Interface Structure

The A1333 consists of two memory blocks. The primary serial interface registers are used for direct writes and reads by the host controller for frequently required data (for example, angle data, warning flags, field strength, and temperature). All forms of communication (even to the extended locations) operate through the primary registers, whether it be via SPI or Manchester.

The primary serial registers also provide a data and address location for accessing extended memory locations. Accessing these extended location is performed in an indirect fashion: the controller writes into the primary interface to give a command to the sensor to access the extended locations. The read/write is executed, and the result is again presented in the primary interface.

This concept is shown in Figure 36.

For writing extended locations, the primary interface offers the registers EWCS, EWA, EWDH, and EWDL. EWA holds the extended address that should be written, and EWDH/EWDL contain the two high bytes and the two low bytes for the extended location contents. The EWCS register is used for commands and status data. For further information and other register fields associated with read transactions, refer to the Write Transaction to EEPROM and Other Extended Locations section.

For reading extended locations, the primary interface offers the registers ERCS, ERA, ERDH, and ERDL. ERA holds the extended address that should be read, and ERDH/ERDL contain the two high bytes and the two low bytes for the extended location contents. The ERCS register is used for commands and status data. For further information and other register fields associated with read transactions, refer to the Read Transaction from EEPROM and Other Extended Locations section..

EEPROM writing requires additional procedures. For more information about EEPROM and shadow memory read and write access, see the EEPROM and Shadow Memory Usage section.

The primary serial interface can be accessed using the SPI and the Manchester interfaces, as detailed in the SPI Interface and Manchester Interface sections.

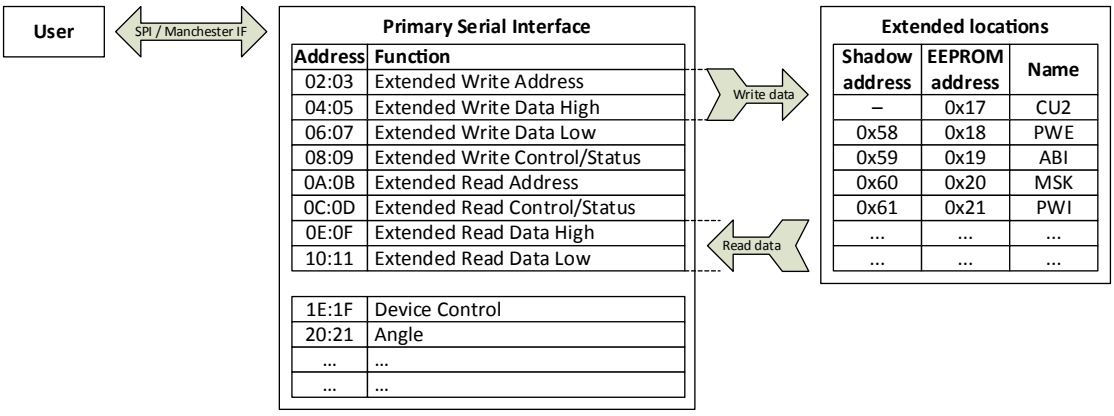

Figure 36: Serial Registers Allow Access to Extended Memory (EEPROM and Shadow)

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SPI Interface

The A1333 provides a full-duplex 4-pin SPI interface for each die, using SPI mode 3 (CPHA = 1, CPOL = 1). All programming can be performed using this interface; all programming can also be performed using the Manchester interface. If the SPI interface is not used, do not leave the chip-select line floating; instead, follow the recommendations in the Application Information section.

The sensor responds to commands received on the controller-output peripheral-input (MOSI), serial clock (SCLK), and chip-select (CSB) pins, and outputs data on the controller-input peripheral-output (MISO) pin. All three input pins are 3.3 V and 5 V SPI compatible, with threshold values determined by factory EEPROM settings. The MISO output voltage level conforms to a 3.3 V or 5 V SPI level, based on factory settings. Standard parts are shipped with the 3.3 V interface. Contact Allegro for ordering options of the 5 V variant.

The setup for communication using the SPI interface is provided in Figure 37.

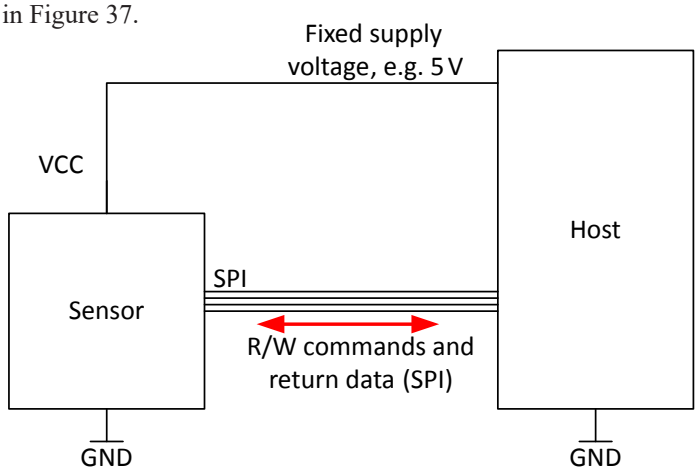

Figure 37: SPI Interface Programming Setup

TIMING

The interface timing parameters from the specification table are defined in Figure 38 and Figure 39.

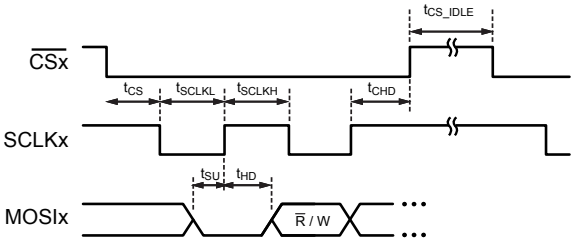

Figure 38: SPI Interface Timings Input

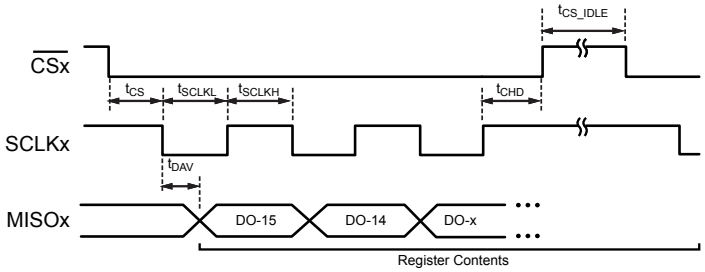

Figure 39: SPI Interface Timings Output

SPURIOUS INTERFACE ERROR (IER) WHEN SHARING SPI LINES

The IER error flag may provide an erroneous indication when the SCLK line is shared among multiple ICs. Ways to avoid this are detailed in Appendix B: SPI Interface Error Flag Description.

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SPI INTERFACE SPECIFICATIONS (for 3.3 V SPI Mode)						
Digital Input High Voltage	V_{IH}	MOSI, SCLK, $\overline{CS}$ pins	2.8	–	3.63	V
Digital Input Low Voltage	V_{IL}	MOSI, SCLK, $\overline{CS}$ pins	–	–	0.5	V
SPI Output High Voltage	V_{OH}	MISO pins, C_L = 20 pF, T_A = 25°C, 5 V compliant	2.93	3.3	3.63	V
SPI Output Low Voltage	V_{OL}	MISO pins, C_L = 20 pF	–	0.3	–	V
SPI INTERFACE SPECIFICATIONS (for 5 V SPI Mode) (*Contact Allegro for 5 V SPI ordering information*)						
Digital Input High Voltage	V_{IH}	MOSI, SCLK, $\overline{CS}$ pins	3.75	–	5.5	V
Digital Input Low Voltage	V_{IL}	MOSI, SCLK, $\overline{CS}$ pins	–	–	0.5	V
SPI Output High Voltage	V_{OH}	MISO pins, C_L = 20 pF, T_A = 25°C, $V_{CC} \geq$ 5.0V	4	5	5.5	V
SPI Output Low Voltage	V_{OL}	MISO pins, C_L = 20 pF	–	0.3	–	V
SPI INTERFACE SPECIFICATIONS						
SPI Clock Frequency [1]	f_{SCLK}	MISO pins, C_L = 20 pF	0.1	–	10	MHz
SPI Clock Duty Cycle [1]	D_{fSCLK}	SPI_{CLKDC}	40	-	60	%
SPI Frame Rate [1]	t_{SPI}		5.8	–	588	kHz
Chip Select to First SCLK Edge [1]	t_{CS}	Time from $\overline{CS}$ going low to SCLK falling edge	50	–	–	ns
Chip Select Idle Time [1]	t_{CS_IDLE}	Time $\overline{CS}$ must be high between SPI message frames	200	–	–	ns
Data Output Valid Time [1]	t_{DAV}	Data output valid after SCLK falling edge	–	30	–	ns
MOSI Setup Time [1]	t_{SU}	Input setup time before SCLK rising edge	25	–	–	ns
MOSI Hold Time [1]	t_{HD}	Input hold time after SCLK rising edge	50	–	–	ns
SCLK to CS Hold Time [1]	t_{CHD}	Hold SCLK high time before $\overline{CS}$ rising edge	5	–	–	ns
Load Capacitance [1]	C_L	Loading on digital output (MISO) pin	–	–	20	pF

[1] Parameter is not guaranteed at final test. Determined by design.

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MESSAGE FRAME SIZE

The SPI interface requires either 16, 17, or 20-bit packet lengths. An extended 20-bit SPI packet allows 4 bits of CRC to accompany every data packet. A 17-bit packet is only allowed if the EEPROM/shadow bit S17 (bit 1 of EEPROM 0x1B) is set to 1.

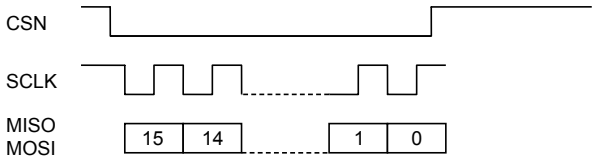

Figure 40: 16-Bit SPI Transaction

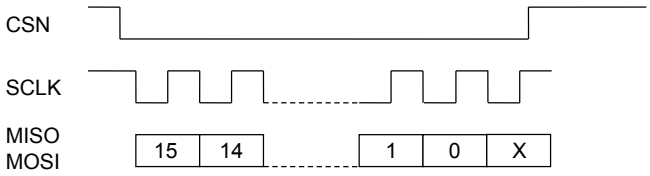

Figure 41: 17-Bit SPI Transaction

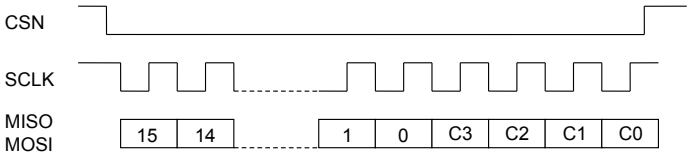

Figure 42: 20-Bit SPI Transaction

If more clock pulses than expected are detected by the sensor in an SPI transaction, the interface warning WARN.IER activates. This warning does not activate for clean SPI transactions with 16 or 20 bits, or with clean 17-bit transactions when S17 is enabled.

The purpose of the 17-bit SPI option is to allow delayed reading of the MISO line by the host. Some hosts allow data to be sampled from the peripheral—not on the rising edge, but on the next falling edge of SCLK. This way, in case of long interface delays caused by large line capacitance or very long cables, the permissible clock speed can be increased. However, a 17th falling edge is required to read the 16th bit coming from the sensor. For the sensor to not display an error when this 17th clock is found, the bit S17 must be set.

21-BIT SPI PACKET

If sharing an SPI bus, the A1333 may exhibit a false IER flag when using the standard SPI packet sizes. To prevent this, a 21-bit SPI packet should be used.

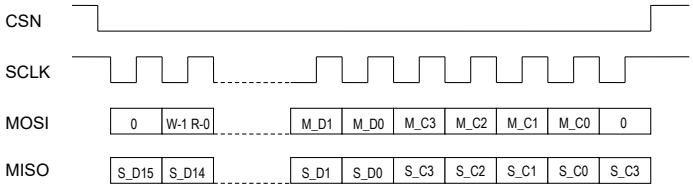

Figure 43: 21-Bit SPI Transaction

The 21st bit sent from the controller should be a logic 0, effectively left-shifting the standard 20-bit packet by 1 bit. The IC response repeats the most-significant bit of the CRC, shifted out on the last SCLK edge. For more information, see Appendix B: SPI Interface Error Flag Description.

WRITE CYCLE

Write cycles consist of a 1 low bit, 1 read/write (R/W) bit (write = high), 6 address bits (corresponding to the primary serial register), 8 data bits, and 4 optional CRC bits. To write a full 16-bit serial register, two write commands are required (even and odd byte addresses). MOSI bits are clocked in on the rising edge of the controller-generated SCLK signal.

READ CYCLE

Reading data always involves at least two SPI frames. In the first frame, the read command is sent; in the second frame, the result from the first read is received. While receiving data from the last read command, it is possible to send another read command (duplexed read). This way, every frame except the first one contains data from the sensor. This is useful for very fast reading of angle data.

When receiving the last frame, the host can transmit a command with MOSI set to all zeros. This represents a read command from register 0x00 and does not cause any reaction from the sensor. Reading from register 0x00 outputs the value 0x0000.

In frames where a previous read command is not sent, the MISO data output should be ignored.

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Because an SPI read command can transmit 16 data bits at one time, and the primary serial registers are built from one even and one odd byte, the entire 16-bit contents of one serial register can be transmitted with one SPI frame. This is accomplished by providing an even serial address value. If an odd value address is sent, only the contents of the single byte are returned, with the eight most significant bits within the SPI packet set to zero. Example: To read all 16 bits of the error register (0x24:0x25), an SPI read request using address 0x24 should be sent. If only the 8 LSBs are desired, the address 0x25 should be used. Examples of both an SPI write and an SPI read request, using a 16-bit SPI message frame, are shown in Figure 44.

(A) SPI write example (duplexed read available)

(B) SPI read example: register selection (duplexed read available)

(C) SPI read example: data output from selected register

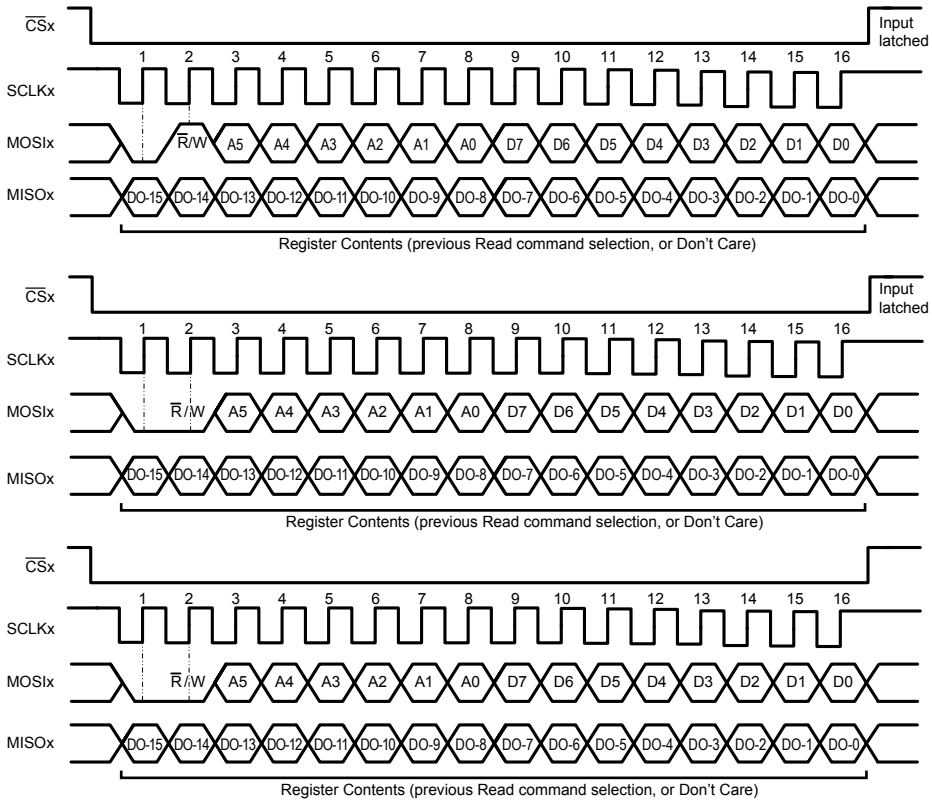

Figure 44: SPI Read and Write Pulse Sequences

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CRC

If the user wants to check the data coming from the sensor, it is possible to use 20-bit SPI frames. Without requiring an additional setting, a 4-bit CRC is automatically generated and placed on the MISO line if more than 16 bits are read from the sensor.

The four additional CRC bits on the MOSI line coming from the host are ignored by the sensor, unless the PWI.SC bit is set within EEPROM (0x1B, bit 0). When the incoming CRC check is enabled, an incoming SPI packet with an incorrect CRC is discarded, and the CRC error flag is set in the serial register WARN.CRC.

The CRC is based on the polynomial $x^4 + x + 1$, with the linear feedback shift register values preset to all 1s. The 16-bit packet is shifted through, from bit 15 (MSB) to bit 0 (LSB). The CRC logic is shown in Figure 45. Data are fed into the CRC logic with MSB first. The output is sent as C3-C2-C1-C0.

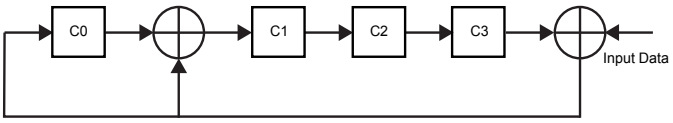

Figure 45: SPI CRC

The CRC output by the sensor on the MISO pin is always correct. The CRC from the host on the MOSI pin must be correct if the CRC enable bit PWI.SC in the EEPROM is set.

NOTE: If the extended read data (ERD) register is read before the ERCS.ERD bit indicates a read has completed, there is a possibility of a CRC error, because the data could change during the read. Do not read the ERD register until it is known to be stable based on the completed bit indication or waiting sufficient time.

The CRC can be calculated with the following C code:

```
/*
* CalculateCRC
*
* Take the 16-bit input and generate a 4-bit CRC
* Polynomial = x^4 + x + 1
* LFSR preset to all 1's
*/
uint8_t CalculateCRC(uint16_t input)
{
    bool CRC0 = true;
    bool CRC1 = true;
    bool CRC2 = true;
    bool CRC3 = true;
    int  i;
    bool DoInvert;
    uint16_t mask = 0x8000;

    for (i = 0; i < 16; ++i)
    {
        DoInvert = ((input & mask) != 0) ^ CRC3;
        CRC3 = CRC2;
        CRC2 = CRC1;
        CRC1 = CRC0 ^ DoInvert;
        CRC0 = DoInvert;
        mask >>= 1;
    }

    return (CRC3 ? 8U : 0U) + (CRC2 ? 4U : 0U) + (CRC1 ? 2U
: 0U) + (CRC0 ? 1U : 0U);
}
```


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Manchester Interface

To facilitate addressable device programming when using the unidirectional PWM, ABI, or UVW protocols, with no need for additional wiring, the A1333 incorporates a serial interface on the VCC line (Note: The A1333 may also be programmed via SPI, with additional wiring connections).

This interface allows an external controller to read and write registers in the A1333 EEPROM and volatile memory. The device uses a point-to-point communication protocol, based on Manchester encoding per G.E. Thomas (a rising edge indicates a 0 and a falling edge indicates a 1), with address and data transmitted MSB first. The addressable Manchester code implementation uses the logic states of the SA0/SA1 pins to set address values for each die. In this way, individual communication with up to four A1333 dies is possible. To prevent any undesired programming of the A1333, the serial interface can be disabled by setting the disable Manchester bit, PWI.DM, to 1. With this bit set, the sensor ignores any Manchester input on VCC.

The setup for communication using the Manchester interface is shown in Figure 46.

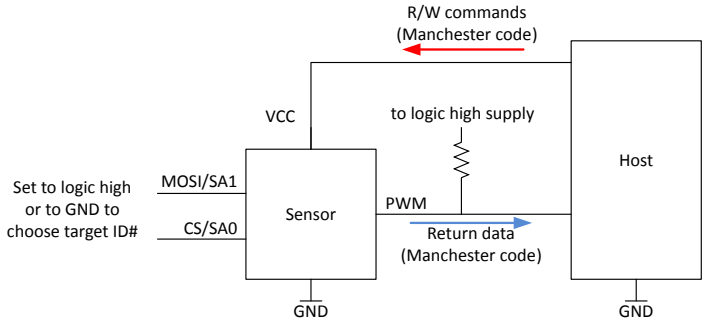

Figure 46: Manchester Interface Programming Setup

CONCEPT OF MANCHESTER COMMUNICATION

The Manchester interface allows programming and readout with a minimal number of pins involved. This is beneficial for sensor subassemblies connected to wiring harnesses, because fewer connections are needed. The supply level is typically modulated between 5 and 8 volts ($V_{MAN(H)}$ and $V_{MAN(L)}$) to produce a “low” signal and a “high” signal. In the absence of a clock signal, Manchester encoding is used, allowing the sensor to determine the bit rate that the host is using.

The controller can freely choose any supported Manchester communication frequency for each transaction. The sensor recognizes the transaction speed used by the controller and sends the response at the same data rate.

As Manchester commands are sent on the supply line, the speed is usually limited by capacitances on the supply line. A reduction of the bit rate, or using a stronger line driver, can help to ensure stable communication.

If a correct read command is sent, the sensor responds to the controller using the open-drain output on the PWM line. The high level is determined by the PWM pull-up (usually 3.3 V or 5 V), and the low level is close to GND. The PWM uses an open-drain output, setting the logic levels to GND and logic-level high (see Figure 46). A sufficient pull-up resistor (e.g., 4.7 kΩ) must be used to pull the line to a maximum logic high level V_{IN}.

ENTERING MANCHESTER COMMUNICATION MODE

Provided the disable Manchester bit is not set in EEPROM, the A1333 continuously monitors the VCC line for valid Manchester commands. The part does not take action until a valid Manchester access code is received.

There are two special Manchester code commands used to activate or deactivate the serial interface and to specify the output format used during read operations:

1. Manchester Access Code: Enters Manchester communication mode; Manchester code output on the PWM pin. For an example, see the Manchester Access Code section.
2. Manchester Exit Code; returns the PWM pin to typical operation. For an example, see the Manchester Exit Code section.

Once the Manchester communication mode is entered, the PWM output pin ceases to provide angle data, interrupting any data transmission in progress.

TRANSACTION TYPES

The A1333 receives all commands via the VCC pin, and responds to read commands via the PWM pin. This implementation of Manchester encoding requires the communication pulses to be within a high ($V_{MAN(H)}$) and low ($V_{MAN(L)}$) range of voltages on the VCC line. Each transaction is initiated by a command from the controller; the sensor does not initiate any transactions. Two commands are recognized by the A1333: write and read.

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CONTROLLER MANCHESTER MESSAGE STRUCTURE

The general format of a command message frame is shown in Figure 47. Note that, in the Manchester coding used, a bit value of 1 is indicated by a falling edge within the bit boundary, and a bit value of zero is indicated by a rising edge within the bit boundary.

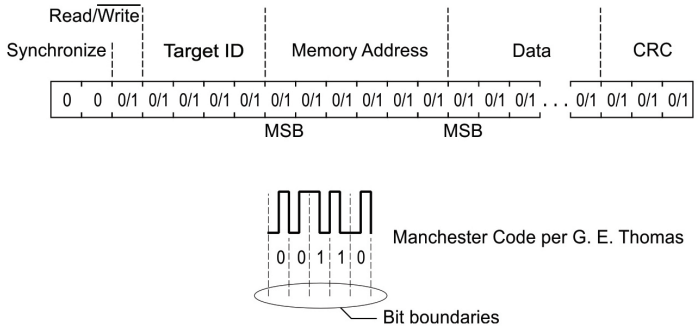

Figure 47: Manchester Message Format

A brief description of each bit is provided in Table 5.

Table 5: Manchester Command General Format

Bits	Parameter Name	Description
2	Synchronization	Value 00 sent to identify a command start and to synchronize sensor clock
1	Read/Write	0 = write, 1 = read
4	Target ID	Select the target ID for this transaction. [ID3 ID2 ID1 ID0] are each adressed/ ignored by a 1/0 at their address, so that a write to [0011] writes to ID0 and ID1. Reading from several sensors at the same time is not supported. Writing to [0000] is a broadcast write; it is written to all sensor dies.
6	Address	Serial address for read/write
16	Data	Only for writes: 16 bit write data. Omit for read commands
3	CRC	3-bit CRC, needed for all commands

When the A1333 is operating in PWM mode, the die ID value is determined by the state of the CSN and MOSI pins, as detailed in Table 6.

Table 6: Pin Values

MOSI/SA1	CS/SA0	ID Value
0	0	ID0
0	1	ID1
1	0	ID2
1	1	ID3

Using the 4 bits of the chip-select field, die can be selected via their ID value, allowing up to four die to be individually addressed and providing for different group addressing schemes.

Example: If target ID = [1 0 1 0], all die with ID3 or ID1 are selected. If target ID is set to [0 0 0 0], an ID comparison is not performed, allowing all sensors to be addressed at once. In case of PWM line-sharing for Manchester communication, reading must be performed one die at a time.

Table 7: Target ID

Target ID			
ID3	ID2	ID1	ID0

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SENSOR MANCHESTER MESSAGE STRUCTURE

If a read command with the desired register number was sent from the controller to the sensor, the device responds with a read response frame using the Manchester protocol over the PWM output.

The following command messages can be exchanged between the device and the external controller:

- Manchester access code (host to sensor)
- Manchester exit code (host to sensor)
- Manchester write command (host to sensor)
- Manchester read command (host to sensor)
- Manchester read response (sensor to host)

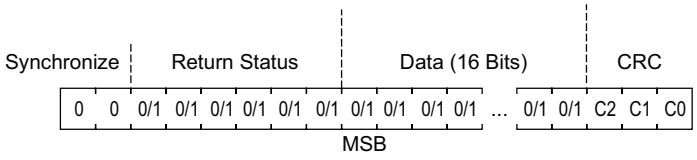

Figure 48: Manchester Message Format

In addition to the contents of the requested memory location, a return status field is included with every read response. This field provides the ID used to communicate with the part and any errors that may have occurred during the transaction. These bits are:

- **ID:** ID (CSN/MOSI) unless BC = 1 (ID is 00)
- **BC:** Broadcast; ID field was zero or SPI mode active
- **AE:** Abort error; edge-detection failure after synchronization detection
- **OR:** Overrun error; a new Manchester command has been received before the previous request could be completed
- **CS:** Checksum error; a prior command had a checksum error

For EEPROM address information, refer to the the EEPROM/ Shadow Memory Table. For serial address locations, refer to the Primary Serial Interface Register Reference section.

Table 8: Return Status Bits

Return Status Bits (6 bits)					
5	**4**	**3**	**2**	**1**	**0**
ID		BC	AE	OR	CS

MANCHESTER ACCESS CODE

The Manchester access code must be sent before other Manchester commands.

The Manchester access code always operates as a broadcast pulse, meaning the sensor does not look at the target ID field. For example, if two sensors configured with ID0 and ID1 respectively are sharing a common VCC line, a Manchester access code with a target ID value of [0 0 1 0] results in both sensors entering Manchester serial communication mode.

Table 9: Manchester Access Code

Bits	Parameter Name	Description
2	Synchronization	00
1	Read/Write	0
4	Target ID	0000 (this command is always a broadcast, even if it is addressed)
6	Address	111111 (fixed number for Manchester access message)
16	Data	0x62D2 (fixed number for Manchester access message)
3	CRC	3-bit CRC

An example is shown in Figure 49, with target ID = [0 0 0 1], data = access code = 0x62D2, and CRC = 110.

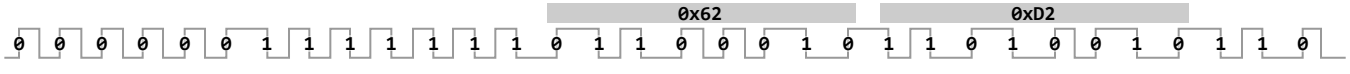

Figure 49: Target ID = [0 0 0 1], Data = Access Code = 0x62D2, CRC = 110

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MANCHESTER EXIT CODE

The Manchester exit code can be sent after Manchester access is complete in order to avoid accidental decoding of Manchester commands.

The Manchester exit code always operates as a broadcast pulse, meaning the sensor does not look at the target ID field. For example, if two sensors configured with ID0 and ID1 respectively are sharing a common VCC line, a Manchester access code with a target ID value of [0 0 1 0] results in both sensors exiting Manchester serial communication mode.

Table 10: Manchester Exit Code

Bits	Parameter Name	Description
2	Synchronization	00
1	Read/Write	0
4	Target ID	0000 (this command is always a broadcast, even if it is addressed)
6	Address	111111 (fixed number for Manchester exit message)
16	Data	0x0000 (any value except 0x62D2 can be used for Manchester exit message)
3	CRC	3-bit CRC

An example is provided in Figure 50, with target ID = [0 0 0 1], data = 0x0000, and CRC = 110.

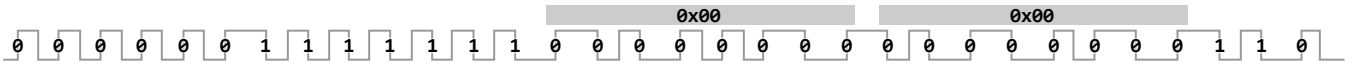

Figure 50: Target ID = [0 0 0 1], Data = 0x0000, CRC = 110

MANCHESTER READ COMMAND

Determines the serial address within the sensor from which the next read response transmits data. The sensor must receive a Manchester access code before it responds to a read command.

This command is sent by the controller.

Table 11: Manchester Read Command

Bits	Parameter Name	Description
2	Synchronization	00
1	Read/Write	1
4	Target ID	Depends on targeted sensor ID; e.g., to target ID0, use 0001
6	Address	Serial register address; e.g., 0x10 for READ_DATA_LO, or 0x20 for ANGLE
3	CRC	3-bit CRC

An example is shown in Figure 51, where register 0x20 ANGLE is read from target ID [0 0 0 1] with CRC = 111. The two synchronization pulses from the read response on the PWM return line are also shown.

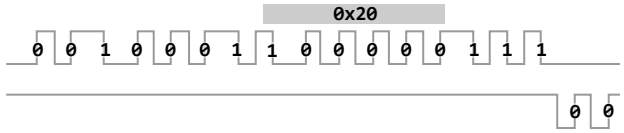

Figure 51: Target ID = [0 0 0 1], Angle = 0x20, CRC = 111

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MANCHESTER READ RESPONSE

The read response transmits data from the sensor to the controller after a read command. These data are sent by the sensor on the open-drain PWM pin. A pull-up resistor is needed for this to work.

A read from an even address returns an even byte [15:8] and an odd byte [7:0].

A read from an odd address returns an odd byte [7:0] only. Data bits [15:8] are zeroes.

Table 12: Manchester Read Response

Bits	Parameter Name	Description
2	Synchronization	00
2	ID	Target ID of the responding sensor die. 00 for ID0, 01 for ID1, 10 for ID2, 11 for ID3.
1	BC flag	Broadcast: Value set to 1 if read command was a broadcast command (Target-ID set to [0 0 0 0]), 0 if not
1	AE flag	Abort error: Value set to 1 if a previous transaction was aborted and discarded, typically caused by incorrect bit lengths; 0 is there was no problem. The error is stored until it can be transmitted on the next read response and is cleared afterward.
1	OR flag	Overrun error: If a command is sent to the sensor while the sensor is still sending a read response and this command is completely transmitted before the read response finishes, an overrun error has occurred. This error is then stored until it can be transmitted on the next read response and is cleared afterward.
1	CS flag	CRC error: Value set to 1 if a previous transaction had an incorrect CRC; 0 means there was no problem. The error is stored until it can be transmitted on the next read response and is cleared afterward.
16	data	Read from an even address: even byte [15:8] and odd byte [7:0]. Read from an odd address: odd byte [7:0] only; data bits [15:8] are zeroes.
3	CRC	3-bit CRC

An example is shown in Figure 52 where register 0x20 ANGLE is read, and the response is ID 00 (ID0), the four flags are all zeros (no errors), the data is 0x5C34, and the CRC is 100.

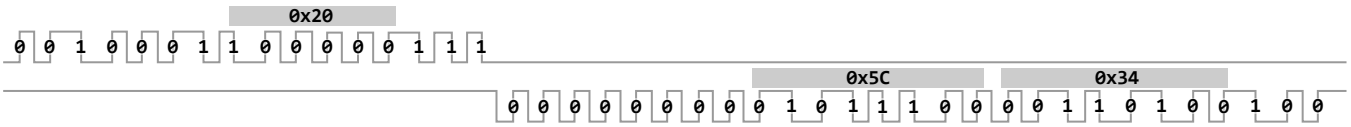

Figure 52: ID = 00, Error Flag = 0000, Data = 0x5C34, CRC = 100

MANCHESTER READ RESPONSE DELAY

The Manchester read response starts at the end of the read command. The response may start a ¼-bit time before the CRC is finished transmitting (overlap with last CRC bit) or ¼-bit time after the CRC finishes transmitting.

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CRC

The serial Manchester interface uses a cyclic redundancy check (CRC) for data-bit error checking of all the bits coming after the two synchronization bits. The synchronization bits are not included in the CRC. The CRC algorithm is based on the polynomial:

$$g(x) = x^3 + x + 1.$$

The calculation is represented graphically in Figure 53. The trailing 3 bits of a message frame comprise the CRC token. The CRC is initialized at 111. Data are fed into the CRC logic with MSB first. Output is sent as C2-C1-C0.

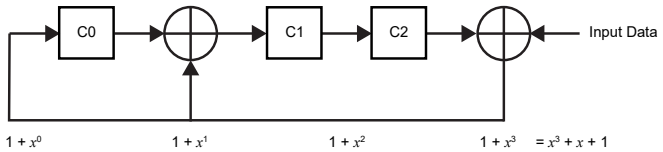

Figure 53: Manchester CRC Calculation

The 3-bit Manchester CRC can be calculated using the following C code:

```
// command: the manchester command, right justified, does
not include the space for the CRC
// numberOfBits: number of bits in the command not includ-
ing the 2 zero sync bits at the start of the command and the
three CRC bits
// Returns: The three bit CRC
// This code can be tested at http://codepad.org/yqTKnfmD

uint16_t ManchesterCRC(uint64_t data, uint16_t numberOfBits)
{
	bool C0 = false;
	bool C1 = false;
	bool C2 = false;
	bool C0p = true;
	bool C1p = true;
	bool C2p = true;
	uint64_t bitMask = 1;

	bitMask <<= numberOfBits - 1;

	// Calculate the state machine
	for (; bitMask != 0; bitMask >>= 1)
	{
		C2 = C1p;
		C0 = C2p ^ ((data & bitMask) != 0);
		C1 = C0 ^ C0p;

		C0p = C0;
		C1p = C1;
		C2p = C2;
	}

	return (C2 ? 4U : 0U) + (C1 ? 2U : 0U) + (C0 ? 1U :
0U);
}
```


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EEPROM AND SHADOW MEMORY USAGE

The device uses EEPROM to permanently store configuration parameters for operation. EEPROM is user-programmable and permanently stores operation parameter values or customer information. The operation parameters are downloaded to shadow (volatile) memory at power-up. Shadow fields are initially loaded from corresponding fields in EEPROM, but can be overwritten, either by performing an extended write to the shadow addresses, or by reprogramming the corresponding EEPROM fields and power cycling the IC. Use of shadow memory is substantially faster than accessing EEPROM. In situations where many parameters need to be tested quickly, shadow memory is recommended for trying parameter values before permanently programming them into EEPROM. The shadow memory registers have the same format as the EEPROM and are accessed at extended addresses 0x40 higher than the equivalent EEPROM address. Unused bits in the EEPROM do not exist in the related shadow register and return 0 when read. Shadow registers do not contain the ECC bits. Shadow registers have the same protection restrictions as the EEPROM. All registers can be read without unlocking. The mapping of bits from register addresses in EEPROM to their corresponding register addresses in shadow memory is provided in the EEPROM/Shadow Memory Table section.

Enabling EEPROM Access

To enable EEPROM write access after power-on-reset, an unlock code needs to be written to the serial register KEYCODE. This involves five write commands, which should be executed one after the other:

1. Write 0x00 to register 0x3C [15:8]
2. Write 0x27 to register 0x3C [15:8]
3. Write 0x81 to register 0x3C [15:8]
4. Write 0x1F to register 0x3C [15:8]
5. Write 0x77 to register 0x3C [15:8]

This needs to be performed once after power-on reset if the customer intends to write to the EEPROM.

Writing to serial registers and reading from serial registers does not require a special procedure after power-on.

Reading all EEPROM cells is always possible.

When performing EEPROM margin checking, the device must be unlocked.

EEPROM Write Lock

It is possible to protect the EEPROM from accidental writes.

- Setting the EEPROM field LOCK to the value 0xC (1100 in binary) blocks any writes to the EEPROM, so that permanent changes are not possible anymore. Temporary changes to the setting are still possible by writing to the shadow memory, but these changes are lost after a power cycle.
  This lock is permanent and cannot be reversed. Reading of the settings remains possible.
- Setting the EEPROM field LOCK to the value 0x3 (0011 in binary) locks EEPROM writes AND shadow memory writes. This means none of the sensor settings can be changed anymore. This lock is permanent and cannot be reversed. Reading of the settings remains possible.

Write Transaction to EEPROM and Other Extended Locations

Invoking an extended write access is a three-step process:

1. Write the extended address into the EWA register (using SPI or Manchester direct access). EWA is the 8-bit extended address that determines which extended memory address is to be accessed.
2. Write the data that is to be transferred into the EWD registers (using SPI or Manchester direct access). To load all 32 bits of data, this action spans four SPI writes or two Manchester packets.
3. Invoke the extended access by writing the direct EWCS.EXW bit with 1.

The 32 bits of data in EWD are then written to the address specified in EWA.

The EWCS.WDN bit can be polled to determine when the write completes. This is only necessary for EEPROM writes, which can take up to 24 ms to complete. Shadow register writes complete immediately in one system clock cycle after synchronization.

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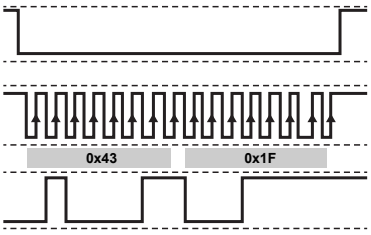
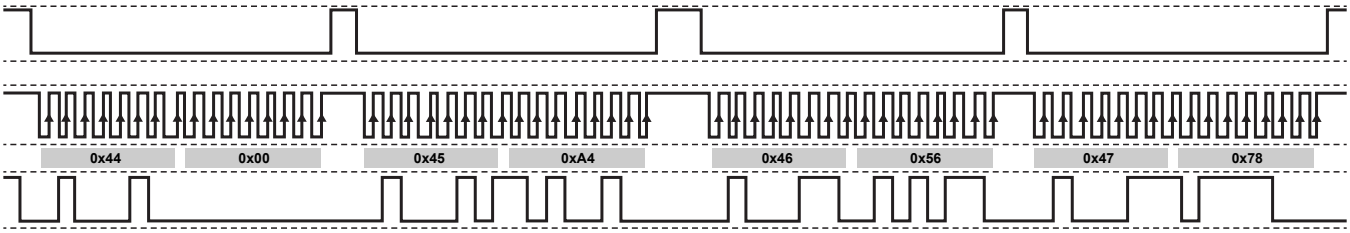
For example, to write location 0x1F in the EEPROM with 0x00A45678:

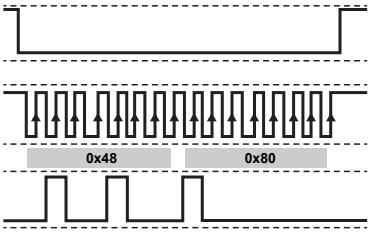
• Write 0x1F to the lower 8 bits of the EWA register (0x1F to EWA + 1 Address 0x03)



• Write 0x00A45678 to EWD (0x00 to EWD, 0xA4 to EWD + 1, 0x56 to EWD + 2, 0x78 to EWD + 3)

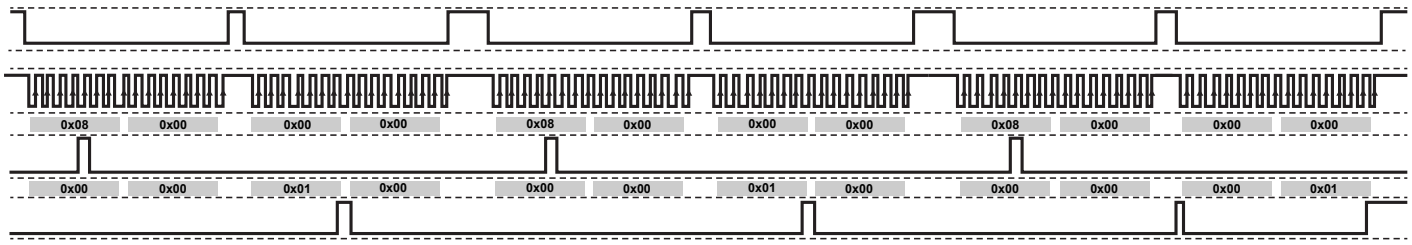


• Write 0x80 to EWCS



• Read EWCS + 1 until bit 0 (WDN) is set, or wait enough time.

In the example, register 0x08 is read, so that the second output byte is from register 0x09, then a waiting period occurs before bit 0 becomes 1, which happens in the last read.



If an access violation occurs (address not unlocked), the transaction is terminated, the corresponding RDN or WDN bit becomes set, and the XEE warning bit asserts. The XEE bit in the ERR register also becomes set if the EEPROM write aborts.

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After writing to the EEPROM, verify that the write was successful by performing an EEPROM margin check.

EEPROM Margin Check

Due to nonidealities in transistors, current slowly leaks into or out of EEPROM cells and can, over time, cause small changes in the stored voltage level. Variances in voltage levels of the charge pump can result in a variety of stored EEPROM cell voltages when programming. If this value is marginally close to the threshold, the small drift over lifetime can cause this value to move across the threshold. This results in a corrupted EEPROM value. Because this drift happens slowly over time, if there is an issue, it may not appear for years. For this reason, it is important to perform margin testing (margining) to verify the internal voltage levels of EEPROM cells after programming and to ensure future issues do not occur.

Margining is performed by Allegro on all registers at final test. Because EEPROM cell voltages are only modified when writing to the cell, it is not necessary to perform margining on registers that have not been modified.

Margining is performed in two steps: the first checks the validity of the voltage stored on digital 1 cells, and the second checks the voltage stored on digital 0 cells. It is important to perform both steps to ensure that issues do not occur.

To perform margining, a value of 0b0001 must be written to the SPECIAL field of the CTRL register. This reduces the internal threshold value. Once this value is written, an EEPROM read uses this lower threshold when reading EEPROM values. Perform a read on all EEPROM registers that are being tested, and confirm they read correctly. If a stored voltage is marginal to the typical operating threshold, it appears as the value 1 when it should be 0.

Repeat this test with the value of 0b0010 in the SPECIAL register to raise the threshold to greater than typical operation. Again, read all EEPROM registers being tested. In this test, if a stored high voltage is marginal to the typical threshold, it appears as the value 0 when it should be 1.

If, during either test, a bit is read incorrectly, perform another EEPROM write of the desired values to the register, and retest the margins.

Unlike other values in the SPECIAL field, these values persist and can be read to confirm the write was successful. As a result, the SPECIAL register must be cleared (or power cycled) to return the threshold value to its typical level.

In Figure 54, $V_{NOM(H)}$ represents the nominal voltage programmed into EEPROM cells containing a 1, and $V_{NOM(L)}$ represents the nominal voltage programmed into EEPROM cells containing a 0. The red and blue lines represent the actual voltage levels in the programmed cells for values of 1 and 0, respectively. As can be observed, at time 0 when the margin test is run, both high and low levels still appear to be the correct values when the threshold is moved to the margin testing levels.

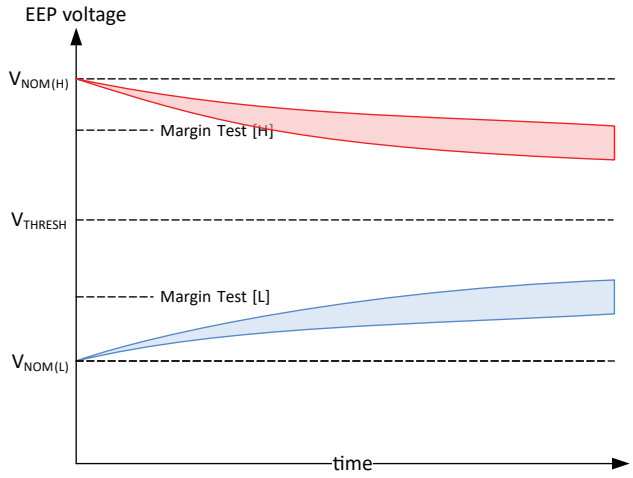

Figure 54: Example of Passing Programming Voltages

In Figure 55, the high and low voltage levels at the time of programming are further from their target. The drift over time results in these values crossing V_{THRESH} and becoming corrupted. At time 0 when the margin test is run, these values fail and are reported as errors to be reprogrammed.

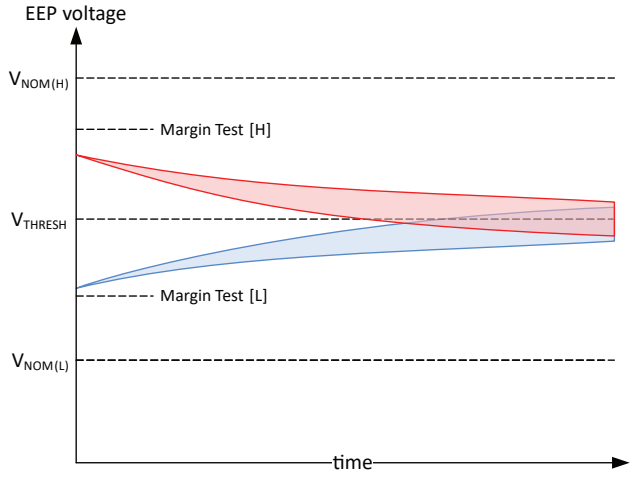

Figure 55: Example of Failing Programming Voltages

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Margining is shown below as a list of high-level steps. For details about performing individual steps, see the associated sections.

1. Clear the ERR and WARN registers.
   A. Set the CTRL.CLW and CTRL.CLE bits.
2. Enable EEPROM access.
3. Write new data to the EEPROM as desired.
4. Check the following flags for EEPROM errors: ESE, EUE, XEE,IER, CRC, and BSY.
   A. If any are asserted, the EEPROM write may have failed.
   B. A second write attempt is recommended.
5. Set CTRL.SPECIAL to 0001b to enable low-voltage margining.
6. Read all EEPROM addresses changed in step 3 and verify their contents.
   A. Verify the ESE and EUE error flags are clear.
7. Set CTRL.SPECIAL to 0010b to enable high-voltage margining.
8. Read all EEPROM addresses changed in step 3 and verify their contents.
   A. Verify the ESE and EUE error flags are clear.
9. If any EEPROM value read with a low or high threshold differs from the desired EEPROM or if either the ESE or EUE bits are set, EEPROM margining has failed.
   A. One additional write attempt and margin check should be accomplished. If margin failures persist following a second EEPROM write, the device should be discarded.

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Read Transaction from EEPROM and Other Extended Locations

Extended access is provided to additional memory space via the direct registers. This access includes the EEPROM and EEPROM shadow registers. All extended registers are up to 32 bits wide. Invoking an extended read access is a three-step process:

1. Write the extended address to be read into the ERA register (using SPI or Manchester direct access). ERA is the 8-bit extended address that determines which extended memory address is to be accessed.
2. Invoke the extended access by writing the direct ERCS.EXT bit with 1. The address specified in ERA is then read, and the data is loaded into the ERD registers.
3. Read the ERD registers (using SPI or Manchester direct access) to obtain the extended data. Obtaining all 32 bits takes multiple packets.

EEPROM read accesses may take up to 2 µs to complete. The ERCS.RDN bit can be polled to determine if the read access is complete before reading the data. Shadow register reads complete in one system clock cycle after synchronization. Do not attempt to read the ERD registers if the read access is potentially in process, because it could change during the serial access and the data would be inconsistent. It is also possible that an SPI CRC error would be detected if the data were to change during the serial read via the SPI interface.

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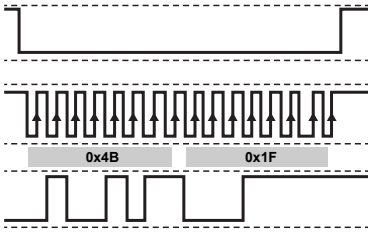
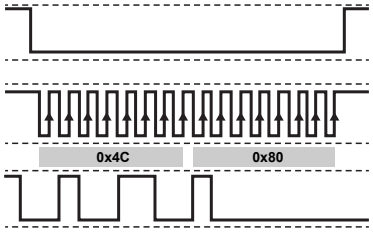
For example, to read location 0x1F in the EEPROM:

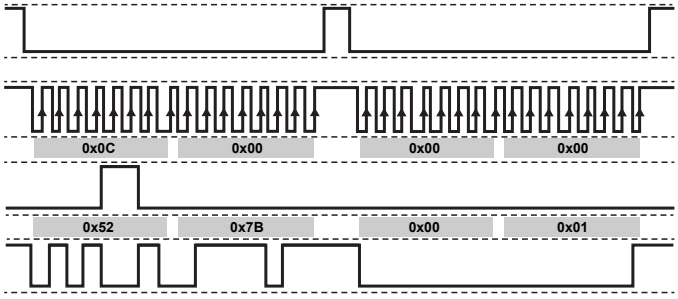
• Write 0x1F to the lower 8 bits of ERA (0x1F to ERA + 1, address 0x0B).



• Write 0x80 to ERCS.

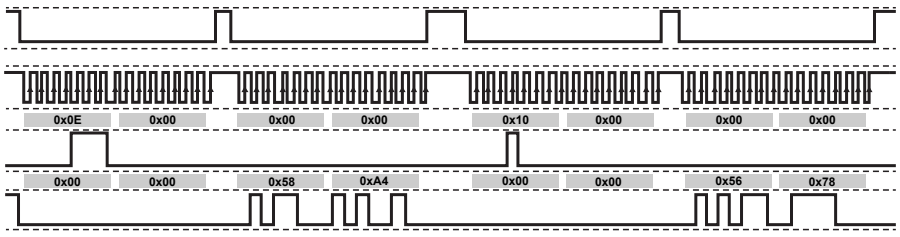


• Read ERCS + 1 until bit 0 (RDN) is set, or wait enough time.
In the example, register 0x0C is read, so that the last bit of the second output byte contains the RDN bit.



• Read ERDH (upper 16 bits of read data).
• Read ERDL (lower 16 bits of read data).
In the example below, the result for the data at address 0x1F is 0x58A45678. In this value:

- □ Bits [31:26] are the EEPROM CRC.
- □ Bits [25:24] are unused and zero.
- □ Bits [23:0] are the EEPROM values that can be used. These are the 24 bits containing the data 0xA45678 that was written in the EEPROM write example.



Note that it would have been possible to pipeline transactions in this example, i.e., send a new command while reading return data from the old command. This way, the transaction could have been performed in 5 SPI frames instead of 8.

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Shadow Memory Read and Write Transactions

Shadow memory read and write transactions are identical to those for EEPROM: Instead of addressing to the EEPROM extended address, address the shadow extended addresses, which are located at an offset of 0x40 above the EEPROM. For all addresses, refer to the EEPROM/Shadow Memory Table.

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PRIMARY SERIAL INTERFACE REGISTER REFERENCE

Table 13: Primary Serial Interface Registers Bits Map

Address [1] (0x00)	Register Symbol	Read/ Write	Addressed Byte (MSB)								Addressed Byte + 1 (LSB)								LSB Address
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x00	NOP	RO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x01
0x02	EWA	RW	0	0	0	0	0	0	0	0	WRITE_ADR								0x03
0x04	EWDH	RW	WRITE_DATA_HI																0x05
0x06	EWDL	RW	WRITE_DATA_LO																0x07
0x08	EWCS	WO/RO	EXW	0	0	0	0	0	0	WIP	0	0	0	0	0	0	0	WDN	0x09
0x0A	ERA	RW	0	0	0	0	0	0	0	0	READ_ADR								0x0B
0x0C	ERCS	WO/RO	EXR	0	0	0	0	0	0	RIP	0	0	0	0	0	0	0	RDN	0x0D
0x0E	ERDH	RO	READ_DATA_HI																0x0F
0x10	ERDL	RO	READ_DATA_LO																0x11
0x12 0x14 0x16 0x18 0x1A 0x1C	Unused	RO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x13 0x15 0x17 0x19 0x1B 0x1D
0x1E	CTRL	RW/WO	SPECIAL				0	CLS	CLW	CLE	INITIATE_SPECIAL								0x1F
0x20	ANG	RO	0	EF	UV	P	ANGLE												0x21
0x22	STA	RO	1	0	0	0	0	0	DIEID		ROT	0	SDN	BDN	LBR	CSTR	BIP	AOK	0x23
0x24	ERR	RO	1	0	1	0	WAR	STF	AVG	ABI	PLK	ZIE	EUE	OFE	UVD	UVA	MSL	RST	0x25
0x26	WARN	RO	1	0	1	1	IER	CRC	0	SRW	XEE	TR	ESE	SAT	TCW	BSY	MSH	TOV	0x27
0x28	TSEN	RO	1	1	1	1	TEMPERATURE												0x29
0x2A	FIELD	RO	1	1	1	0	GAUSS												0x2B
0x2C	TURNS	RO	1	1	0	P	TURNS												0x2D
0x2E	Unused	RO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x2F
0x30	HANG	RO	0	EF	UV	P	ANGLE_HYS												0x31
0x32	ANG15	RO	0	ANGLE_15															0x33
0x34	ZANG	RO	0	EF	UV	P	ANGLE_ZCD												0x35
0x36 0x38 0x3A	Unused	RO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x37 0x39 0x3B
0x3C	IKEY	WO/RO	KEYCODE								0	0	0	0	0	0	0	CUL	0x3D
0x3E	Unused	RO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x3F

[1] Addresses that span multiple bytes are addressed by the most significant byte.

Address 0x00:0x00 (NOP)—Null Register

Address	0x00								0x01							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

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Address 0x02:0x03 (EWA)—Extended Write Address

Address	0x02								0x03							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	WRITE_ADDR							
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

WRITE_ADDR [7:0]

Address to be used for an extended write. Address ranges:
0x00:0x1F—EEPROM (requires ≈ 24 ms following execution of a write)
0x40:0x5F—Shadow

Address 0x04:0x05 (EWDH)—Extended Write Data High

Address	0x04								0x05							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WRITE_DATA_HI															
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

WRITE_DATA_HI [15:0]

Upper 16 bits of data for an extended write operation.

Address 0x06:0x07 (EWDL)—Extended Write Data Low

Address	0x06								0x07							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WRITE_DATA_LO															
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

WRITE_DATA_LO [15:0]

Lower 16 bits of data for an extended write operation.

Address 0x08:0x09 (EWCS)—Extended Write Control and Status

Address	0x08								0x09							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXW	0	0	0	0	0	0	WIP	0	0	0	0	0	0	0	WDN
R/W	W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

EXW [15]

Initiate extended write by writing with 1. Sets WIP, clears WDN. Write-only, always reads back 0.

WIP [8]

Write in progress when 1 .

WDN [0]

Write is complete when 1; clears when EXR is set to 1.

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Address 0x0A:0x0B (ERA)—Extended Read Address

Address	0x0A								0x0B							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	READ_ADDR							
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

READ_ADDR [7:0]

Address to be used for an extended read. Address ranges:
0x00:0x1F—EEPROM (requires ≈2 µs)
0x40:0x5F—Shadow

Address 0x0C:0x0D (ERCS)—Extended Read Control and Status

Address	0x0C								0x0D							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXR	0	0	0	0	0	0	RIP	0	0	0	0	0	0	0	RDN
R/W	W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

EXR [15]

Initiate extended read by writing with 1. Sets RIP, clears RDN. Write-only, always reads back 0.

RIP [8]

Read in progress when 1 .

RDN [0]

Read is complete when 1; clears when EXR is set to 1.

Address 0x0E:0x0F (ERDH)—Extended Read Data High

Address	0x0E								0x0F							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	READ_DATA_HI															
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

READ_DATA_HI [15:0]

Upper 16 bits of data from extended read operation, valid when ERCS.
RDN set to 1 .

Address 0x10:0x11 (ERDL)—Extended Read Data Low

Address	0x10								0x11							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	READ_DATA_LO															
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

READ_DATA_LO [15:0]

Lower 16 bits of data from extended read operation, valid when ERCS.
RDN set to 1.

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Address 0x1E:0x1F (CTRL)—Device Control

Address	0x1E								0x1F							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPECIAL				0	CLS	CLW	CLE	INITIATE_SPECIAL							
R/W	R/W	R/W	R/W	R/W	R	R/W	W	W	W	W	W	W	W	W	W	W

SPECIAL [15:12]

Defines specific actions to be taken by the IC. Many actions are only invoked after the CTRL.INITIATE_SPECIAL field is written with the correct value. Aside from EEPROM margining, this field returns 0x00 on completion.

Value	Description
0000	No action.
0001	Enable EEPROM low-voltage margin. IC must be unlocked.
0010	Enable EEPROM high-voltage margin. IC must be unlocked.
0100	Turns-counter reset. Initiate with 0x46.
0101	Reload EEPROM. Requires IC to be unlocked. Initiate with 0xA5.
0110	No action.
0111	Hard reset. Requires unlock of part. Initiate with 0x5A.
1001	Run CVH self-test. Initiate with 0xB9.
1010	Run logic BIST. Initiate with 0xB9.
1011	Run both CVH self-test and logic BIST. Tests are run in parallel. Initiate with 0xB9.

CLS [10]

Clear status register bits SDN and BDN, when set to 1.
STA.SDN indicates that a SPECIAL access task (i.e., CVH self-test) is complete.
STA.BDN indicates the IC has booted properly and completed any start-up self-tests.

CLW [9]

Clear warning (WARN) register when set to 1.
Clears bits that were previously read from the WARN (register 0x26:0x27).
Write-only, always returns 0.

CLE [8]

Clear error (ERR) register when set to 1.
Clears bits that were previously read from the ERR (register 0x24:25).
Write-only, always returns 0.

INITIATE_SPECIAL [7:0]

Write after setting certain CTRL.SPECIAL bits to initiate the selected action(s).
Always returns 0s.

Value	Description
0xB9	Initiate self-tests.
0x46	Initiate turns-counter reset.
0x5A	Initiate hard reset.

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Address 0x20:0x21 (ANG)—Current Angle Reading (12 bits)

Address	0x20								0x21							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	EF	UV	P	ANGLE											
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

EF [14]

Error flag. If any unmasked bit in ERR or WARN is set, value is 1.

Value	Description
0	No unmasked errors
1	Unmasked error is present

UV [13]

Undervoltage flag (real time). Logical OR of analog and digital UV flags (UVD and UVA flags). Conditions are real time, but may be masked by EEPROM error mask bits.

Value	Description
0	No undervoltage condition detected
1	Undervoltage condition detected

P [12]

Parity bit. Odd parity is calculated across all bits (EF, UV, and ANGLE). Result is that there should always be an odd number of ones in this 16-bit word.

ANGLE [11:0]

Angle from PLL after processing.
Angle in degrees is 12-bit value × (360/4096).

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Address 0x22:0x23 (STA)—Device Status

Address	0x22								0x23							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	1	0	0	0	0	0	DIE_ID		ROT	0	SDN	BDN	LBR	CSTR	BIP	AOK
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

RIDC [15:12]

Register ID bits. Used to distinguish this registers from other serial registers. Hard-coded value.

Value	Description
1000	Register ID value

DIE_ID [9:8]

Die ID, loaded from EEPROM (for multi-die packages). Used for identification purposes only. Does not impact sensor functionality. Set in factory by Allegro.

ROT [7]

Indicates observed rotation direction, based on the hysteresis logic. Valid only if hysteresis is enabled (see EEPROM 0x1C).

Value	Description
0	Increasing angles
1	Decreasing angles

SDN [5]

SPECIAL access (from CTRL register) done. Clears to 0 when a SPECIAL command is triggered, sets value of 1 when complete. Can clear with CTRL.CLS bit = 1.

Value	Description
0	SPECIAL command in progress, unless cleared previously
1	SPECIAL command completed

BDN [4]

Boot complete. EEPROM loaded and any startup self-tests are complete. Can clear with CTRL.CLS bit = 1.

Value	Description
0	Boot not complete, unless cleared previously
1	Boot complete

LBR [3]

Logic BIST (LBIST) running.

Value	Description
0	LBIST not running
1	LBIST running

CSTR [2]

CVH self-test running.

Value	Description
0	CVH self-test not running
1	CVH self-test running

BIP [1]

Boot in progress. Output values may not be valid.

Value	Description
0	Boot not in progress
1	Sensor is undergoing its boot sequence

AOK [0]

Angle output is OK. Indicates the PLL is locked and stat-up sequence has completed.

Value	Description
0	Angle is not valid
1	PLL is locked, angle value is valid

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Address 0x24:0x25 (ERR)—Device Error Flags

This is the error register. All errors are latched, meaning they remain high after they occur. Errors need to be read and then cleared in order to remove them. It is important that the user clears errors so that subsequent errors become visible. This is especially important for the RST error flag (reset), which is always enabled after power-on. If it is not removed, an unexpected reset cannot be discovered.

Address	0x24								0x25							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	1	0	1	0	WAR	STF	AVG	ABI	PLK	ZIE	EUE	OFE	UVD	UVA	MSL	RST
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

RIDC [15:12]

Register ID bits. Used to distinguish this registers from other serial registers. Hard-coded value.

Value	Description
1010	Register ID value

WAR [11]

Warning. An unmasked bit within the WARN register is asserted. May be masked by setting MSK.WAR bit in EEPROM.

Value	Description
0	No unmasked flag set in the WARN register (0x26:27)
1	Unmasked flag set in the WARN register

STF [10]

Self-test failure. Indicates either LBIST or CVH self-test failed.

Value	Description
0	No self-test failure
1	Self-test failure

AVG [9]

Angle averaging error. Indicates the ORATE value is too high for the rotation velocity, and the averaged angle value is corrupted.
The ORATE setting allows multiple angle values to be averaged together, for improved precision. This reduces the response time of the sensor, and can result in corrupted angle values if the velocity is too high.

Value	Description
0	No averaging error
1	Averaging error

ABI [8]

ABI integrity fault. The quadrature integrity of the ABI could not be maintained.

Value	Description
0	No ABI integrity fault
1	ABI integrity fault

PLK [7]

PLL lost lock. This indicates the PLL is not tracking the incoming angle properly. Angle value is corrupt.

Value	Description
0	No PLL lock.
1	PLL lost lock. Angle value invalid.

ZIE [6]

Zero-crossing integrity error. A zero-crossing did not occur within the maximum time expected, likely indicating a missing magnet or extreme rotation.

Value	Description
0	No zero-crossing error
1	Zero-crossing error

EUE [5]

EEPROM uncorrectable error. A multi-bit EEPROM read occurred. EEPROM bit errors are only checked on EEPROM load (i.e., power-up or reset).

Value	Description
0	No multi-bit EEPROM error
1	Multi-bit EEPROM error

OFE [4]

Oscillator frequency error. One of the oscillator watchdog circuits monitoring the high-frequency and low-frequency oscillators has tripped.

Value	Description
0	No oscillator error
1	Oscillator watchdog error

UVD [3]

VCC undervoltage detector tripped. Continues to set until fault goes away (and ERR register is cleared). This is the VCC input pin voltage.

Value	Description
0	No VCC voltage error
1	VCC undervoltage error detected

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UVA [2]

Undervoltage detector tripped. Continues to set until fault goes away (and ERR register is cleared). This is the analog regulator output.

Value	Description
0	No voltage error
1	Voltage error on the analog regulator output

MSL [1]

Magnetic sense low fault. Magnetic sense was below the low limit threshold.
Low limit threshold is set via the COM.MAG_THRES_LO field in EEPROM.
By default, this is set to ≈200 G.

Value	Description
0	No magnetic field low fault
1	Magnetic field lower than threshold

RST [0]

Reset condition. Sets on power-on reset or hard reset. Does not set on LBIST. Indicates volatile registers have been re-initialized.

Value	Description
0	No reset
1	Device has been reset. Volatile registers are re-initialized.

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Address 0x26:0x27 (WARN)—Device Warning Flags

This is the warning register. All warnings are latched, meaning they remain high after they occur. Warnings need to be read and then cleared in order to remove them. Warnings indicate either communication-type conditions or conditions that may result in a degradation of the angle accuracy, but are less likely to indicate a corruption of the angle than are errors.

Address	0x26								0x27							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	1	0	1	1	IER	CRC	0	SRW	XEE	TR	ESE	SAT	TCW	BSY	MSH	TOV
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

RIDC [15:12]

Register ID bits. Used to distinguish this register from other serial registers. Hard-coded value.

Value	Description
1011	Register ID value

IER [11]

Interface error. Invalid number of bits in SPI packet, or bit 15 of MOSI data = 1. Packet was discarded.
Also indicates a Manchester error.

Value	Description
0	No interface error
1	Interface error

CRC [10]

Incoming SPI CRC error. Packet was discarded.
Incoming CRC is only checked if the PWI.SC bit in EEPROM is set.

Value	Description
0	No incoming SPI CRC error
1	Incoming SPI CRC is bad

SRW [8]

Slew-rate warning. This warning is asserted if the ABI slew-rate limiting is enabled and a condition that requires the limiting to be applied has occurred.
The purpose of slew-rate limiting is to prevent an ABI integrity error.

Value	Description
0	Slew-rate limiting is not active
1	Slew-rate limiting is active ABI output is incrementing at the designated slew rate

XEE [7]

Extended execute error. A command initiated by an extended write failed. Write failed due to access error (not unlocked) or EEPROM write failure.

Value	Description
0	No incoming extended error
1	Extended execute error

TR [6]

Temperature out of range. The temperature sensor calculated a temperature below –60°C or above 180°C. Temperature saturates at those limits.

Value	Description
0	Temperature sensor in range
1	Sensed temperature is below -60° or above 180°C

ESE [5]

EEPROM soft error. A correctable (single-bit) EEPROM read occurred. EEPROM bit errors are only checked on EEPROM load (power-on or reset).

Value	Description
0	No single bit EEPROM error
1	EEPROM single bit error detected and corrected

SAT [4]

Aggregate saturation flag. Shows that any internal signals have saturated, likely to have been cause by extremely strong or weak fields.

Value	Description
0	No saturation detected within the signal chain
1	Saturation conditions detected within the signal chain

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TCW [3]

Turns-counter warning. Greater than 135° of angle change between turns-count updates. Indicates an unexpectedly large angle step between ZCD angle readings. The most likely cause is a loss of valid magnetic signal (i.e., magnet absence). Check the measured field strength (register 0x2A).

Value	Description
0	No turns-count warning
1	Angle difference between two successive ZCD samples is > 135°

BSY [2]

Extended access overflow. An extended write or extended read was initiated before the previous had completed.

Value	Description
0	No extended access error
1	Extended access error

MSH [1]

Magnetic sense high fault. Magnetic sense exceeded the high-limit threshold.
The high-limit threshold is set via the COM.MAG_THRES_HI field in EEPROM.
By default, this field is set to ≈1200 G.

Value	Description
0	No magnetic field high fault
1	Magnetic field exceeded threshold

TOV [0]

Turns-counter overflow error.
The turns-counter surpassed its maximum value of 255 or –256 full rotations.
This is equivalent to a turns register value of 511 or –512 for 180° resolution, or 2047 or –2048 for 45° resolution.
Must be cleared with a turns-count reset (see SPECIAL commands in the CTRL register description, 0x1E).

Value	Description
0	No turns-count overflow error
1	Turns-count overflow error

Address 0x28:0x29 (TSEN)—Temperature Sensor

Address	0x28								0x29							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	1	1	1	1	TEMPERATURE											
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

RIDC [15:12]

Register ID bits. Used to distinguish this registers from other serial registers. Hard-coded value.

Value	Description
1111	Register ID value

TEMPERATURE [11:0]

Current junction temperature from internal temperature sensor relative to room temperature (signed value, 2's complement). Value is in 1/8 of a degree. Temperature °C ≈ (TSEN.TEMPERATURE / 8) + 25.

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Address 0x2A:0x2B (FIELD)—Field Strength (in Gauss)

Address	0x2A								0x2B							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	1	1	1	0	GAUSS											
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

RIDC [15:12]

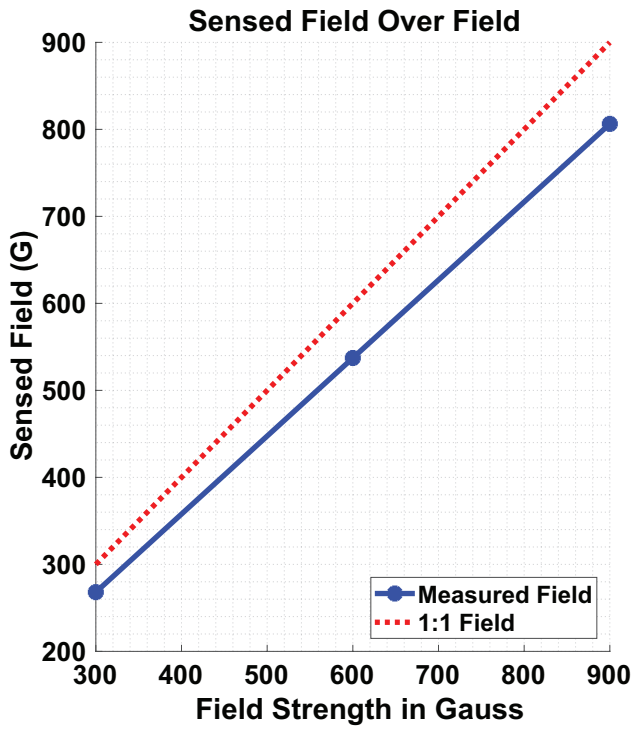
Register ID bits. Used to distinguish this register from other serial registers. Hard-coded value.

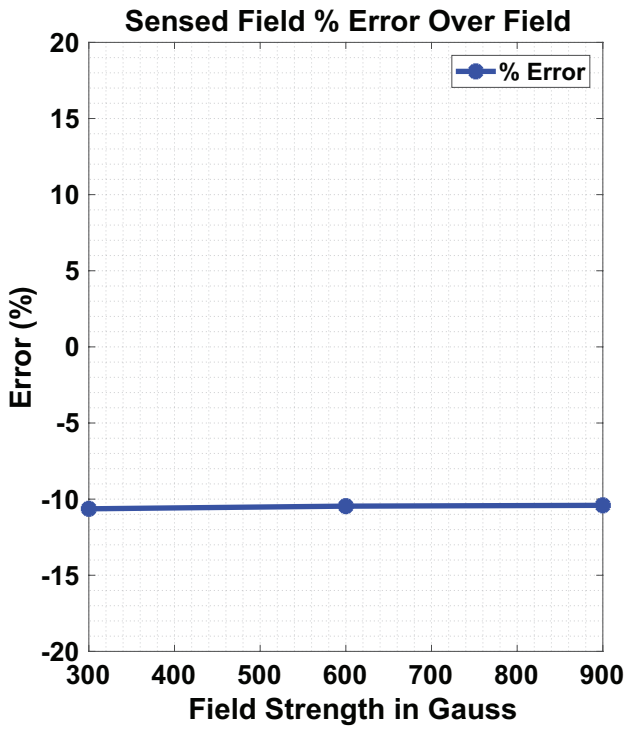
Value	Description
1110	Register ID value

GAUSS [11:0]

Measured field strength in gauss. Updated every 128 µs. Field reading is used for signal path adjustments internal to the IC and is provided for convenient comparison of field readings over magnetic air gap. No guarantee of accuracy is made.

In general, the A1333 field reading is ≈11% less than actual gauss levels.





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Address 0x2C:0x2D (TURNS)—Turns Counter

Address	0x0C								0x0D							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	1	1	0	P	TURNS											
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

RIDC [15:13]

Register ID bits. Used to distinguish this register from other serial registers. Hard-coded value.

Value	Description
110	Register ID value

P [12]

Parity bit. Odd parity is calculated across all bits. Result is that there should always be an odd number of ones in this 16-bit word.

TURNS [11:0]

Signed 2's complement value. Indicates total number of turns relative to angle observed on power-up. Turns resolution set via EEPROM to either 180° or 45°.
The A1333 is capable of tracking up to 256 full mechanical rotations, independent of the resolution selected.

Bit Value	Turns in 180° Mode (Actual Mechanical Full Rotations)	Turns in 45° Mode (Actual Mechanical Full Rotations)
0000 0000 0000	0 (0)	0 (0)
0000 0000 0001	1 (1/2)	1 (1/8)
0001 1111 1111	511 (255.5)	511 (63.875)
0010 0000 0000	–	512 (64)
0111 1111 1111	–	2047(255.875)
1111 1111 1111	–1 (–1/2)	–1 (–1/8th)
1110 0000 0000	–512 (–256)	–512 (–64)
1000 0000 0000	–	–2048 (–256)

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Address 0x30:0x31 (HANG)—Hysteresis Angle Value (12 bits)

Address	0x30								0x31							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	EF	UV	P	ANGLE_HYS											
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

EF [14]

Error flag. If any unmasked bit in ERR or WARN is set, value is 1.

Value	Description
0	No unmasked errors
1	Unmasked error is present

UV [13]

Undervoltage flag (real time). Logical OR of analog and digital UV flags (UVD and UVA flags). Conditions are real time, but may be masked by EEPROM error mask bits.

Value	Description
0	No undervoltage condition detected
1	Undervoltage condition detected

P [12]

Parity bit. Odd parity is calculated across all bits (EF, UV, and ANGLE_HYS). Result is that there should always be an odd number of ones in this 16-bit word.

ANGLE_HYS [11:0]

Angle from PLL after hysteresis processing.
Angle in degrees is 12-bit value × (360/4096).

Address 0x32:0x33 (ANG15)—Current Angle Reading (15 bits)

Address	0x32								0x33							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	ANGLE_15														
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

ANGLE_15 [14:0]

15-bit compensated angle (not rounded).
Angle in degrees is a 15-bit value × (360/32768)

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Address 0x34:0x35 (ZANG)—ZCD Angle

Angle from the ZCD signal path is used for turns-counting. This angle is not compensated over temperature and does not exactly match the PLL angle value.

Address	0x34								0x35							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	EF	UV	P	ANGLE_ZCD											
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

EF [14]

Error flag. If any unmasked bit in ERR or WARN is set, value is 1.

Value	Description
0	No unmasked errors
1	Unmasked error is present

UV [13]

Undervoltage flag (real time). Logical OR of analog and digital UV flags (UVD and UVA flags). Conditions are real time, but may be masked by EEPROM error mask bits.

Value	Description
0	No undervoltage condition detected
1	Undervoltage condition detected

P [12]

Parity bit. Odd parity is calculated across all bits (EF, UV, and ANGLE_ ZCD). Result is that there should always be an odd number of ones in this 16-bit word.

ANGLE_ZCD [11:0]

Angle from the ZCD signal path. Not compensated.
Angle in degrees is 12-bit value × (360/4096).

Address 0x3C:0x3D (KEY)—Key Register

Address	0x3C								0x3D							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEYCODE								0	0	0	0	0	0	0	CUL
R/W	W	W	W	W	W	W	W	W	R	R	R	R	R	R	R	R

KEYCODE [15:8]

Unlock code is entered here. Once unlocked, EEPROM and shadow registers may be written. In addition, some SPECIAL commands require a device unlock.
Unlocking requires five successive writes to the KEYCODE field, following the unlock sequence shown below.
The CUL bit indicates a successful unlock.

Write #	Code
1	0x00
2	0x27
3	0x81
4	0x1F
5	0x77

CUL [0]

Indicates the device is unlocked.

Value	Description
0	Device is not unlocked
1	Device is unlocked

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EEPROM/SHADOW MEMORY TABLE

The EEPROM/shadow register bitmap is shown below.

All EEPROM and shadow contents can be read by the user, without unlocking. Writing requires device unlock.

Table 14: EEPROM / Shadow Memory Map

EEPROM Address	Shadow Memory Address	Register Name	Bits																											
			31:26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x18	0x58	PWE	ECC	–	–	–	–	–	–	–	–	–	–	–	–	–	TOV	TR	MSH	SAT	ESE	MSL	UV	AVG	ZIE	PLK	STF	EUE	OFE
0x19	0x59	ABI	ECC	–	–	–	–	ABI_SLEW_TIME						INV	-X-	-X-	AHE	–	–	INDEX_MODE		WDH	PLH	IOE	UVW	RESOLUTION_PAIRS			
0x1A	0x5A	MSK	ECC	–	–	IER	CRC	-X-	SRW	XEE	TR	ESE	SAT	TCW	BSY	MSH	TOV	WAR	STF	AVG	ABI	PLK	ZIE	EUE	OFE	UVD	UVA	MSL	RST
0x1B	0x5B	PWI	ECC	–	–	PEN	PWM_BAND			PWM_FREQ				–	PHE	PEO	PES	–	–	–	–	–	–	–	–	DM	–	S17	SC
0x1C	0x5C	ANG	ECC	–	–	ORATE				RD	RO	HYSTERESIS						ZERO_OFFSET											
0x1D	0x5D	LPC	ECC	–	–	T45	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
0x1E	0x5E	COM	ECC	–	–	LOCK				LBE	CSE	–	–	–	–	DST	DHR	MAG_THRES_HI					MAG_THRES_LO						
0x1F	–	CUS	ECC	–	–	Customer EEPROM Space																							

Address 0x18 (PWE)—PWM Error Enable

This address space contains the PWM error enable bits. When set to 1, the PWM output responds to errors, as set via the PWI.PEO and PWI.PES bits.

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	–	–	–	–	–	–	–	–	–	–	–	TOV	TR	MSH	SAT	ESE	MSL	UV	AVG	ZIE	PLK	STF	EUE	OFE
Default	–	–	–	–	–	–	–	–	–	–	–	0	0	0	0	0	0	0	0	0	0	0	0	0

TOV [12]

PWM turns-counter overflow error enable.
Duty cycle 72.5%, if PWI.PEO and PWI.PES are 1.

Value	Description
0	PWM does not respond to a TOV error
1	PWM output respond to a TOV error

MSH [10]

PWM magnetic sense high error enable.
Duty cycle 61.25%, if PWI.PEO and PWI.PES are 1.

Value	Description
0	PWM does not respond to a MSH error
1	PWM output respond to a MSH error

TR [11]

PWM temperature out of range error enable.
Duty cycle 66.875%, if PWI.PEO and PWI.PES are 1.

Value	Description
0	PWM does not respond to a TR error
1	PWM output respond to a TR error

SAT [9]

PWM saturation error enable.
Duty cycle 55.625%, if PWI.PEO and PWI.PES are 1.

Value	Description
0	PWM does not respond to a SAT error
1	PWM output respond to a SAT error

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ESE [8]

PWM EEPROM soft error enable.
Duty cycle 50%, if PWI.PEO and PWI.PES are 1.

Value	Description
0	PWM does not respond to a ESE error
1	PWM output respond to a ESE error

MSL [7]

PWM magnetic sense low error enable.
Duty cycle 44.375%, if PWI.PEO and PWI.PES are 1.

Value	Description
0	PWM does not respond to a MSL error
1	PWM output respond to a MSL error

UV [6]

PWM undervoltage error enable.
Duty cycle 38.75%, if PWI.PEO and PWI.PES are 1.

Value	Description
0	PWM does not respond to an UV error
1	PWM output respond to a UV error

AVG [5]

PWM averaging error enable.
Duty cycle 33.125%, if PWI.PEO and PWI.PES are 1.

Value	Description
0	PWM does not respond to a AVG error
1	PWM output respond to a AVG error

ZIE [4]

PWM zero-crossing error enable.
Duty cycle 27.5%, if PWI.PEO and PWI.PES are 1.

Value	Description
0	PWM does not respond to a ZIE error
1	PWM output respond to a ZIE error

PLK [3]

PWM PLL lost lock error enable.
Duty cycle 21.875%, if PWI.PEO and PWI.PES are 1.

Value	Description
0	PWM does not respond to a PLK error
1	PWM output respond to a PLK error

STF [2]

PWM self-test error enable.
Duty cycle 16.25%, if PWI.PEO and PWI.PES are 1.

Value	Description
0	PWM does not respond to a STF error
1	PWM output respond to a STF error

EUE [1]

PWM EEPROM uncorrectable error enable.
Duty cycle 10.625%, if PWI.PEO and PWI.PES are 1.

Value	Description
0	PWM does not respond to a EUE error
1	PWM output respond to a EUE error

OFE [0]

PWM oscillator frequency error enable.
Duty cycle 5%, if PWI.PEO and PWI.PES are 1.

Value	Description
0	PWM does not respond to a OFE error
1	PWM output respond to a OFE error

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Address 0x19(ABI)—ABI Control

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	–	–	ABI_SLEW_TIME						INV	-X-	-X-	AHE	–	–	INDEX_MODE		WDH	PLH	IOE	UVW	RESOLUTION_PAIRS			
Default	–	–	0	0	1	0	0	0	0	–	–	1	0	0	0	0	0	0	1	0	0	1	0	0

ABI_SLEW_TIME [21:16]

ABI slew time rate. A value of 0 disables slew limiting.
Minimum edged-to-edge time for ABI output is defined by:

$$(N + 1) \times 125\ ns$$

where N is the value of ABI_SLEW_TIME.
This limits the maximum ABI velocity. Reducing the ABI resolution can be used to counteract this.

Value	Description
00 0000	Slew limiting disable
00 0001	250 ns of slew control
…	…
11 1111	8 µs of slew control

INV [15]

Invert ABI/UVW signals.

Value	Description
0	ABI/UVW signals behave as shown below for an increasing angle value. Q1 through Q4 represent changes in angle at the ABI resolution.

State Name	A	B
Q1	0	0
Q2	0	1
Q3	1	1
Q4	1	0

Value	Description
1	ABI/UVW signals are inverted and behave as shown below for an increasing angle value. Q1 through Q4 represent changes in angle at the ABI resolution.

State Name	A	B
Q1	1	1
Q2	1	0
Q3	0	0
Q4	0	1

AHE [12]

ABI hysteresis enable. When 1, hysteresis is applied to the ABI or UVW angle.

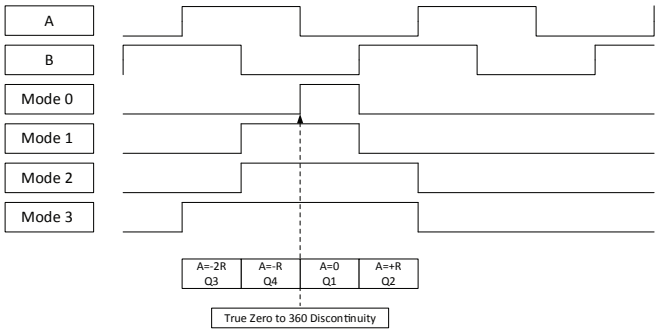
Value	Description
0	Hysteresis is not applied to ABI or UVW
1	Hysteresis applied to ABI or UVW outputs

INDEX_MODE [9:8]

Defines the width and placement of the “I” pulse in ABI.

Value	Description
0	“I” pulse is set only at 0° to +R
1	“I” pulse set between –R to +R
2	“I” pulse set between –R to +2R
3	“I” pulse set between –2R and +2R

“R” indicates the ABI quadrature resolution.



WDH [7]

Enable ABI all high (before inversion) as error mode if oscillator frequency watchdog error trips.

Value	Description
0	ABI pins do not respond to an OFE flag
1	ABI outputs go high if an OFE is detected

PLH [6]

Enable ABI all high (before inversion) as error mode if a PLL loss of lock is detected.

Value	Description
0	ABI pins do not respond to an PLK flag
1	ABI outputs go high if the PLK flag is set

IOE [5]

Incremental output enable.

Value	Description
0	ABI/UVW pins are not active
1	ABI/UVW pins are active; behavior defined by ABI.UVW bit

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UVW [4]

Define behavior of the ABI/UVW pins if ABI.IOE = 1.

Value	Description
0	ABI active
1	UVW active

RESOLUTION_PAIRS [3:0]

Defines resolution of ABI/UVW outputs.
In ABI mode, cycle resolution = $2^{(14-n)}$, where n is the RESOLUTION_PAIRS value.
In UVW mode, the number of pole pairs is n + 1.

Value	AB Cycles per Rev	UVW Pole Pairs
0000	–	1
0001	–	2
0010	–	3
0011	2^{11} = 2048	4
0100	2^{10} = 1024	5
…	…	…
1110	2^{0} = 1	15
1111	N/A	16

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Address 0x1A (MSK)—Mask Bits

This address range contains error mask bits. When set, the applicable error condition does not assert the EF bit in the various angle and turns-count registers.

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IER	CRC	-X-	SRW	XEE	TR	ESE	SAT	TCW	BSY	MSH	TOV	WAR	STF	AVG	ABI	PLK	ZIE	EUE	OFE	UVD	UVA	MSL	RST
Default	0	0	–	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

IER [23]
Masks the IER flag from setting the EF bit.

CRC [22]
Masks the CRC flag from setting the EF bit.

SRW [20]
Masks the SRW flag from setting the EF bit.

XEE [19]
Masks the XEE flag from setting the EF bit.

TR [18]
Masks the TR flag from setting the EF bit.

ESE [17]
Masks the ESE flag from setting the EF bit.

SAT [16]
Masks the SAT flag from setting the EF bit.

TCW [15]
Masks the TCW flag from setting the EF bit.

BSY [14]
Masks the BSY flag from setting the EF bit.

MSH [13]
Masks the MSH flag from setting the EF bit.

TOV [12]
Masks the TOV flag from setting the EF bit.

WAR [11]
Masks the WAR flag from setting the EF bit.

STF [10]
Masks the STF flag from setting the EF bit.

AVG [9]
Masks the AVG flag from setting the EF bit.

ABI [8]
Masks the ABI flag from setting the EF bit.

PLK [7]
Masks the PLK flag from setting the EF bit.

ZIE [6]
Masks the ZIE flag from setting the EF bit.

EUE [5]
Masks the EUE flag from setting the EF bit.

OFE [4]
Masks the OFE flag from setting the EF bit.

UVD [3]
Masks the UVD flag from setting the EF bit.

UVA [2]
Masks the UVA flag from setting the EF bit.

MSL [1]
Masks the MSL flag from setting the EF bit.

RST [0]
Masks the RST flag from setting the EF bit.

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Address 0x1B (PWI)—PWM Interface Control

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PEN	PWM_BAND			PWM_FREQ				–	PHE	PEO	PES	–	–	–	–	–	–	–	–	DM	–	S17	SC
Default	0	1	1	0	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

PEN [23]

PWM enable.

Value	Description
0	PWM pin tri-stated
1	PWM enabled

PWM_BAND [22:20]

PWM frequency band. Defines the PWM carrier frequency when combined with PWM_FREQ.

PWM_FREQ [19:16]

PWM frequency select. Defines the PWM carrier frequency when combined with PWM_BAND.

Table 15: Nominal PWM Carrier Frequencies

		PWM_BAND							
		0	1	2	3	4	5	6	7
PWM_FREQ	0	3125	2778	2273	1667	1087	641	352	185
	1	3101	2740	2222	1613	1042	610	333	175
	2	3077	2703	2174	1563	1000	581	316	166
	3	3053	2667	2128	1515	962	556	301	157
	4	3030	2632	2083	1471	926	532	287	150
	5	3008	2597	2041	1429	893	510	275	143
	6	2985	2564	2000	1389	862	490	263	137
	7	2963	2532	1961	1351	833	472	253	131
	8	2941	2500	1923	1316	806	455	243	126
	9	2920	2469	1887	1282	781	439	234	121
	10	2899	2439	1852	1250	758	424	225	116
	11	2878	2410	1818	1220	735	410	217	112
	12	2857	2381	1786	1190	714	397	210	108
	13	2837	2353	1754	1163	694	385	203	105
	14	2817	2326	1724	1136	676	373	197	101
	15	2797	2299	1695	1111	658	362	191	98

PHE [14]

PWM hysteresis enable.

Value	Description
0	No hysteresis applied to PWM output
1	Hysteresis settings applied to PWM output

PEO [13]

PWM error output enable. If 1, PWM responds to errors, as defined by the PES bit.

Value	Description
0	PWM output does not respond to error flags
1	PWM output responds to errors, as defined by the PWI.PES field

PES [12]

PWM error select, if PEO = 1.

Value	Description
0	PWM output tri-states for all enabled error conditions (see PWE address space)
1	For all enabled errors the PWM carrier frequency is halved and the highest-priority error is identified by a specific duty cycle; see the PWE address space description

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DM [3]

Disable Manchester interface.

Value	Description
0	Manchester functions as typical
1	A1333 does not respond to a Manchester command on the V_{CC} line

S17 [1]

A1333 ignores the 17th SPI clock. Allows negative edge sampling at the MCU (host).

SC [0]

A1333 monitors the incoming CRC.

Value	Description
0	Incoming CRC is not monitored
1	A1333 monitors incoming CRC and discards the packet if it is corrupt

Address 0x1C (ANG)

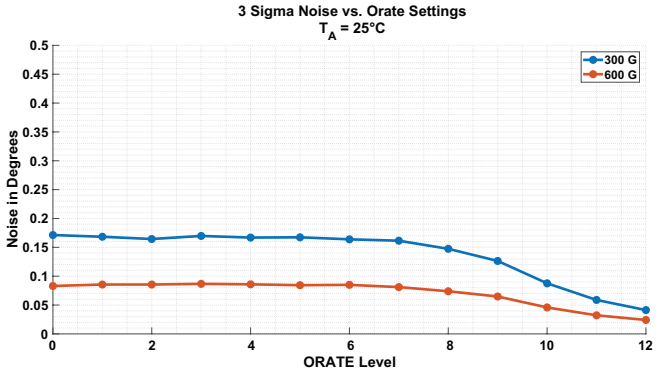
Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ORATE				RD	RO	HYSTERESIS						ZERO_OFFSET											
Default	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ORATE [23:20]

Reduces the output rate by averaging samples. 2^{ORATE} samples are averaged. ORATE values greater than 12 are reduced to 12 in the logic, meaning that up to 4096 samples = 4 ms can be selected for the averaging time.

Value	Description
0000	1 sample. 1 µs update rate.
0001	2 samples. 2 µs update rate.
0010	4 samples. 4 µs update rate.
…	…
1100	4096 samples. ≈4 ms update rate.

The majority of angle noise is composed of low-frequency content. Due to this, noticeable improvements in IC resolution are not observed until relatively high values of ORATE (8 or greater, corresponding to 256 samples). Because of this, non-zero ORATE settings are not recommended, except in cases where sensor response time is not a major concern (i.e., low-rpm applications).



RD [19]

Rotates die. Rotates final angle 180°. Last step in the angle algorithm. This is a convenient setting to adjust one die in a dual-die package for conformance to the other die. Occurs after the ZERO_OFFSET and RO adjustments.

Value	Description
0	Rotation is not applied
1	180° added to final angle

RO [18]

Rotation direction. If set to 0, increasing angle movement is in the clockwise direction when looking down on the top of the die. If set to 1, increasing angle movement is in the counter-clockwise direction. Occurs after the ZERO_OFFSET adjust and prior to the RD manipulation.

Value	Description
0	Output angle increases with a clockwise rotation (when viewed from above the magnet and device)
1	Output angle increases with a counter-clockwise rotation (when viewed from above the magnet and device)

HYSTERESIS [17:12]

Angle hysteresis threshold. In 14-bit resolution. Provides ≈0 to 1.384° of hysteresis.

Value	Description
00 0000	No hysteresis
00 0001	≈0.022° of hysteresis
…	…
11 1111	≈1.384° of hysteresis

ZERO_OFFSET [11:0]

Post-compensation zero offset (or DC adjust), at 12-bit resolution. This value is subtracted from the measured angle value. Operation occurs prior to the RD and RO manipulations.

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Address 0x1D (LPC)

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	T45	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Default	1	–	0	0	0	0	0	0	1	0	1	1	0	0	1	0	1	0	0	1	1	1	1	1

T45 [23]

Defines the resolution of the turns-counter.

Value	Description
0	Turns-counter measures 180° of rotation
1	Turns-counter measures 45° of rotation

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Address 0x1E (COM)

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LOCK				LBE	CSE	–	–	–	–	DST	DHR	MAG_THRES_HI						MAG_THRES_LO					
Default	0	0	0	0	1	1	–	–	–	–	0	0	1	0	0	1	0	1	0	0	1	1	0	1

LOCK [23:20]

EEPROM and shadow memory lock.
Permanent lock.

Value	Description
1100	Writing to EEPROM is locked
0011	Writing to EEPROM and shadow memory is locked

LBE [19]

Power-up Logic BIST enable.
LBIST requires ≈30 ms to run.

Value	Description
0	LBIST is not run on power-up
1	LBIST is run on power-up

LBIST and CVH self-test are run in parallel. Therefore if both are enabled on power-up, power-on time is ≈30 ms.

CSE [18]

Power-up CVH self-test enable.
CVH self-test requires ≈30 ms to run.

Value	Description
0	CVH is not run on power-up
1	CVH is run on power-up

LBIST and CVH self-test are run in parallel. Therefore, if both are enabled on power-up, power-on time is ≈30 ms.

DST [13]

Disable Self-test initiation from the serial register.

Value	Description
0	Self-tests may be initiated via a SPECIAL serial register command
1	Prevents running either LBIST or CVH self-test from the CTRL register

DHR [12]

Disable Hard reset from the serial register.

Value	Description
0	Hard reset may be initiated via a SPECIAL serial register command
1	Prevents initiating a hard reset from the CTRL register.

MAG_THRES_HI [11:6]

Magnetic threshold high value. Determine set point of the MSH flag. When set to 0, check is disabled.
Limit increases in 32 G increments. Set to 1184 G at factory.

Value	Description
00 0000	High-field flag disabled
00 0001	32 G
00 0010	64 G
…	…
10 0101	1184 G
…	…
11 1111	2016 G

MAG_THRES_LO [5:0]

Magnetic threshold low value. Determine set point of the MSL flag. When set to 0, check is disabled.
Limit increased in 16 G increments. Set to 208 G at factory.

Value	Description
00 0000	Low-field flag disabled
00 0001	16 G
00 0010	32 G
…	…
00 1101	208 G
…	…
11 1111	1008 G

Address 0x1F (CUST)

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Customer EEPROM Space																							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CUSTOMER [23:0]

Customer EEPROM space.

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SAFETY AND DIAGNOSTICS

The A1333 was developed in accordance with the ASIL design flow (ISO 26262) and incorporates several internal diagnostics as well as error/warning/status flags enabling the host microntroller to assess the operational status of the die.

A short summary of the A1333 diagnostics is provided below. A complete listing and discussion of the A1333 safety features is provided in the A1333 Safety Manual, which is available upon request.

Built-In Self-Tests

The A1333 features two built-in-self-tests (BISTs) that can be configured to run at power-up and can also be initiated at any time by the system microcontroller via a serial register write. A failure of any one of the self-tests asserts the self-test failure flag, STF, within the error register.

CVH SELF-TEST

CVH self-test is a method of verifying the operation of the CVH transducer without applying an external magnetic field. This feature is useful for both manufacturing test and for integration debug. The CVH self-test is implemented by changing the switch configuration from the typical operating mode into a test configuration, allowing a test current to drive the CVH in place of the magnetic field. By changing the direction of the test current and by changing the elements in the CVH that are driven, the self-test circuit emulates a changing angle of magnetic field. The measured angle is monitored to determine a passing or failing device. CVH self-test typically takes 30 ms to run (when run in parallel with LBIST, the entire test time is 30 ms).

LOGIC BUILT-IN SELF-TEST (LBIST)

Logic BIST is implemented to verify the integrity of the A1333 logic. It can be executed in parallel with the CVH self-test. LBIST is effectively a form of auto-driven scan. The logic to be tested is divided into 31 scan chains. The chains are fed in parallel by a 31-bit linear feedback shift register (LFSR) to generate pseudo-random data. The output of the scan chains are fed back into a multiple-input shift register (MISR) that accumulates the shifted bits into a 31-bit signature.

LBIST takes ≈30 ms to complete (when run in parallel with CHV self-test, the entire test time is ≈30 ms).

Status, Error, and Warning Flags

The A1333 features many flags used to detect faulty external or internal conditions. Select conditions are briefly described in Table 16.

All flags can be read through the serial registers via SPI or Manchester communication. All unmasked error flags assert the general error flag ,which is included in the angle register (0x20), providing an overview of the sensor status.

Error reporting when using PWM or ABI is more limited and is discussed later.

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Table 16: Status and Error Flags

Fault Condition	Description	Sensor Response
$V_{CC} < V_{UVD}$	Indicates V_{CC} is below expected level.	UVD flag set in ERR register UV flag set in ANG register EF flag set in ANG register
Field > High Threshold	Sensor monitors field level in case of mechanical failure. High level is programmable from 0 to 2016 G in 32 G steps. By default, set to ≈1184 G.	MSH flag set in WARN register EF flag set in ANG register
Field < Low Threshold	Sensor monitors field level in case of mechanical failure. Low level is programmable from 0 to 1008 G in 16 G steps. By default, set to ≈208 G.	MSL flag set in ERR register EF flag set in ANG register
$T_A < –60°C$ or $T_A > 180°C$	Ambient temperature beyond maximum detectable value.	TR flag set in WARN register EF flag set in ANG register
Oscillator Frequency Discrepancy	The A1333 cross-checks the high- and low-frequency oscillators for proper functionality.	OFE flag set in ERR register EF flag set in ANG register
Single-Bit EEPROM Error (Correctable)	Detects and corrects single-bit EEPROM errors.	ESE bit set in WARN register EF flag set in ANG register
Multi-Bit EEPROM Failure (Uncorrectable)	Detects multi-bit EEPROM errors.	EUE bit set in ERR register EF flag set in ANG register
Signal Path Failure	Multiple comparisons and checks within the signal path: • Main signal path output compared to the ZCD signal path • PLL lock status monitored • Main signal path is checked for saturation	PLK or ZIE set within the ERR register EF flag set within the ANG register
Loss of V_{CC}	Determines if system power was lost. Indicates all volatile registers have been reset (such as turns-count).	RST bit set in ERR register EF flag set in ANG register
ABI Integrity Fault	Excessive noise or excessive rotational velocity for a given ABI resolution. IC monitors state of ABI and flags skipped states.	ABI bit set in ERR register EF flag set in ANG register
Analog Regulator Drift	IC monitors output of analog regulator, ensuring transducer is supplied with proper voltage.	UVA bit set in ERR register UV flag set in ANG register EF flag set in ANG register
Excessive Magnet Travel	Sensor detects when > 256 rotations have occurred, indicating the turns-counter has saturated.	TOV bit set in WARN register EF flag set in ANG register
Excessive Magnet Velocity for Turns-Counting	If the sensor detects > 135° travel between successive turns-count updates.	TCW bit set in WARN register EF flag set in ANG register
Excessive Magnet Velocity for Given ORATE Setting	Indicates the angle reading spanned more than two quadrants during the ORATE sample period; therefore, the average might be incorrect. Can occur under extreme velocity and high averaging, or when a magnetic field is not present and the samples out of the CVH are random.	AVG bit set in ERR register EF flag set in the ANG register
Incoming SPI Packet Corruption	IER error detects an invalid number of SCLKs, or a 1 in the MSB on MOSI. If using 20-bit SPI packets and incoming CRC validation is enabled (SC bit in EEPROM 0x1B), the CRC flag asserts.	Depending on implementation and amount of corruption: IER bit set in WARN register CRC bit set in WARN register EF flag set in ANG register

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ERROR REPORTING IN PWM

The PWM output can be configured to change state if certain errors occur. There are three options:

- No error reporting
- Tristate the PWM
- Halve the carrier frequency and represent the error via different duty cycles

Two EEPROM bits, PEO and PES, control how errors are reported in PWM mode, both of which are in the PWS address row of EEPROM:

Table 17: PWM Error Output Enable Option (PEO)

Code	Description
0	PWM does not respond to errors.
1	PWM output responds to errors as selected with the PES field.

Table 18: PWM Error Select (PES)

Code	Description
0	PWM tristates on an error.
1	PWM carrier frequency halved and highest priority error output on PWM as selected duty cycle.

The error priority and corresponding duty cycle are shown in Table 19 below, with the high priority error dictating the PWM duty cycle.

Each error code must be enabled via EEPROM. This prevents losing the PWM output due to a spurious error.

The enable bits can be found within the PWE (0x18) EEPROM row.

Table 19: PWM Error Duty Cycle and Priority

Error	Priority	Duty Cycle %	Description / Persistence
OFE	1 (highest)	5	Watchdog error. Permanent.
EUE	2	10.625	EEPROM uncorrectable error. Permanent.
STF	3	16.25	Self-test failure. Permanent.
PLK	4	21.875	PLL not locked. Persists until PLL locks.
ZIE	5	27.5	Zero-crossing integrity error. Persists until goes away.
AVG	6	33.125	Angle averaging error. Outputs once then clears.
UV	7	38.75	Undervoltage (UVA and/or UVCC dependent on serial error masks). Persists until no unmasked undervoltage.
MSL	8	44.375	Persists until field strength higher than low threshold.
ESE	9	50	EEPROM correctable error. Outputs once then clears.
SAT	10	55.625	Persists until no saturation warnings.
MSH	11	61.25	Persists until field strength lower than high threshold.
TR	12	66.875	Persists until temperature within range.
TOV	13 (lowest)	72.5	Turns-counter overflow. Persists until cleared via CTRL register.

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ERROR REPORTING IN ABI/UVW

Error reporting when using ABI/UVW requires the transmission of angle data to be interrupted. As a result, only the two most severe errors are allowed to interrupt the pulse stream, preventing potential spurious errors from interrupting the primary mission of the IC.

As further assurance against undesired ABI/UVW interruption, error reporting must be individually enabled in EEPROM. The error conditions that may be reported are:

- Oscillator frequency error
- PLL loss of lock error

When enabled, and an error occurs, all three ABI lines are brought high (prior to inversion, if enabled). This is an undefined state in both ABI (if using default I mode width) and UVW.

Error reporting is enabled via the following two EEPROM bits, housed within address row 0x19.

WDH [7]

Enable ABI all high (before inversion) as error mode if oscillator frequency watchdog error trips.

Value	Description
0	ABI pins do not respond to an OFE flag
1	ABI outputs go high if an OFE is detected

PLH [6]

Enable ABI all high (before inversion) as error mode if a PLL loss of lock is detected.

Value	Description
0	ABI pins do not respond to an PLK flag
1	ABI outputs go high if the PLK flag is set

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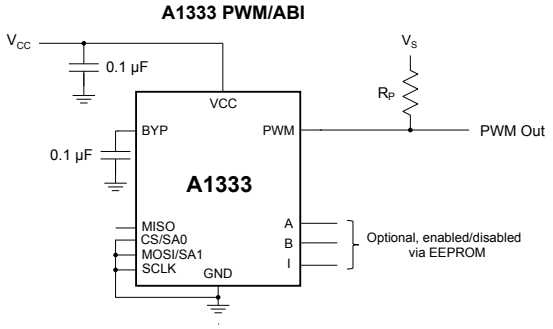
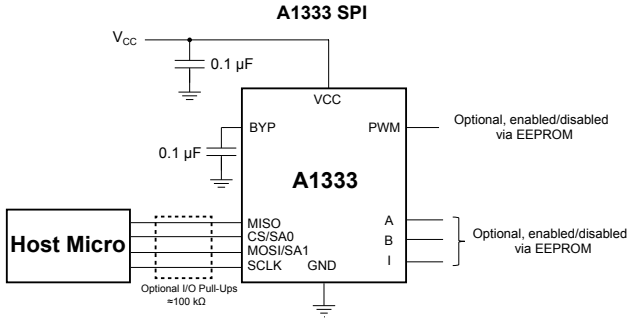
APPLICATION INFORMATION

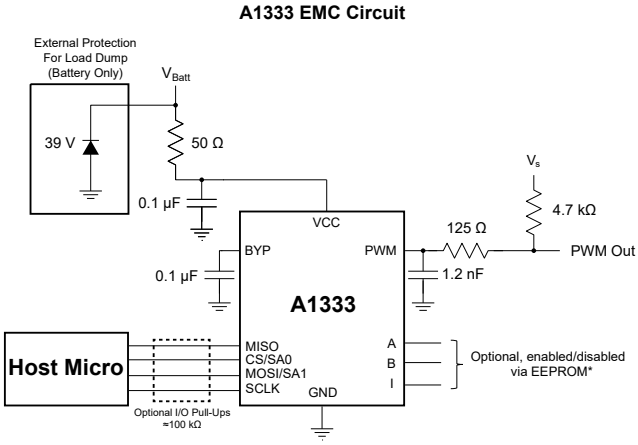
The A1333 features SPI, PWM, ABI/UVW, and Manchester outputs. Basic reference circuits for connecting the A1333 are shown in Figure 56.



Typical A1333 configuration using PWM output.
Digital reads/writes requests transmitted via Manchester encoding on the V_{CC} line.
SA0/SA1 brought to BYP or GND to configure Manchester address.



Typical A1333 configuration using SPI interface.



A1333 reference design for stringent EMC requirements.
*If using ABI outputs, a 10 nF capacitor to GND on each line is recommended (this added capacitance will reduce the edge rates on ABI).

Figure 56: A1333 PWM/ABI, SPI, and EMC Application Circuits

ESD Performance

The ESD performance of the A1333 device is shown in Table 20. For questions regarding ESD optimization, contact Allegro.

Table 20: HBM ESD Rating (per AEC-Q100 002)

Package	ESD Rating
TSSOP-14	5 kV
eTSSOP-24	3 kV [1]

[1] With GND pins of both die shorted together, IC performs to a 4 kV level.

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Setting the Zero-Degree Position

When shipped from the factory, the default angle value when oriented as shown in Figure 57 is 0° for both die. In some cases, the end user may want to program an angle offset in the A1333 to compensate for variations in magnetic assemblies, or for applications where absolute system-level readings are required.

The internal algorithm for computing the output angle is:

$$Angle_{out} = Angle_{RAW} - ZERO\_OFFSET$$

where ZERO_OFFSET is a 12-bit field in EEPROM.

To "zero out" the A1333 reported angle, during final application calibration, position the magnet above the A1333 in the desired zero-degree position and read the reported angle. This angle becomes the necessary ZERO_OFFSET value to "zero-out" the angle.

In some cases, it may be convenient to have a 180° offset between die. The RD field (bit 19 of EEPROM location 0x19) allows a 180° offset to be applied. When set, this bit adds 180° to the output of the die (occurs after ZERO_OFFSET and rotation adjustments).

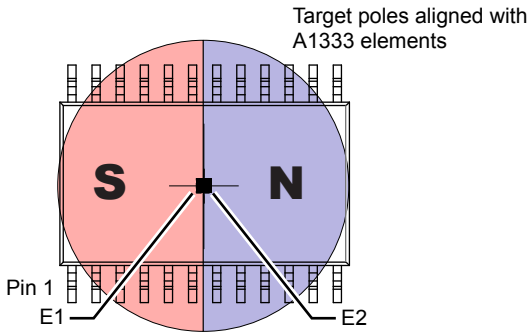


Figure 57: Orientation of Magnet Relative to Primary and Secondary Die

Magnetic Target Requirements

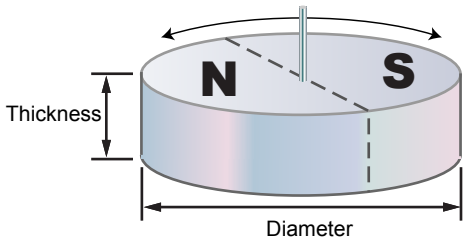
The A1333 is designed to operate with magnets constructed with a variety of magnetic materials, geometries, and field strengths. A list of common magnet dimensions is provided in Table 21.

The A1333 actively measures and adapts to its magnetic environment. This allows operation throughout a large range of field strengths (recommended range is 300 to 1000 G; however, operation beyond this range does not result in long-term damage).

Due to the greater signal-to-noise ratio provided at greater field strengths, performance inherently increases with increasing field strength. Typical angle performance over applied field strength is shown in Figure 59 and Figure 60.

Table 21: Target Magnet Parameters

Magnetic Material	Diameter (mm)	Thickness (mm)
Neodymium (sintered) [1]	10	2.5
Neodymium (sintered)	8	3
Neodymium/SmCo	6	2.5



[1] A sintered neodymium magnet with 10 mm (or greater) diameter and 2.5 mm thickness is the recommended magnet for redundant applications.

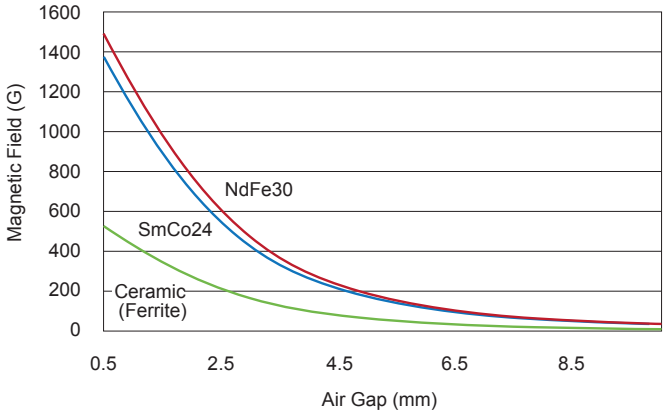


Figure 58: Magnetic Field versus Air Gap for Magnet 6 mm in Diameter and 2.5 mm Thick

Allegro can provide similar curves for customer application magnets upon request. Allegro recommends larger magnets for applications that require optimized-accuracy performance.

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Magnet Misalignment

Magnetic misalignment with the A1333 package impacts the linearity of the observed magnetic signal and consequently the resulting accuracy. The influence of mechanical misalignment can be minimized by reducing the overall air gap and by choosing a larger magnet diameter. The influence of magnet diameter on eccentricity error is shown in Figure 59.

The dual-die variant of the A1333 uses a stacked-die approach, resulting in a common eccentricity value for both die. This eliminates the native misalignment present in side-by-side packaging options.

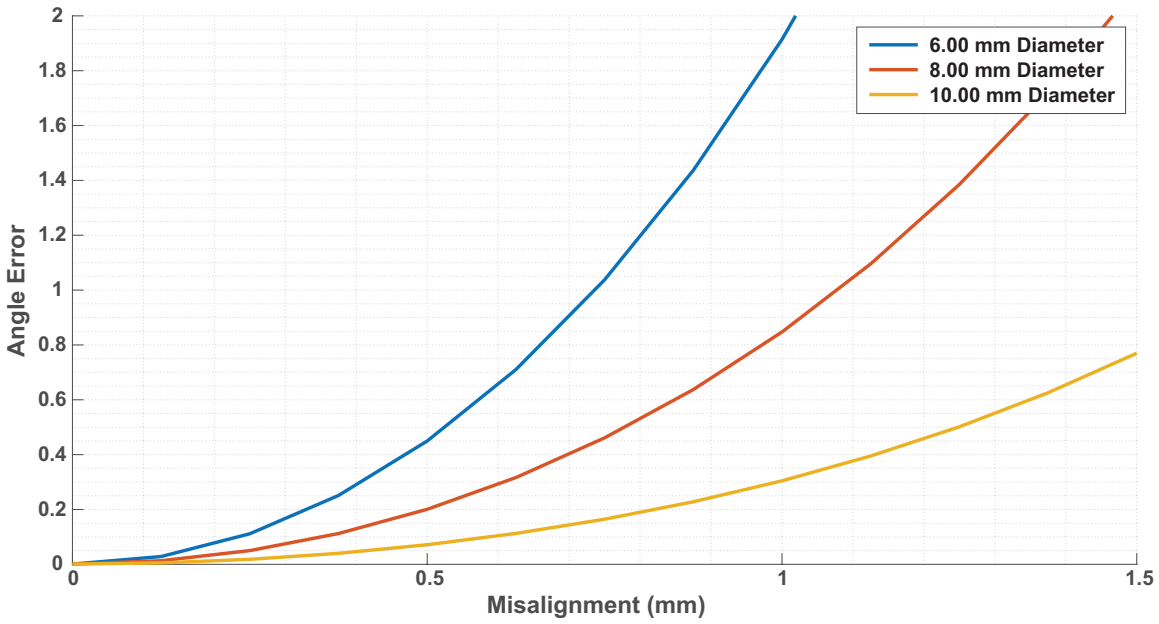

Figure 59: Simulated Error versus Eccentricity for Different Sizes of Magnet Diameter, at 2.0 mm Air Gap

Typical Systemic error versus magnet-to-sensor eccentricity (d_{axial}). Note: Systemic error refers to application errors in alignment and system timing. It does not refer to sensor IC device errors. The data in this graph is simulated with ideal magnetization.

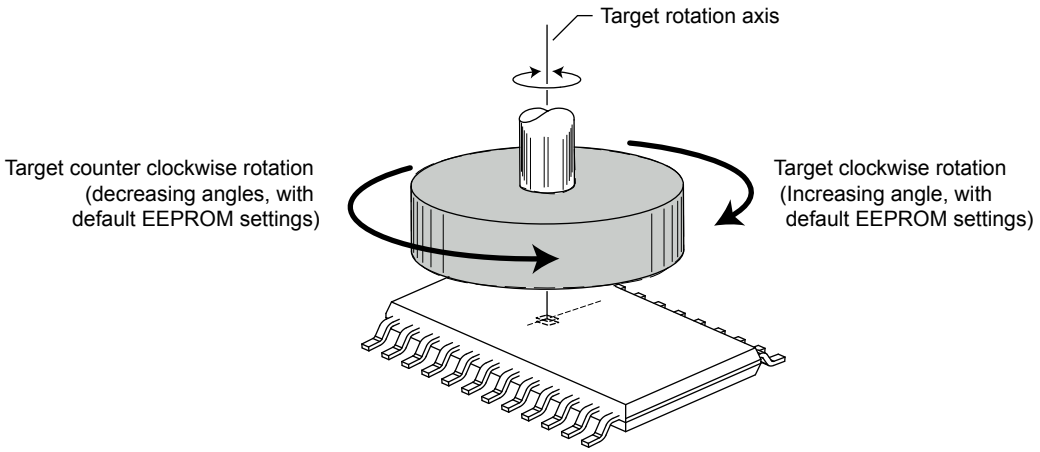

Figure 60: Rotation Direction Definition

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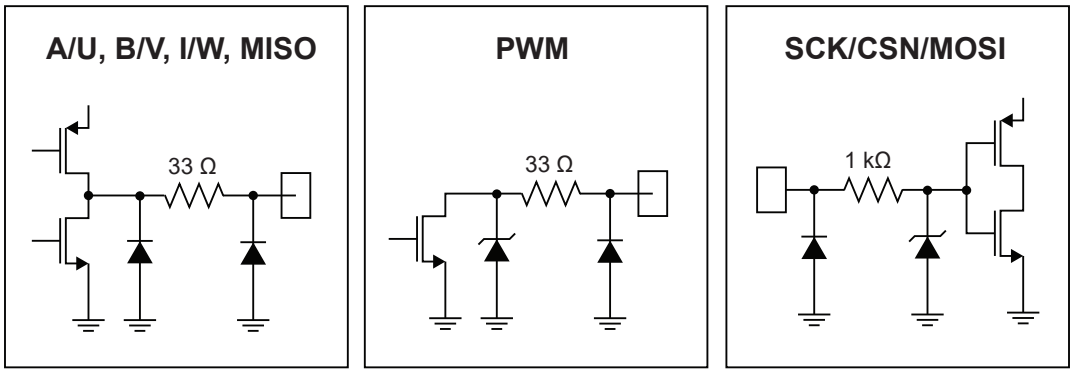
I/O STRUCTURES



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PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use
(Reference Allegro DWG-0000379, Rev. 3 and JEDEC MO-153ADT)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

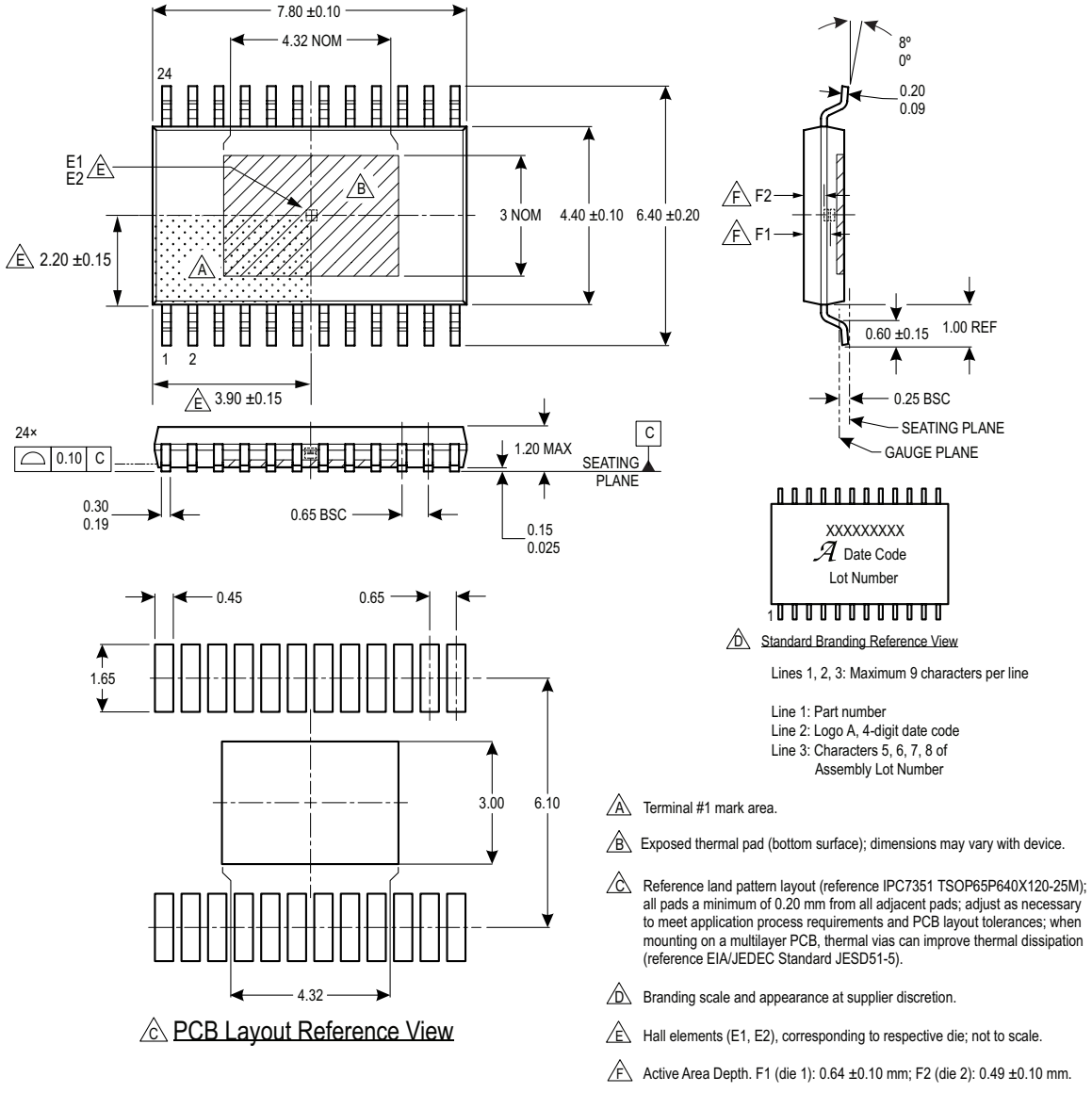

Figure 61: Package LP, 24-Pin TSSOP with Exposed Thermal Pad

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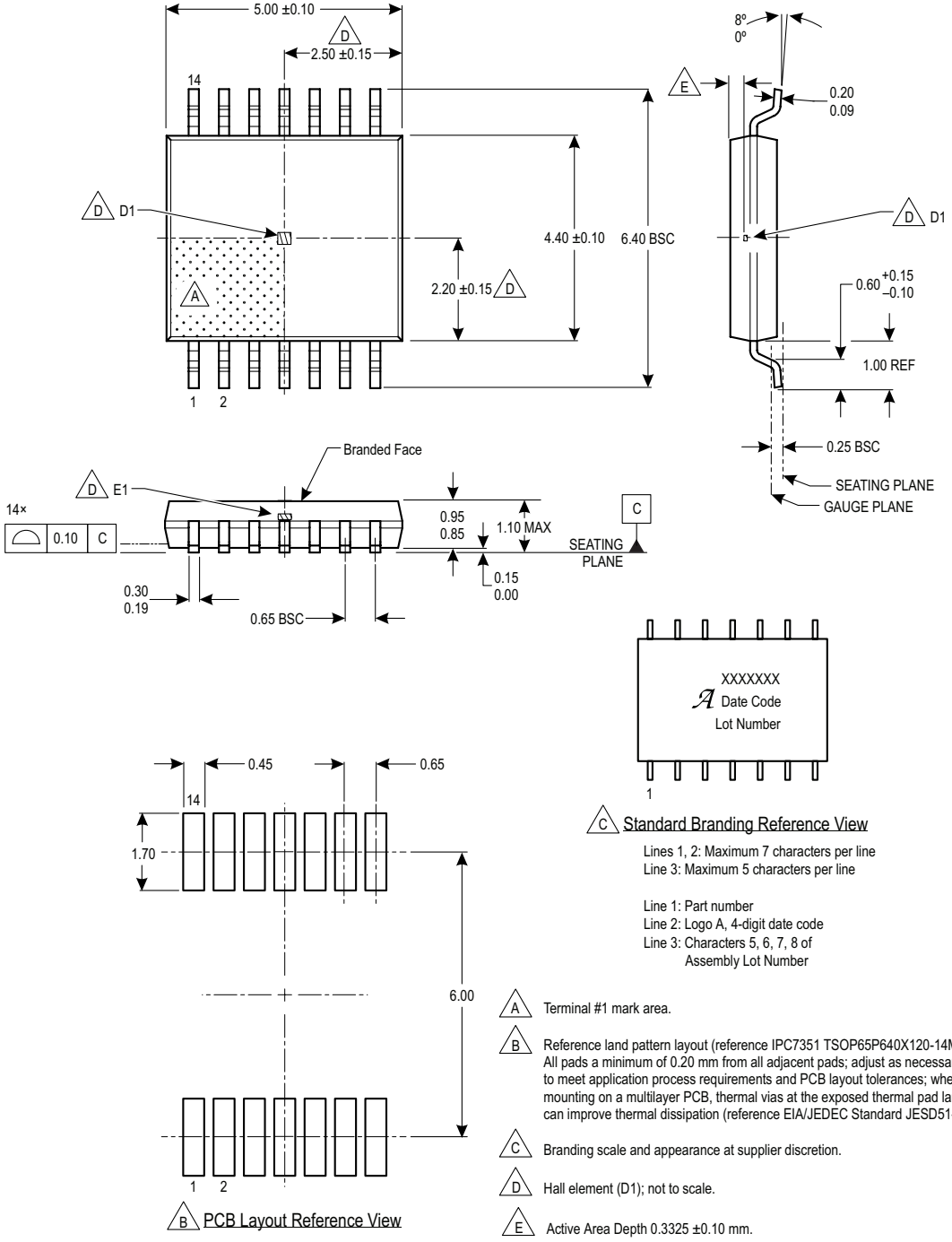
For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000381, Rev. 1)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



C Standard Branding Reference View

Lines 1, 2: Maximum 7 characters per line
Line 3: Maximum 5 characters per line

Line 1: Part number
Line 2: Logo A, 4-digit date code
Line 3: Characters 5, 6, 7, 8 of
Assembly Lot Number

B PCB Layout Reference View

A Terminal #1 mark area.

B Reference land pattern layout (reference IPC7351 TSOP65P640X120-14M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5).

C Branding scale and appearance at supplier discretion.

D Hall element (D1); not to scale.

E Active Area Depth 0.3325 ±0.10 mm.

Figure 62: Package LE, 14-Pin TSSOP

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APPENDIX A: ANGLE ERROR AND DRIFT DEFINITION

Angle error is the difference between the actual position of the magnet and the position of the magnet as measured by the angle sensor IC (without noise). This measurement is performed by reading the angle sensor IC output and comparing it with a high-resolution encoder (refer to Figure 63).

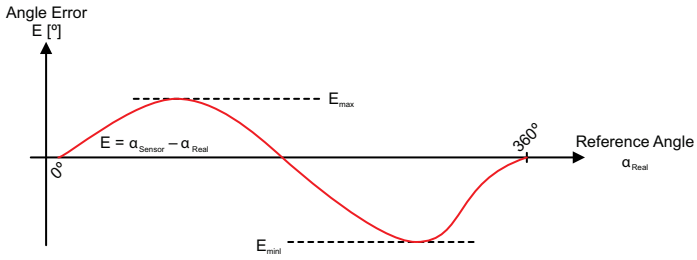

Figure 63: Angle Error Definition

Angle Error Definition

Throughout this document, the term angle error is used extensively. Thus, it is necessary to introduce a single angle error definition for a full magnetic rotation. Angle error is calculated according to:

$$AngleError = max(|E_{max}| , |E_{min}|)$$

In other words, it is the maximum deviation from a perfect straight line between 0 and 360 degrees. For the purposes of a generic definition, the offset of the IC angle profile is removed prior to the error calculation (this can be observed in Figure 63). The offset itself depends on the starting IC angle position relative to the encoder 0° and, thus, can differ anywhere from 0° to 360°.

Angle Drift

Angle drift is the change in the observed angular position over temperature, relative to 25°C.

During Allegro factory trim, drift is measured at 150°C. The value is calculated using:

$$Angle_{Drift} = Angle_{25°C} - Angle_{150°C}$$

where each angle value is an array corresponding to 16 angular positions around a circle.

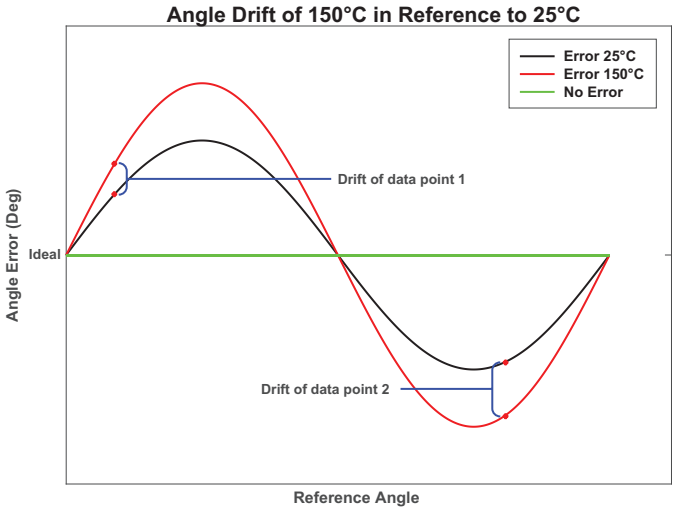

Figure 64: Angle Drift of 150°C in Reference to 25°C [1]

[1] Note that the data above is simply a representation of angle drift; it is not real data.

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APPENDIX B: SPI INTERFACE ERROR FLAG DESCRIPTION

IER Flag

The IER flag is located in bit 11 of the WARN serial register (0x26:0x27). This flag is designed to assert when the IC detects an improper communication frame, via either SPI or Manchester. For the purposes of this appendix, only the behavior in regard to the SPI bus is discussed. The IER flag asserts when the following conditions exist:

- An improper number of SPI clocks are detected
- The MSB of the MOSI packet is a logic 1

Table 22: WARN Serial Register

Address	0x26								0x27							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	1	0	1	1	IER	CRC	0	SRW	XEE	TR	ESE	SAT	TCW	BSY	MSH	TOV
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Behavior When Sharing SPI lines

The IER flag may provide an erroneous indication when sharing the SCLK line among multiple ICs. In the case where an IC is held inactive by bringing the CS line high, the inactive IC(s) continue to count falling SCLK edges. This results in an invalid number of observed SCLK edges and assertion of the IER flag on the next SPI transaction of the IC. False IER flag assertions differ based on the size of the SPI packet.

16-BIT AND 17-BIT SPI PACKETS

The IER flag always asserts if, during the CS high period, the SCLK line is brought low as follows:

- At least one time if using a 16-bit SPI packet and the S17 bit is set to 0 (EEPROM 0x1B, bit 1).
  - □ Default setting for S17 is 0.
- At least twice if using a 16-bit packet and the S17 bit is a 1.
  - □ Based on signal timing, there is a possibility that the IER flag will assert if SCLK is brought low only once with S17 set.
- At least once if using a 17-bit packet and the S17 bit is a 1.

Impact of IER Flagging with 16-/17-Bit Packets

When an incorrect number of SCLK edges is observed by the IC, the following occurs:

1. The IER flag triggers.
2. If the packet preceding the CS high time is a read:
   A. If SCLK drops low within 70 ns of the CS rising edge, there is a possibility the read will be discarded. If this occurs, the output corresponds to the last valid read request for that device.
   B. If the SCLK edge occurs after 70 ns of the CS rising edge, the read is not discarded, potentially corrupting the next immediate response from the device.
3. If the packet preceding the CS high time is a write:
   A. If SCLK drops low within 70 ns of the CS rising edge, there is a possibility the write will be discarded.
   B. If the SCLK edge occurs after 70 ns of the CS rising edge, the write occurs, but the IER flag still asserts.

20-BIT SPI PACKETS

When using 20-bit SPI packets, the IER flag may occur when the SCLK line is brought low while CS is high. The probability of a false IER flag asserting is timing dependent and differs from device to device, but should not occur on more than 3.2% of all SPI transactions. Lab characterization has shown significantly lower assertion rates, with false flags on 0.00% to 0.80% of all SPI transactions.

Impact of IER flagging with a 20-Bit Packet

When using a 20-bit SPI packet, the following occurs if an incorrect number of SCLK edges is observed:

1. The IER flag triggers.
2. If the packet preceding the CS high time is a read:
   A. If SCLK drops low within 70 ns of the CS rising edge, there is a possibility the read will be discarded. If this occurs, the output corresponds to the last valid read request for that device.
   B. If the SCLK edge occurs after 70 ns of the CS rising edge, the read occurs as expected.
3. If the packet preceding the CS high time is a write:
   A. If SCLK drops low within 70 ns of the CS rising edge, there is a possibility the write will be discarded.
   B. If the SCLK edge occurs after 70 ns of the CS rising edge, the write occurs, but the IER flag still asserts.

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Avoiding IER Flag Assertion

The following methods may be used to avoid false IER flag assertions:

1. Use dedicated SCLK lines for each IC and hold the SCLK line high when CS is high.
   A. This prevents the IC from observing SCLK edge transitions when CS is high.

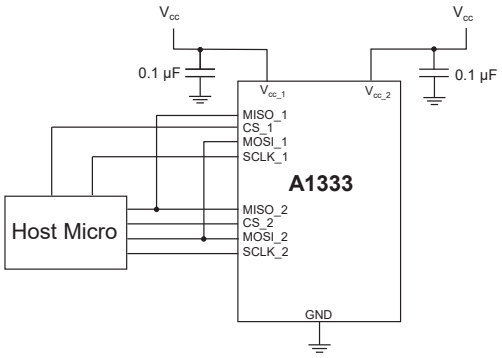

Figure 65: Separate SCLK Lines

2. Use a 21-bit SPI packet.
   A. When using a 21-bit SPI packet, the IC does not count SCLK edges when the CS pin is held high. This prevents the IER flag from improperly asserting, with the exception of power-on.

USING A 21-BIT SPI PACKET

Special EEPROM programming is not required for the A1333 to support a SPI packet size of 21 bits; the controller must simply send 21 SCLK pulses during the CS low period. The format of the SPI message is shown in Figure 66.

The controller-output peripheral-input (MOSI) signal consists of: a 1 synchronization bit defined as a logic 0, 1 $\overline{R}$/W bit, 6 address bits, 8 data bits, 4 CRC bits, and an additional logic 0. The extra logic 0 sent on the 21st clock tick effectively shifts the standard 20-bit packet left by one place value.

The controller-input peripheral-output (MISO) signal consists of: 16 data bits, the contents of which are determined by the address of the register being read, 4 CRC bits, and a repeat of the MSB of the CRC value shown in bold in Figure 66. The repeated CRC bit shifted out on the 21st clock edge should be ignored by the controller when processing the CRC to validate the message contents.

POWER-ON BEHAVIOR WITH A 21-BIT SPI PACKET

If the SCLK line is shared on two or more ICs, the IER flag asserts on all idle A1333 die (CS held high) after the first SPI transaction (on the bus), following power-up. This occurs independent of the 21-bit SPI packet. This spurious IER flag asserts, on the idle die, only during the first SPI transaction. All subsequent SPI transactions process correctly. This spurious assertion does not affect any future reads or writes to the device while power is maintained. If the IC is programmed to validate the CRC on MOSI, a CRC error flag (bit 10 of the WARN serial register) also asserts, related to the spurious detection of a bad SPI packet

Due to the initial assertion of the IER flag, it is recommended to clear all error and warning flags on all A1333 ICs following power-on (this is a good practice, independent of the false IER flag assertion). By doing this, the false IER flag is cleared, preventing it from masking a real SPI communication issue.

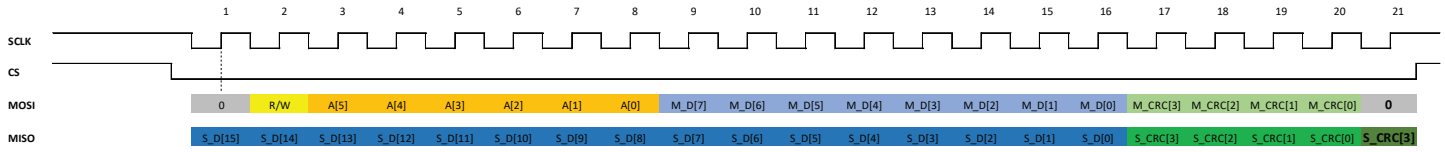

Figure 66: 21-Bit SPI Packet Format

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Additional SPI Examples

The examples in this section show differing SPI implementations. All figures assume a shared SPI bus (MISO, MOSI, SCLK) between two sensors, with individual CS lines.

An example of pipelining SPI reads between two sensors is shown in Figure 67; this can result in discarded packets or corrupted data when used with 16- or 17-bit SPI packets. In this example, SPI reads are bounced between Sensor 1 and Sensor 2, one frame at a time. During the interval in which the CS lines are high, the inoperative sensor detects an incorrect number of edges, asserting the IER flag and potentially corrupting the following read response.

Figure 68 is a modified version of the pipelining shown in Figure 67. The first read response from each sensor is known to be corrupt, and is ignored. Because of this, the second read request (which results in the first read response in the next sequence) can be a NOP command, resulting in all zeros from the device (a NOP command is a read of serial register 0x0, which is hard-coded with all 0s). Inserting a NOP command between each valid read response ensures the data placed in the SPI buffers prior to the second response is valid.

It should be noted that the IER flag asserts upon every change-over to a new die (CS line) when using this implementation due to the incorrect number of SCLK edges detected during the CS high period.

A 20-bit SPI packet is shown in Figure 69. This removes the potential for incorrectly read data (assuming the SCLK edge occurs 70 ns or later following the CS rising edge), allowing the two sensors to be addressed in a sequential manner, one frame per each sensor. This implementation has the added advantage of including a 4-bit CRC within each response. The IER flag may still assert when using a 20-bit packet.

Implementation of a 21-bit SPI packet is shown in Figure 70. This removes the false IER flag assertion and any potential for incorrect data interpretation. Allegro recommends using a 21-bit SPI packet when sharing SPI lines.

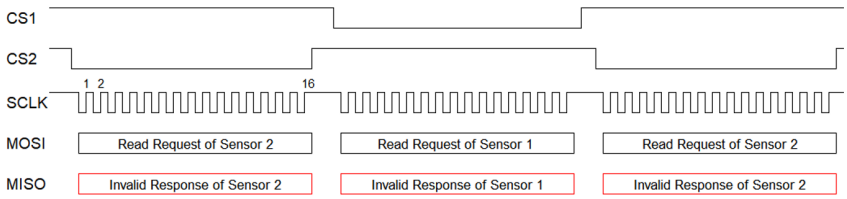

Figure 67: Implementation of SPI Using 16- or 17-Bit Packets Resulting in IER Flag Assertion and Potentially Corrupted Data

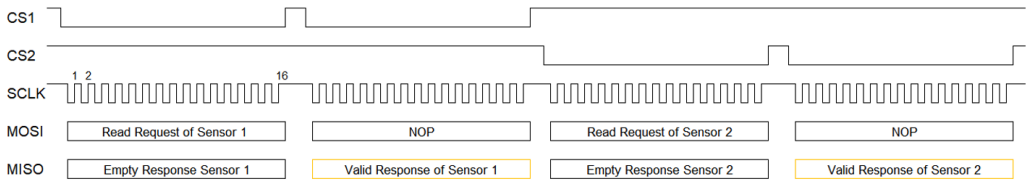

Figure 68: Implementation of SPI Using 16- or 17-Bit Packets; Valid Data, IER Flag Still Asserts

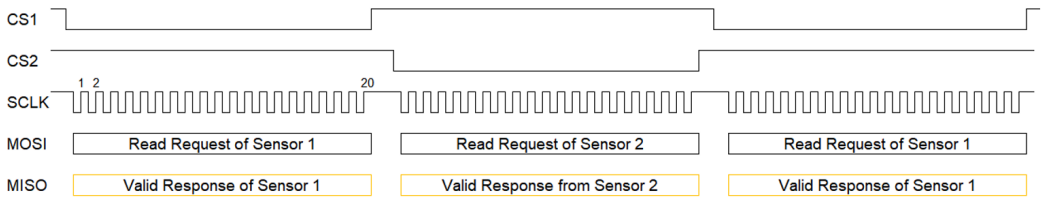

Figure 69: SPI Implementation Using 20-Bit Packets; Data Contents are Valid, However IER Flag May Still Assert

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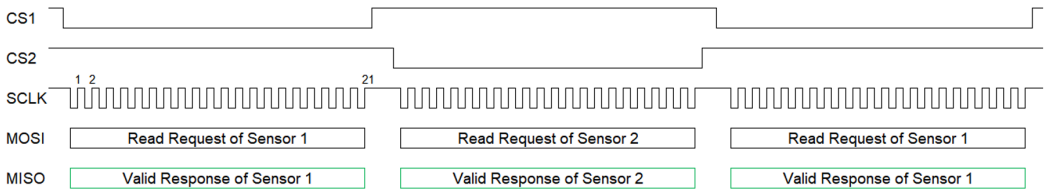

Figure 70: SPI Implementation Using 21-Bit Packets; Data Contents are Valid; No False IER Flag Generation

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Revision History

Number	Date	Description
–	September 25, 2017	Initial release
1	February 23, 2018	Updated Response Time value (p. 8), Typical Performance Characteristics section (p. 9-10), Figure 12 (p. 13), Figure 13 (p. 14), Device Programming Interfaces section (p. 26-42), Table 12 heading (p. 43), TCW[3] (page 52), Mag_Thresh_Hi and Mag_Thresh_Lo descriptions (p. 64), Table 15 (p. 66), Setting the Zero-Degree Position section (p. 70), Magnetic Target Requirements section (p. 70-71), I/O Structures (p. 73), and Package Outline Drawings active area depths (p. 74-75). Added 5 V interface voltage part variant, Manchester Interface Specifications (p. 7), Impact of High Speed Sensing section (p. 11-12). Removed CRC Documentation appendix.
2	August 1, 2018	Added A1333LLPTR-5-DD-T to Selection Guide (page 2).
3	October 15, 2018	Updated ASIL Status
4	November 1, 2019	Minor editorial updates
5	January 10, 2020	Updated Figure 1 (p. 1), Table of Contents (p. 3); Added SPI Frame Rate test condition (p. 6); Added Maximum Sourcing Current and Maximum Sinking Current characteristics (p. 7); Updated Response Time (p. 8), Figure 3 and 4 (p. 9); Added Figures 11 to 14 (p. 11-12); Updated Impact of High Speed Sensing section (p. 15); Added Measured Performance over RPM section (p. 15); Updated Figure 20 (p. 16), Figure 21 (p. 17); Added ABI Behavior at Power-Up section (p. 22); Updated Figure 29 (p. 23), Slew Rate Limiting for ABI section (p. 24); Added Effective Speed of Slew Time section (p. 24); Updated Brushless DC Motor Output section (p. 25-26); Added Spurious Interface Error (IER) When Sharing SPI Lines section (p. 30); Added 21-Bit SPI Packet section (p. 32); Updated Figure 53 (p. 40), Enabling EEPROM Access section (p. 41); Added EEPROM Margin Check section (p. 43-44); Updated INITIATE_SPECIAL description (p. 51), GAUSS description (p. 58), ABI_SLEW_TIME bit range (p. 64), ORATE (p. 68); Figure 56 and Table 20 (p. 75), Figure 63 (p. 80), Figure 64 (p. 81), Figure 65 (p. A-1), Angle Error equation (p. A-1); Added Appendix B (p. B-1 to B-4).
6	July 1, 2020	Updated LE-14 and LP-24 package drawing Hall element tolerances (p. 79-80)
7	October 8, 2020	Updated SPI Interface section (p. 30)
8	February 1, 2021	Updated LE-14 package drawing (p. 80).
9	April 20, 2021	Updated Power-On Time maximum values and footnote (p. 6), Angle Measurement section (page 14), and Table 8 (page 37)
10	April 22, 2022	Updated LP-24 package drawing (page 79)
11	April 19, 2023	Updated “ISO 26262:2011” to “ISO 26262” (page 1)
12	May 14, 2024	Corrected reverse voltage specifications (page 2), updated EEPROM margin test (page 44), updated SPECIAL [15:12] definition in the device control register (page 51), and made minor editorial corrections throughout (all pages) including: removal of archaic language (master changed to controller, slave changed to peripheral, and normal changed to typical), removal of future tense (“will”) wherever possible, minimization of use of title case (except for headings and captions) and quotation marks, removal of trailing zeros to the right of decimal points, replacement of N/A with an en-dash (–), and addition of hyperlinks for cross-referenced sections.

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