

Memory FeRAM

64K (8K × 8) Bit SPI

MB85RS64VY (AEC-Q100 Compliant)

■ DESCRIPTION

MB85RS64VY is a FeRAM (Ferroelectric Random Access Memory) chip in a configuration of 8,192 words × 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells. This product is specifically targeted for high-temperature environment such as automotive applications.

MB85RS64VY adopts the Serial Peripheral Interface (SPI).

The MB85RS64VY is able to retain data without using a back-up battery, as is needed for SRAM.

The memory cells used in the MB85RS64VY can be used for 10^{13} read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E²PROM.

As MB85RS64VY does not need any waiting time in writing process, the write cycle time of MB85RS64VY is much shorter than that of Flash memories or E²PROM.

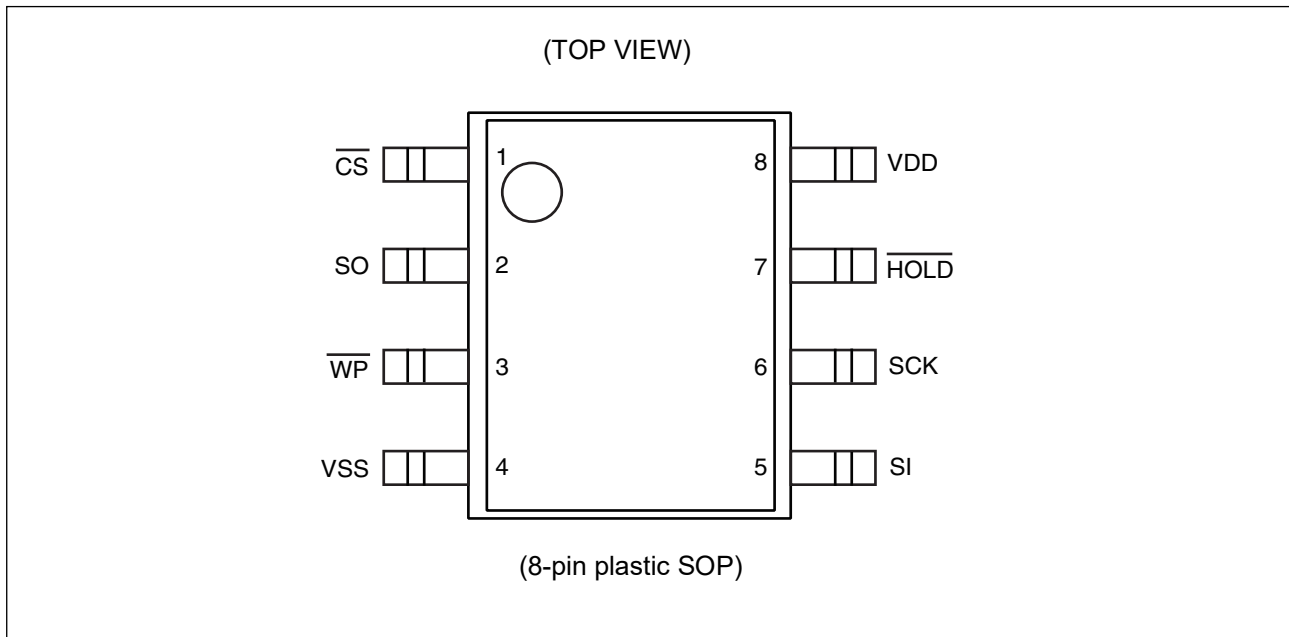
■ FEATURES

- Bit configuration : 8,192 words × 8 bits
- Serial Peripheral Interface : SPI (Serial Peripheral Interface)
Correspondent to SPI mode 0 (0, 0) and mode 3 (1, 1)
- Operating frequency : 25 MHz (Max,@2.7V to 4.5V), 33MHz(Max,@4.5V to 5.5V)
- High endurance : 10^{13} times / byte
- Data retention : 70.4 years (+85 °C),
19.1 years (+105 °C)
5.9 years (+125 °C) or more
Under evaluation for more than 5.9 years(+125 °C)
- Operating power supply voltage : 2.7V to 5.5V
- Low power consumption : Operating power supply current
1.8 mA (Max@25 MHz), 2.3 mA (Max@33MHz)
Standby current 30 μA (Max)
Sleep current 12 μA (Max)
- Operation ambient temperature range : - 40 °C to +125 °C
- Package : 8-pin plastic SOP
AEC-Q100 Grade 1 compliant
RoHS compliant

Fujitsu Semiconductor Memory Solutions Limited has changed its name to RAMXEED Limited. RAMXEED Limited will continue to offer and support existing products while maintaining Fujitsu's part number unchanged.

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■ PIN ASSIGNMENT

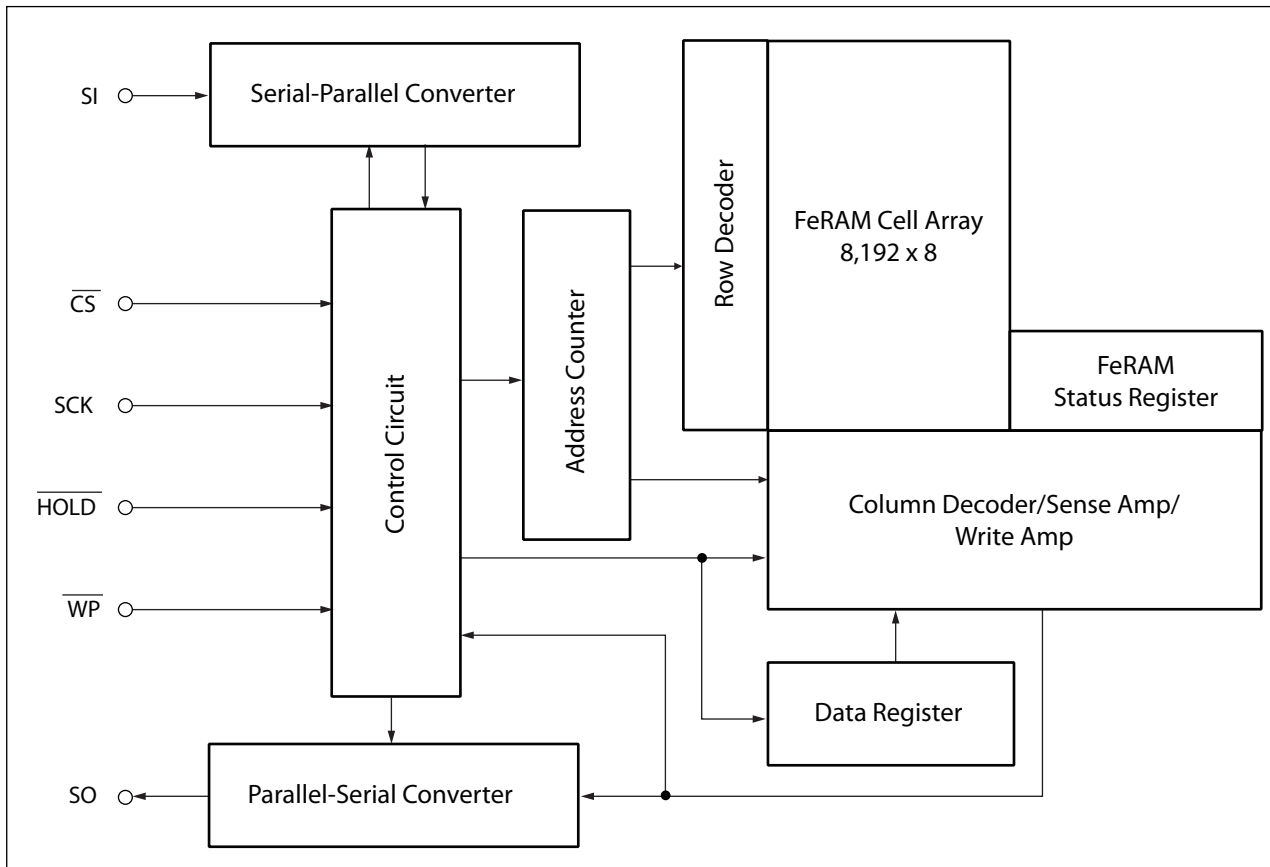


■ PIN FUNCTIONAL DESCRIPTIONS

Pin No.	Pin Name	Functional description
1	$\overline{\text{CS}}$	Chip Select pin This is an input pin to make chips select. When $\overline{\text{CS}}$ is "H" level, device is in deselect (standby) status and SO becomes High-Z. Inputs from other pins are ignored for this time. When $\overline{\text{CS}}$ is "L" level, device is in select (active) status. $\overline{\text{CS}}$ has to be "L" level before inputting op-code.
3	$\overline{\text{WP}}$	Write Protect pin This is a pin to control writing to a status register. The writing of status register (see "■ STATUS REGISTER") is protected in related with $\overline{\text{WP}}$ and WPEN. See "■ WRITING PROTECT" for detail.
7	$\overline{\text{HOLD}}$	Hold pin This pin is used to interrupt serial input/output without making chips deselect. When $\overline{\text{HOLD}}$ is "L" level, hold operation is activated, SO becomes High-Z, SCK and SI become do not care. See "■ HOLD OPERATION" for detail.
6	SCK	Serial Clock pin This is a clock input pin to input/output serial data. SI is loaded synchronously to a rising edge, SO is output synchronously to a falling edge.
5	SI	Serial Data Input pin This is an input pin of serial data. This inputs op-code, address, and writing data.
2	SO	Serial Data Output pin This is an output pin of serial data. Reading data of FeRAM memory cell array and status register data are output. This is High-Z during standby.
8	VDD	Supply Voltage pin
4	VSS	Ground pin

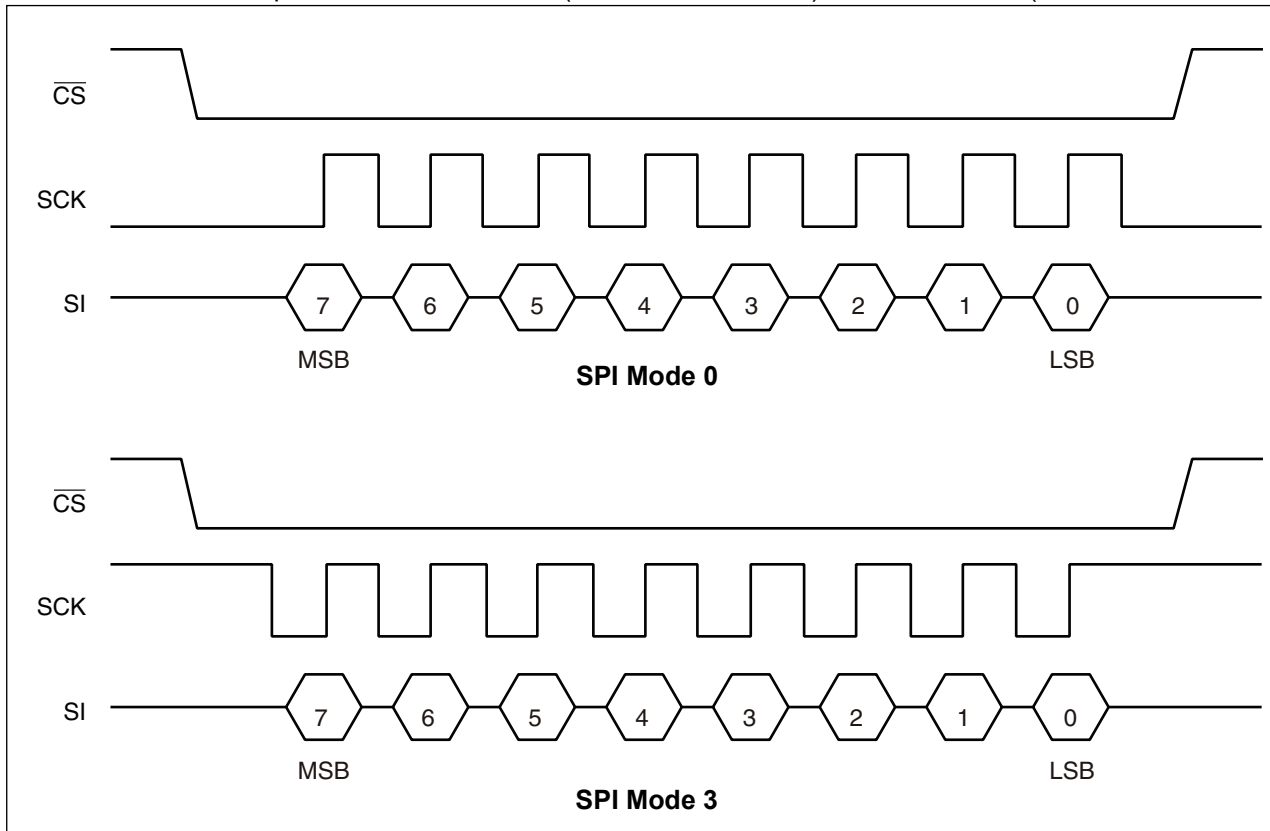
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■ BLOCK DIAGRAM



■ SPI MODE

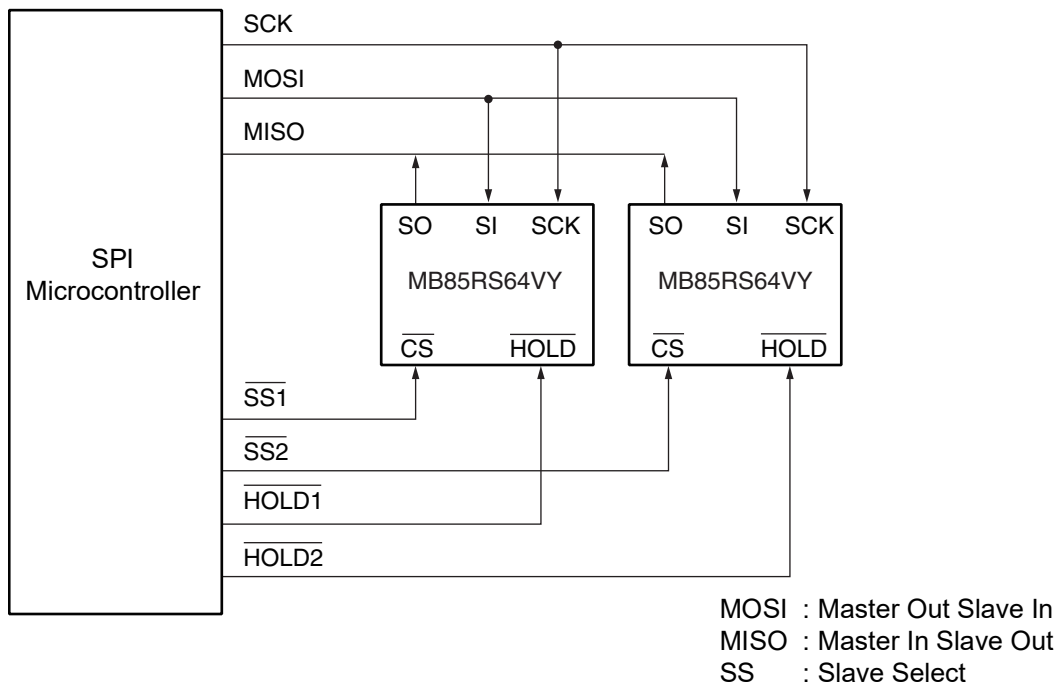
MB85RS64VY corresponds to the SPI mode 0 (CPOL = 0, CPHA = 0), and SPI mode 3 (CPOL = 1, CPHA = 1)



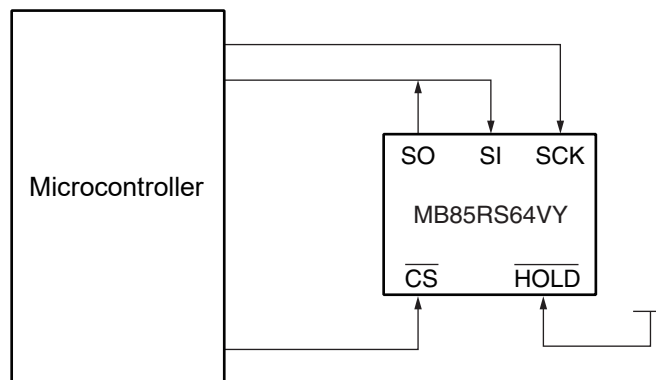
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■ SERIAL PERIPHERAL INTERFACE (SPI)

MB85RS64VY works as a slave of SPI. More than 2 devices can be connected by using microcontroller equipped with SPI port. By using a microcontroller not equipped with SPI port, SI and SO can be bus connected to use.



System Configuration with SPI Port



System Configuration without SPI Port

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■ STATUS REGISTER

Bit No.	Bit Name	Function
7	WPEN	Status Register Write Protect This is a bit composed of nonvolatile memories (FeRAM). WPEN protects writing to a status register (refer to “■ WRITING PROTECT”) relating with \overline{WP} input. Writing with the WRSR command and reading with the RDSR command are possible.
6 to 4	—	Not Used Bits These are bits composed of nonvolatile memories, writing with the WRSR command is possible. These bits are not used but they are read with the RDSR command.
3	BP1	Block Protect This is a bit composed of nonvolatile memory. This defines size of write protect block for the WRITE command (refer to “■ BLOCK PROTECT”). Writing with the WRSR command and reading with the RDSR command are possible.
2	BP0	
1	WEL	Write Enable Latch This indicates FeRAM Array and status register are writable. The WREN command is for setting, and the WRDI command is for resetting. With the RDSR command, reading is possible but writing is not possible with the WRSR command. WEL is reset after the following operations. <ul style="list-style-type: none"> After power ON. After WRDI command recognition. Return from Sleep Mode. Achieving continuous writing mode, WEL is not reset after following operations making it possible to execute writing commands continuously. <ul style="list-style-type: none"> After WRSR command recognition. After WRITE command recognition.
0	0	This is a bit fixed to “0”.

■ OP-CODE

MB85RS64VY accepts 8 kinds of command specified in op-code. Op-code is a code composed of 8 bits shown in the table below. Do not input invalid codes other than those codes. If CS is risen while inputting op-code, the command are not performed.

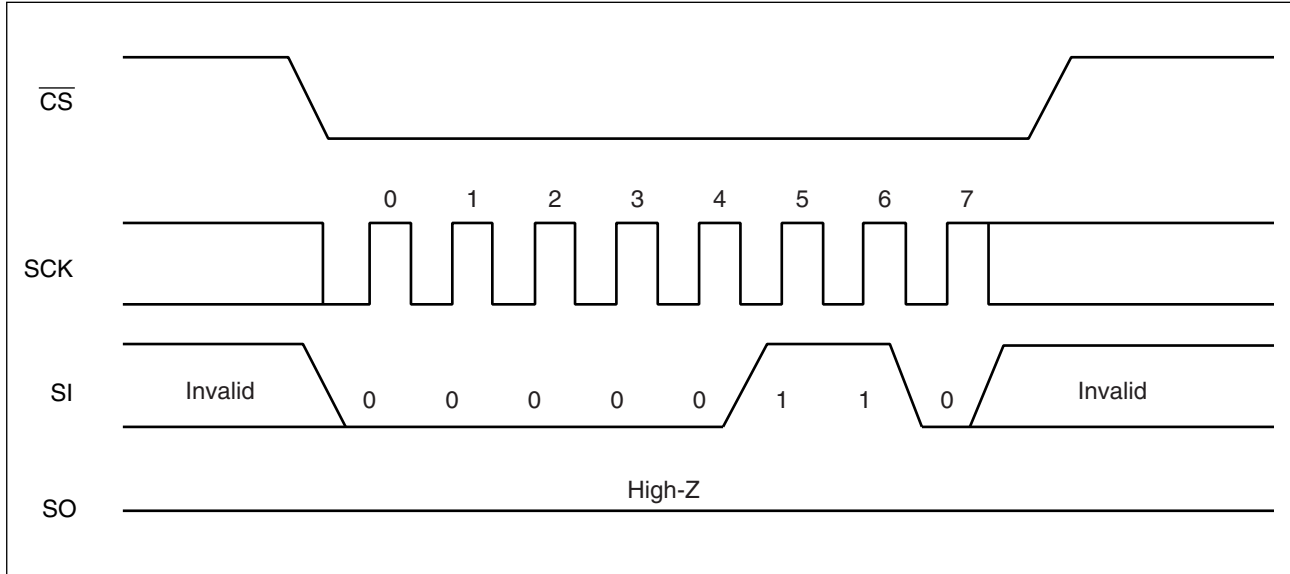
Name	Description	Op-code
WREN	Set Write Enable Latch	0000 0110 _B
WRDI	Reset Write Enable Latch	0000 0100 _B
RDSR	Read Status Register	0000 0101 _B
WRSR	Write Status Register	0000 0001 _B
READ	Read Memory Code	0000 0011 _B
WRITE	Write Memory Code	0000 0010 _B
RDID	Read Device ID	1001 1111 _B
SLEEP	Sleep Mode	1011 1001 _B
RFU	Reserved for future use	1100 0011 _B
		1100 0110 _B
		1100 1110 _B
		1100 1111 _B

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■ COMMAND

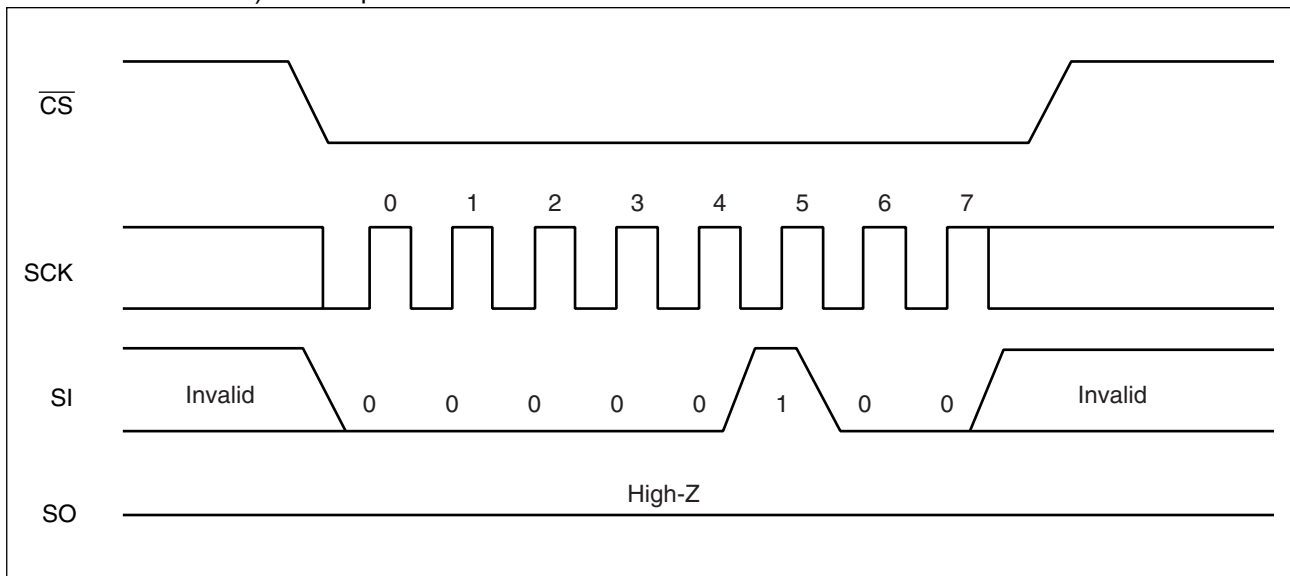
• WREN

The WREN command sets WEL (Write Enable Latch) bit to 1. WEL has to be set with the WREN command before writing operation (WRSR command and WRITE command) .



• WRDI

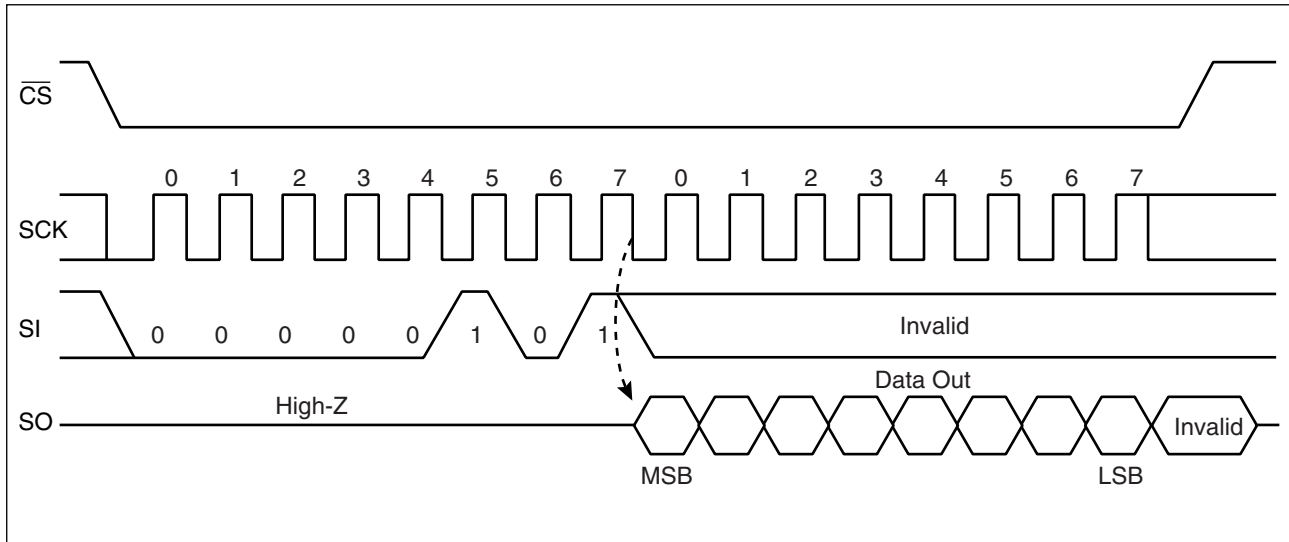
The WRDI command resets WEL (Write Enable Latch) bit to 0. Writing operation (WRSR command and WRITE command) are not performed when WEL is reset.



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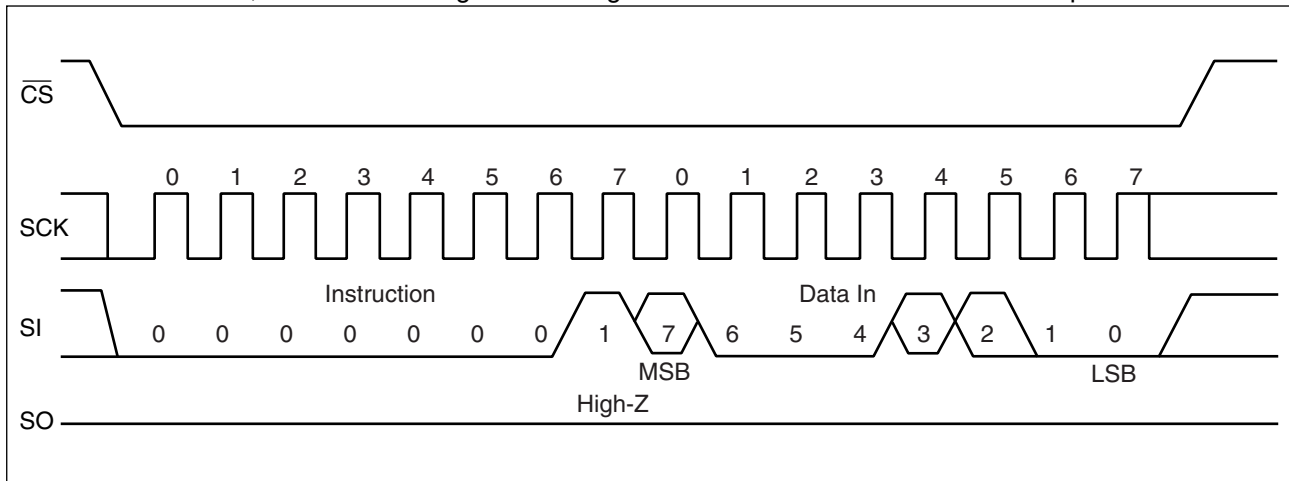
• RDSR

The RDSR command reads status register data. After op-code of RDSR is input to SI, 8-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. In the RDSR command, repeated reading of status register is enabled by sending SCK continuously before rising of \overline{CS} .



• WRSR

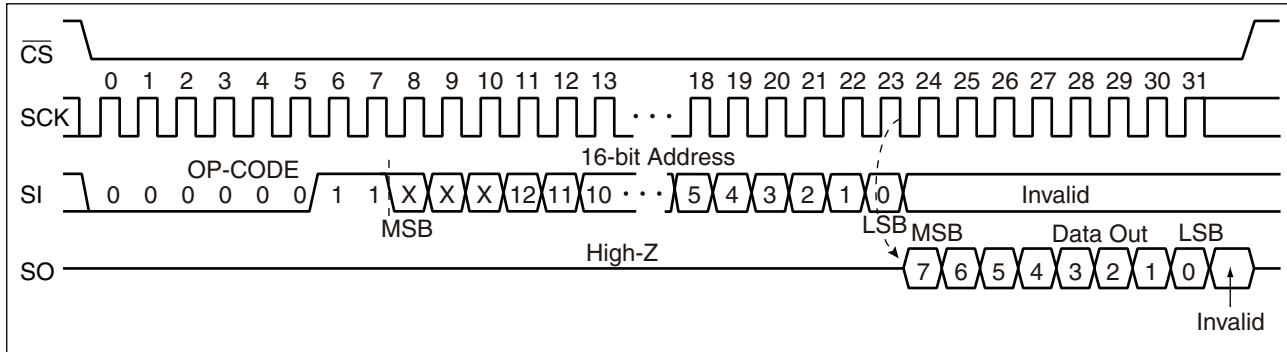
The WRSR command writes data to the nonvolatile memory bit of status register. After performing WRSR op-code to a SI pin, 8 bits writing data is input. WEL (Write Enable Latch) is not able to be written with WRSR command. A SI value correspondent to bit 1 is ignored. Bit 0 of the status register is fixed to "0" and cannot be written. The SI value corresponding to bit 0 is ignored. \overline{WP} signal level shall be fixed before performing WRSR command, and do not change the \overline{WP} signal level until the end of command sequence.



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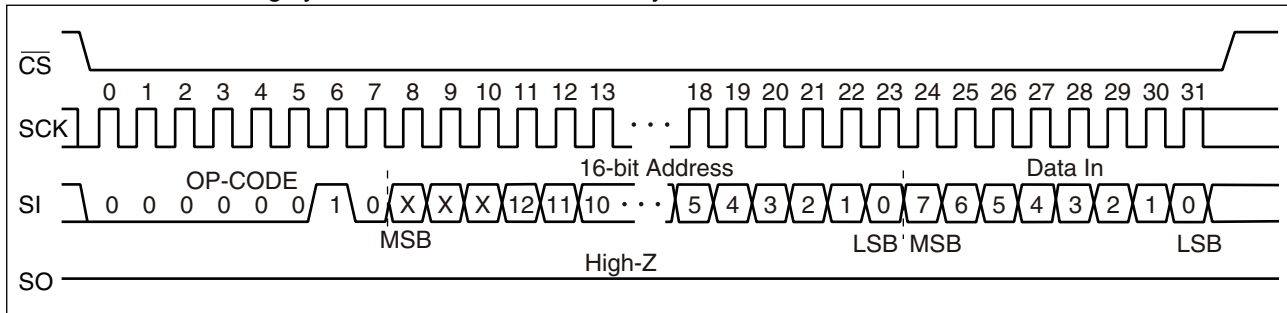
• READ

The READ command reads FeRAM memory cell array data. Arbitrary 16 bits address and op-code of READ are input to SI. The upper three address bits are invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When \overline{CS} is risen, the READ command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before \overline{CS} rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely.



• WRITE

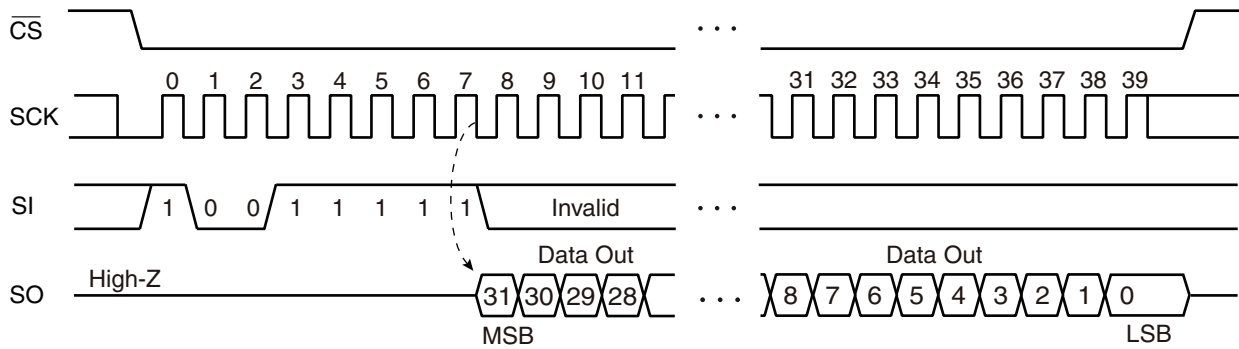
The WRITE command writes data to FeRAM memory cell array. WRITE op-code, arbitrary 16 bits of address and 8 bits of writing data are input to SI. The upper three address bits are invalid. When 8 bits of writing data is input, data is written to FeRAM memory cell array. Risen \overline{CS} will terminate the WRITE command, but if you continue sending the writing data for 8 bits each before \overline{CS} rising, it is possible to continue writing with automatic address increment. When it reaches the most significant address, it rolls over to the starting address, and writing cycle can be continued infinitely.



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• RDID

The RDID command reads fixed Device ID. After performing RDID op-code to SI, 32-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. The output is in order of Manufacturer ID (8bit)/Continuation code (8bit)/Product ID (1st Byte)/Product ID (2nd Byte). In the RDID command, 32-bit Device ID is output by continuously sending SCK clock, and SO holds the output state of the last bit until CS is risen.



	bit								Hex	
	7	6	5	4	3	2	1	0		
Manufacturer ID	0	0	0	0	0	1	0	0	04 _H	Fujitsu
Continuation code	0	1	1	1	1	1	1	1	7F _H	

	Proprietary use				Density				Hex	
	7	6	5	4	3	2	1	0		
Product ID (1st Byte)	0	0	1	0	0	0	1	1	23 _H	Density: 00011 _B = 64Kbit

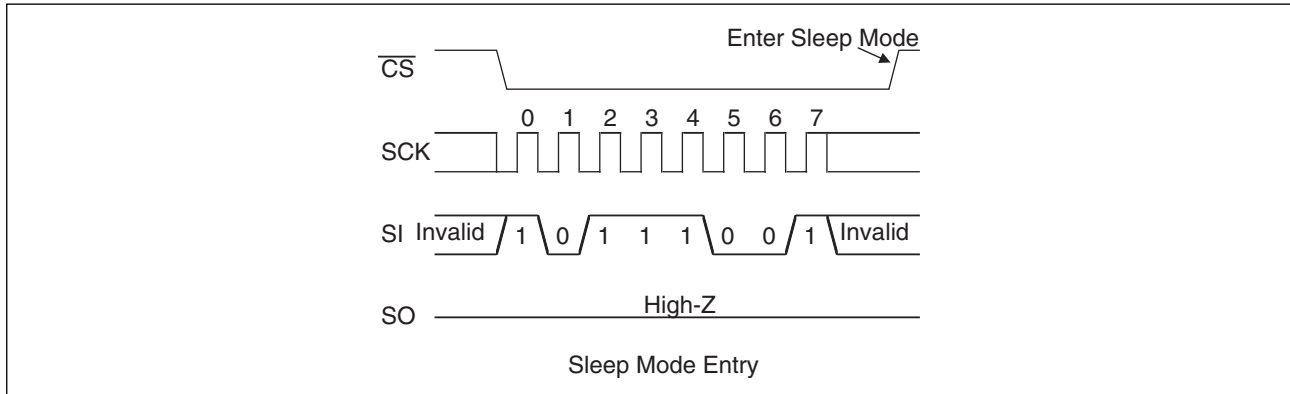
	Proprietary use								Hex
	7	6	5	4	3	2	1	0	
Product ID (2nd Byte)	0	0	0	0	0	0	1	0	02 _H

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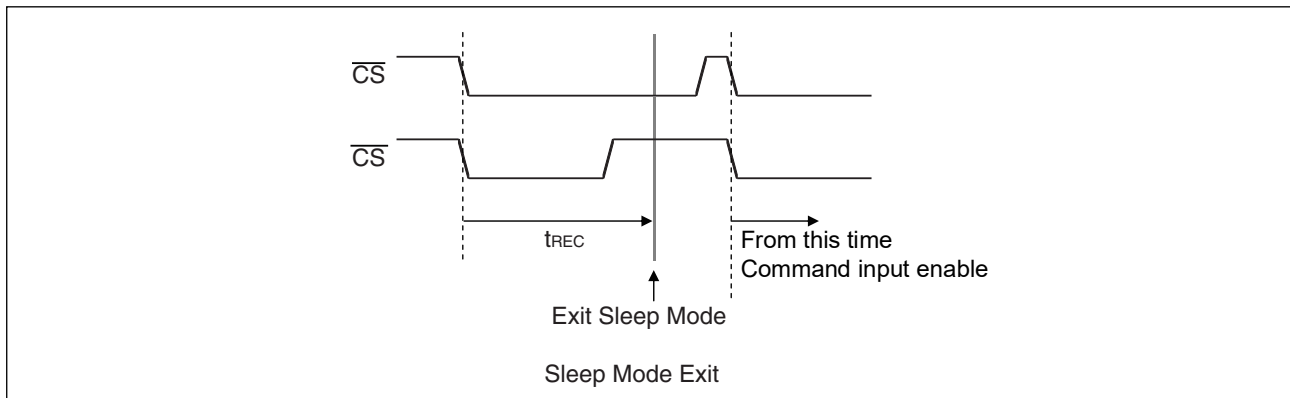
• SLEEP

The SLEEP command shifts the LSI to a low power mode called "SLEEP mode". The transition to the SLEEP mode is carried out at the rising edge of \overline{CS} after operation code in the SLEEP command. However, when at least one SCK clock is inputted before the rising edge of \overline{CS} after operation code in the SLEEP command, this SLEEP command is canceled.

After the SLEEP mode transition, SCK and SI inputs are logically ignored and SO changes to a High-Z state. When inputs other than \overline{CS} are not fixed to VCC or VDD, in some case a shoot-through current may flow.



Returning to a normal operation from the SLEEP mode is carried out after t_{REC} (Max 400 μ s) time from the falling edge of \overline{CS} (see the figure below). It is possible to return \overline{CS} to H level before t_{REC} time. However, it is prohibited to bring down \overline{CS} to L level again during t_{REC} period.



■ BLOCK PROTECT

Writing protect block for WRITE command is configured by the value of BP0 and BP1 in the status register.

BP1	BP0	Protected Block
0	0	None
0	1	1800 _H to 1FFF _H (upper 1/4)
1	0	1000 _H to 1FFF _H (upper 1/2)
1	1	0000 _H to 1FFF _H (all)

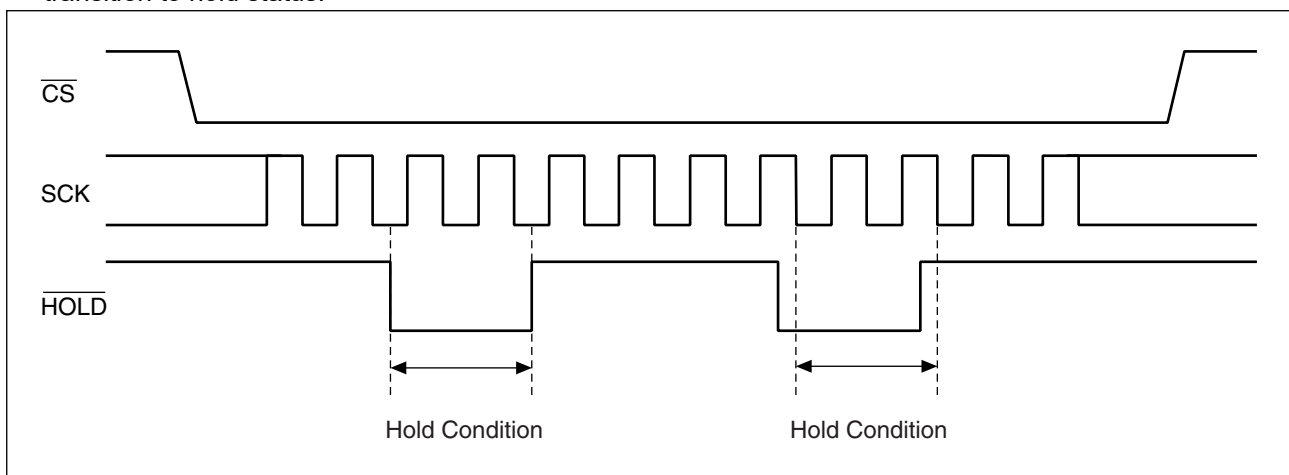
■ WRITING PROTECT

Writing operation of the WRITE command and the WRSR command are protected with the value of WEL, WPEN, WP as shown in the table.

WEL	WPEN	WP	Protected Blocks	Unprotected Blocks	Status Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Unprotected	Unprotected
1	1	0	Protected	Unprotected	Protected
1	1	1	Protected	Unprotected	Unprotected

■ HOLD OPERATION

Hold status is retained without aborting a command if $\overline{\text{HOLD}}$ is "L" level while $\overline{\text{CS}}$ is "L" level. The timing for starting and ending hold status depends on the SCK to be "H" level or "L" level when a $\overline{\text{HOLD}}$ pin input is transitioned to the hold condition as shown in the diagram below. In case the $\overline{\text{HOLD}}$ pin transitioned to "L" level when SCK is "L" level, return the $\overline{\text{HOLD}}$ pin to "H" level at SCK being "L" level. In the same manner, in case the $\overline{\text{HOLD}}$ pin transitioned to "L" level when SCK is "H" level, return the $\overline{\text{HOLD}}$ pin to "H" level at SCK being "H" level. Arbitrary command operation is interrupted in hold status, SCK and SI inputs become do not care. And, SO becomes High-Z while reading command (RDSR, READ). If $\overline{\text{CS}}$ is rising during hold status, a command is aborted. In case the command is aborted before its recognition, WEL holds the value before transition to hold status.



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■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V _{DD}	- 0.5	+ 6.0	V
Input voltage*	V _{IN}	- 0.5	V _{DD} + 0.5(≤ 6.0)	V
Output voltage*	V _{OUT}	- 0.5	V _{DD} + 0.5(≤ 6.0)	V
Operation ambient temperature	T _A	- 40	+ 125	°C
Storage temperature	T _{stg}	- 55	+ 150	°C

*: These parameters are based on the condition that V_{SS} is 0 V.

WARNING: Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.
Do not exceed any of these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage*1	V _{DD}	2.7	—	5.5	V
Operation ambient temperature*2	T _A	- 40	—	+ 125	°C

*1: These parameters are based on the condition that V_{SS} is 0 V.

*2: Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition.

Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

MB85RS64VY(AEC-Q100 Compliant)

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit	
			Min	Typ	Max		
Input leakage current*1	I _{LI}	\overline{WP} , \overline{HOLD} , SCK, \overline{CS} SI = 0 V to V _{DD}	25 °C	—	—	1	μA
			125 °C	—	—	2	
Output leakage current*2	I _{LO}	SO = 0 V to V _{DD}	25 °C	—	—	1	μA
			125 °C	—	—	2	
Operating power supply current*3	I _{DD}	SCK = 33MHz	—	1.9	2.3	mA	
		SCK = 25MHz	—	1.5	1.8		
Standby current	I _{SB}	$\overline{SCK} = \overline{SI} = \overline{CS} = \overline{WP} = \overline{HOLD} = V_{DD}$	—	13	30	μA	
Sleep current	I _{ZZ}	$\overline{CS} = V_{DD}$ All other inputs V _{SS} or V _{DD}	—	5	12	μA	
Input high voltage	V _{IH}	V _{DD} = 2.7 V to 5.5 V	V _{DD} × 0.7	—	V _{DD} + 0.3	V	
Input low voltage	V _{IL}	V _{DD} = 2.7 V to 5.5 V	- 0.3	—	V _{DD} × 0.3	V	
Output high voltage	V _{OH}	I _{OH} = - 2 mA	V _{DD} - 0.5	—	—	V	
Output low voltage	V _{OL}	I _{OL} = 2 mA	—	—	0.4	V	

*1 : Applicable pin : \overline{CS} , \overline{WP} , \overline{HOLD} , SCK, SI

*2 : Applicable pin : SO

*3 : Input voltage magnitude : V_{DD} - 0.2 V or V_{SS}

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2. AC Characteristics

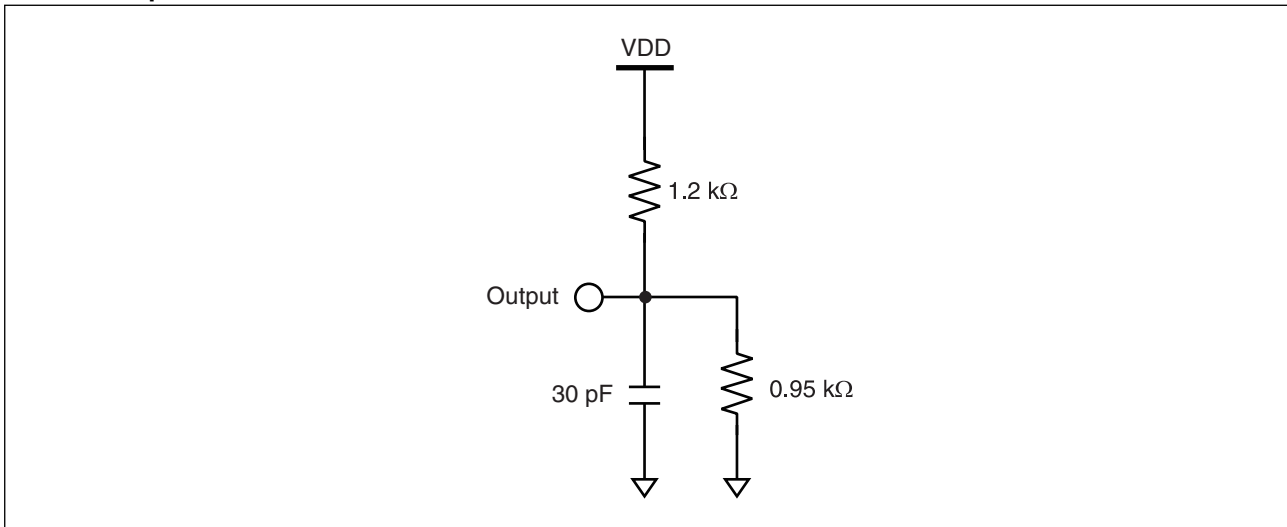
Parameter	Symbol	Value (V _{DD} = 2.7 V to 4.5 V)		Value (V _{DD} = 4.5 V to 5.5 V)		Unit
		Min	Max	Min	Max	
SCK clock frequency	f _{CK}	0	25	0	33	MHz
Clock high time	t _{CH}	15	—	13	—	ns
Clock low time	t _{CL}	15	—	13	—	ns
Chip select set up time	t _{CSU}	10	—	10	—	ns
Chip select hold time	t _{CSH}	10	—	10	—	ns
Output disable time	t _{OD}	—	16	—	16	ns
Output data valid time	t _{ODV}	—	18	—	13	ns
Output hold time	t _{OH}	0	—	0	—	ns
Deselect time	t _D	40	—	40	—	ns
Data in rising time	t _R	—	50	—	50	ns
Data falling time	t _F	—	50	—	50	ns
Data set up time	t _{SU}	5	—	5	—	ns
Data hold time	t _H	5	—	5	—	ns
HOLD set uptime	t _{HS}	10	—	10	—	ns
HOLD hold time	t _{HH}	10	—	10	—	ns
HOLD output floating time	t _{HZ}	—	20	—	20	ns
HOLD output active time	t _{LZ}	—	20	—	20	ns
SLEEP recovery time	t _{REC}	—	400	—	400	μs

AC Test Condition

Power supply voltage	: 2.7 V to 5.5 V Operation
Operation ambient temperature	: -40 °C to +125 °C
Input voltage magnitude	: $V_{DD} \times 0.7 \leq V_{IH} \leq V_{DD}$ $0 \leq V_{IL} \leq V_{DD} \times 0.3$
Input rising time	: 5 ns
Input falling time	: 5 ns
Input judge level	: V _{DD} /2
Output judge level	: V _{DD} /2

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AC Load Equivalent Circuit



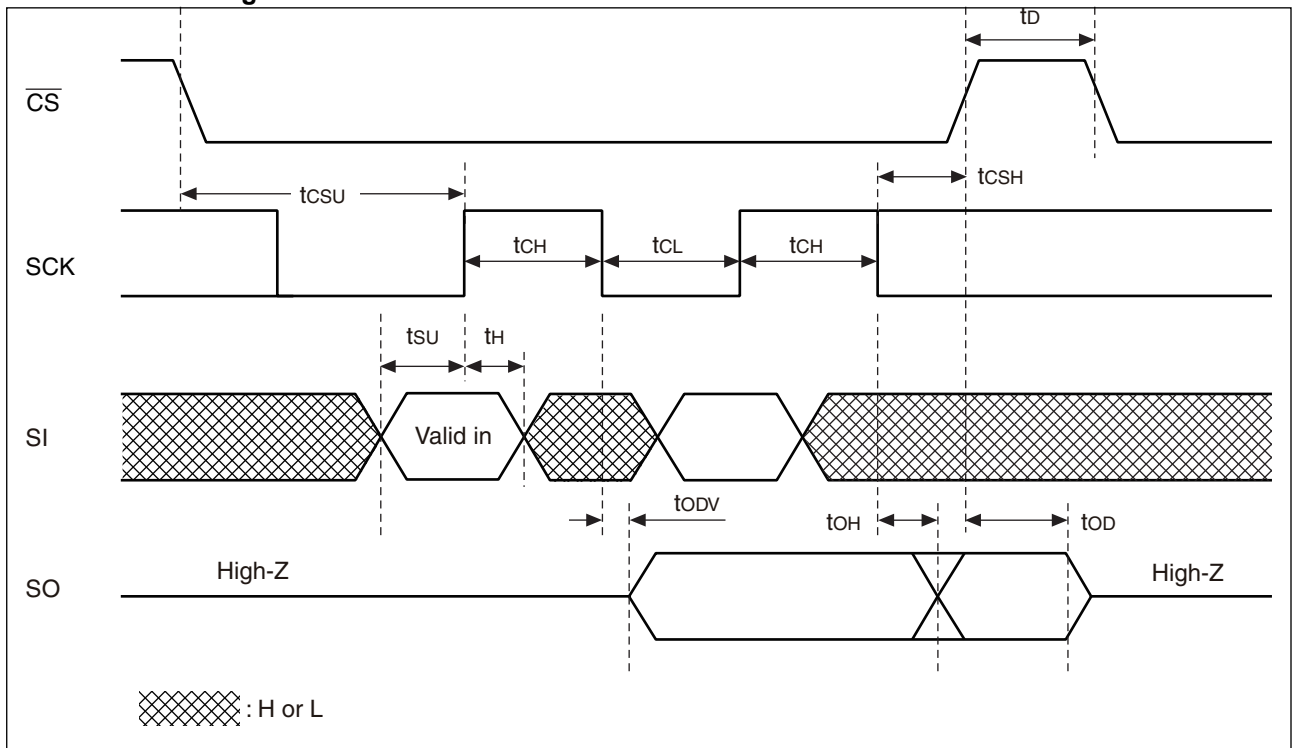
3. Pin Capacitance

Parameter	Symbol	Condition	Value		Unit
			Min	Max	
Output capacitance	C_O	$V_{DD} = 5.0 \text{ V}$, $V_{IN} = V_{OUT} = 0 \text{ V to } V_{DD}$, $f = 1 \text{ MHz}$, $T_A = +25 \text{ }^\circ\text{C}$	—	8	pF
Input capacitance	C_I		—	6	pF

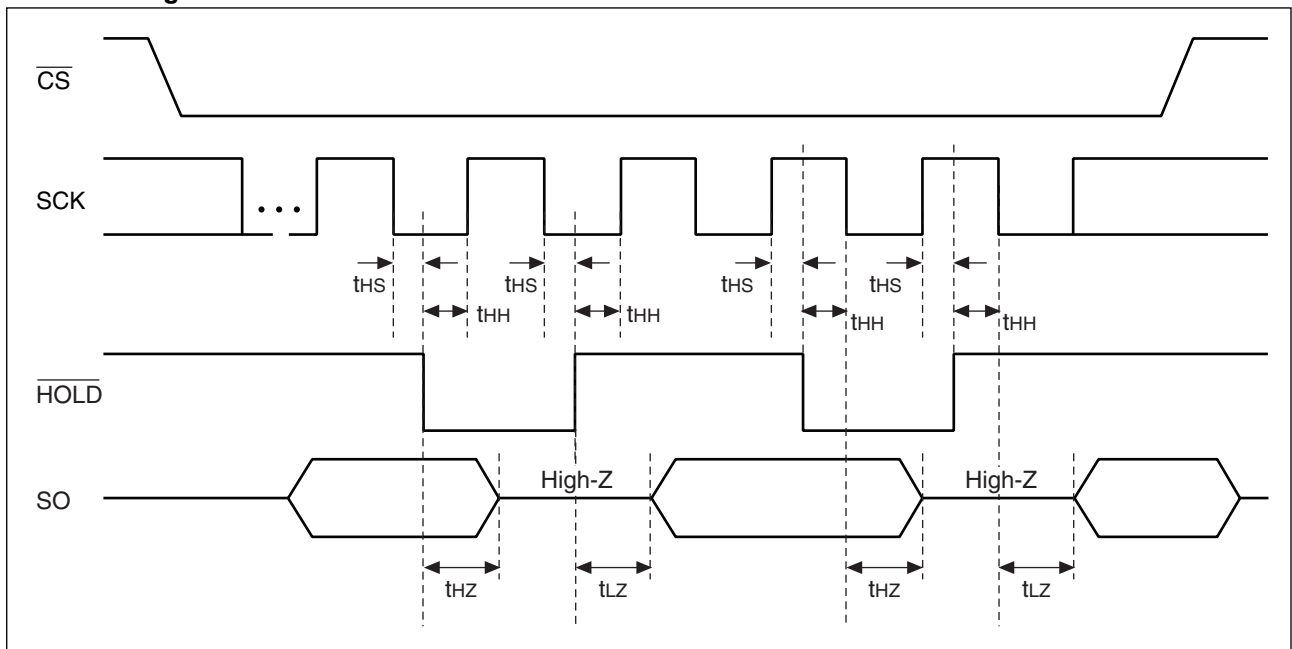
MB85RS64VY(AEC-Q100 Compliant)

■ TIMING DIAGRAM

• Serial Data Timing

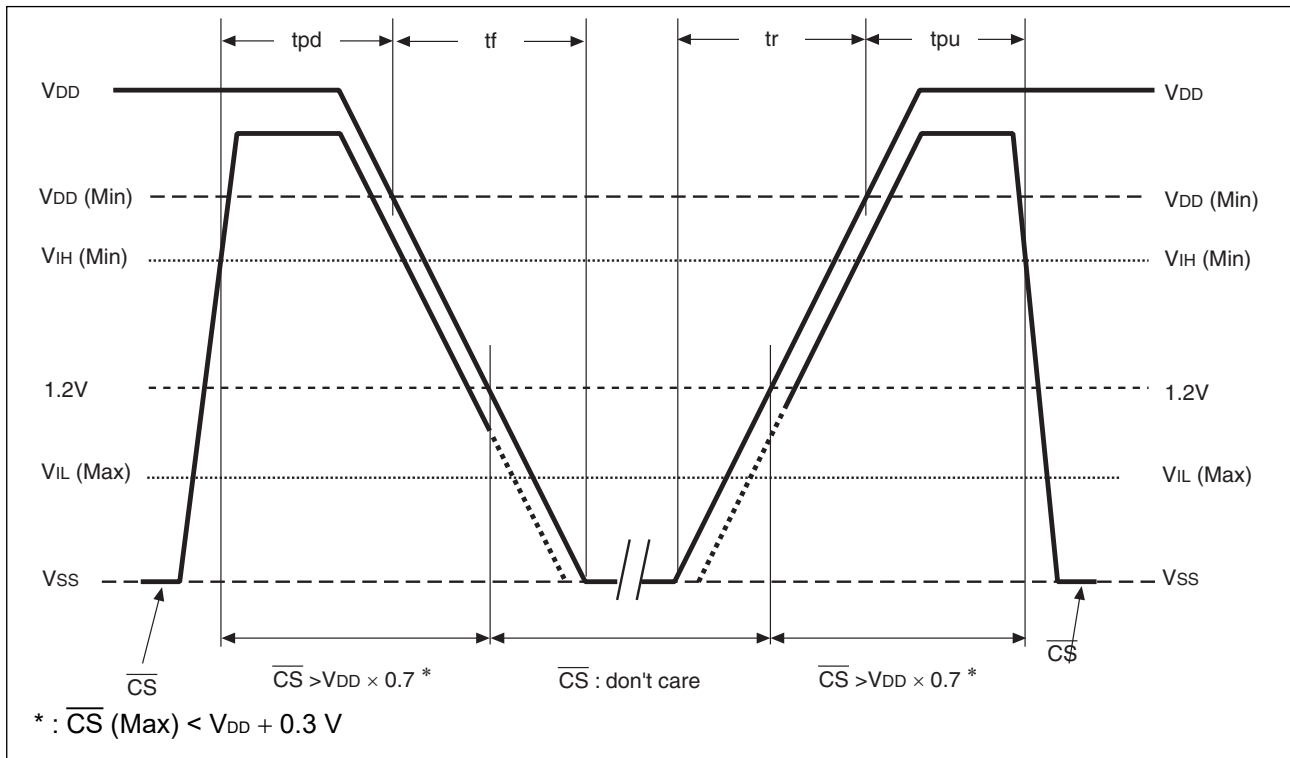


• Hold Timing



MB85RS64VY(AEC-Q100 Compliant)

■ POWER ON/OFF SEQUENCE



Parameter	Symbol	Value		Unit
		Min	Max	
\overline{CS} level hold time at power OFF	tpd	400	—	ns
\overline{CS} level hold time at power ON	tpu	250	—	μs
Power supply rising time	tr	0.05	—	ms/V
Power supply falling time	tf	0.1	—	ms/V

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed.

■ FeRAM CHARACTERISTICS

Parameter	Value		Unit	Remarks
	Min	Max		
Read/Write Endurance ^{*1}	10^{13}	—	Times/byte	Total number of reading and writing. Operation Ambient Temperature $T_A = +125 \text{ }^\circ\text{C}$
Data Retention ^{*2}	5.9 or more ^{*3}	—	Years	Operation Ambient Temperature $T_A = +125 \text{ }^\circ\text{C}$
	19.1	—		Operation Ambient Temperature $T_A = +105 \text{ }^\circ\text{C}$
	70.4	—		Operation Ambient Temperature $T_A = +85 \text{ }^\circ\text{C}$

*1 : Total number of reading and writing defines the minimum value of endurance, as an FeRAM memory operates with destructive readout mechanism.

*2: Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

*3: Under evaluation for more than 5.9 year(+125 °C).

MB85RS64VY(AEC-Q100 Compliant)

■ NOTE ON USE

We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.

■ ESD AND LATCH-UP

Test	DUT	Value
ESD HBM (Human Body Model) JESD22-A114 compliant	MB85RS64VYPNF-GS-AWE2 MB85RS64VYPNF-GS-AWERE2 MB85RS64VYPNF-GS-BCE1 MB85RS64VYPNF-GS-BCERE1	$\geq 2000 \text{ V} $
ESD CDM (Charged Device Model) JESD22-C101 compliant		$\geq 1000 \text{ V} $
Latch-Up (I-test) JESD78 compliant		$\geq 125 \text{ mA} $
Latch-Up (V_{supply} overvoltage test) JESD78 compliant		$\geq 8.25 \text{ V}$

■ REFLOW CONDITIONS AND FLOOR LIFE

[JEDEC MSL] : Moisture Sensitivity Level 3 (IPC/JEDEC J-STD-020E)

■ Current status on Contained Restricted Substances

This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

MB85RS64VY(AEC-Q100 Compliant)

■ ORDERING INFORMATION

Part number	Package	Shipping form	Minimum shipping quantity
MB85RS64VYPNF-GS-AWE2	8-pin plastic SOP	Tube	— *
MB85RS64VYPNF-GS-BCE1			
MB85RS64VYPNF-GS-AWERE2	8-pin plastic SOP	Embossed Carrier tape	1500
MB85RS64VYPNF-GS-BCERE1			

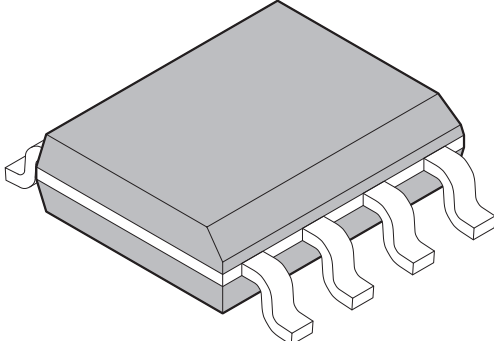
* : Please contact our sales office about minimum shipping quantity.

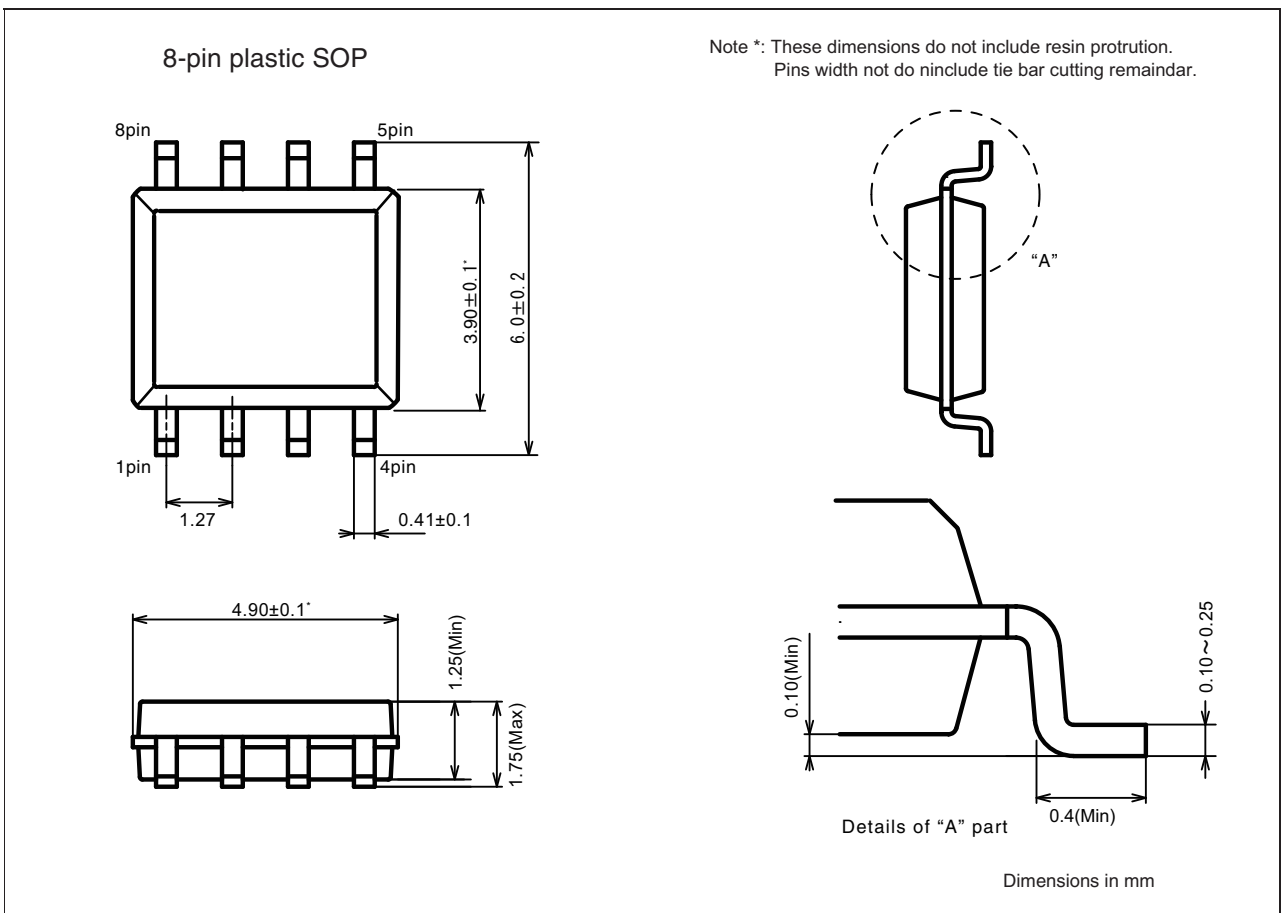
Note: MB85RS64VYPNF-GS has two basic part numbers, “-AW” and “-BC”, corresponding to each assembly site.

MB85RS64VY(AEC-Q100 Compliant)

■ PACKAGE DIMENSION

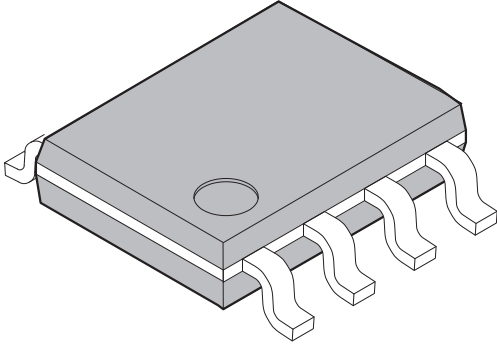
(1) MB85RS64VYPNF-GS-AWE2/MB85RS64VYPNF-GS-AWERE2

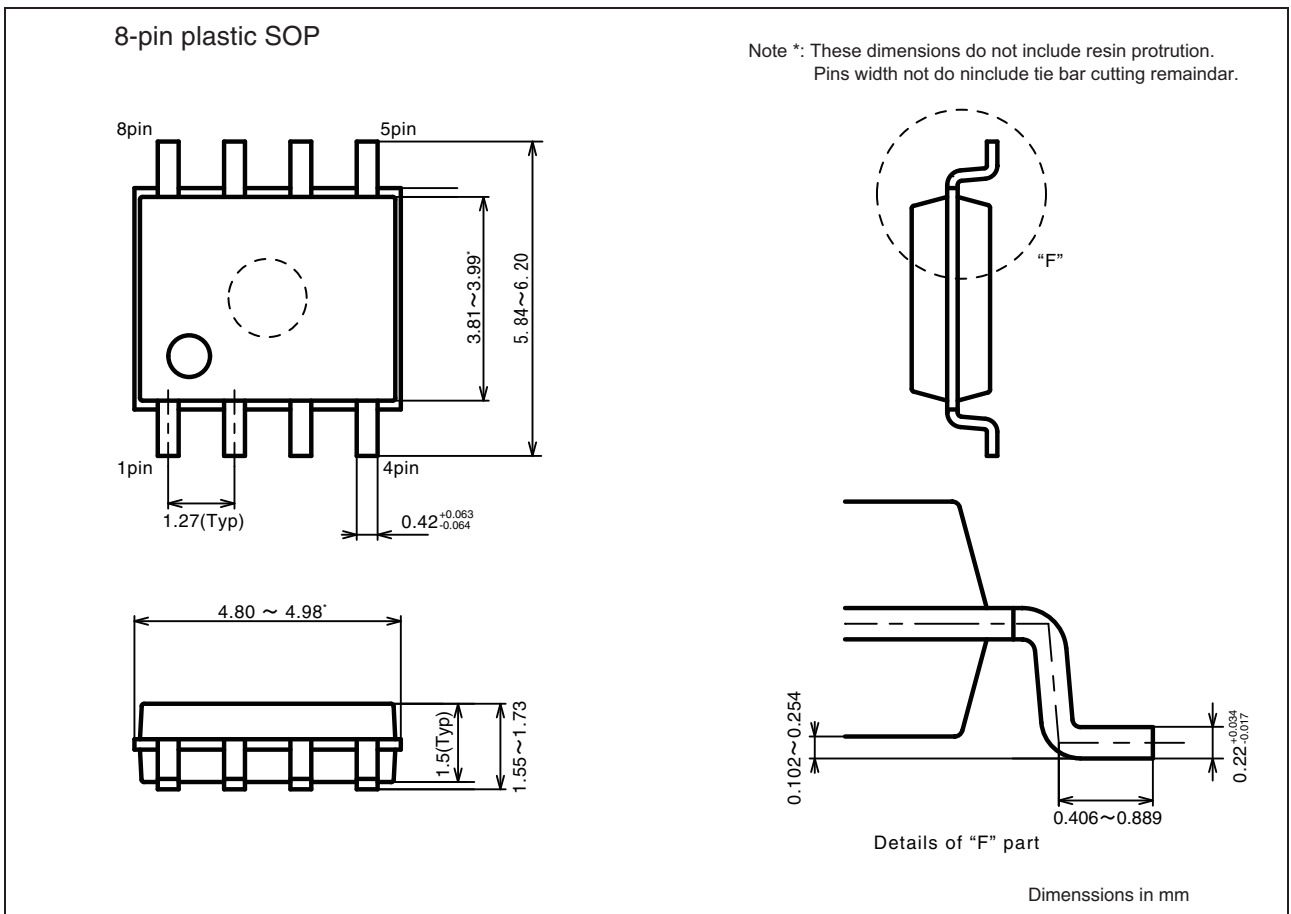
<p>8-pin plastic SOP</p>  <p>MB85RS64VYPNF-GS-AWE2, MB85RS64VYPNF-GS-AWERE2</p>	Lead pitch	1.27 mm
	Package width × package length	3.9 mm × 4.9 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.75 mm MAX



MB85RS64VY(AEC-Q100 Compliant)

(2) MB85RS64VYPNF-GS-BCE1/MB85RS64VYPNF-GS-BCERE1

<p>8-pin plastic SOP</p>  <p>MB85RS64VYPNF-GS-BCE1, MB85RS64VYPNF-GS-BCERE1</p>	Lead pitch	1.27 mm	
	Package width × package length	3.9 mm × 4.89 mm	
	Lead shape	Gullwing	
	Sealing method	Plastic mold	
	Mounting height	1.73 mm MAX	

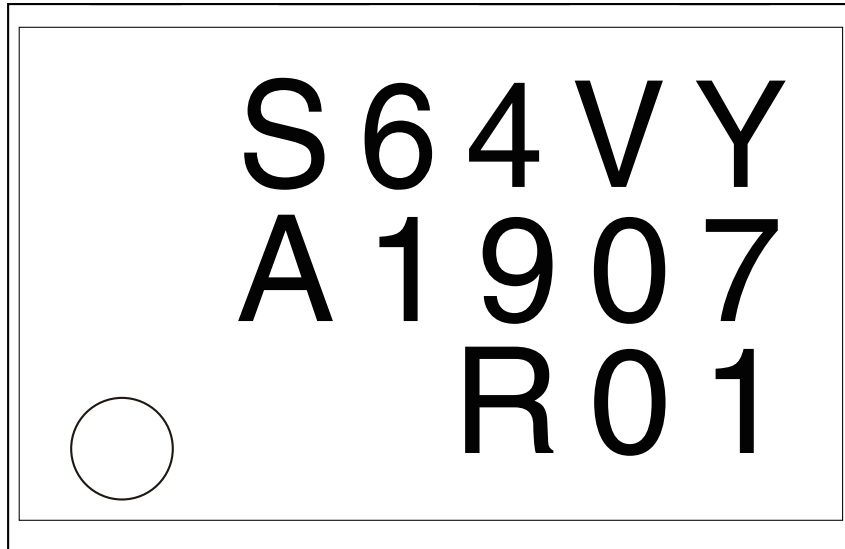


MB85RS64VY(AEC-Q100 Compliant)

■ MARKING (Example)

(1) MB85RS64VYPNF-GS-AWE2/MB85RS64VYPNF-GS-AWERE2

[MB85RS64VYPNF-GS-AWE2]
[MB85RS64VYPNF-GS-AWERE2]

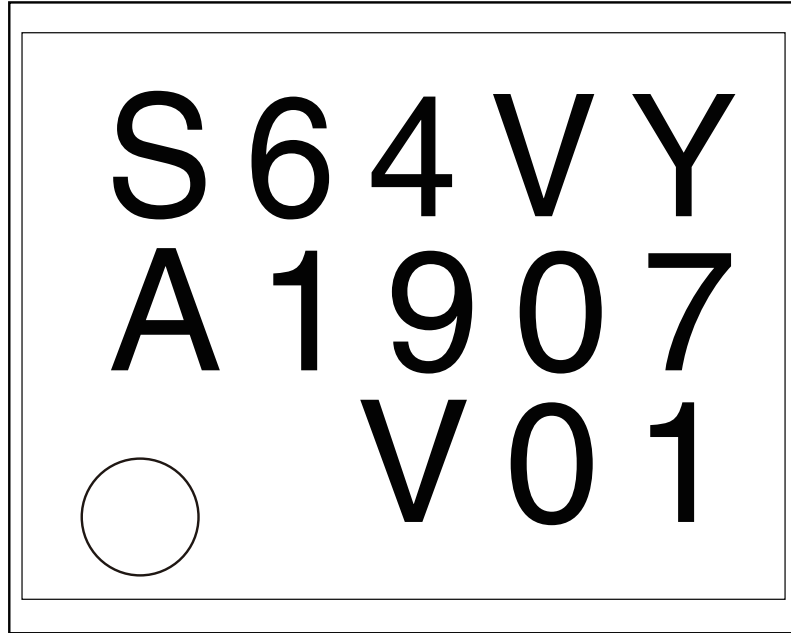


S64VY: Product name
A1907 : A(CS code) + 1907(Year and Week code)
R01 : Trace code

MB85RS64VY(AEC-Q100 Compliant)

(2) MB85RS64VYPNF-GS-BCE1/MB85RS64VYPNF-GS-BCERE1

[MB85RS64VYPNF-GS-BCE1]
[MB85RS64VYPNF-GS-BCERE1]



S64VY : Product name
A1907 : A(CS code) + 1907(Year + Week code)
V01 : Trace code

MB85RS64VY(AEC-Q100 Compliant)

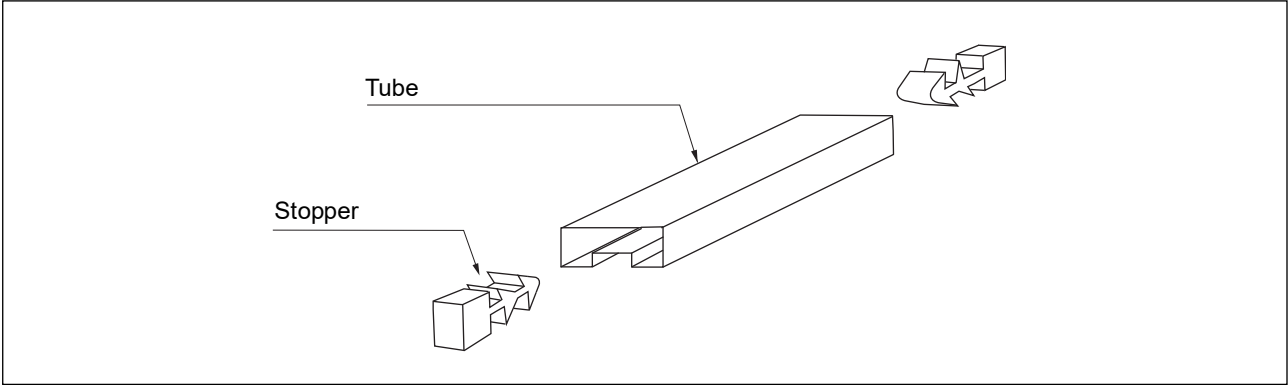
■ PACKING INFORMATION

(1) MB85RS64VYPNF-GS-AWE2/MB85RS64VYPNF-GS-AWERE2

1. Tube (MB85RS64VYPNF-GS-AWE2)

1.1 Tube Dimensions

- Tube/stopper shape (example)



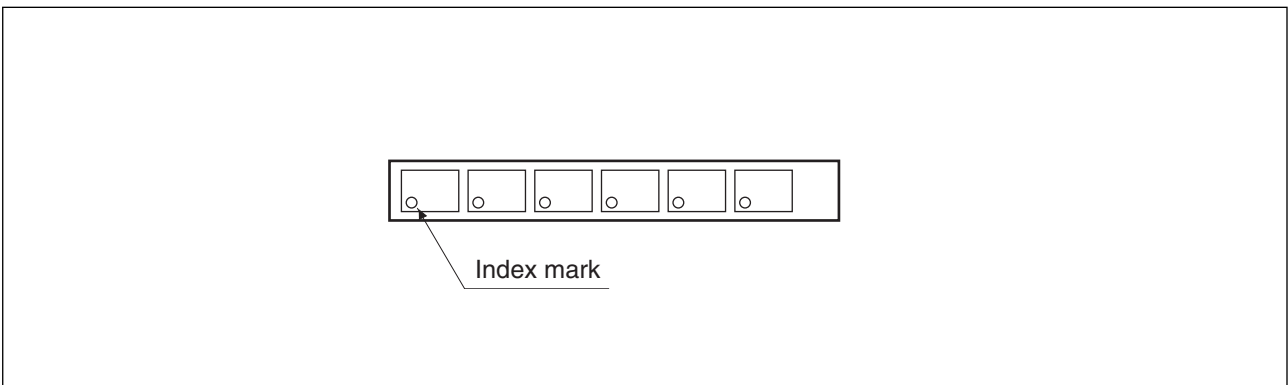
- Tube cross-sections and Maximum quantity

Maximum quantity		
pcs/tube	pcs/inner box	pcs/outer box
85	4,250	25,500

No heat resistance.
Package should not be baked by using tube.

(Dimensions in mm)

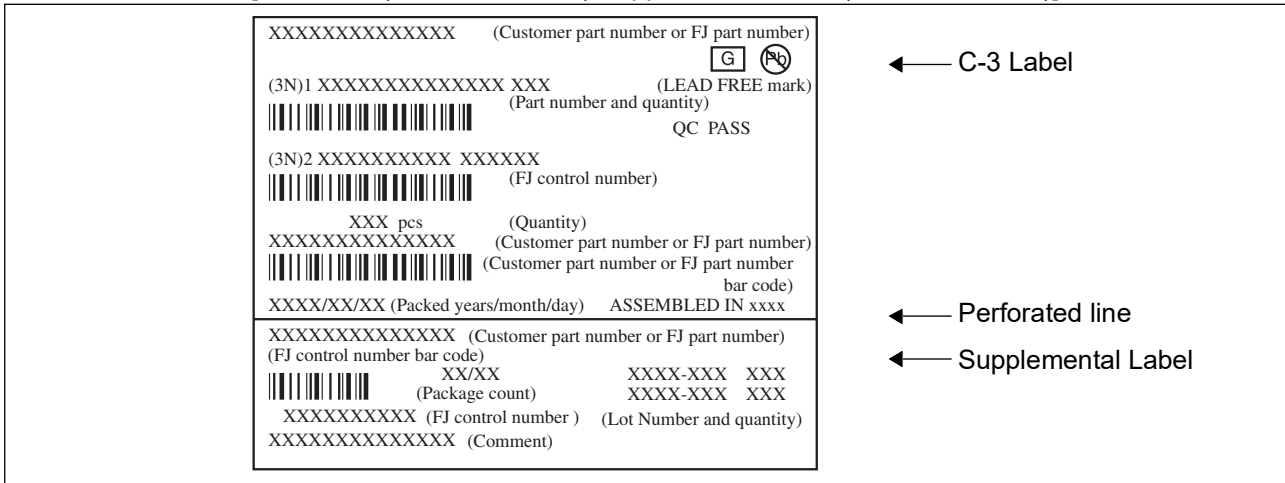
- Direction of index in tube



MB85RS64VY(AEC-Q100 Compliant)

1.2 Product label indicators (example)

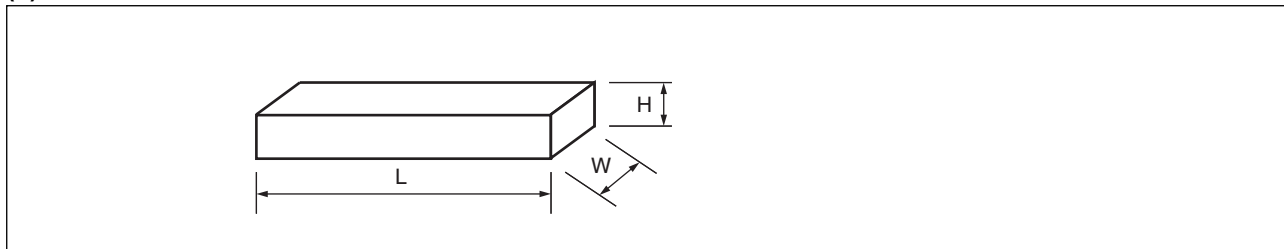
Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
 [C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]



MB85RS64VY(AEC-Q100 Compliant)

1.3 Dimensions for Containers

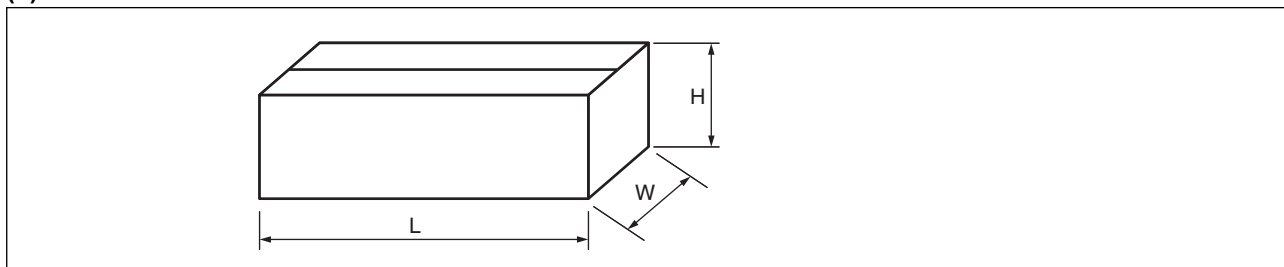
(1) Dimensions for inner box



L	W	H
549	125	81

(Dimensions in mm)

(2) Dimensions for outer box



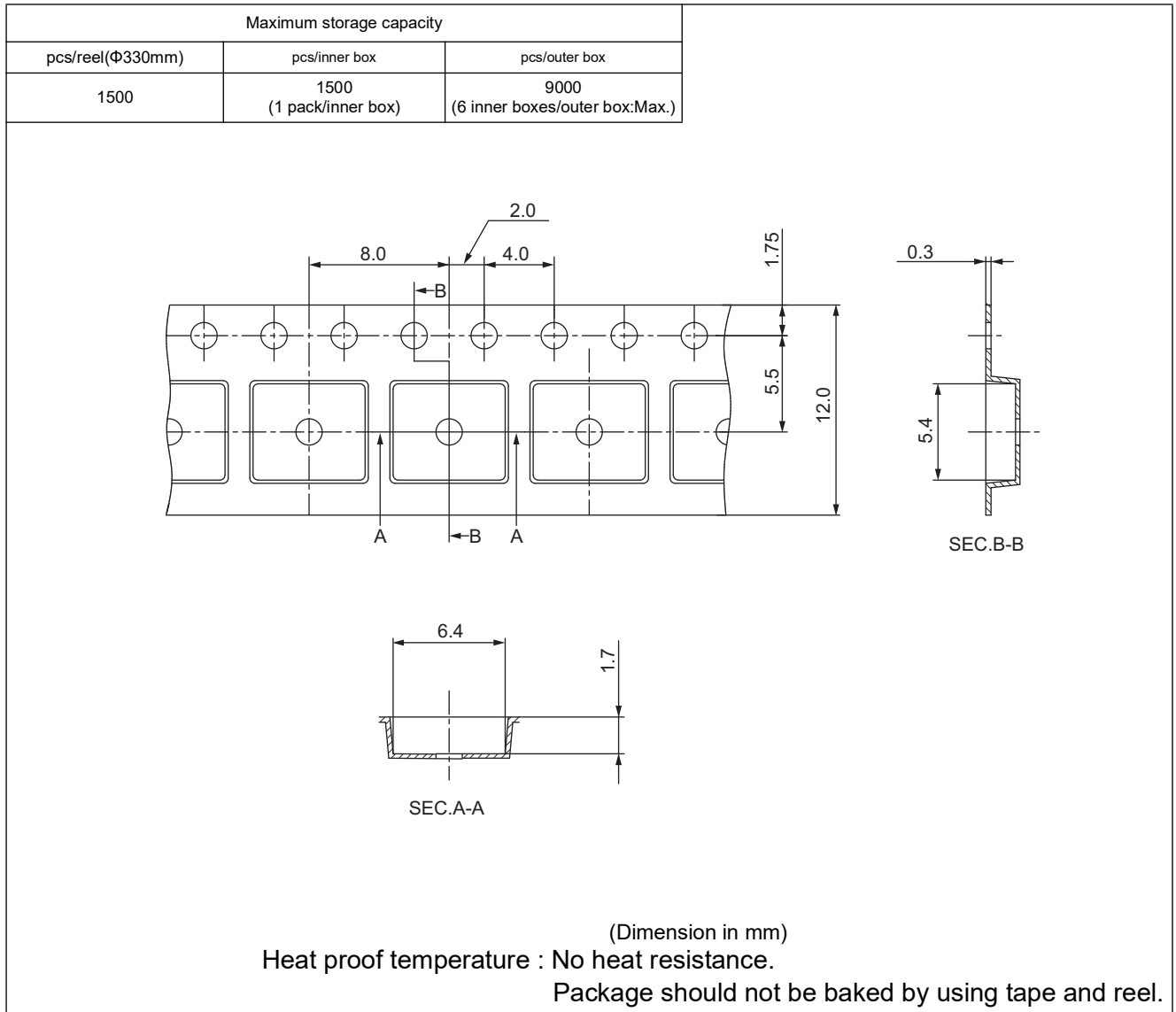
L	W	H
567	272	269

(Dimensions in mm)

MB85RS64VY(AEC-Q100 Compliant)

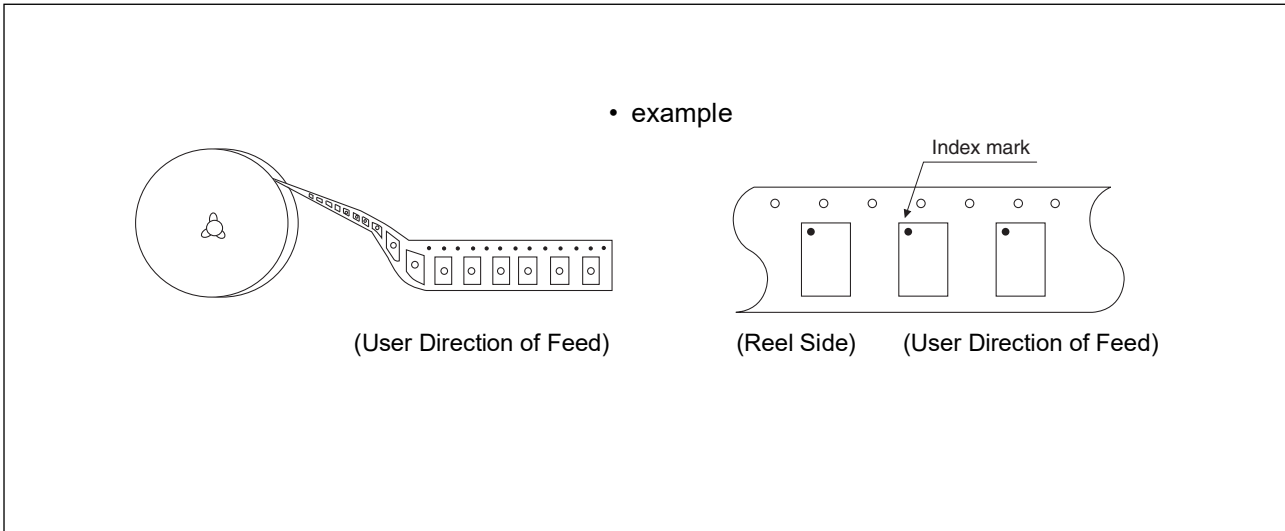
2. Emboss Tape (MB85RS64VYPNF-GS-AWERE2)

2.1 Tape Dimensions (not drawn to scale) (8-pin plastic SOP)

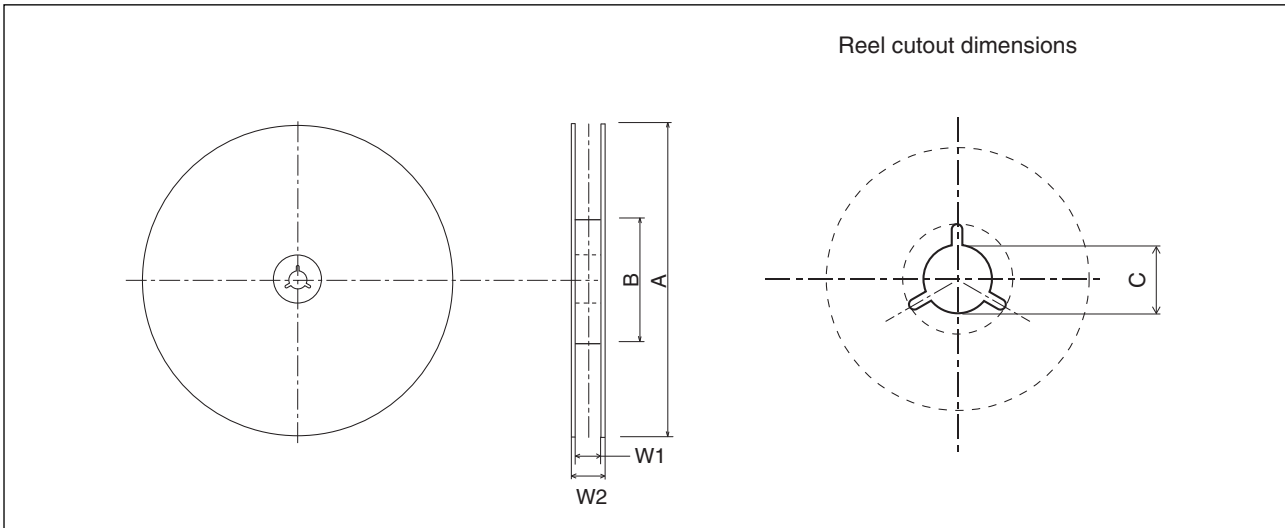


MB85RS64VY(AEC-Q100 Compliant)

2.2 IC orientation



2.3 Reel dimensions



Dimensions in mm

A	B	C	W1	W2
330	100	13	13.5	17.5

MB85RS64VY(AEC-Q100 Compliant)

2.4 Product label indicators (examples)

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss tapping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]

XXXXXXXXXXXXXXXXXX (Customer part number or FJ part number)		← C-3 Label
(3N)1 XXXXXXXXXXXXXXXXXX XXX (LEAD FREE mark)	(Part number and quantity)	
	QC PASS	
(3N)2 XXXXXXXXXXXXXXXXXX XXXXXX (FJ control number)		
XXX pcs (Quantity)		
XXXXXXXXXXXXXXXXXX (Customer part number or FJ part number)	(Customer part number or FJ part number bar code)	← Perforated line
XXXX/XX/XX (Packed years/month/day)	ASSEMBLED IN xxx	
XXXXXXXXXXXXXXXXXX (Customer part number or FJ part number)	(FJ control number bar code)	← Supplemental Label
	XX/XX (Package count)	
XXXXXXXXXXXXXXX (FJ control number)	XXXX-XXX XXX (Lot Number and quantity)	
XXXXXXXXXXXXXXXXXX (Comment)		

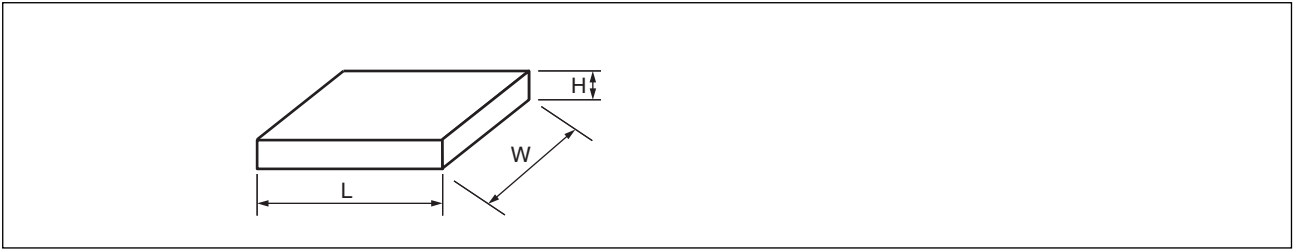
Label II: Moisture Barrier Bag (It sticks it on the Aluminum laminated bag)
[MSL Label (100mm × 70mm)]

<p>MOISTURE-SENSITIVE DEVICES</p> <p>注意</p> <ol style="list-style-type: none"> ドライパック包装の保管期限は、24ヶ月（25℃/80%RH未満）です。 本製品の耐熱温度は、<u>260℃</u> です。 袋開封後は、下記a) b)条件下で、ご使用ください。 <ol style="list-style-type: none"> <u>168</u> 時間以内 (30℃/60%RH以下) J-STD-033条件 以下の条件の場合は、実装前にベークしてください。 <ol style="list-style-type: none"> 23±5℃の環境下でインジケータカードの10%を超えた場合 3a、3bの条件に合致しない場合 ベークが必要な場合はIPC/JEDEC J-STD-033 参照してください。 <p>CAUTION</p> <ol style="list-style-type: none"> Calculated shelf life in sealed bag: 24 months at <25℃ / 80% RH Peak package body temperature: <u>260℃</u> After bag is opened, devices that will be subjected to reflow solder or other high temperature process must <ol style="list-style-type: none"> Mounted within: <u>168 hours</u> of factory conditions ≤30℃/60%RH Stored per J-STD-033 Devices require bake, before mounting, if: <ol style="list-style-type: none"> Humidity Indicator Card is > 10% when read at 23±5℃ 3a or 3b not met. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure. 	<p>LEVEL</p> <p>3</p>	← MSL label
<p>包装日：品名ラベルをご確認ください Bag Seal Date: See adjacent bar code label</p>	<p>* F 0 0 0 1 *</p>	
<p>Note: Level and body temperature defined by IPC/JEDEC J-STD-020</p>		

MB85RS64VY(AEC-Q100 Compliant)

2.5 Dimensions for Containers

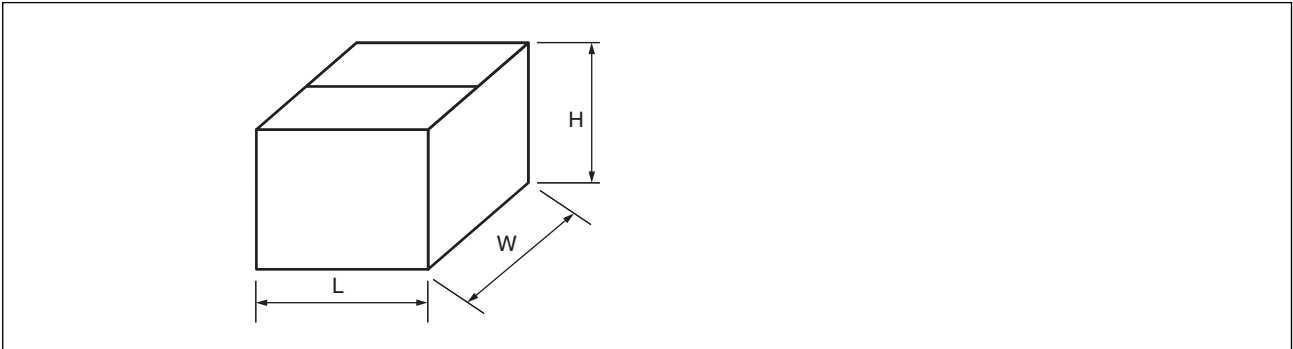
(1) Dimensions for inner box



Tape width	L	W	H
12	350	335	35

(Dimensions in mm)

(2) Dimensions for outer box



L	W	H
384	368	225

(Dimensions in mm)

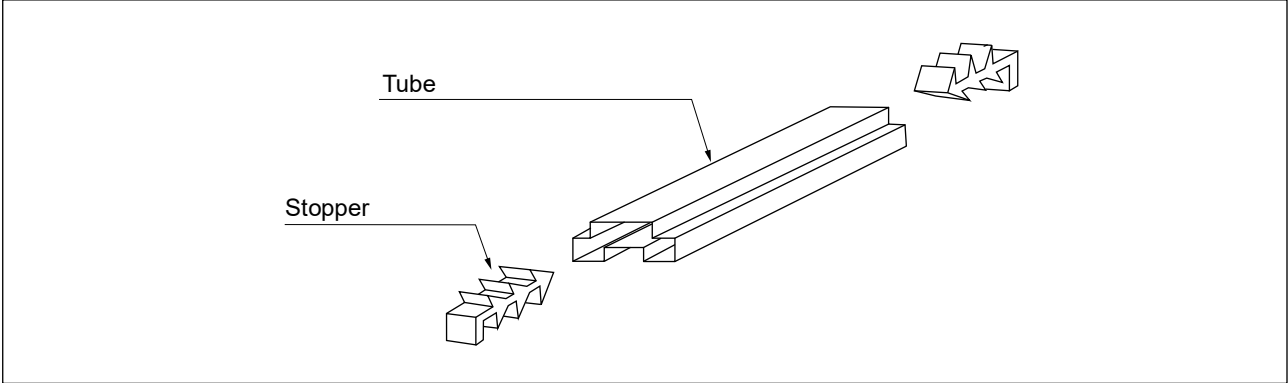
MB85RS64VY(AEC-Q100 Compliant)

(2)MB85RS64VYPNF-GS-BCE1/MB85RS64VYPNF-GS-BCERE1

1. Tube (MB85RS64VYPNF-GS-BCE1)

1.1 Tube Dimensions

- Tube/stopper shape (example)



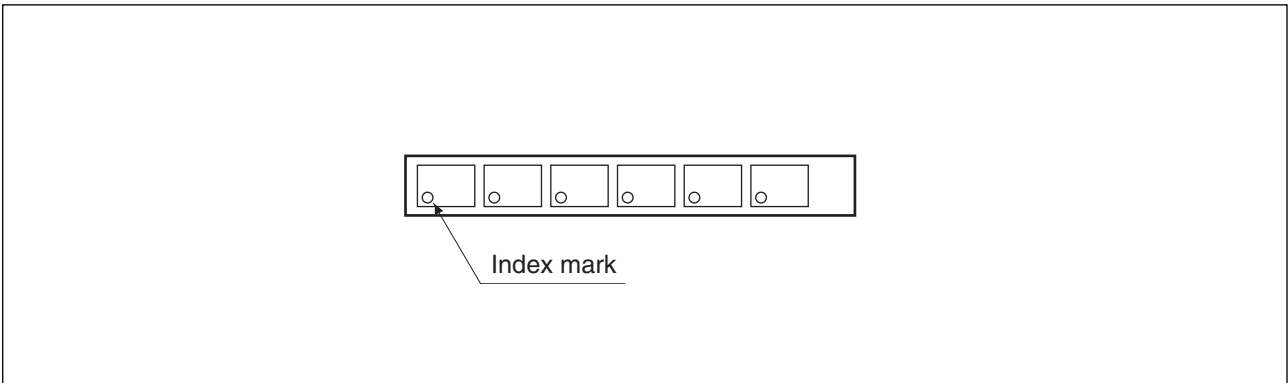
- Tube cross-sections and Maximum quantity

Maximum quantity		
pcs/tube(500mm)	pcs/inner box	pcs/outer box
85	4,250	17,000

No heat resistance.
Package should not be baked by using tube.

(Dimensions in mm)

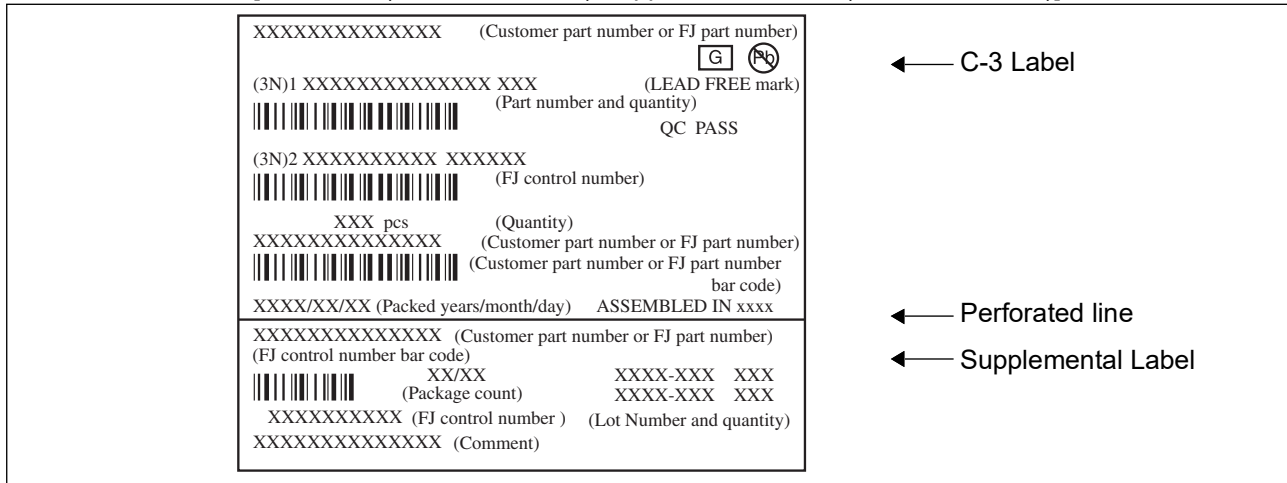
- Direction of index in tube



MB85RS64VY(AEC-Q100 Compliant)

1.2 Product label indicators (example)

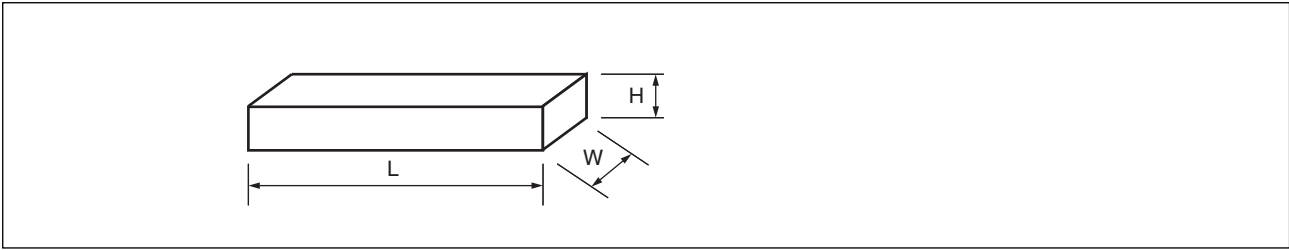
Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
 [C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]



MB85RS64VY(AEC-Q100 Compliant)

1.3 Dimensions for Containers

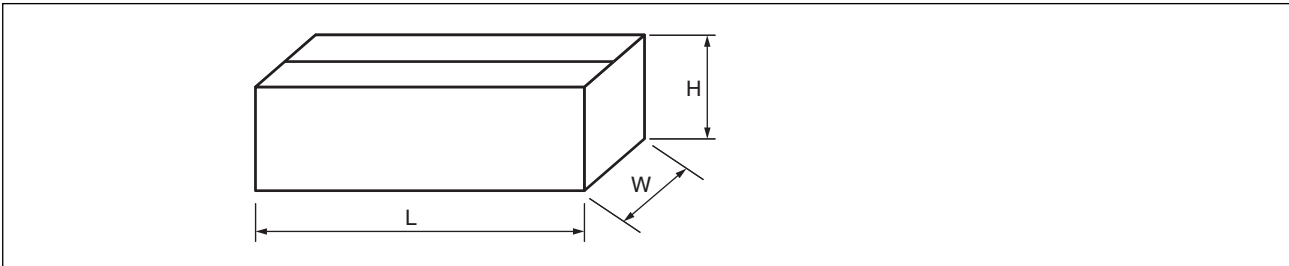
(1) Dimensions for inner box



L	W	H
540	125	75

(Dimensions in mm)

(2) Dimensions for outer box



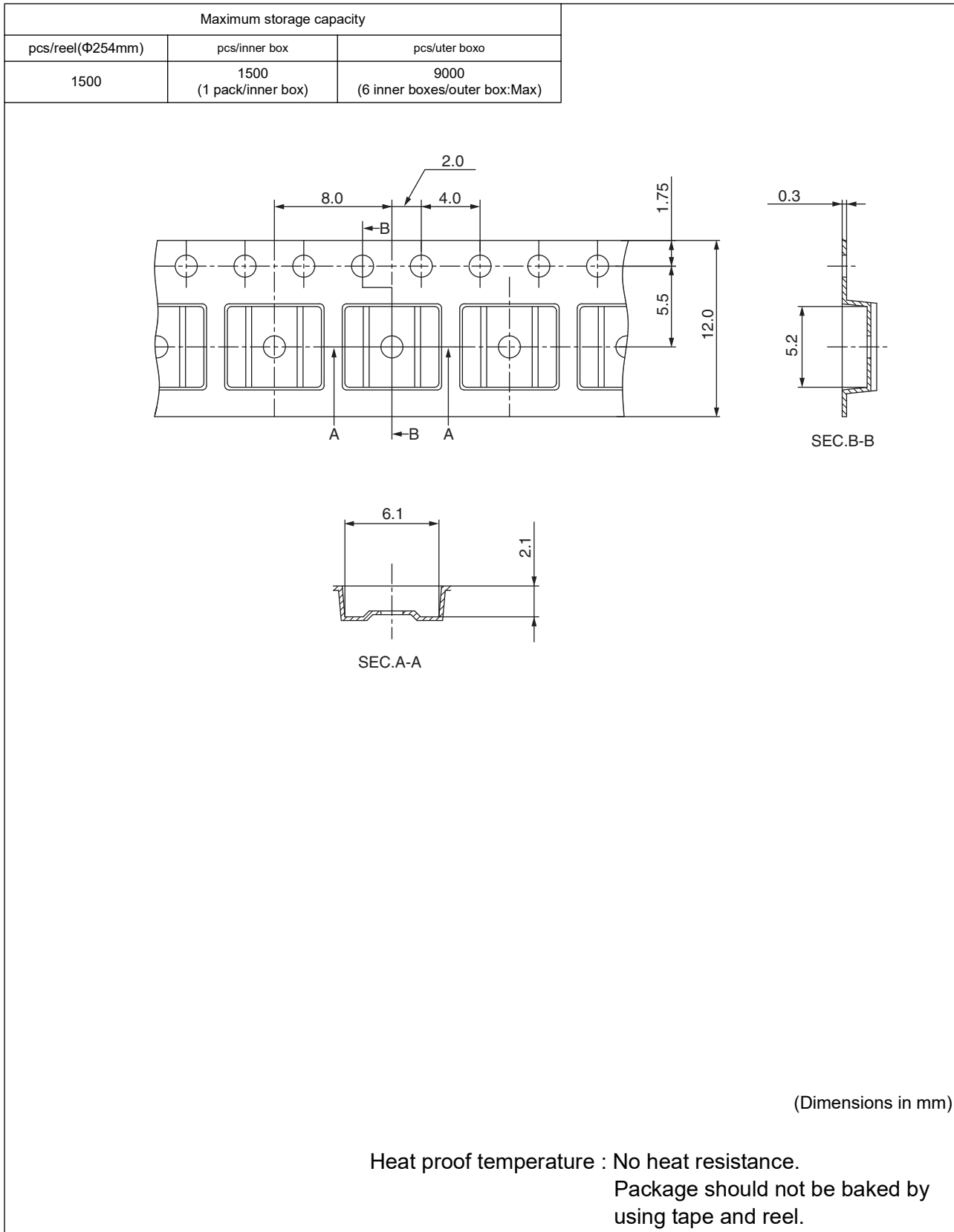
L	W	H
549	277	180

(Dimensions in mm)

MB85RS64VY(AEC-Q100 Compliant)

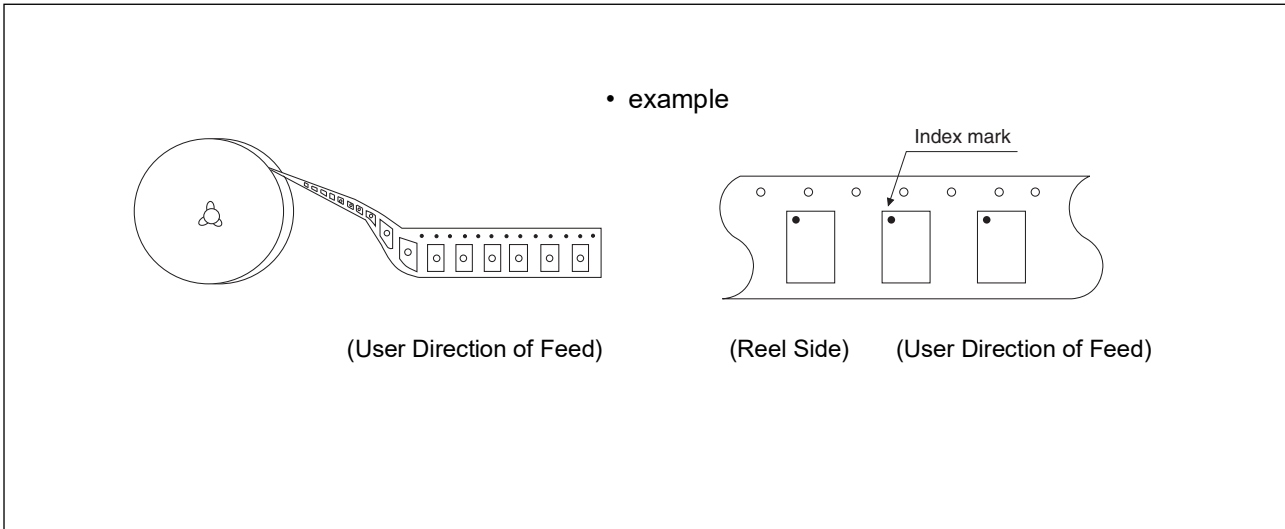
2. Emboss Tape (MB85RS64VYPNF-GS-BCERE1)

2.1 Tape Dimensions (not drawn to scale) (8-pin plastic SOP)

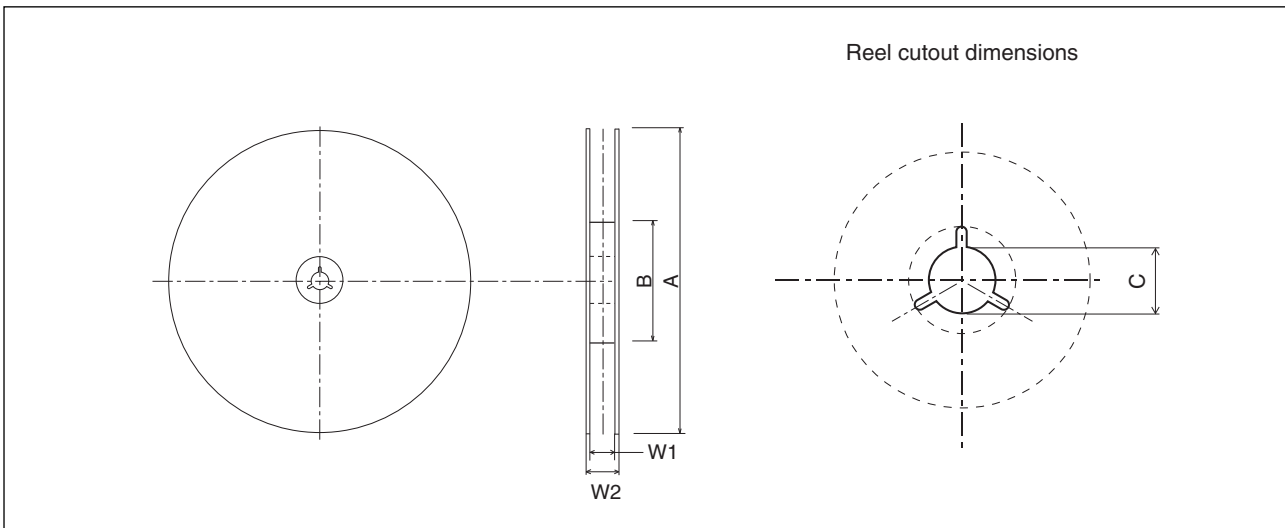


MB85RS64VY(AEC-Q100 Compliant)

2.2 IC orientation



2.3 Reel dimensions



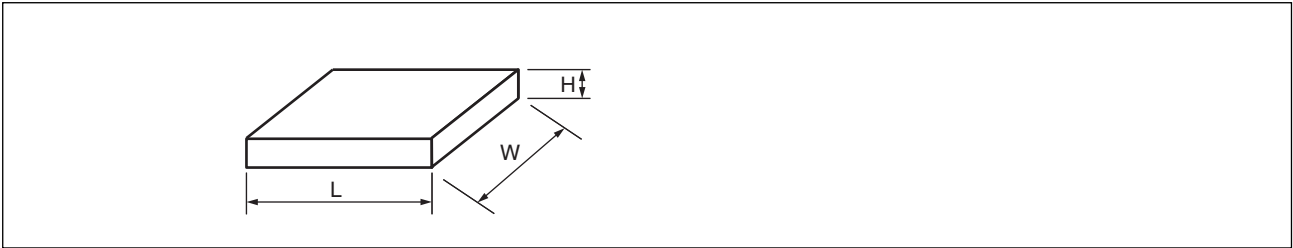
Dimensions in mm

A	B	C	W1	W2
254	100	13	13.5	17.5

MB85RS64VY(AEC-Q100 Compliant)

2.5 Dimensions for Containers

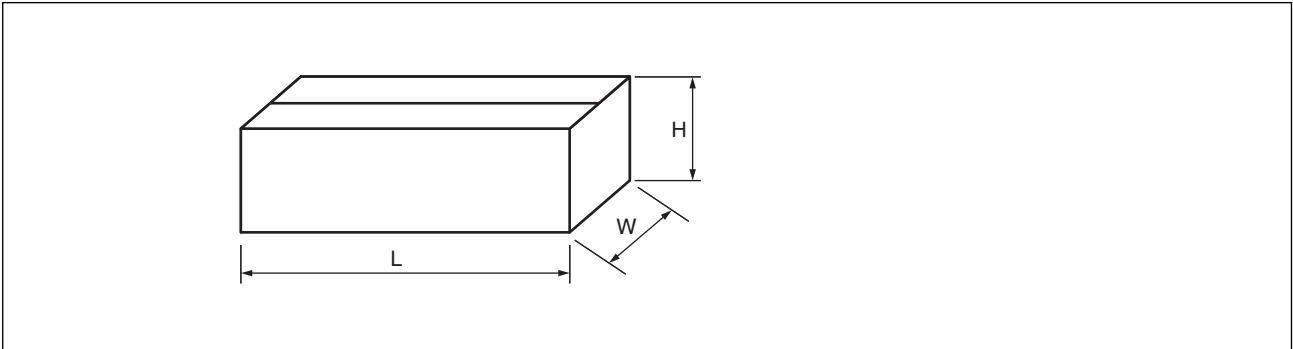
(1) Dimensions for inner box



Tape width	L	W	H
12	265	262	51

(Dimensions in mm)

(2) Dimensions for outer box



L	W	H
549	277	180

(Dimensions in mm)

MB85RS64VY(AEC-Q100 Compliant)

■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn left side of that page.

Page	Section	Change Results
—	Overall	Following technical word is revised to more commonly used one. FRAM to FeRAM

MB85RS64VY(AEC-Q100 Compliant)

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