

## Memory FeRAM

# 1 M Bit (128 K × 8)

# MB85R1001A

### ■ DESCRIPTIONS

The MB85R1001A is an FeRAM (Ferroelectric Random Access Memory) chip consisting of 131,072 words × 8 bits of nonvolatile memory cells fabricated using ferroelectric process and silicon gate CMOS process technologies.

The MB85R1001A is able to retain data without using a back-up battery, as is needed for SRAM.

The memory cells used in the MB85R1001A can be used for  $10^{10}$  read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E<sup>2</sup>PROM.

The MB85R1001A uses a pseudo-SRAM interface.

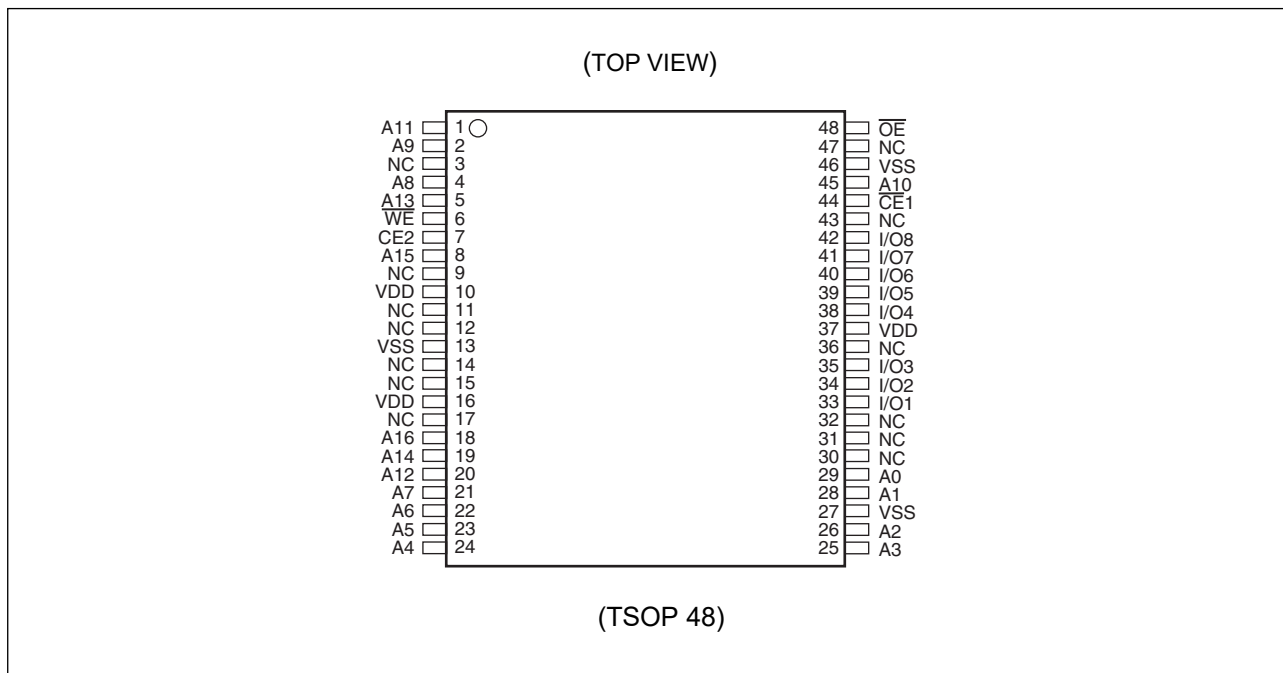
### ■ FEATURES

- Bit configuration : 131,072 words × 8 bits
- Read/write endurance :  $10^{10}$  times / byte
- Data retention : 10 years ( + 55 °C), 55 years ( + 35 °C)
- Operating power supply voltage : 3.0 V to 3.6 V
- Low power operation : Operating power supply current 10 mA (Typ)  
Standby current 10 μA (Typ)
- Operation ambient temperature range : - 40 °C to + 85 °C
- Package : 48-pin plastic TSOP  
RoHS compliant

Fujitsu Semiconductor Memory Solutions Limited has changed its name to RAMXEED Limited. RAMXEED Limited will continue to offer and support existing products while maintaining Fujitsu's part number unchanged.

# MB85R1001A

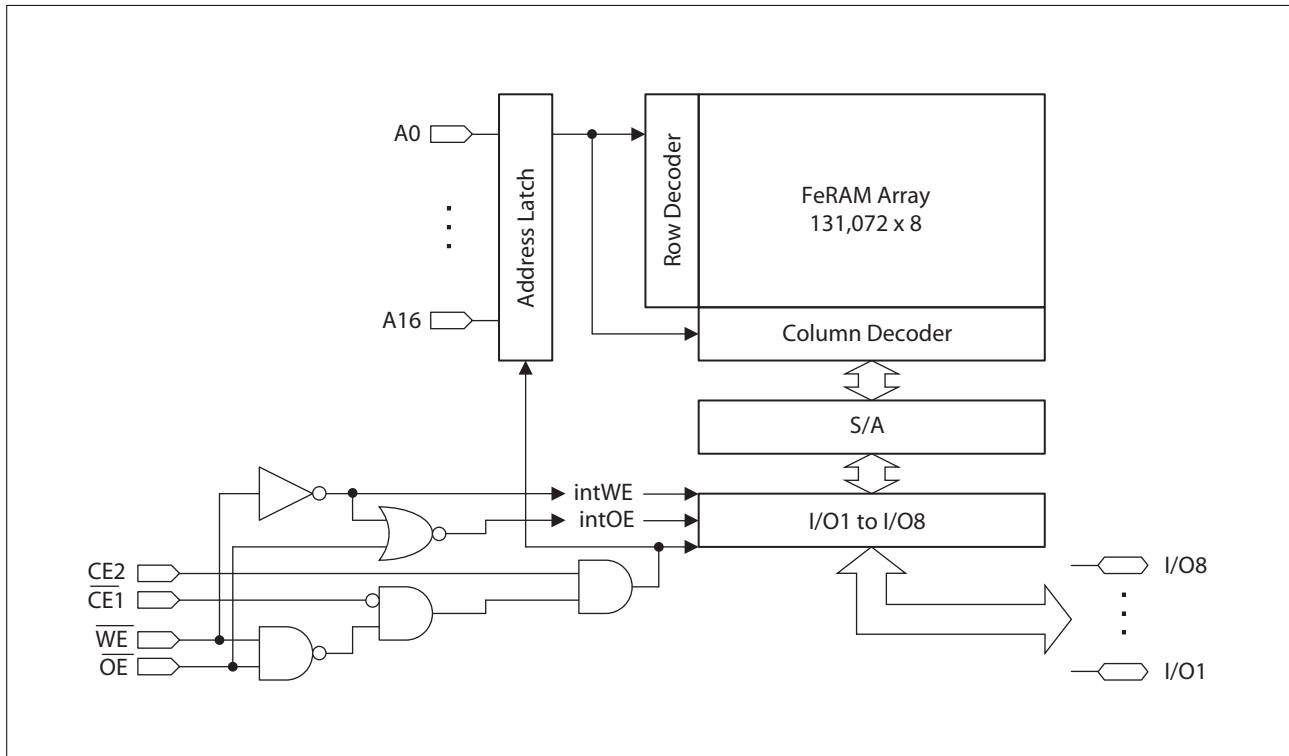
## ■ PIN ASSIGNMENTS



## ■ PIN DESCRIPTIONS

Pin Number	Pin Name	Functional Description
1, 2, 4, 5, 8, 18 to 26, 28, 29, 45	A0 to A16	Address Input pins
33 to 35, 38 to 42	I/O1 to I/O8	Data Input/Output pins
44	$\overline{CE1}$	Chip Enable 1 Input pin
7	CE2	Chip Enable 2 Input pin
6	$\overline{WE}$	Write Enable Input pin
48	$\overline{OE}$	Output Enable Input pin
10, 16, 37	VDD	Supply Voltage pins Connect all three pins to the power supply.
13, 27, 46	VSS	Ground pins Connect all three pins to ground.
3, 9, 11, 12, 14, 15, 17, 30 to 32, 36, 43, 47	NC	No Connect pins Leave these pins open, or connect to VDD or VSS.

## ■ BLOCK DIAGRAM



## ■ FUNCTIONAL TRUTH TABLE

Operation Mode	CE1	CE2	WE	OE	I/O1 to I/O8	Supply Current
Standby Precharge	H	X	X	X	Hi-Z	Standby (I <sub>SB</sub> )
	X	L	X	X		
	X	X	H	H		
Read	$\overline{\downarrow}$	H	H	L	Data Output	Operation (I <sub>DD</sub> )
	L	$\uparrow$				
Read (Pseudo-SRAM, $\overline{OE}$ control*1)	L	H	H	$\overline{\downarrow}$		
Write	$\overline{\downarrow}$	H	L	H	Data Input	
	L	$\uparrow$				
Write (Pseudo-SRAM, $\overline{WE}$ control*2)	L	H	$\overline{\downarrow}$	H		

Note: L = V<sub>IL</sub>, H = V<sub>IH</sub>, X can be either H, L,  $\overline{\downarrow}$  or  $\uparrow$ , Hi-Z = High Impedance

$\overline{\downarrow}$  : Latch address and latch data at falling edge,  $\uparrow$  : Latch address and latch data at rising edge

\*1 :  $\overline{OE}$  control of the Pseudo-SRAM means the valid address at the falling edge of  $\overline{OE}$  to read.

\*2 :  $\overline{WE}$  control of the Pseudo-SRAM means the valid address and data at the falling edge of  $\overline{WE}$  to write.

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## ■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power Supply Voltage*	V <sub>DD</sub>	- 0.5	+ 4.0	V
Input Pin Voltage*	V <sub>IN</sub>	- 0.5	V <sub>DD</sub> + 0.5 ( ≤ 4.0)	V
Output Pin Voltage*	V <sub>OUT</sub>	- 0.5	V <sub>DD</sub> + 0.5 ( ≤ 4.0)	V
Operation ambient temperature	T <sub>A</sub>	- 40	+ 85	°C
Storage Temperature	T <sub>STG</sub>	- 55	+ 125	°C

\* : All voltages are referenced to VSS = 0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage <sup>*1</sup>	V <sub>DD</sub>	3.0	3.3	3.6	V
Operation ambient temperature <sup>*2</sup>	T <sub>A</sub>	- 40	—	+ 85	°C

\*1 : All voltages are referenced to VSS = 0 V.

\*2 : Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

## ■ ELECTRICAL CHARACTERISTICS

### 1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Leakage Current	$ I_{LI} $	$V_{IN} = 0\text{ V to }V_{DD}$	—	—	10	$\mu\text{A}$
Output Leakage Current	$ I_{LO} $	$V_{OUT} = 0\text{ V to }V_{DD}$ , $\overline{CE1} = V_{IH}$ or $\overline{OE} = V_{IH}$	—	—	10	$\mu\text{A}$
Operating Power Supply Current* <sup>1</sup>	$I_{DD}$	$\overline{CE1} = 0.2\text{ V}$ , $\overline{CE2} = V_{DD}-0.2\text{ V}$ , $I_{out} = 0\text{ mA}$	—	10	15	mA
Standby Current* <sup>2</sup>	$I_{SB}$	$\overline{CE1} \geq V_{DD}-0.2\text{ V}$	—	10	50	$\mu\text{A}$
		$\overline{CE2} \leq 0.2\text{ V}$				
		$\overline{OE} \geq V_{DD}-0.2\text{ V}$ , $\overline{WE} \geq V_{DD}-0.2\text{ V}$				
High Level Input Voltage	$V_{IH}$	$V_{DD} = 3.0\text{ V to }3.6\text{ V}$	$V_{DD} \times 0.8$	—	$V_{DD} + 0.5$ ( $\leq 4.0$ )	V
Low Level Input Voltage	$V_{IL}$	$V_{DD} = 3.0\text{ V to }3.6\text{ V}$	-0.5	—	+0.6	V
High Level Output Voltage	$V_{OH}$	$I_{OH} = -1.0\text{ mA}$	$V_{DD} \times 0.8$	—	—	V
Low Level Output Voltage	$V_{OL}$	$I_{OL} = 2.0\text{ mA}$	—	—	0.4	V

\*1 : During the measurement of  $I_{DD}$ , the Address and Data In were taken to only change once per active cycle.  
 $I_{out}$ : output current

\*2 : All pins other than setting pins shall be input at the CMOS level voltages such as  $H \geq V_{DD} - 0.2\text{ V}$ ,  $L \leq 0.2\text{ V}$ .

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## 2. AC Characteristics

### • AC Test Conditions

Power Supply Voltage	: 3.0 V to 3.6 V
Operation Ambient Temperature	: -40 °C to +85 °C
Input Voltage Amplitude	: 0.3 V to 2.7 V
Input Rising Time	: 5 ns
Input Falling Time	: 5 ns
Input Evaluation Level	: 2.0 V / 0.8 V
Output Evaluation Level	: 2.0 V / 0.8 V
Output Load Capacitance	: 50 pF

### (1) Read Cycle

Parameter	Symbol	Value		Unit
		Min	Max	
Read Cycle Time	$t_{RC}$	150	—	ns
CE1 Active Time	$t_{CA1}$	120	—	ns
CE2 Active Time	$t_{CA2}$	120	—	ns
OE Active Time	$t_{RP}$	120	—	ns
Precharge Time	$t_{PC}$	20	—	ns
Address Setup Time	$t_{AS}$	0	—	ns
Address Hold Time	$t_{AH}$	50	—	ns
OE Setup Time	$t_{ES}$	0	—	ns
Output Hold Time	$t_{OH}$	0	—	ns
Output Set Time	$t_{LZ}$	30	—	ns
CE1 Access Time	$t_{CE1}$	—	100	ns
CE2 Access Time	$t_{CE2}$	—	100	ns
OE Access Time	$t_{OE}$	—	100	ns
Output Floating Time	$t_{OHZ}$	—	20	ns

### (2) Write Cycle

Parameter	Symbol	Value		Unit
		Min	Max	
Write Cycle Time	$t_{WC}$	150	—	ns
CE1 Active Time	$t_{CA1}$	120	—	ns
CE2 Active Time	$t_{CA2}$	120	—	ns
Precharge Time	$t_{PC}$	20	—	ns
Address Setup Time	$t_{AS}$	0	—	ns
Address Hold Time	$t_{AH}$	50	—	ns
Write Pulse Width	$t_{WP}$	120	—	ns
Data Setup Time	$t_{DS}$	0	—	ns
Data Hold Time	$t_{DH}$	50	—	ns
Write Setup Time	$t_{WS}$	0	—	ns

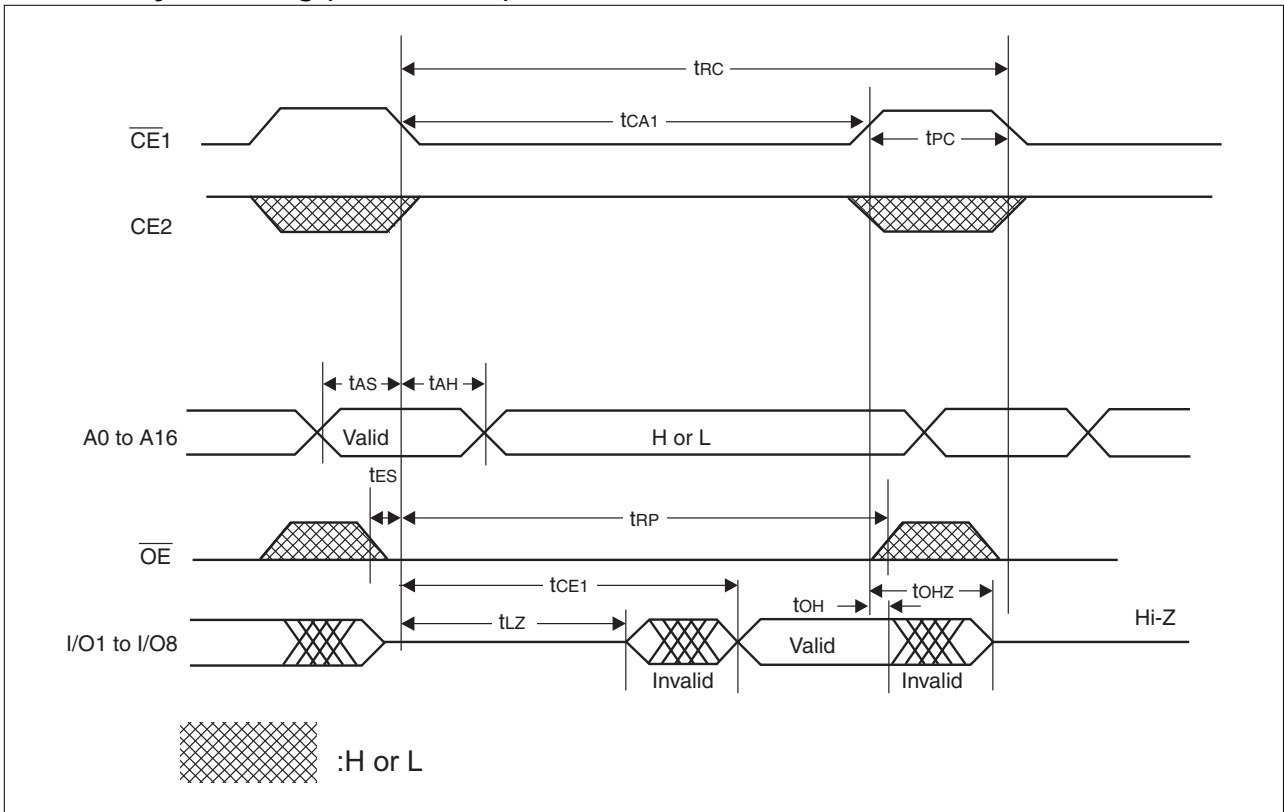
### 3. Pin Capacitance

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Capacitance	$C_{IN}$	$V_{DD} = V_{IN} = V_{OUT} = 0\text{ V}$ , $f = 1\text{ MHz}$ , $T_A = +25\text{ °C}$	—	—	10	pF
Output Capacitance	$C_{OUT}$		—	—	10	pF

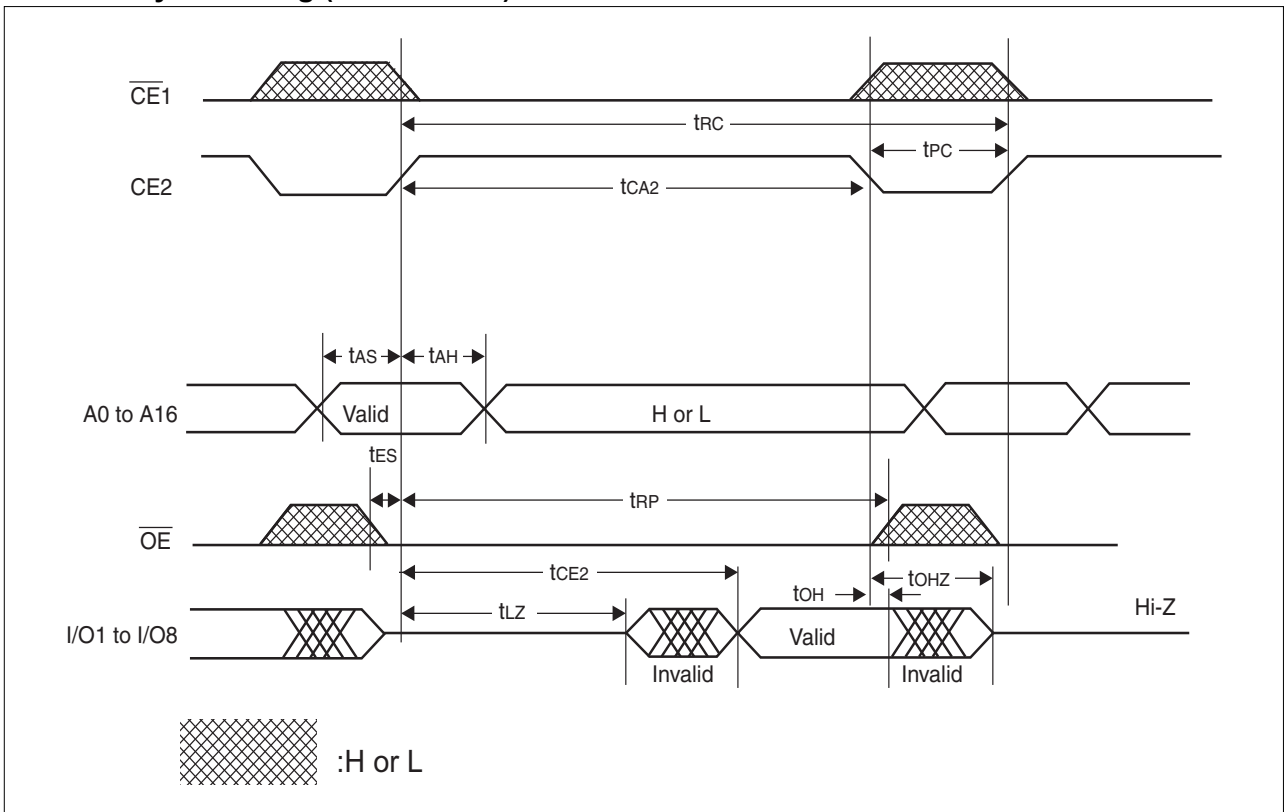
# MB85R1001A

## ■ TIMING DIAGRAMS

### 1. Read Cycle Timing ( $\overline{CE1}$ Control)

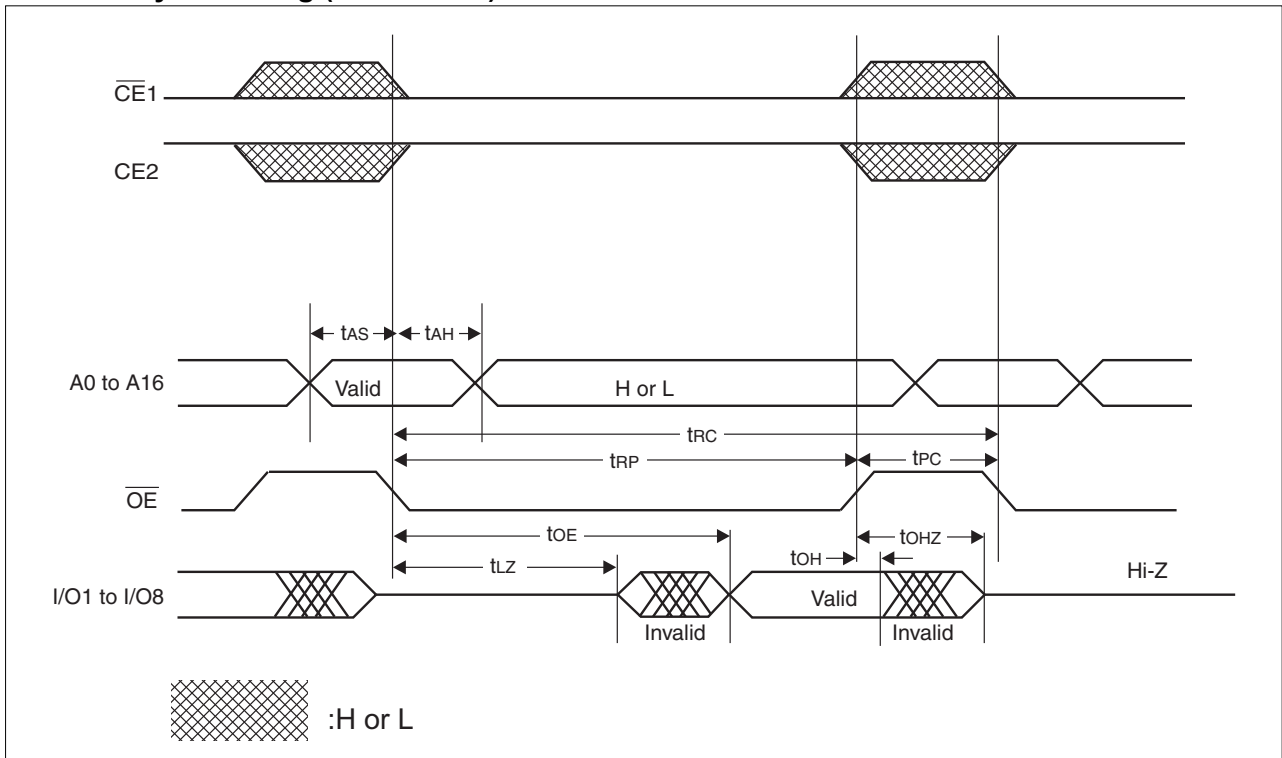


### 2. Read Cycle Timing (CE2 Control)

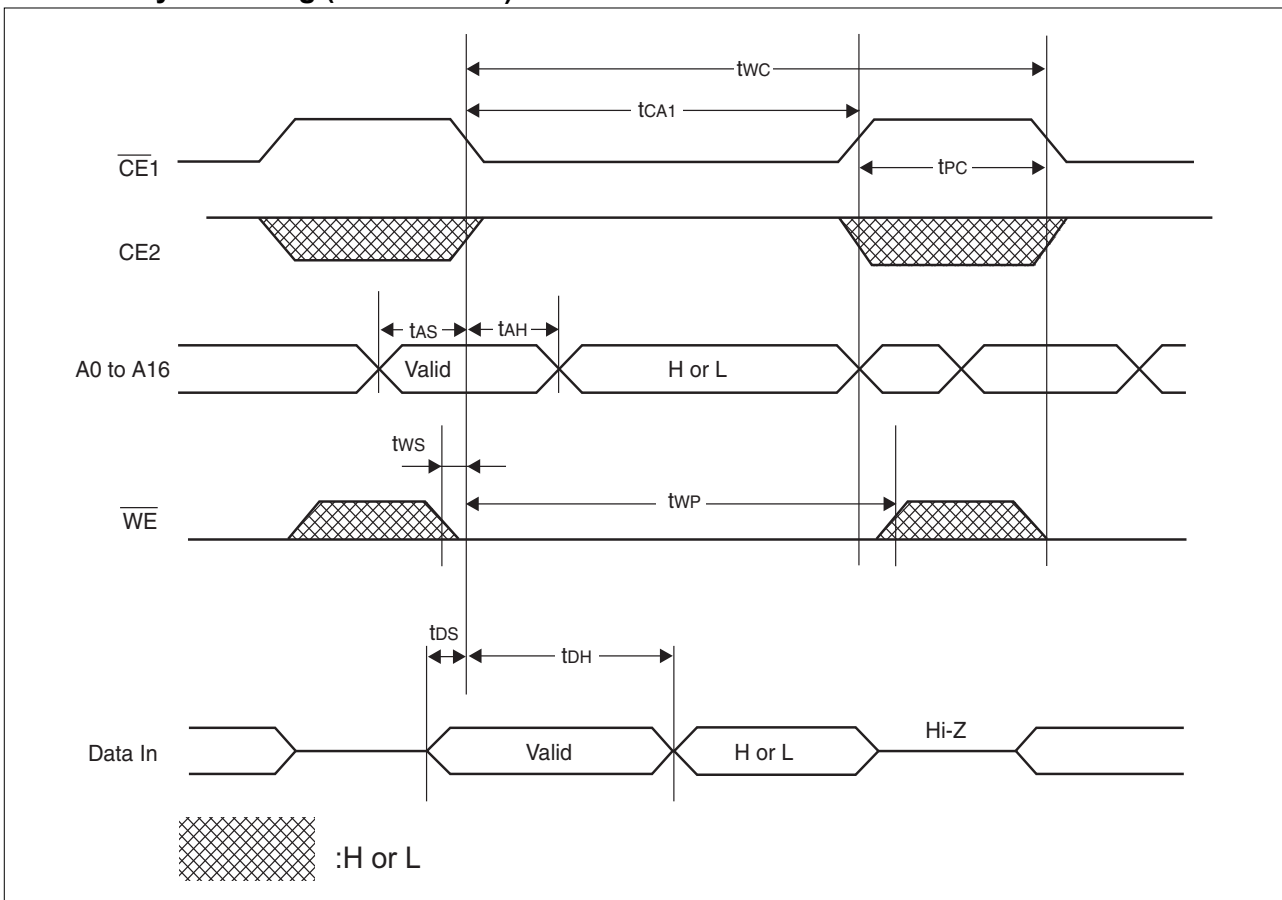




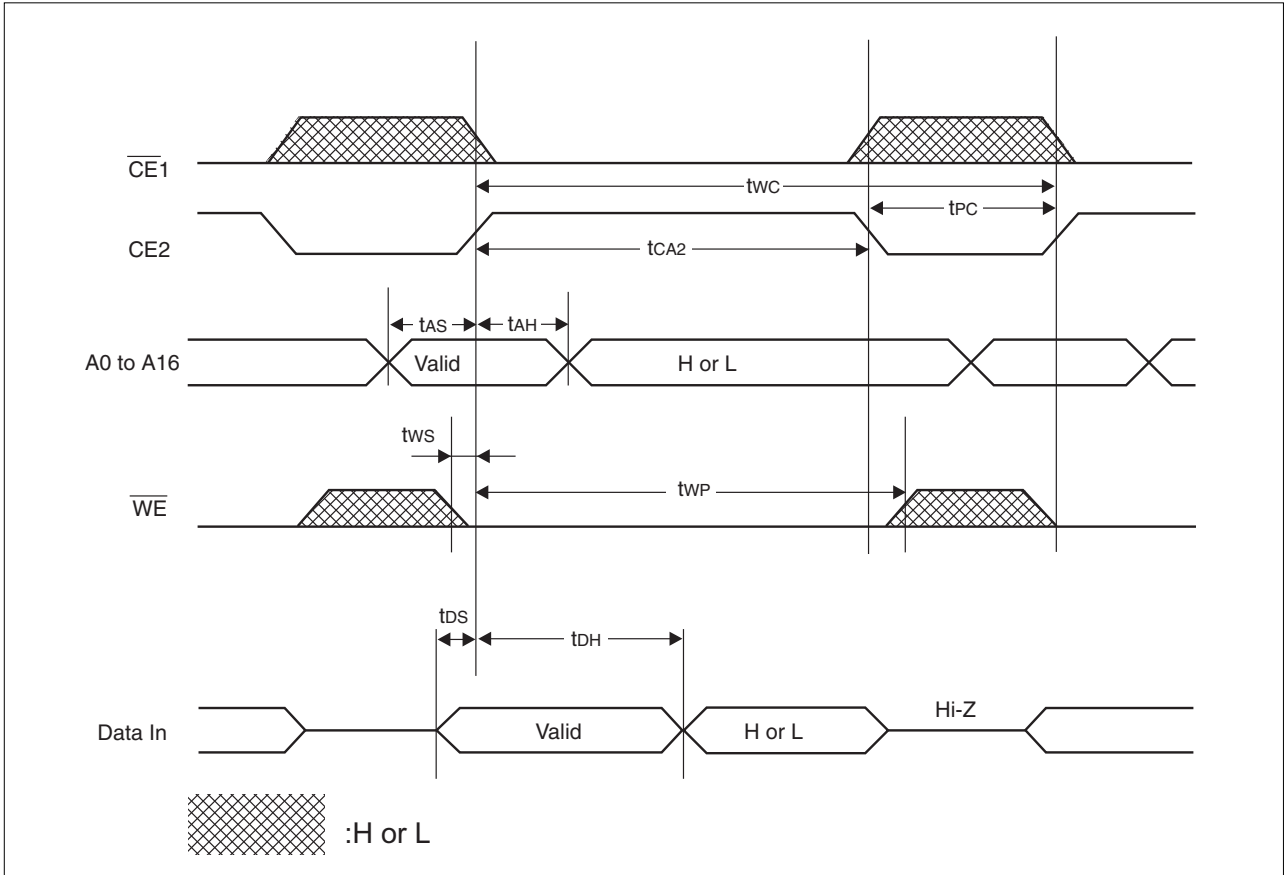
### 3. Read Cycle Timing ( $\overline{OE}$ Control)



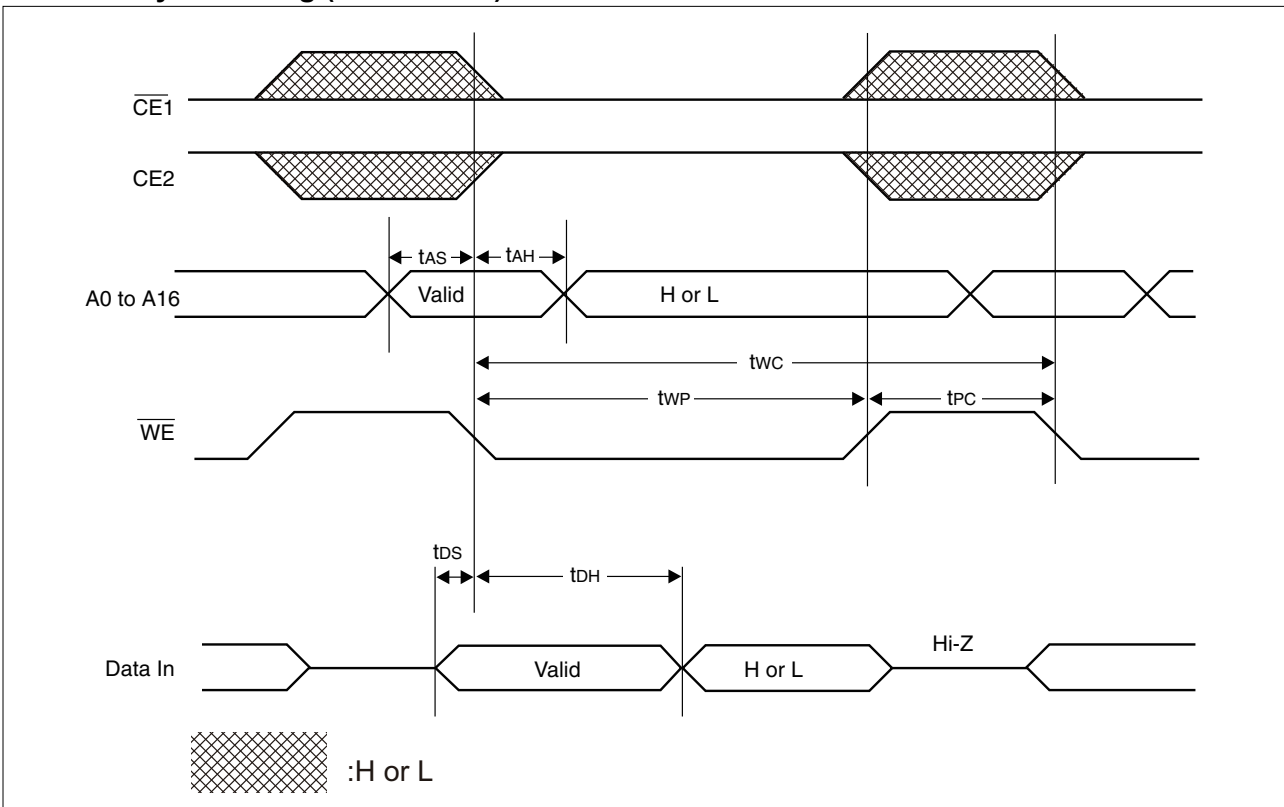
### 4. Write Cycle Timing ( $\overline{CE1}$ Control)



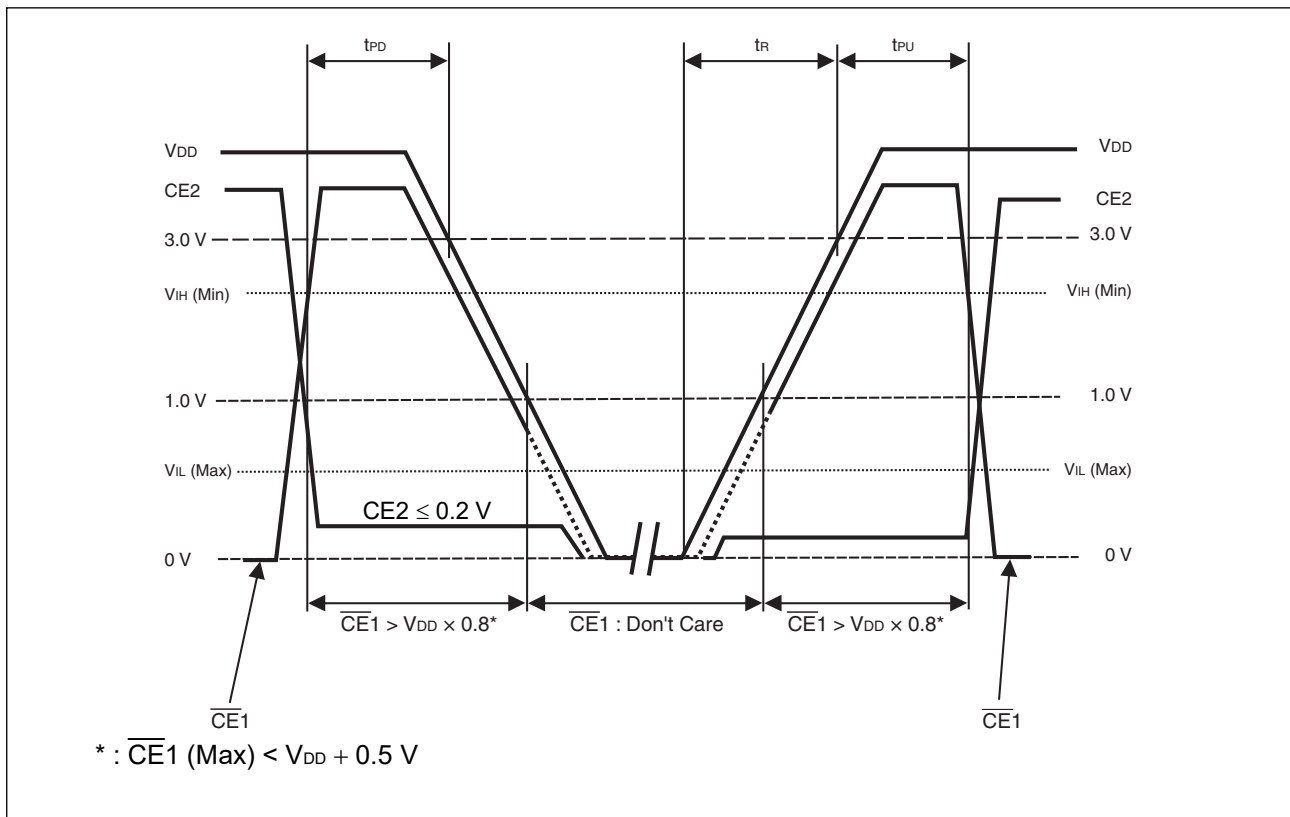
## 5. Write Cycle Timing (CE2 Control)



## 6. Write Cycle Timing (WE Control)



## ■ POWER ON/OFF SEQUENCE



Parameter	Symbol	Value			Unit
		Min	Typ	Max	
$\overline{CE1}$ level hold time for Power OFF	$t_{PD}$	85	—	—	ns
$\overline{CE1}$ level hold time for Power ON	$t_{PU}$	85	—	—	ns
Power supply rising time	$t_R$	0.05	—	200	ms

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed.

In case the power is turned on or off, use the power supply reset IC and fix the CE2 to low level, to prevent unexpected writing. Use either of  $\overline{CE1}$  or CE2, or both to disable control of the device.

## ■ FeRAM CHARACTERISTICS

Item	Min	Max	Unit	Parameter
Read/Write Endurance*1	$10^{10}$	—	Times/byte	Operation Ambient Temperature $T_A = +85 \text{ }^\circ\text{C}$
Data Retention*2	10	—	Years	Operation Ambient Temperature $T_A = +55 \text{ }^\circ\text{C}$
	55	—		Operation Ambient Temperature $T_A = +35 \text{ }^\circ\text{C}$

\*1 : Total number of reading and writing defines the minimum value of endurance, as an FeRAM memory operates with destructive readout mechanism.

\*2 : Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

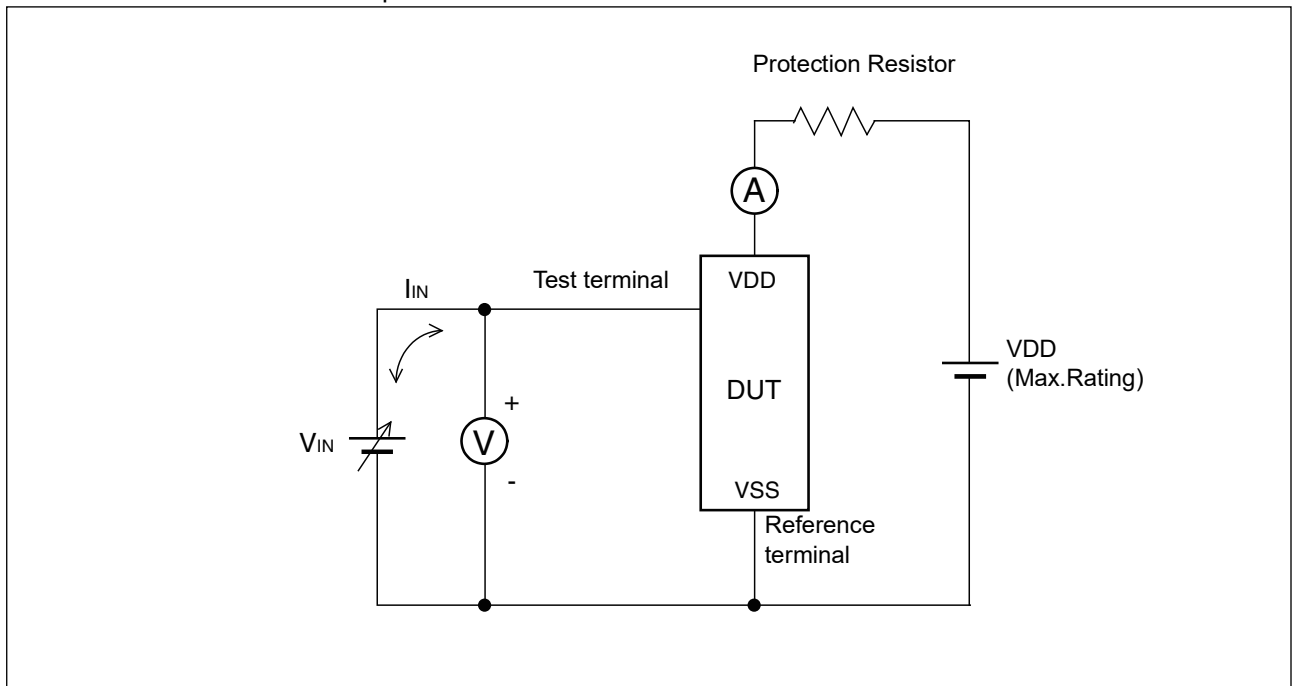
## ■ NOTES ON USE

We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.

## ■ ESD AND LATCH-UP

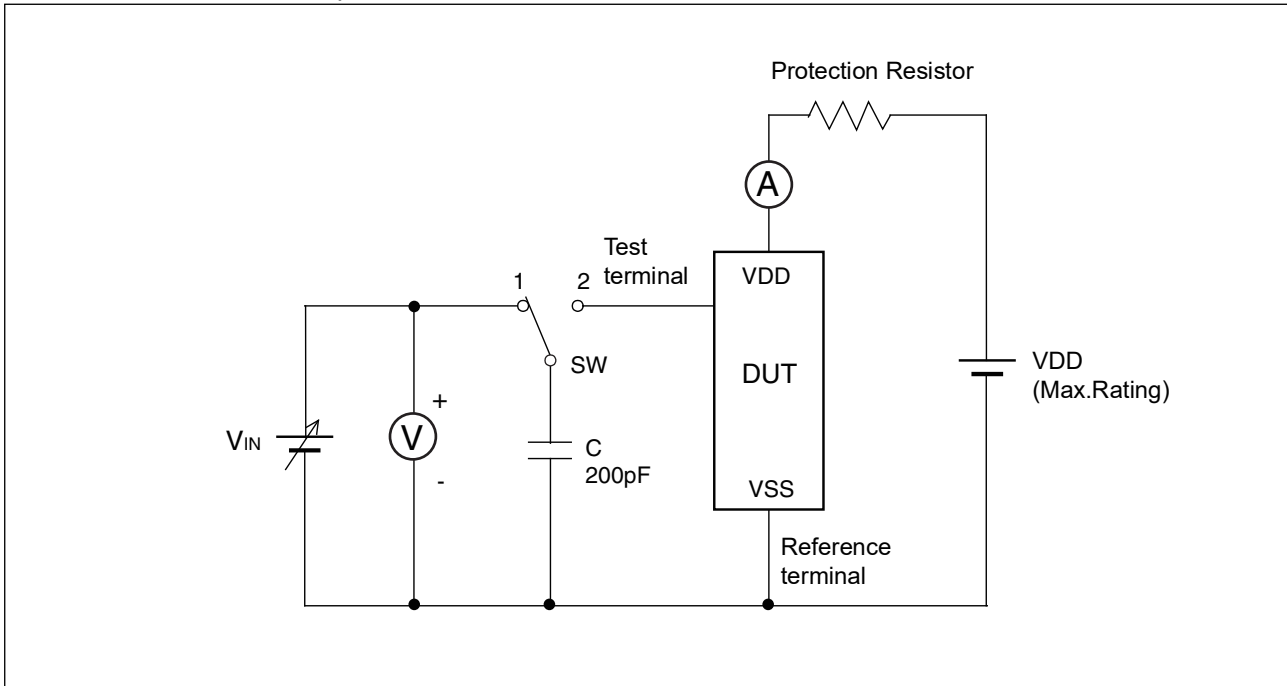
Test	DUT	Value
ESD HBM (Human Body Model) JESD22-A114 compliant	MB85R1001ANC-GE1	$\geq  2000 \text{ V} $
ESD MM (Machine Model) JESD22-A115 compliant		$\geq  200 \text{ V} $
ESD CDM (Charged Device Model) JESD22-C101 compliant		$\geq  1000 \text{ V} $
Latch-Up (I-test) JESD78 compliant		—
Latch-Up ( $V_{\text{supply}}$ overvoltage test) JESD78 compliant		—
Latch-Up (Current Method) Proprietary method		$\geq  300 \text{ mA} $
Latch-Up (C-V Method) Proprietary method		—

- Current method of Latch-Up Resistance Test



Note : The voltage  $V_{\text{IN}}$  is increased gradually and the current  $I_{\text{IN}}$  of 300 mA at maximum shall flow. Confirm the latch up does not occur under  $I_{\text{IN}} = \pm 300 \text{ mA}$ . In case the specific requirement is specified for I/O and  $I_{\text{IN}}$  cannot be 300 mA, the voltage shall be increased to the level that meets the specific requirement.

• C-V method of Latch-Up Resistance Test



Note : Charge voltage alternately switching 1 and 2 approximately 2 sec interval. This switching process is considered as one cycle.  
Repeat this process 5 times. However, if the latch-up condition occurs before completing 5 times, this test must be stopped immediately.

## ■ REFLOW CONDITIONS AND FLOOR LIFE

[ JEDEC MSL ] : Moisture Sensitivity Level 3 (IPC/JEDEC J-STD-020E)

## ■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES

This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

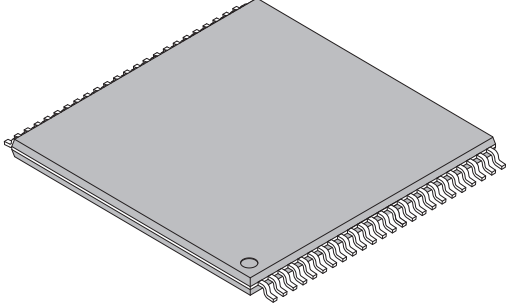
# MB85R1001A

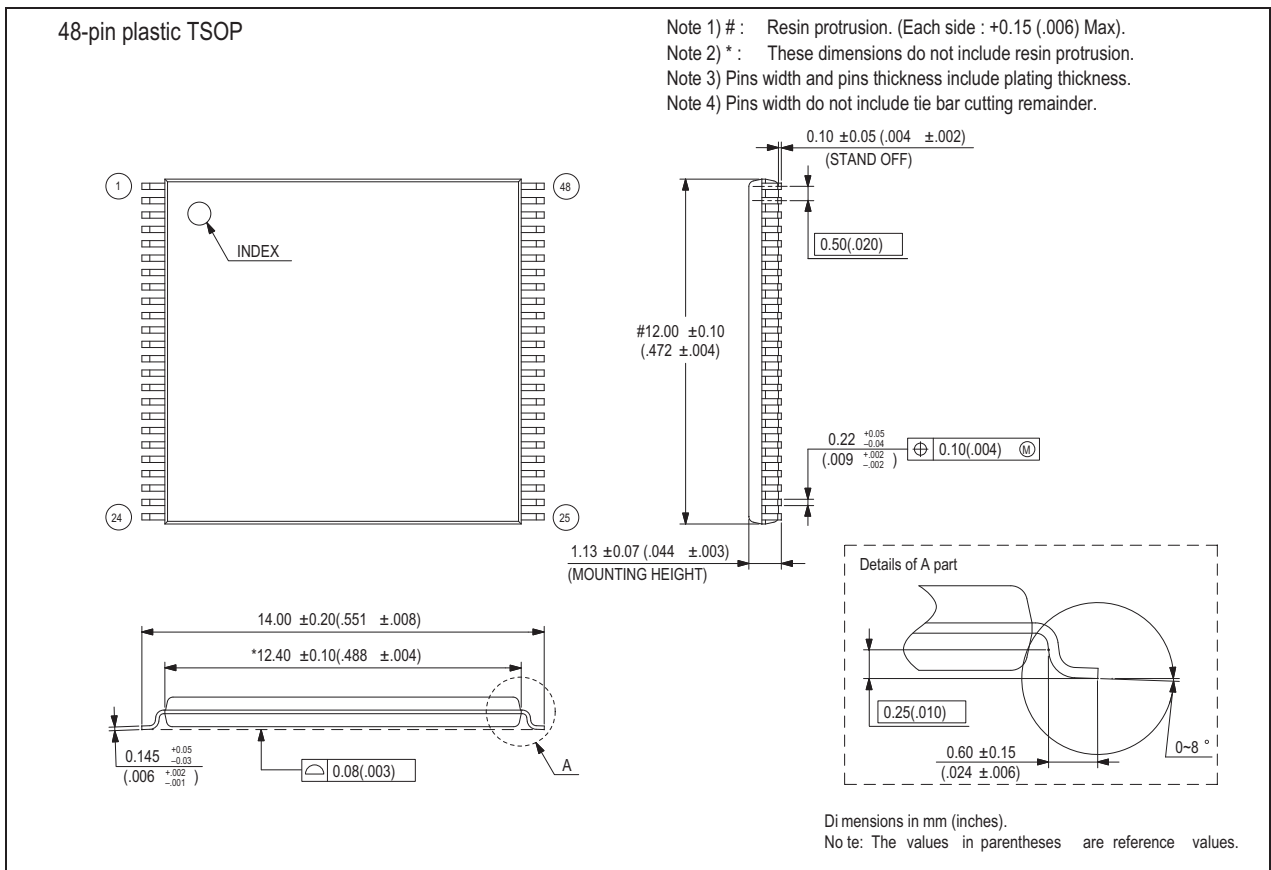
## ■ ORDERING INFORMATION

Part Number	Package	Shipping form	Minimum shipping quantity
MB85R1001ANC-GE1	48-pin plastic TSOP	Tray	—*

\*: Please contact our sales office about minimum shipping quantity.

## ■ PACKAGE DIMENSIONS

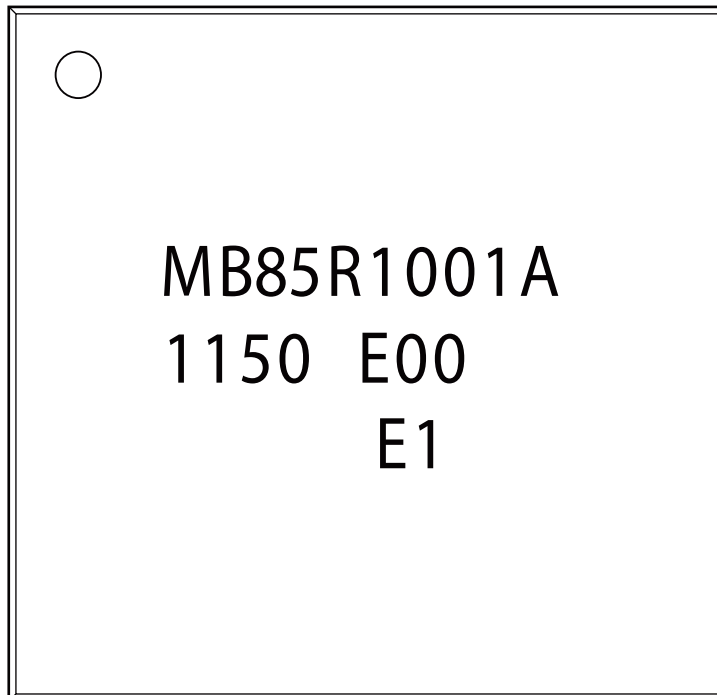
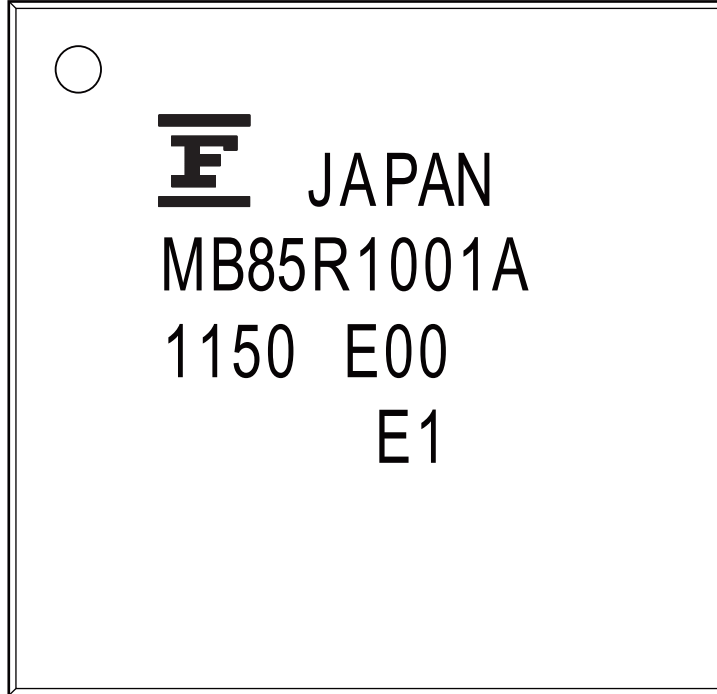
<p>48-pin plastic TSOP</p>  <p>MB85R1001ANC-GE1</p>	Lead pitch	0.50 mm
	Package width × package length	12.00 mm × 12.40 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.20 mm MAX



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## ■ MARKING(example)

[MB85R1001ANC-GE1]



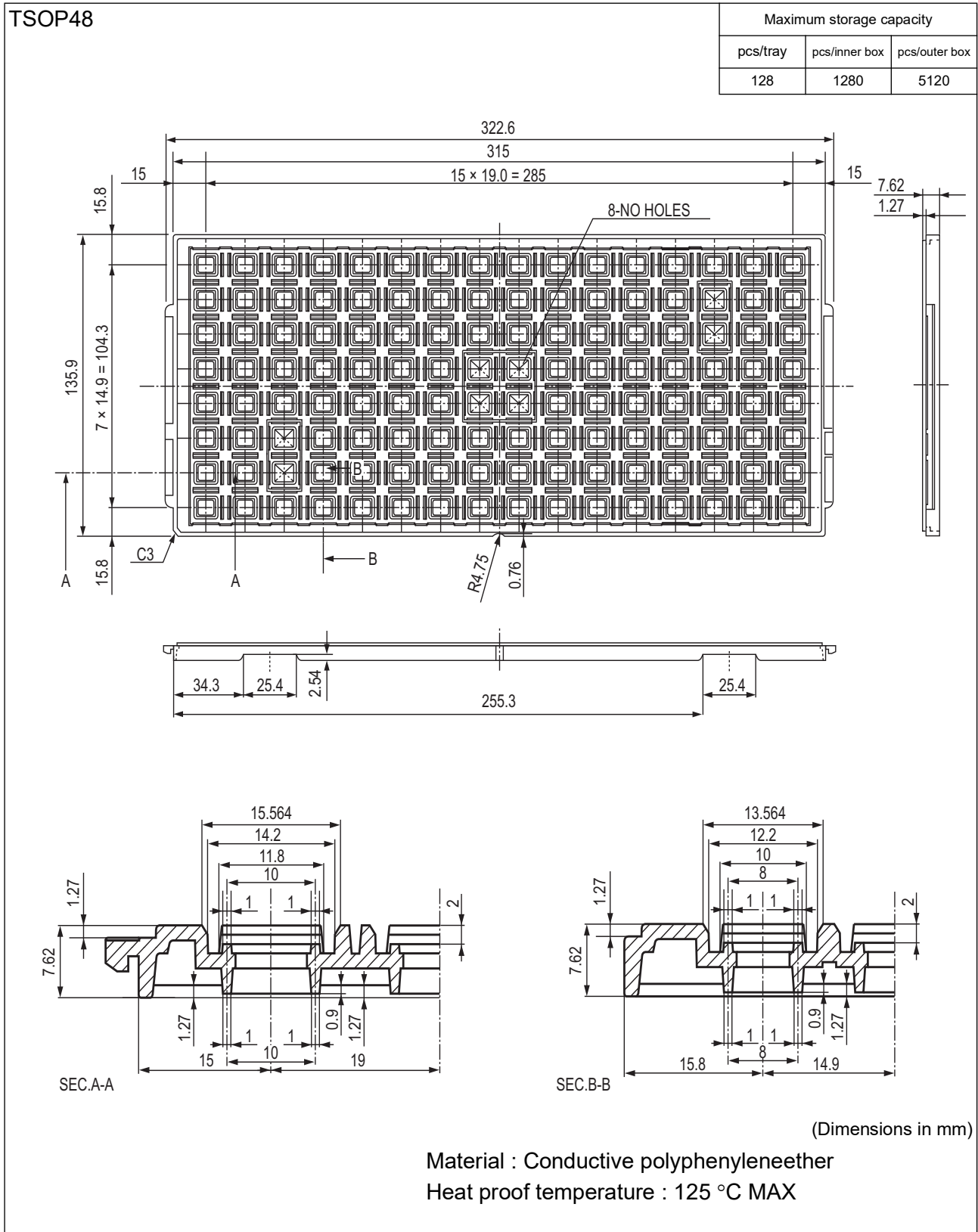
[TSOP 48]



## ■ SHIPPING FORM

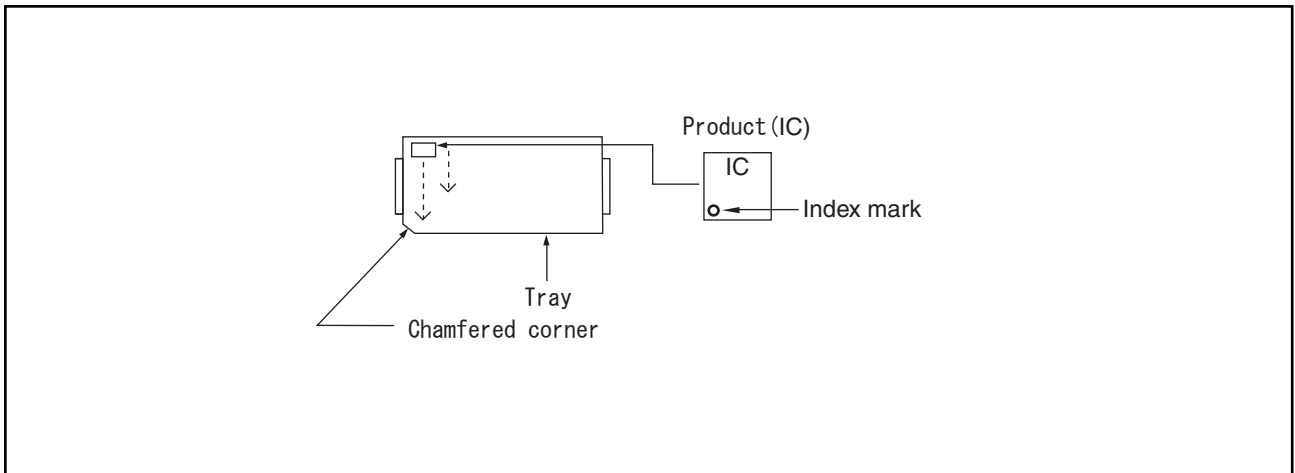
### 1. Tray

#### 1.1 Tray Dimensions



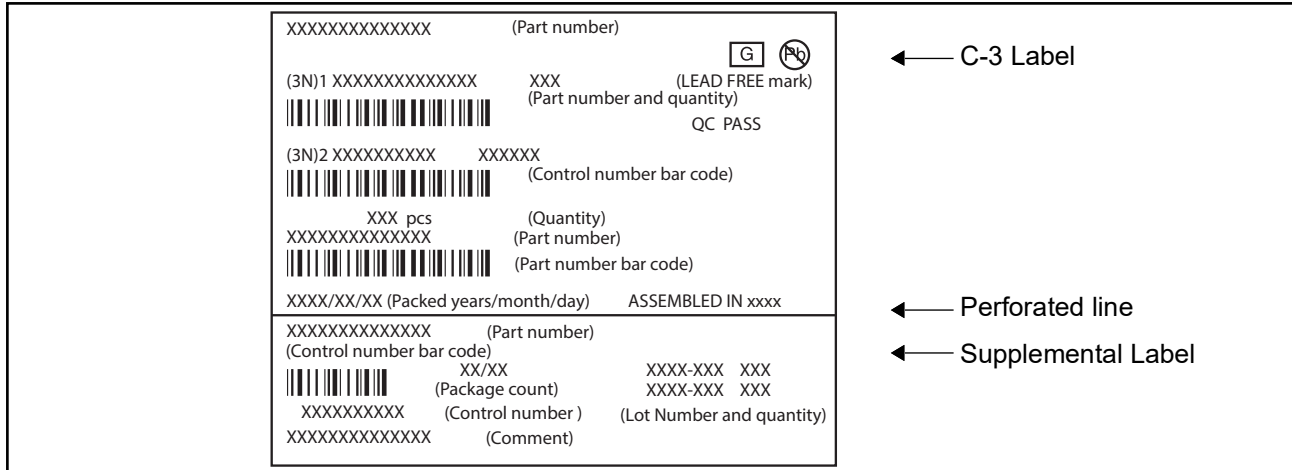
# MB85R1001A

## 1.2 IC orientation



## 1.3 Product label indicators

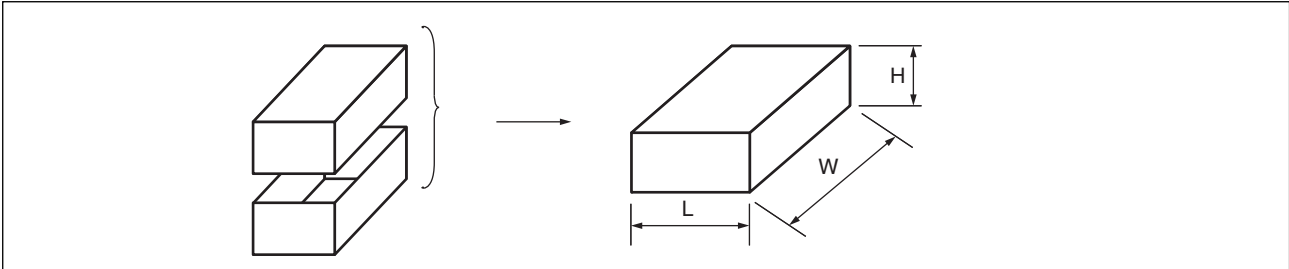
**Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)  
[C-3 Label (50mm x 100mm) Supplemental Label (20mm x 100mm)]**



# MB85R1001A

## 1.4 Dimensions for Containers

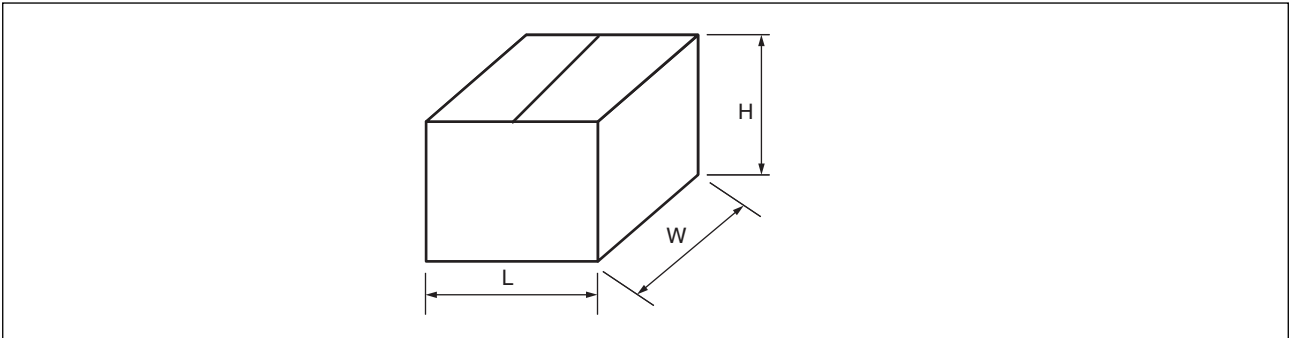
### (1) Dimensions for inner box



L	W	H
165	360	75

(Dimensions in mm)

### (2) Dimensions for outer box



L	W	H
355	385	195

(Dimensions in mm)

## ■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

Page	Section	Change Results
16	MARKING	New marking format is added.

# MB85R1001A

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