Analog Reinvented

ES9290

32-bit Stereo Channel High Performance CODEC

Product Datasheet

The SABRE® ES9290 is a synchronous stereo analog-to-digital (A/D) and digital-to-analog (D/A) CODEC targeted for professional audio interfaces such as Professional Audio Interfaces, Live stream media, High-quality microphones, professional DAW (Digital Audio Workstation) Audio Recording, and Active speakers.

The ES9290 is a cost-effective solution that has 2 integrated ADCs & DACs which use ESS' patented Hyperstream® IV Architecture, which delivers unprecedented audio sound quality and specifications, including a DNR of +116dB and a THD+N of -110dB/-108dB (DAC/ADC) per channel. A direct monitoring path is also provided with very low latency.

The SABRE CODEC supports synchronous I²S master/slave, and TDM input and outputs.

The ES9290 has built-in programmable gain amplifiers (PGAs) with a gain of up to +30dB, $2V_{rms}$ line driver buffers for simplification of BOM requirements, custom pre-programmed filters as well as high pass filters that are complementary to both ADC & DAC, and a Digital Full Biquad (DBQ) filter with many presets and for custom biquad filters.

The ES9290 ADCs have an Ultra-Low noise floor bandwidth of 200kHz. This bandwidth is up to 10 times wider than the competition.

Low latency Direct Monitoring and stereo ADC/DAC mixing are new advanced features.

FEATURE	DESCRIPTION
+116dB DNR per Ch, DAC & ADC -110dB/-108dB THD+N per Ch. (DAC/ADC) +122dB/+119dB DNR mono DAC/ADC differential -116dB THD+N mono DAC differential	High performance dynamic range and very low distortion for both ADCs & DACs
High Sample Rates	Up to 768kHz (in 64FS mode)
Customizable Filter Characteristics	Presets of digital optimal filters for ADC & DAC, and a DBQ for High Pass Filters and RIAA filters that are customizable
Multiple I/O Formats Available	I²S & TDM inputs/outputs are available, TDM daisy chain is supported
I²C, SPI, and Hardware interface control	Configured by microcontroller or other I²C/SPI source, or pins through Hardware Mode for simplification of control
Direct Monitoring	Low Latency direct monitoring
Programmable Input Amplifies (PGA)	PGA frontend with gain of +0 to +30dB in +3dB steps with 5kΩ input impedance
Digital Volume Control (I²C/SPI) Digital Gain Control (I²C/SPI)	-127 to +6dB in increments of +0.5dB +0 to +42dB in increments of +6dB for creating maximum gain
Integrated DAC Line Driver	Simplifying BOM requirements for the DAC output stage
Programmable MICBIAS	Programmable Microphone BIAS for Analog microphone support
Integrated Analog PLL	Reduces need for additional clocks
Ultra-Low Noise Floor Bandwidth on ADC	200kHz bandwidth enabling higher resolution at higher sample rates
Integrated low noise reference regulators	Reduced BOM cost, PCB area and improved DNR
Low Power Consumption	Simplifies power supply design
Low Pin Count Packaging	5mm x 5mm 40 pin QFN

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- Professional Digital Audio Workstation (DAW) Audio Recording
- Very High-Quality Microphones
- Live Stream Media
- Professional Audio Interfaces
- Powered (Active) Speakers

Functional Block Diagram

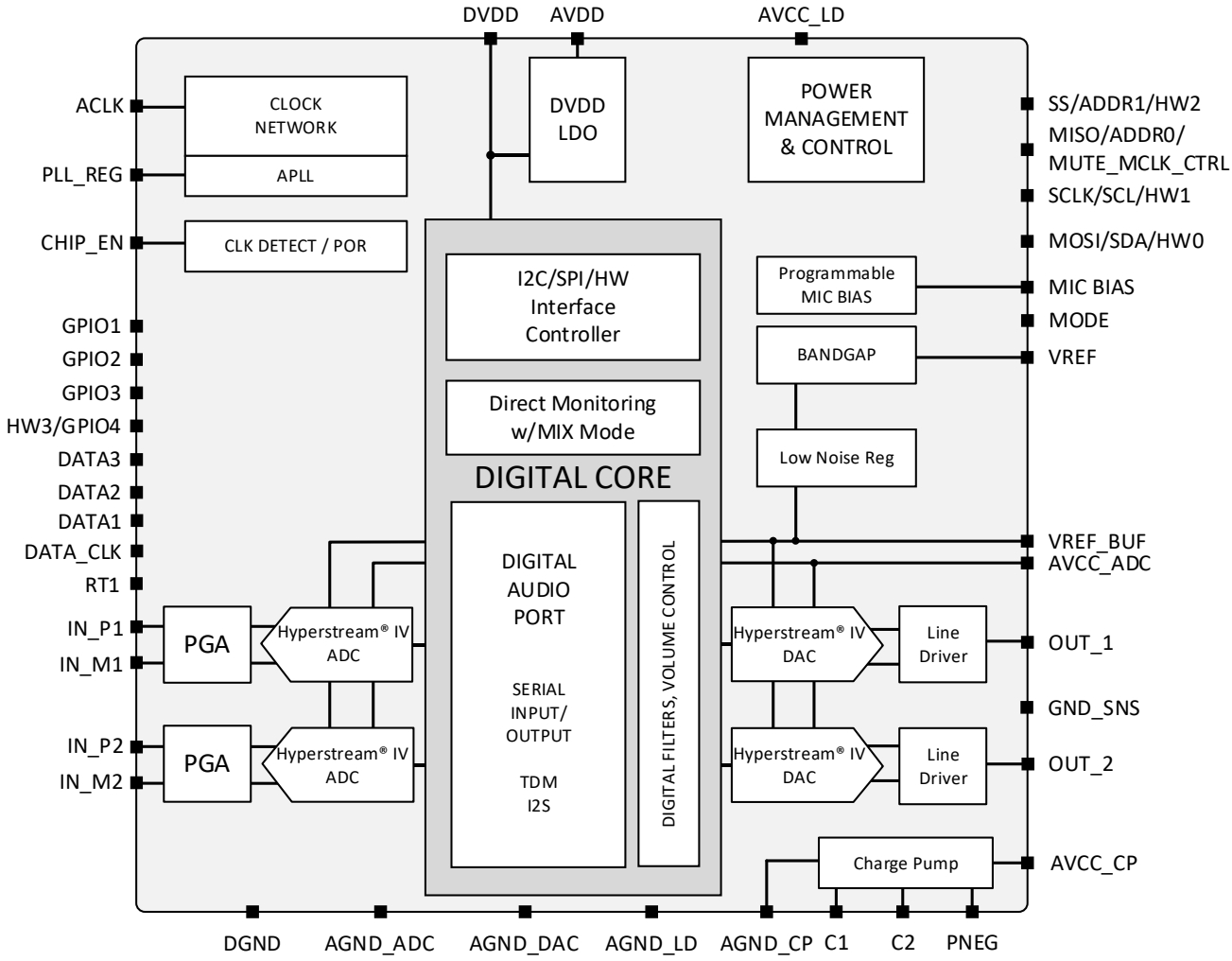


Figure 1 - ES9290 Block Diagram

ES9290 Package

40 QFN Pinout

(Pin 41 is QFN package pad, see package dimensions)

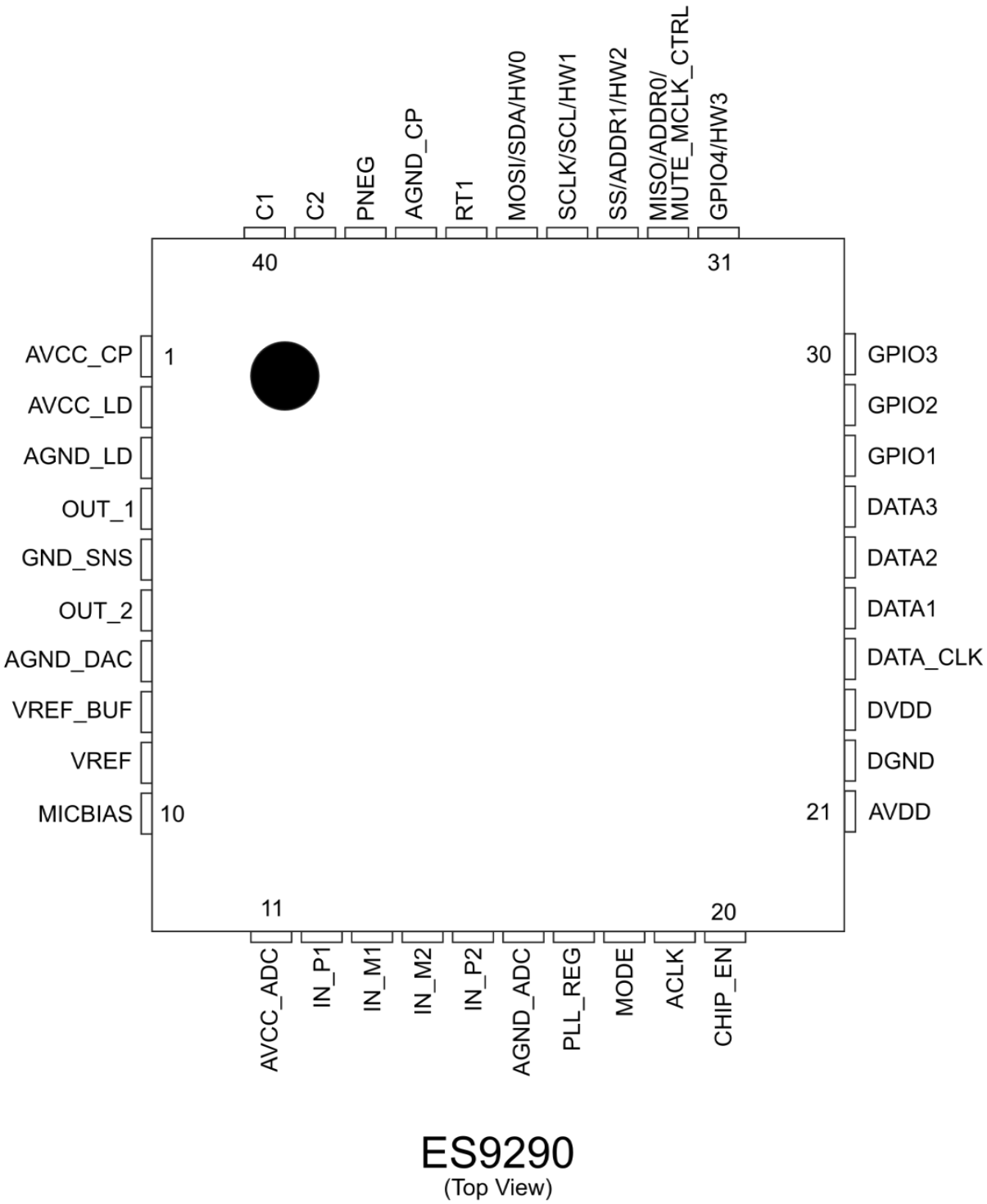


Figure 2 - 40 QFN Pinout

40 QFN Pin List

Pin	Name	Pin Type	Reset State	Pin Description
1	AVCC_CP	Power	Power	3.3V Supply for Charge Pump
2	AVCC_LD	Power	Power	3.3V Supply for Line Driver
3	AGND_LD	Ground	Ground	Analog Ground for Line Driver
4	OUT_1	A O	Ground	Line Driver Output 1
5	GND_SNS	A I/O	-	Line Driver Ground Sense
6	OUT_2	A O	Ground	Line Driver Output 2
7	AGND_DAC	Ground	Ground	Analog Ground for DAC
8	VREF_BUF	A I/O	P/D	Low Noise Supply for DAC/ADC, internally generated
9	VREF	A I/O	P/D	Low Noise Voltage Reference, internally generated
10	MICBIAS	A I/O	P/D	Low Noise Supply for Microphone Bias, internally generated
11	AVCC_ADC	Power	Power	3.3V Supply for ADC
12	IN_P1	A I	HiZ	ADC Channel 1 Differential Positive (+) Input
13	IN_M1	A I	HiZ	ADC Channel 1 Differential Negative (-) Input
14	IN_M2	A I	HiZ	ADC Channel 2 Differential Negative (-) Input
15	IN_P2	A I	HiZ	ADC Channel 2 Differential Positive (+) Input
16	AGND_ADC	Ground	Ground	Analog Ground for ADC
17	PLL_REG	A I/O	P/D	Low Noise Supply for PLL, internally generated
18	MODE	D I/O	HiZ	I²C/SPI Control Selection or HW Mode
19	ACLK	Clock I	HiZ	Clock Input
20	CHIP_EN	D I/O	D I/O	Active-High Chip Enable (Defines Reset State)
21	AVDD	Power	Power	3.3V Supply for Digital I/O
22	DGND	Ground	Ground	Digital Ground for Digital Core
23	DVDD	A I/O	P/D	1.2V Supply for Digital Core, internally generated
24	DATA_CLK	D I/O	HiZ	Serial Data Clock Pin
25	DATA1	D I/O	HiZ	Serial DATA1
26	DATA2	D I/O	HiZ	Serial DATA2
27	DATA3	D I/O	HiZ	Serial DATA3
28	GPIO1	D I/O	HiZ	General I/O 1
29	GPIO2	D I/O	HiZ	General I/O 2
30	GPIO3	D I/O	HiZ	General I/O 3
31	GPIO4	D I/O	HiZ	General I/O 4
	HW3	D I/O	HiZ	Hardware 3 interface pin, controlled by MODE
32	MISO	D I/O	HiZ	SPI Main In Sub Out pin, controlled by MODE
	ADDR0			I²C Address 0 pin, controlled by MODE
	MUTE_MCLK_CTRL			Hardware Mute Control pin, controlled by MODE
33	SS	D I/O	HiZ	SPI Slave Select pin, controlled by MODE
	ADDR1			I²C Address 1 pin, controlled by MODE

	HW2			Hardware 2 interface pin, controlled by MODE
34	SCLK	D I/O	HiZ	SPI Serial Clock pin, controlled by MODE
	SCL			I²C Serial Clock pin, controlled by MODE
	HW1			Hardware 1 interface pin, controlled by MODE
35	MOSI	D I/O	HiZ	SPI Main Out Sub In pin, controlled by MODE
	SDA			I²C Serial Data pin, controlled by MODE
	HW0			Hardware 0 interface pin, controlled by MODE
36	RT1	D I/O	HiZ	Reserved. Must be connected to GND for normal operation.
37	AGND_CP	Ground	Ground	Analog Ground for Charge Pump
38	PNEG	A I/O	Ground	-3.3V Supply for Line Driver, internally generated.
39	C2	A I/O Neg	Ground	Charge Pump negative flying capacitor pin
40	C1	A I/O	Ground	Charge Pump positive flying capacitor pin
41	Package Pad[1]	-	-	Not electrically connected, used for heat dissipation. Connect to DGND.

Table 1 - 40 QFN Pin List

*Note: A = Analog, D = Digital, I/O = Digital Input/Output, P/D = Power Down

[1] Pin 41 is the package pad. See 40 QFN package dimensions for sizing. Connect to DGND.

Feature List

Configuration Modes

The ES9290 has 4 control programming modes which are controlled by the state of the MODE pin (Pin 18).

MODE PIN	Configuration
0	I²C Interface
Pull 0	HW control mode (see Hardware Mode Table)
Pull 1	HW control mode (see Hardware Mode Table)
1	SPI Interface

Table 2 - Mode Pin Configuration Options

Design Information

Hardware pins can be configured in 4 different ways. Each pin can be tied-high (1), pulled-high (Pull 1), pulled-low (Pull 0), or tied-low (0). HW0 and HW1 pins are always tied-high or tied-low. These 4 options also apply to MUTE_CTRL.

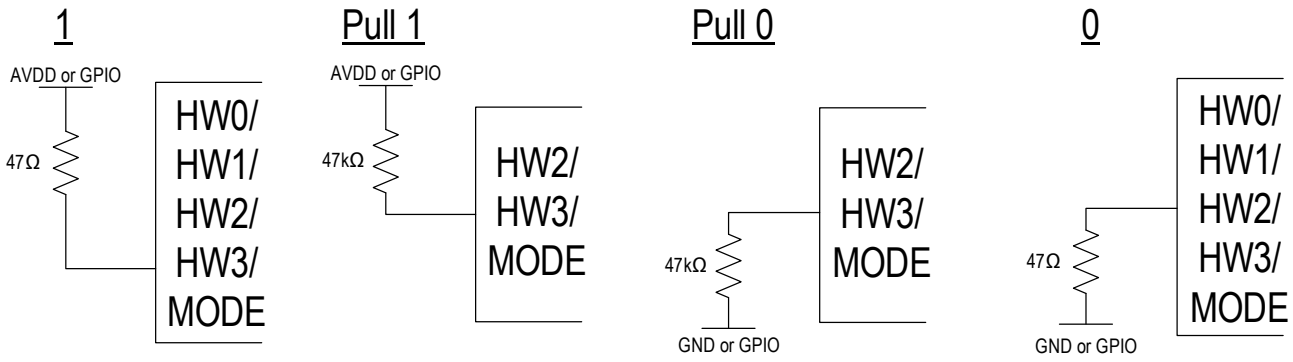


Figure 3 - Example Hardware Mode Pin Configurations

Software Mode

The ES9290 supports I²C or SPI serial communication in software mode. There are two types of registers, read/write registers and read-only registers. Software modes are set when the MODE pin is a 0 (0V) for I²C or a 1 (AVDD) for SPI.

A system clock is not required to read and write registers.

I²C Slave Interface Commands

- MODE (Pin 18) – 0 V
- Connect per I²C standard
  - SDA (Pin 35)
  - SCL (Pin 34)
  - ADDR0 (Pin 32)
  - ADDR1 (Pin 33)

I²C Address	ADDR1	ADDR0
0x30	GND	GND
0x32	GND	AVDD
0x34	AVDD	GND
0x36	AVDD	AVDD

Table 3 - I²C Addresses

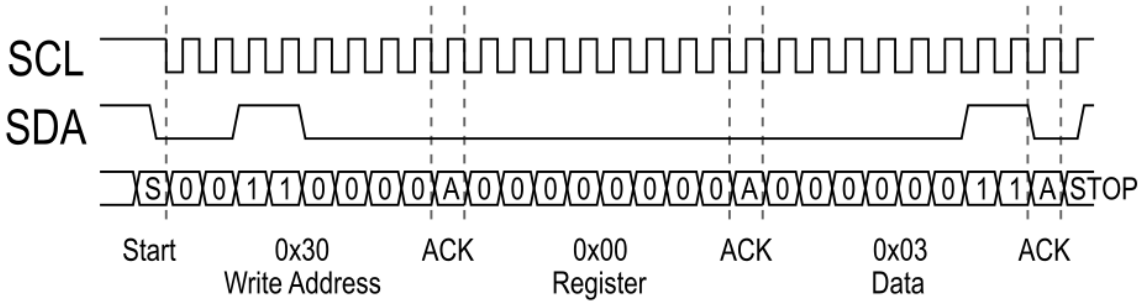


Figure 4 - I²C Write Example

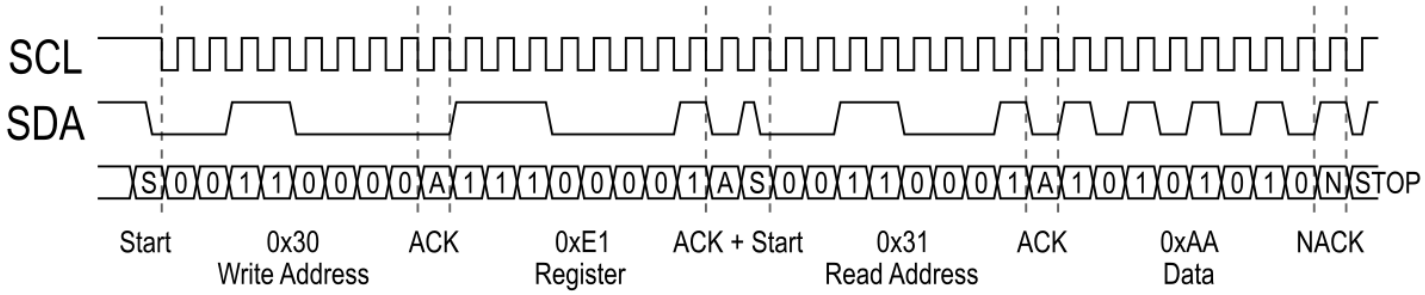


Figure 5 - I²C Read Example

Note: CHIP_ID is 0xAA in Register 225 (0xE1)

I²C Slave Interface Timing

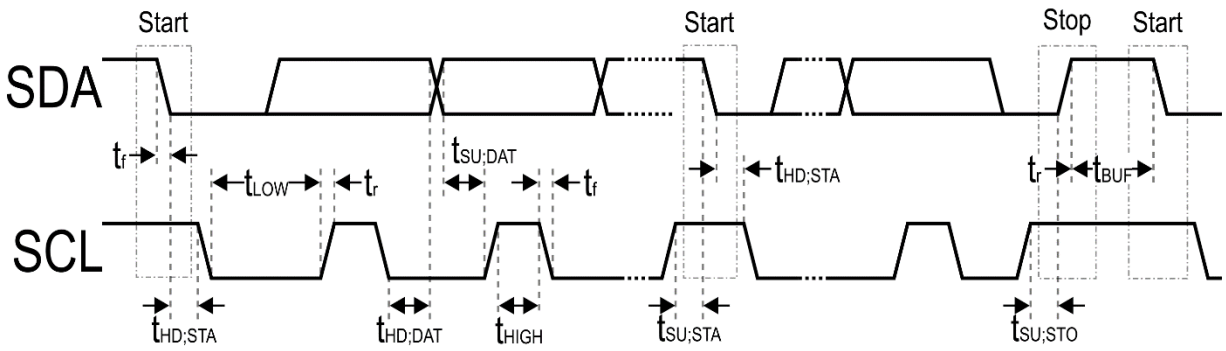


Figure 6 - I²C Slave Control Interface Timing

Parameter	Symbol	CLK Constraint	Standard-Mode		Fast-Mode		Unit
			MIN	MAX	MIN	MAX	
SCL Clock Frequency	f_{SCL}	< CLK/20	0	100	0	400	kHz
START condition hold time	$t_{HD;STA}$		4.0	-	0.6	-	µs
LOW period of SCL	t_{LOW}	>10/CLK	4.7	-	1.3	-	µs
HIGH period of SCL (>10/CLK)	t_{HIGH}	>10/CLK	4.0	-	0.6	-	µs
START condition setup time (repeat)	$t_{SU;STA}$		4.7	-	0.6	-	µs
SDA hold time from SCL falling - All except NACK read - NACK read only	$t_{HD;DAT}$		0 2/CLK	-	0 2/CLK	-	µs s
SDA setup time from SCL rising	$t_{SU;DAT}$		250	-	100	-	ns
Rise time of SDA and SCL	t_r		-	1000	-	300	ns
Fall time of SDA and SCL	t_f		-	300	-	300	ns
STOP condition setup time	$t_{SU;STO}$		4	-	0.6	-	µs
Bus free time between transmissions	t_{BUF}		4.7	-	1.3	-	µs
Capacitive load for each bus line	C_b		-	400	-	400	pF

Table 4 - I²C Slave Interface Timing Definitions

SPI Slave Interface Commands

- MODE (Pin 18) - AVDD
- Connect per SPI standard
  - MOSI (Pin 35)
  - SCLK (Pin 34)
  - SS (Pin 33)
  - MISO (Pin 32)

SPI Command	First Byte
Write	0x03
Read	0x01

Table 5 - SPI Commands

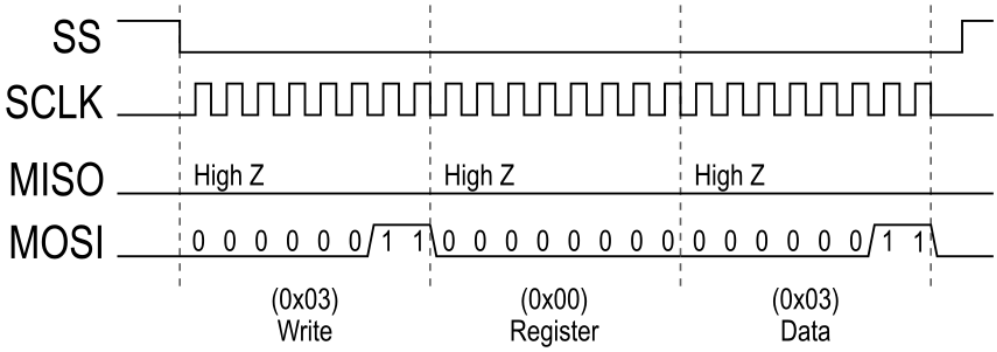


Figure 7 - SPI Single Byte Write

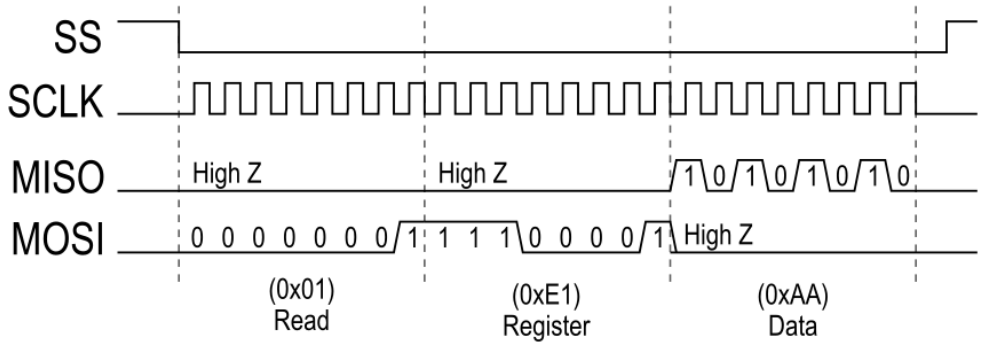


Figure 8 - SPI Single Byte Read

Note: CHIP_ID is 0xAA in Register 225 (0xE1)

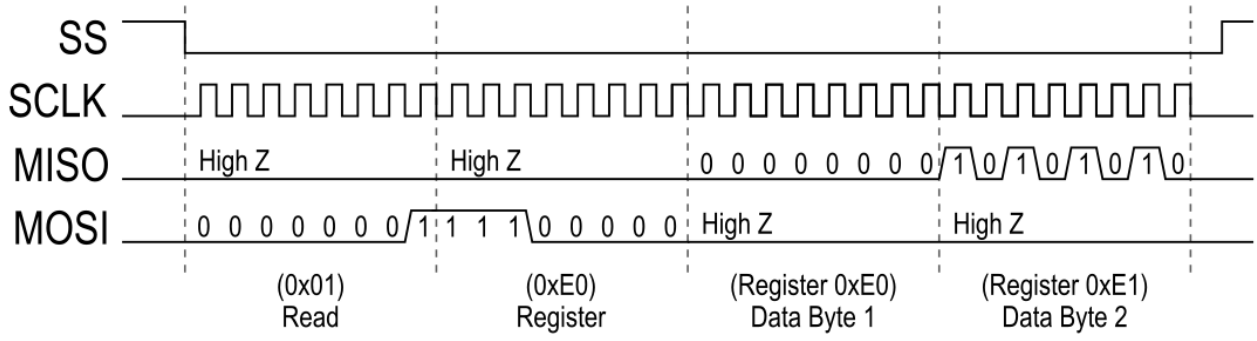


Figure 9 - SPI Multi Byte Read

SPI Slave Interface Timing

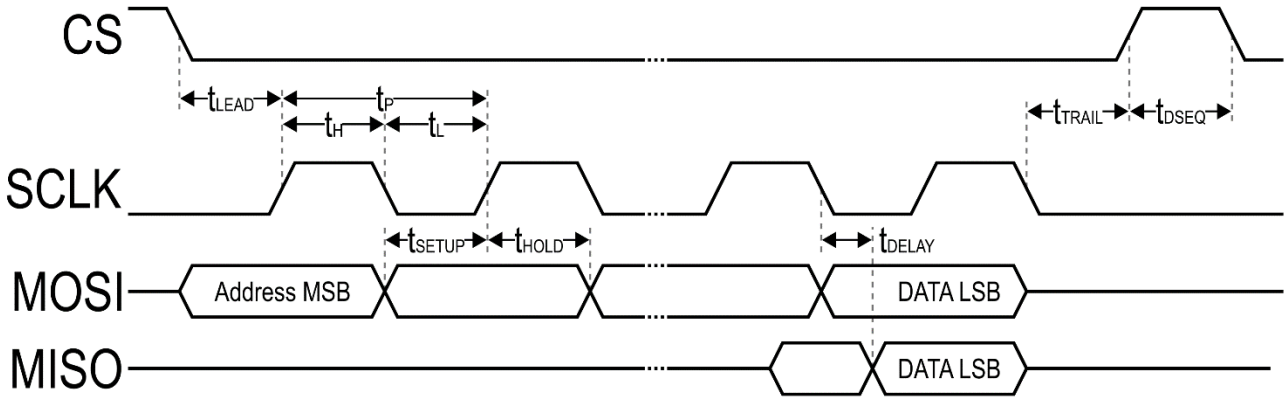


Figure 10 - SPI Slave Interface Timing

Parameter	Symbol	Min [ns]	Max [ns]
CS Lead Time (SCLK rising edge)	t_{LEAD}	4	-
CS Trail Time (SCLK falling edge)	t_{TRAIL}	4	-
MOSI Data Setup Time	t_{SETUP_MOSI}	-36	-
MOSI Data Hold Time	t_{HOLD_MOSI}	60	-
SCLK-MISO Delay Time	t_{DELAY_MISO}	-	74
SCLK Period	t_{P_SCLK}	122	-
SCLK High Pulse Duration	t_{H_SCLK}	94	-
SCLK Low Pulse Duration	t_{L_SCLK}	60	-
Sequential Transfer Delay	t_{DSEQ}	38	-

Table 6 - SPI Slave Interface Timing

Hardware Mode

The ES9290 has pre-configured modes that can be set with external pin configuration. These modes configure the CODEC for different input/output serial data rates and set the muting. Hardware modes also support stereo digital PDM microphones as inputs. Each hardware mode pin has 4 states that can be found in Design Information.

These modes are set with pins:

- MODE (Pin 18)
- HW0 (Pin 35)
- HW1 (Pin 34)
- HW2 (Pin 33)
- HW3 (Pin 31)

Input Select

The ES9290 supports an analog input signal and a digital input from a PDM microphone. In all Hardware Modes, HW3 (Pin 31) sets the input mode between the analog PGA or digital PDM Decoder.

Pin	State	Input	Conditions
HW3/GPIO4	0	Analog - ADC	Daisy Chain
	Pull 0		Parallel
	Pull 1	Digital - PDM	-
	1		-

Table 7 - Input Mode Selection with HW3 in Hardware Mode

Mute Control

Set MUTE_MCLK_CTRL (Pin 32) to mute the output while in Hardware Mode:

MUTE_MCLK_CTRL (Pin 32)	Mute Condition	MCLK
0	Mute	24.576MHz
1	Unmute	24.576MHz
Pull 0	Mute	49.152MHz
Pull 1	Unmute	49.152MHz

Table 8 - Mute Control in Hardware Mode

Note: If MUTE_MCLK_CTRL (Pin 32) is set incorrectly, it may seem that the ADC or DAC has higher noise than specified.

Note: If using the APLL as the MCLK source, MUTE_MCLK_CTRL must be set to 0 or 1.

GPIO Functions in Hardware Mode

The ES9290 supports specific functions through the GPIO pins in hardware modes. The tables below show the available controls in hardware modes. These include PGA gain, Mic Bias enable, and choosing between PDM or analog input for the ADC. These functions are supported in hardware modes.

HW3 State	Supported HW Modes	GPIO #	Input/Output	HW Mode Function
0	0 - 15	GPIO1	-	High Z
		GPIO2	-	High Z
0	16 - 31	GPIO1	Output	DAC_TSD
		GPIO2	Input	ADC_RSD
Pull 0	All	GPIO1	Input	PGA Gain & Mic Bias
		GPIO2		

Table 9 - Analog ADC GPIO Functions in Hardware Mode

HW3 State	Supported HW Modes	GPIO #	Input/Output	HW Mode Function
Pull 1 / 1	All	GPIO1	Input	PDM_DATA
		GPIO2	Output	PDM_CLK

Table 10 - Digital PDM GPIO Functions in Hardware Mode

[GPIO2, GPIO1]	PGA Gain	Mic Bias
2'b00	+0dB	Disabled
2'b01	+18dB	Enabled (2.85V)
2'b10	+24dB	Enabled (2.85V)
2'b11	+30dB	Enabled (2.85V)

Table 11 - PGA Gain and Mic Bias in Hardware Mode

GPIO3	ADC DC Block
1'b0	Disabled
1'b1	Enabled

Table 12 - ADC DC Block in Hardware Mode

Hardware Mode Pin Configuration

HW Mode	Description	FS [kHz]	BCK [MHz]	MODE	HW2	HW1	HW0
32-bit PCM Master Modes (Ext MCLK)							
0	I²S with Ext MCLK	MCLK/128	MCLK/2 (64*FS)	Pull 0	0	0	0
1	I²S with Ext MCLK	MCLK/256	MCLK/4 (64*FS)	Pull 0	0	0	1
2	I²S with Ext MCLK	MCLK/512	MCLK/8 (64*FS)	Pull 0	0	1	0
3	I²S with Ext MCLK	MCLK/1024	MCLK/16 (64*FS)	Pull 0	0	1	1
4	LJ with Ext MCLK	MCLK/128	MCLK/2 (64*FS)	Pull 0	Pull 0	0	0
5	LJ with Ext MCLK	MCLK/256	MCLK/4 (64*FS)	Pull 0	Pull 0	0	1
6	LJ with Ext MCLK	MCLK/512	MCLK/8 (64*FS)	Pull 0	Pull 0	1	0
7	LJ with Ext MCLK	MCLK/1024	MCLK/16 (64*FS)	Pull 0	Pull 0	1	1
32-bit PCM Slave Modes (PLL or Ext MCLK)							
8	I²S with Ext MCLK, Auto FS	8 ≤ FS ≤ 384	64*FS	Pull 0	Pull 1	0	0
9	I²S with PLL from BCK	48	3.072	Pull 0	Pull 1	0	1
10	I²S with PLL from BCK	96	6.144	Pull 0	Pull 1	1	0
11	I²S with PLL from BCK	192	12.288	Pull 0	Pull 1	1	1
12	LJ with Ext MCLK	8 ≤ FS ≤ 384	64*FS	Pull 0	1	0	0
13	LJ with PLL from BCK	48	3.072	Pull 0	1	0	1
14	LJ with PLL from BCK	96	6.144	Pull 0	1	1	0
15	LJ with PLL from BCK	192	12.288	Pull 0	1	1	1
32-bit TDM LJ Slave Modes, Autodetect FS & CH Num							
16	TDM LJ Channel Slots = 1,2	8 ≤ FS ≤ 384	Auto (64FS, 128FS, 256FS, 512FS, 1024FS)	Pull 1	0	0	0
17	TDM LJ Channel Slots = 3,4	8 ≤ FS ≤ 384	Auto (128FS, 256FS, 512FS, 1024FS)	Pull 1	0	0	1
18	TDM LJ Channel Slots = 5,6	8 ≤ FS ≤ 192	Auto (256FS, 512FS, 1024FS)	Pull 1	0	1	0
19	TDM LJ Channel Slots = 7,8	8 ≤ FS ≤ 192	Auto (256FS, 512FS, 1024FS)	Pull 1	0	1	1
20	TDM LJ Channel Slots = 9,10	8 ≤ FS ≤ 96	Auto (512FS, 1024FS)	Pull 1	Pull 0	0	0
21	TDM LJ Channel Slots = 11,12	8 ≤ FS ≤ 96	Auto (512FS, 1024FS)	Pull 1	Pull 0	0	1
22	TDM LJ Channel Slots = 13,14	8 ≤ FS ≤ 96	Auto (512FS, 1024FS)	Pull 1	Pull 0	1	0
23	TDM LJ Channel Slots = 15,16	8 ≤ FS ≤ 96	Auto (512FS, 1024FS)	Pull 1	Pull 0	1	1
16-bit TDM LJ Slave Modes, Autodetect FS & CH Num							
24	TDM LJ Channel Slots = 1,2	8 ≤ FS ≤ 384	Auto (32FS, 64FS, 128FS, 256FS, 512FS)	Pull 1	Pull 1	0	0
25	TDM LJ Channel Slots = 3,4	8 ≤ FS ≤ 384	Auto (64FS, 128FS, 256FS, 512FS)	Pull 1	Pull 1	0	1
26	TDM LJ Channel Slots = 5,6	8 ≤ FS ≤ 192	Auto (128FS, 256FS, 512FS)	Pull 1	Pull 1	1	0
27	TDM LJ Channel Slots = 7,8	8 ≤ FS ≤ 192	Auto (128FS, 256FS, 512FS)	Pull 1	Pull 1	1	1
28	TDM LJ Channel Slots = 9,10	8 ≤ FS ≤ 96	Auto (256FS, 512FS)	Pull 1	1	0	0
29	TDM LJ Channel Slots = 11,12	8 ≤ FS ≤ 96	Auto (256FS, 512FS)	Pull 1	1	0	1
30	TDM LJ Channel Slots = 13,14	8 ≤ FS ≤ 96	Auto (256FS, 512FS)	Pull 1	1	1	0
31	TDM LJ Channel Slots = 15,16	8 ≤ FS ≤ 96	Auto (256FS, 512FS)	Pull 1	1	1	1

Table 13 - Hardware Mode Pin Configurations

Recommended Hardware Mode Setup Sequence

The Hardware Mode setup sequence is shown below with all hardware pins being defined after CHIP_EN is asserted.

Note: It is recommended that MUTE_MCLK_CTRL is set low until the HW mode is finalized and after CHIP_EN is asserted, then asserted last.

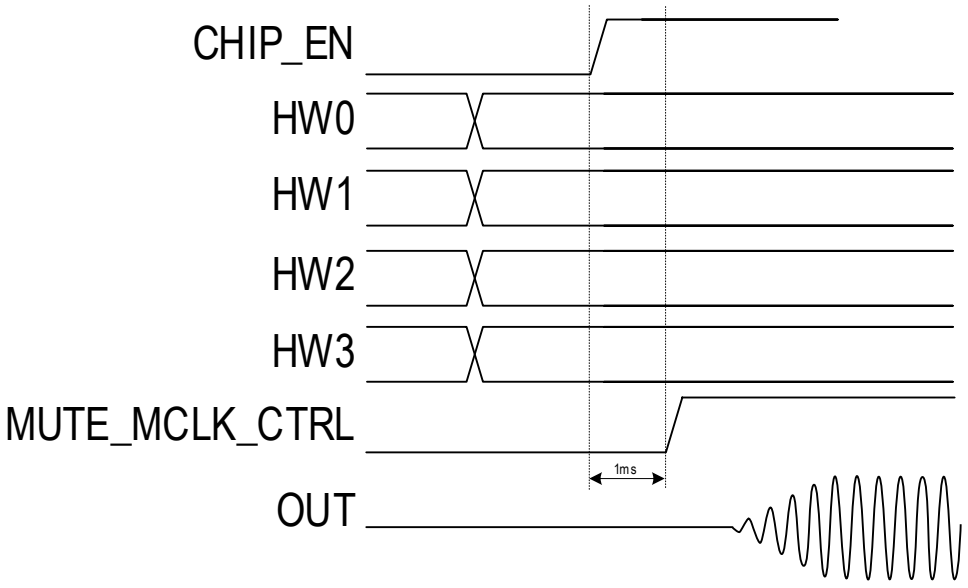


Figure 11 - Hardware Mode Startup Sequence

Digital Features

The ES9290 CODEC features an ADC Digital Signal Path and a DAC Digital Signal Path that can pass audio through both paths alongside monitoring the signal with Direct Monitoring.

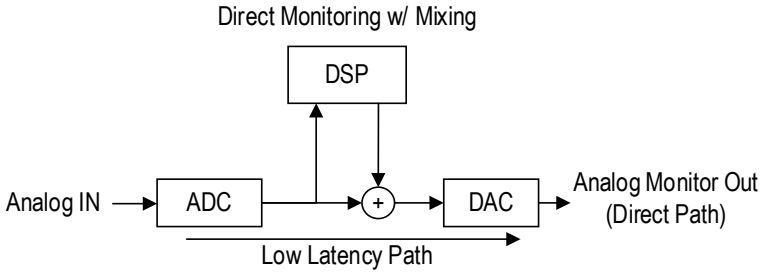


Figure 12 - Direct Monitoring Path

ADC Digital Signal Path

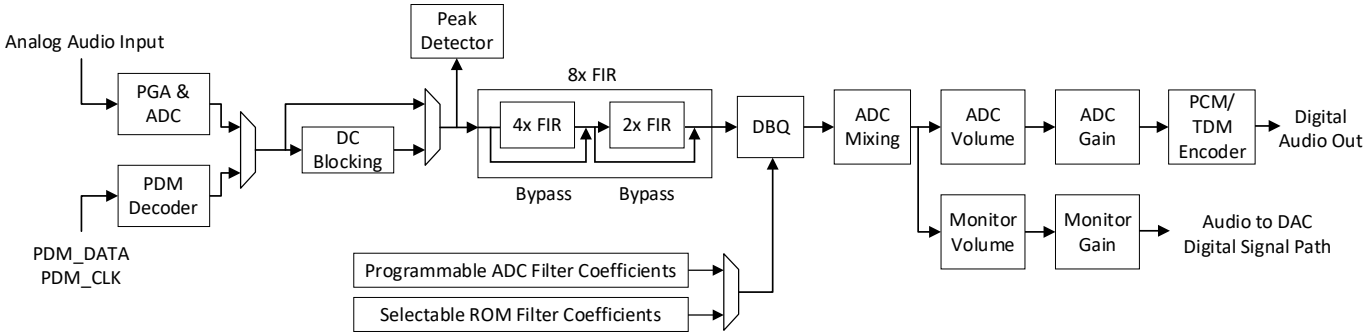


Figure 13 - ADC Digital Signal Path

PDM Decoder

The ES9290 can receive input audio from a PDM microphone using the integrated PDM decoder. To use the PDM signal in software mode, PDM_INPUT_SEL must be set. PDM is also supported in hardware modes. The PDM_DATA in input into GPIO1 and PDM_CLK is output through GPIO2.

Note: If Daisy Chain mode is enabled, PDM_DATA and PDM_CLK use GPIO3/4.

PDM Decoder Registers

- Register 66[4] PDM_PHASE
- Register 66[5] PDM_SAMPLE_EDGE
- Register 66[7] PDM_INPUT_SEL
- Register 67[6:0] MCLK_PDM_DIV

Daisy Chain Mode	PDM_DATA	PDM_CLK
Off	GPIO1	GPIO2
On	GPIO3	GPIO4

Table 14 - PDM Decoder Pins

DC Blocking

The integrated DC Blocking filter exhibits a high cutoff frequency (-3dB @ 0.25Hz).

DC Blocking Registers

- Register 65[6] CH1_DC_BLOCK_EN
- Register 65[6] CH2_DC_BLOCK_EN

Peak Detector

If the peak level of the ES9290 input rises above the programmed PEAK_THRESH_CHx value, the corresponding peak flag will be set. The level will decay at a rate based off the value of PEAK_DECAY_RATE. The peak detection can be toggled on or off using the PEAK_DETECT_CHx_EN registers. The peak can be read from the PEAK CHx READ registers and a flag will be set on the PEAK_FLAG_CHx registers. Normal flag registers will unset the flag once it is no longer asserted except the PEAK_FLAG_LAT_CHx registers which will stay set until it is cleared with INT_CLEAR_CHx_PEAK_LATCH.

GPIO pins can be configured to output the state of any peak flags or latched peak flags if STATUS_MASK_CHx_PEAK_DET or STATUS_MASK_CHx_PEAK_LATCH is set for the corresponding channel.

Peak Enable Registers

- Register 88[1:0] PEAK_DETECT_CHx_EN

Peak Flag GPIO Registers

- Register 18[1:0] STATUS_MASK_CHx_PEAK_LATCH
- Register 18[3:2] STATUS_MASK_CHx_PEAK_DET

Peak Flag and Read Registers

- Register 238-239 PEAK CH1 READ
- Register 240-241 PEAK CH2 READ
- Register 233[5:4] PEAK_FLAG_CHx
- Register 233[7:6] PEAK_FLAG_LAT_CHx
- Register 19[1:0] INT_CLEAR_CHx_PEAK_LATCH

Peak Decay Rate and Threshold Registers

- Register 89[4:0] PEAK_DECAY_RATE
- Register 90-91[7:0] PEAK_THRESH_CH1
- Register 90-91[15:8] PEAK_THRESH_CH2

$$N(t) = N_0 exp\left(\frac{-MCLK\_24M * t}{2^{decay\_rate+9}}\right)$$

$$N(t) = N_0 - \frac{20 * MCLK\_24M * t}{ln(10) * 2^{decay\_rate+9}}[dB]$$

$$\frac{dN}{dt} = -\frac{N * MCLK\_24M}{2^{decay\_rate+9}}[1/s]$$

ADC 8x FIR Filter

Selection of the 8x interpolation filter is chosen from 8 pre-programmed filter shapes. For more information on filters see the ADC: PCM Filter Latency section.

FIR Registers

- Register 64[7:5] ADC_FILTER_SHAPE

ADC Digital Biquad Filter

The ES9290 features a Digital Full Biquad (DBQ) filter for the ADC datapath. The filter comes with 23 preset filters and the ability to make a custom filter via user input coefficients.

The custom filter uses 5 coefficients to shape the filter: -A2, -A1, B2, B1, and B0.
The coefficients are signed 24-bit numbers.

ADC DBQ Filter Registers

- Register 48[4:0] ADC_DBQ_COEFF_SEL (preset filter selection)
- Register 48[7] ADC_DBQ_CLK_FAMILY_SEL
- Register 48[6] ADC_DBQ_80HZ_HPF_EN
- Register 48[5] ADC_DBQ_120HZ_HPF_EN
- Register 49-51 ADC PROG DBQ A2 COEFF
    - Note: Assigns -A2 to the register
- Register 52-54 ADC PROG DBQ A1 COEFF
    - Note: Assigns -A1 to the register
- Register 55-57 ADC PROG DBQ B2 COEFF
- Register 58-60 ADC PROG DBQ B1 COEFF
- Register 61-63 ADC PROG DBQ B0 COEFF

The DBQ is arranged in a transposed direct form 2 format.

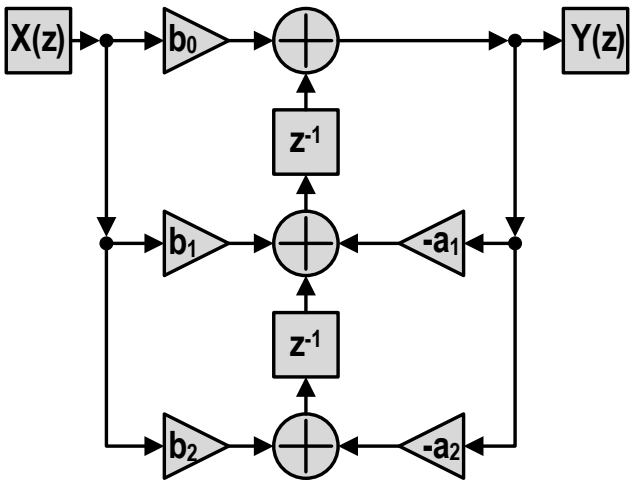


Figure 14 - ADC DBQ format

ADC Mixing

The ES9290 has the ability to mix the incoming ADC_CH1 data into ADC_CH2 and vice versa. The range of mixing is -∞dB (8'hFF) to 0dB (8'h00).

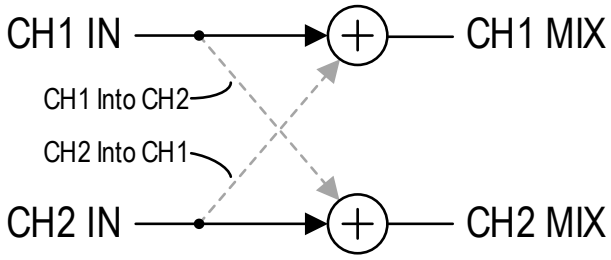


Figure 15 - ADC Mixing

ADC Mixing Registers

- Register 70 ADC MIX VOLUME CH1
- Register 71 ADC MIX VOLUME CH2

ADC Volume

The ADC Volume Control is intended for use during audio playback. Each channel can be digitally attenuated from +1dB to -126dB in 0.5dB steps. When a new volume level is set, the attenuation circuit will ramp softly to the new level at a rate specified in the VOLUME UP RAMP RATE and VOLUME DOWN RAMP RATE registers.

ADC Volume Registers

- Register 68 ADC VOLUME CH1
- Register 69 ADC VOLUME CH2
- Register 14 VOLUME UP RAMP RATE
- Register 15 VOLUME DOWN RAMP RATE

ADC Gain

The ES9290 has an additional digital gain that can be added through registers. Settings for +0dB to +42dB in +6dB steps are available.

ADC Gain Registers

- Register 72[6:4] ADC_DIGITAL_GAIN_CH2
- Register 72[2:0] ADC_DIGITAL_GAIN_CH1

Direct Monitor Volume

The signal from the ADC digital path can be passed into the DAC digital path using the Direct Monitor. The Direct Monitor Volume Control is intended for use during audio playback. Each channel can be digitally attenuated from +1dB to -126dB in 0.5dB steps. When a new volume level is set, the attenuation circuit will ramp softly to the new level at a rate specified in the VOLUME UP RAMP RATE and VOLUME DOWN RAMP RATE registers.

Monitor Volume Registers

- Register 127 DIRECT MONITOR VOLUME CH1
- Register 128 DIRECT MONITOR VOLUME CH2

Note: This is the same Monitor Volume block as seen in the DAC Digital Signal Path.

Direct Monitor Gain

The Direct Monitor uses the same gain settings as the ADC Gain does.

Monitor Gain Registers

- Register 72[6:4] ADC_DIGITAL_GAIN_CH2
- Register 72[2:0] ADC_DIGITAL_GAIN_CH1

Note: This is the same Monitor Gain block as seen in the DAC Digital Signal Path.

PCM/TDM Encoder

The ES9290 integrates a PCM/TDM Encoder that can be mixed with the monitor's output. The PCM/TDM Encoder input has a maximum word width of 32-bits (default) and a maximum bit depth of 32-bit (default). The encoder allows for I^2S, LJ, and TDM output streams.

The PCM/TDM Encoder can support up to 32 different slots and each channel of the DAC can be mapped to any of the 32 slots.

Note: The PCM/TDM Encoder and PCM/TDM Decoder use all the same registers settings and will run with the exact same formatting.

PCM/TDM Encoder Registers

- Register 5[7] TDM_RESYNC
- Register 5[6] AUTO_CH_DETECT
- Register 5[4:0] TDM_CH_NUM
- Register 6[7] ENABLE_WS_MONITOR
- Register 6[6] ENABLE_BCK_MONITOR
- Register 6[5:4] TDM_WORD_WIDTH
- Register 6[3:2] TDM_BIT_DEPTH
- Register 6[1] TDM_VALID_EDGE
- Register 6[0] TDM_LJ

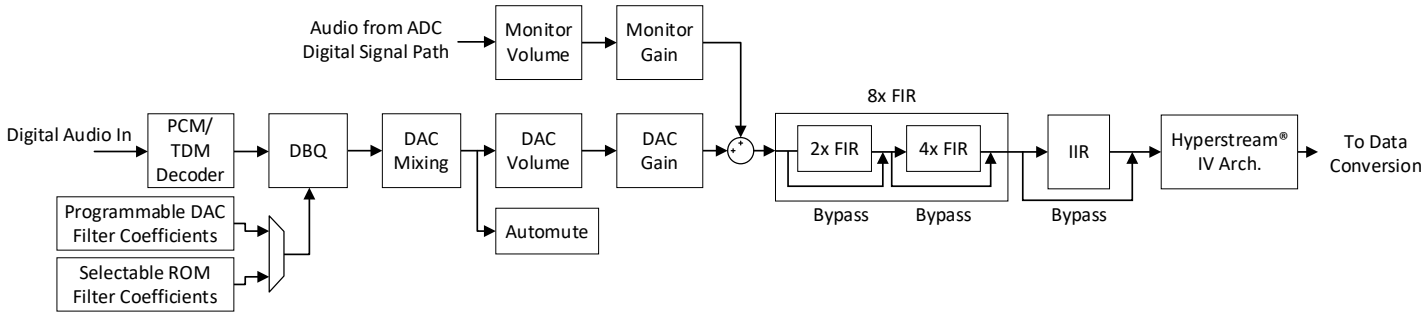
TDM Mapping Registers

- Register 7[4:0] ADC_TDM_SLOT_SEL_CH1
- Register 8[4:0] ADC_TDM_SLOT_SEL_CH2

Daisy Chain Registers

- Register 11[5] ADC_TDM_DAISY_CHAIN
- Register 11[4:0] ADC_TDM_DATA_LATCH_ADJ

DAC Digital Signal Path



PCM/TDM Decoder

The ES9290 integrates a PCM/TDM Decoder that can be mixed with the monitor's output. The PCM/TDM decoder input has a maximum word width of 32-bits (default) and a maximum bit depth of 32-bit (default). The decoder allows for I²S, LJ, RJ and TDM input streams.

The PCM/TDM decoder can support up to 32 different slots and each channel of the DAC can be mapped to any of the 32 slots.

Note: The PCM/TDM Encoder and PCM/TDM Decoder use all the same registers settings and will run in the exact same format.

PCM/TDM Decoder Registers

- Register 5[7] TDM_RESYNC
- Register 5[6] AUTO_CH_DETECT
- Register 5[4:0] TDM_CH_NUM
- Register 6[7] ENABLE_WS_MONITOR
- Register 6[6] ENABLE_BCK_MONITOR
- Register 6[5:4] TDM_WORD_WIDTH
- Register 6[3:2] TDM_BIT_DEPTH
- Register 6[1] TDM_VALID_EDGE
- Register 6[0] TDM_LJ

TDM Mapping Registers

- Register 9[4:0] DAC_TDM_SLOT_SEL_CH1
- Register 10[4:0] DAC_TDM_SLOT_SEL_CH2

Daisy Chain Registers

- Register 12[5] DAC_TDM_DAISY_CHAIN
- Register 12[4:0] DAC_TDM_DATA_LATCH_ADJ

DAC Digital Biquad Filter

The ES9290 features a Digital Full Biquad (DBQ) filter for the DAC datapath. The filter comes with 23 preset filters and the ability to make a custom filter via user input coefficients.

The custom filter uses 5 coefficients to shape the filter: -A2, -A1, B2, B1, and B0.
The coefficients are signed 24-bit numbers.

DAC DBQ Filter Registers

- Register 102[4:0] DAC_DBQ_COEFF_SEL (preset filter selection)
- Register 103-105 DAC PROG DBQ A2 COEFF
  - Note: Assigns -A2 to the register
- Register 106-108 DAC PROG DBQ A1 COEFF
  - Note: Assigns -A1 to the register
- Register 109-111 DAC PROG DBQ B2 COEFF
- Register 112-114 DAC PROG DBQ B1 COEFF
- Register 115-117 DAC PROG DBQ B0 COEFF

The DBQ is arranged in a transposed direct form 2 format.

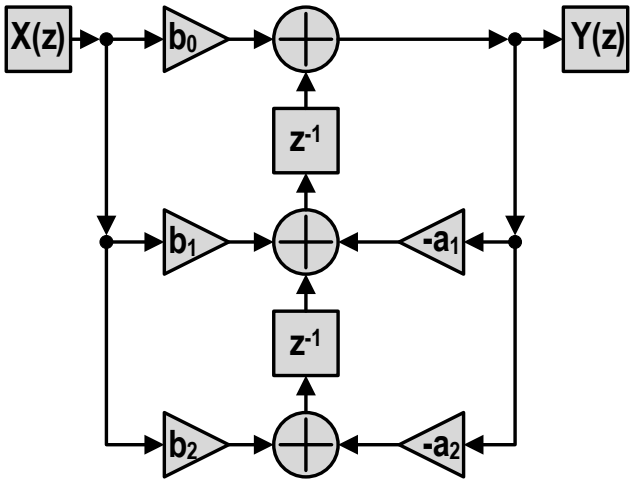


Figure 16 - DAC DBQ format

DAC Mixing

The ES9290 has the ability to mix the incoming TDM Decoder audio data DAC_CH1 data into DAC_CH2 and vice versa. The range of mixing is -∞dB (8'hFF) to 0dB (8'h00).

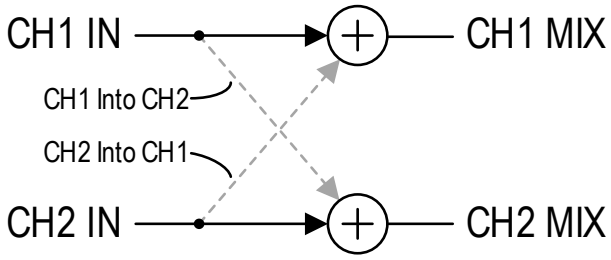


Figure 17 - DAC Mixing

DAC Mixing Registers

- Register 125 DAC MIX VOLUME CH1
- Register 126 DAC MIX VOLUME CH2

DAC Automute

The DAC in the ES9290 features an automute that triggers when the signal is below the specified level for longer than the specified time. The automute will disengage when the signal is above the specified off value for the same amount of time.

Note: Automute will not engage if the ADC monitor is running.

$$Time[s] = \frac{2^{25}}{AUTOMUTE\_TIME * MCLK\_128FS * 2^{64FS\_MODE}}$$

$$Level[dB] = \frac{20 * log_{10}(AUTOMUTE\_LEVEL)}{(2^{16} - 1) * 2^{7}}$$

DAC Automute Registers

- Register 139[1:0] AUTOMUTE_EN_CHx
- Register 140-141[10:0] AUTOMUTE_TIME
- Register 142-143 AUTOMUTE_LEVEL
- Register 144-145 AUTOMUTE_OFF_LEVEL

DAC Volume

The DAC Volume Control is intended for use during audio playback. Each channel can be digitally attenuated from -126dB to +1dB in +0.5dB steps. When a new volume level is set, the attenuation circuit will ramp softly to the new level at a rate specified in the VOLUME UP RAMP RATE and VOLUME DOWN RAMP RATE registers.

DAC Volume Registers

- Register 123 DAC VOLUME CH1
- Register 124 DAC VOLUME CH2
- Register 14 VOLUME UP RAMP RATE
- Register 15 VOLUME DOWN RAMP RATE

DAC Gain

The ES9290 has an additional digital gain that can be added through registers. Settings for +0dB to +42dB in 6dB steps are available.

DAC Gain Registers

- Register 135[6:4] DAC_DIGITAL_GAIN_CH2
- Register 135[2:0] DAC_DIGITAL_GAIN_CH1

Direct Monitor Volume

The signal from the ADC digital path can be passed into the DAC digital path using the Direct Monitor. The Direct Monitor Volume Control is intended for use during audio playback. Each channel can be digitally attenuated from +1dB to -126dB in 0.5dB steps. When a new volume level is set, the attenuation circuit will ramp softly to the new level at a rate specified in the VOLUME UP RAMP RATE and VOLUME DOWN RAMP RATE registers.

Monitor Volume Registers

- Register 127 DIRECT MONITOR VOLUME CH1
- Register 128 DIRECT MONITOR VOLUME CH2

Note: This is the same Monitor Volume block as seen in the ADC Digital Signal Path.

Direct Monitor Gain

The Direct Monitor uses the same gain settings as the ADC Gain does.

Monitor Gain Registers

- Register 72[6:4] ADC_DIGITAL_GAIN_CH2
- Register 72[2:0] ADC_DIGITAL_GAIN_CH1

Note: This is the same Monitor Gain block as seen in the ADC Digital Signal Path.

DAC 8x FIR Filter

Selection of the 8x interpolation filter is chosen from 8 pre-programmed filters. The 2x and 4x filter can be bypassed individually or together. For more information on filters see the DAC: PCM Filter Latency section.

DAC FIR Registers

- Register 118[2:0] DAC_FILTER_SHAPE
- Register 118[3] BYPASS_FIR2X
- Register 118[4] BYPASS_FIR4X

DAC IIR Filter

The IIR filter can be bypassed using Register 118[5] BYPASS_IIR

Pre-Programmed FIR Filters

The ES9290 has 8 pre-programmed digital filters. The latency for each filter reduces (scales) with increasing sample rates. (See Register 64[7:5] ADC_FILTER_SHAPE and Register 118[2:0] DAC_FILTER_SHAPE for configuration)

#	Filter	Description
0	Minimum Phase (default)	Version 2 of minimum phase fast roll-off (#5) with less ripple and more image rejection
1	Linear Phase Apodizing Fast Roll-Off	Full image rejection by FS/2 to avoid any aliasing, with smooth roll-off starting before 20k.
2	Linear Phase Fast Roll-Off	Sabre legacy filter, optimized for image rejection @ 0.55FS
3	Linear Phase Fast Roll-Off Low-Ripple	Sabre legacy filter, optimized for in-band ripple
4	Linear Phase Slow Roll-Off	Sabre legacy filter, optimized for lower latency, but symmetric impulse response
5	Minimum Phase Fast Roll-Off	Low latency, minimal pre ringing and low passband ripple, image rejection @ 0.55FS
6	Minimum Phase Slow Roll-Off	Lowest latency at the cost of image rejection
7	Minimum Phase Fast Roll-Off Low Dispersion	Provides a nice balance of the low latency of minimum phase filters and the low dispersion of linear phase filters. Minimal pre-ringing is added to achieve the low dispersion in the audio band.

Table 15 - Pre-Programmed Digital Filter Descriptions

Note: Minimum Phase filters are asymmetric filters that work to minimize the pre-echo of the filter, while still maintaining an excellent frequency response and they peak earlier than linear phase filters, resulting in a lower group delay. Minimum phase filters usually feature zero cycles of pre-echo, which can result in improved audio quality.

ADC: PCM Filter Latency

The following table shows the simulated latency of each filter at 44.1kHz sampling rate. Measurements were taken from the external impulse response prior to being down sampled to 1FS. The extra sample delay to get the data encoded accounts for external processing time to serialize the data stream. Latency delay will reduce (scale) with sampling rate.

Digital Filter	Delay
Minimum Phase (default)	7.25 / FS
Linear Phase Apodizing Fast Roll-Off	37.13 / FS
Linear Phase Fast Roll-Off	37.25 / FS
Linear Phase Fast Roll-Off Low-Ripple	36.88 / FS
Linear Phase Slow Roll-Off	9.88 / FS
Minimum Phase Fast Roll-Off	7.38 / FS
Minimum Phase Slow Roll-Off	6.25 / FS
Minimum Phase Fast Roll-Off Low Dispersion	16.13 / FS

Table 16 - ADC PCM Filter Latency

ADC: PCM Filter Properties

Minimum Phase					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 FS	Hz
Stop band	-88 dB	0.54 FS			Hz
Group Delay		2.90/FS		9.23/FS	s
Flatness (ripple)	0.0042				dB

Linear Phase Apodizing					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.41 FS	Hz
Stop band	-81.91 dB	0.50 FS			Hz
Group Delay			33.25/FS		s
Flatness (ripple)	0.0043				dB

Linear Phase Fast Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 FS	Hz
Stop band	-77.88 dB	0.54 FS			Hz
Group Delay			33.38/FS		s
Flatness (ripple)	0.0043				dB

Linear Phase Fast Roll-Off Low Ripple					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 FS	Hz
Stop band	-77.46 dB	0.55 FS			Hz
Group Delay			33.00/FS		s
Flatness (ripple)	0.0040				dB

Linear Phase Slow Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.46 FS	Hz
Stop band	-84.63 dB	0.75 FS			Hz
Group Delay			6.05/FS		s
Flatness (ripple)					dB

Minimum Phase Fast Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 FS	Hz
Stop band	-88.26 dB	0.54 FS			Hz
Group Delay		2.95/FS		9.42/FS	s
Flatness (ripple)	0.0054				dB

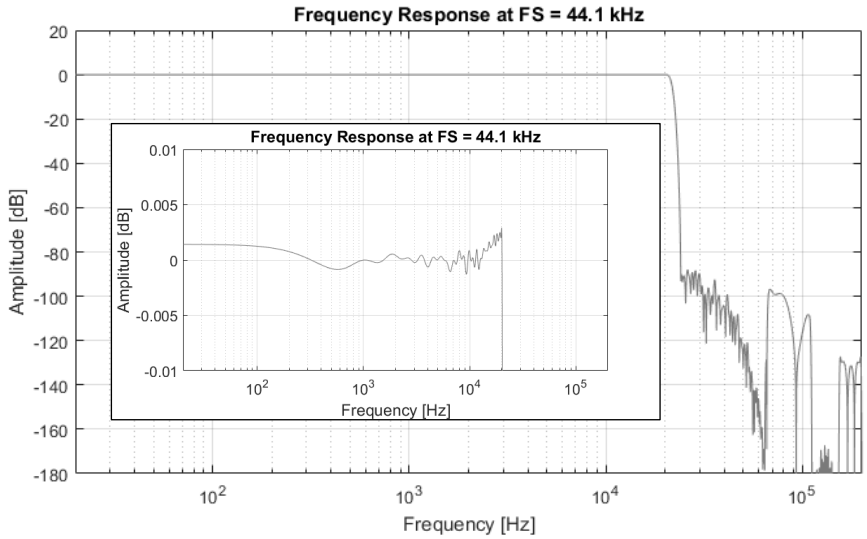
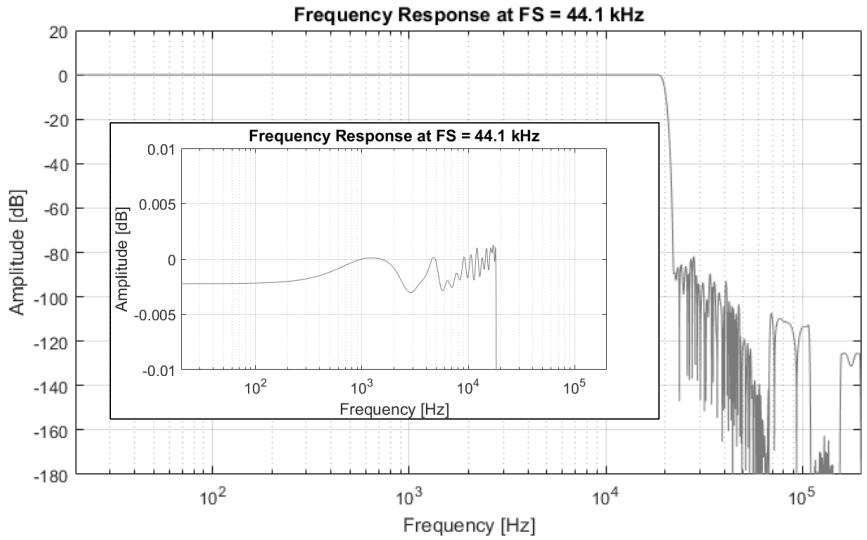
Minimum Phase Slow Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.43 FS	Hz
Stop band	-90.02 dB	0.80 FS			Hz
Group Delay		2.03/FS		3.51/FS	s
Flatness (ripple)					dB

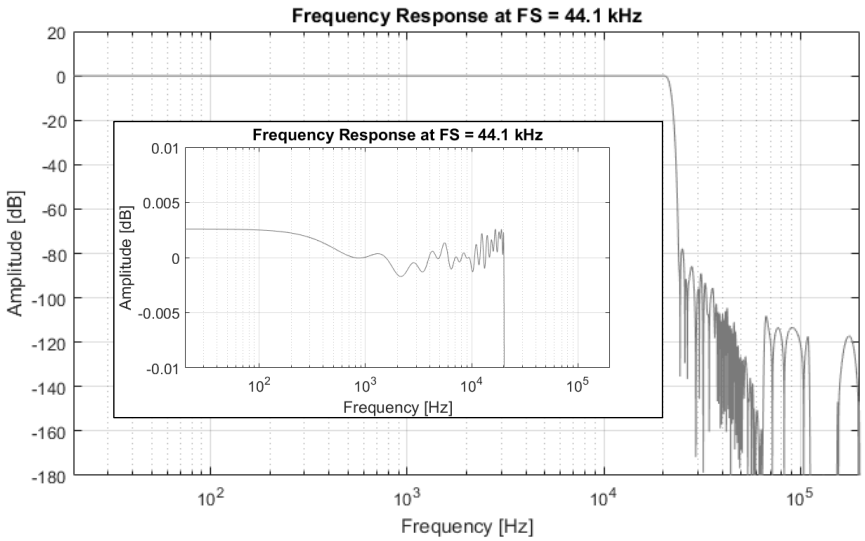
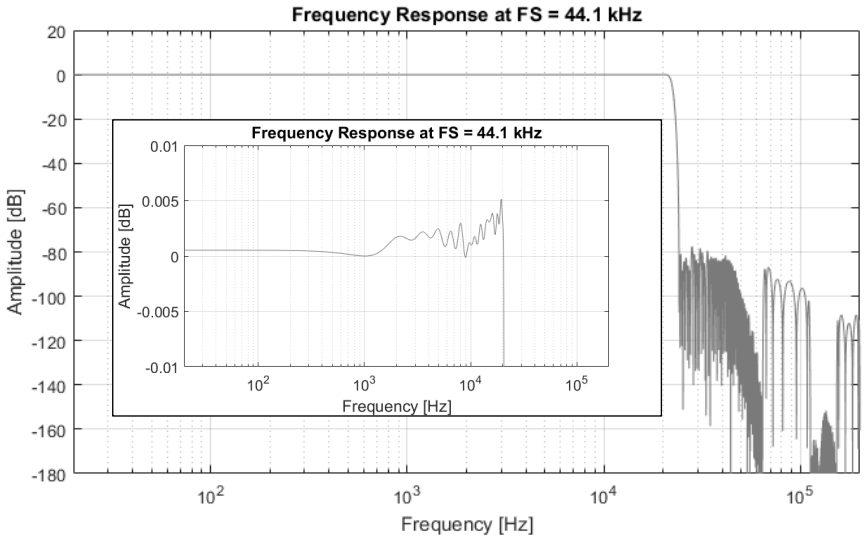
Minimum Phase Slow Roll-Off Low Dispersion					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.43 FS	Hz
Stop band	-90.02 dB	0.80 FS			Hz
Group Delay		12.16/FS		12.43/FS	s
Flatness (ripple)					dB

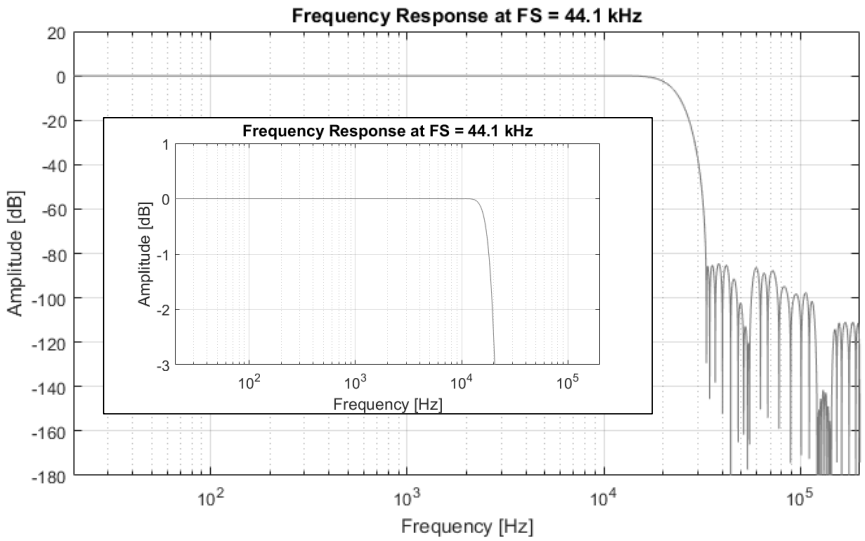
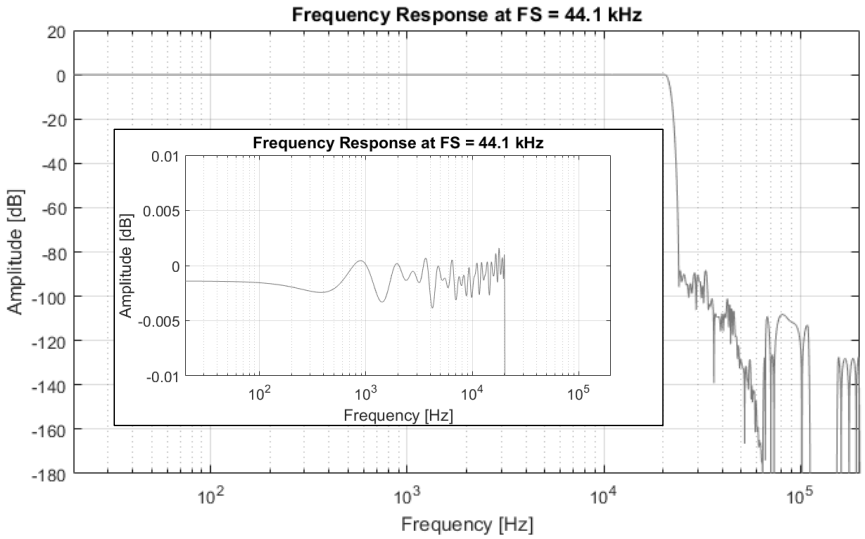
Table 17 - ADC PCM Filter Properties

ADC: PCM Filter Frequency Response

The following frequency responses were obtained from software simulations of these filters. Simulation sample rate is 44.1kHz.

Filter	Frequency Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-Off	
Linear Phase Fast Roll-Off Low Ripple	

Linear Phase Slow Roll-Off	
Minimum Phase Fast Roll-Off	

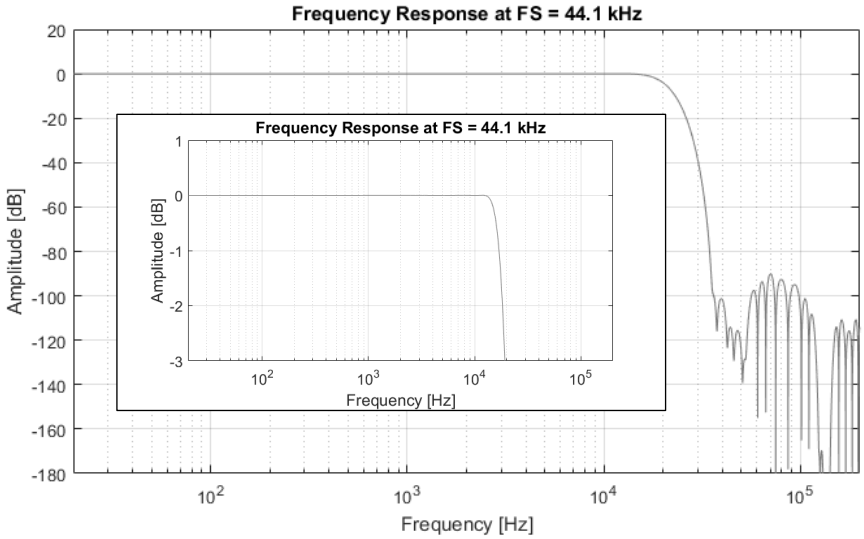
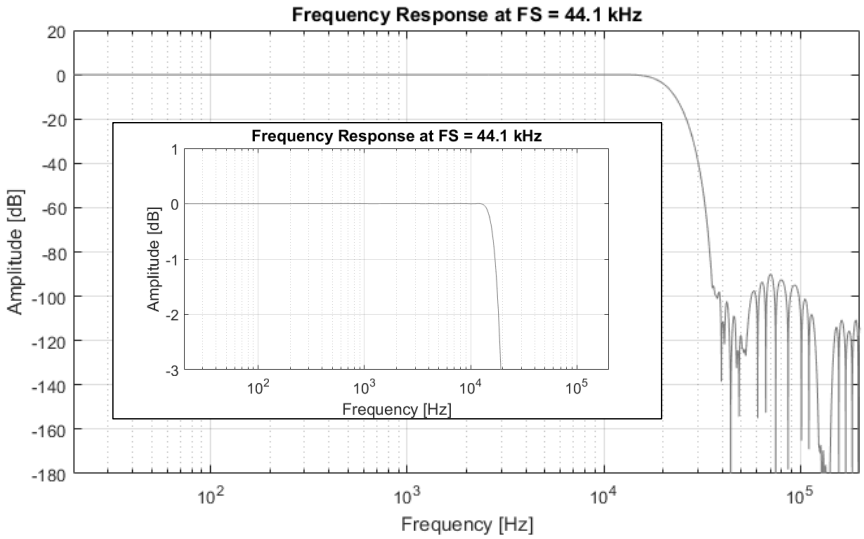
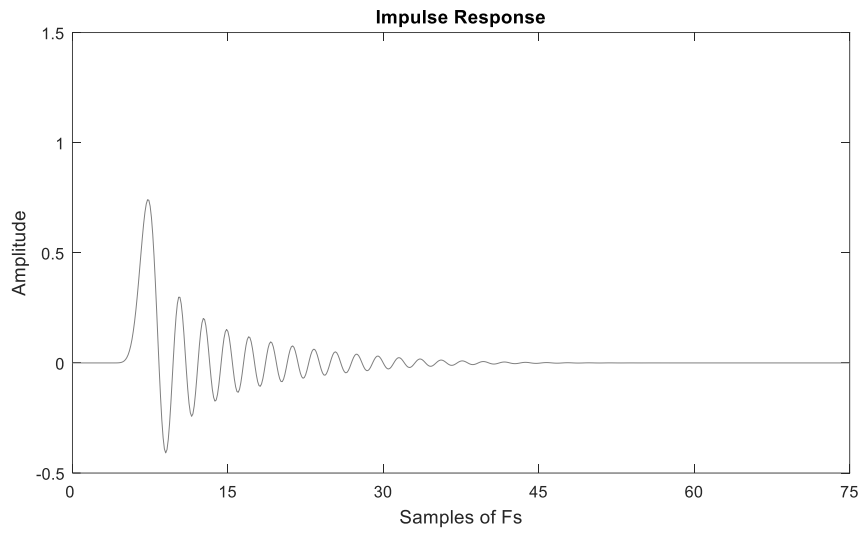
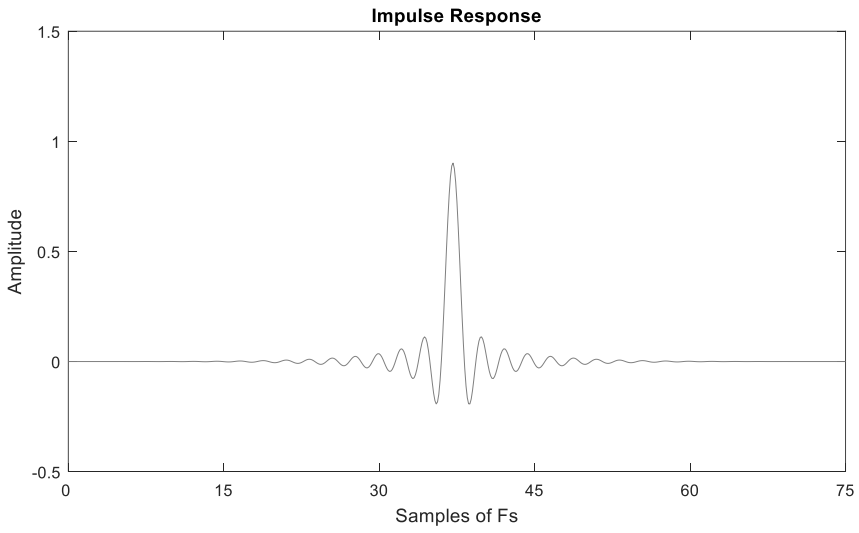
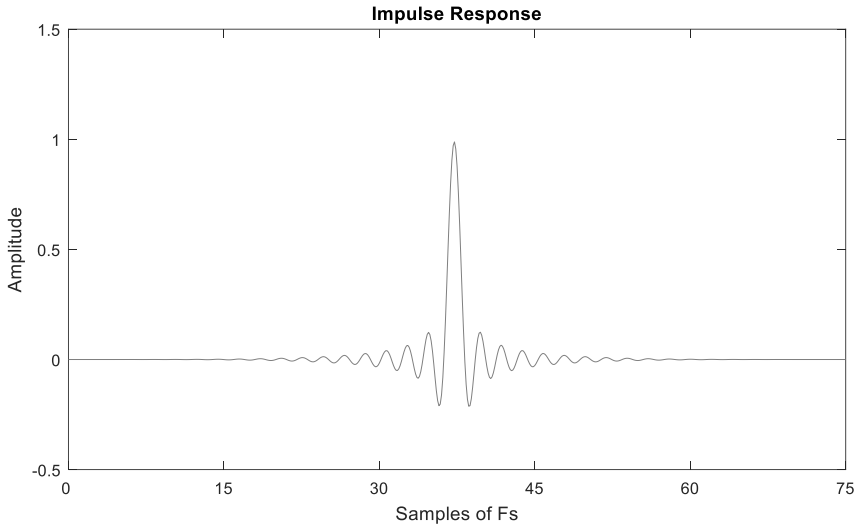
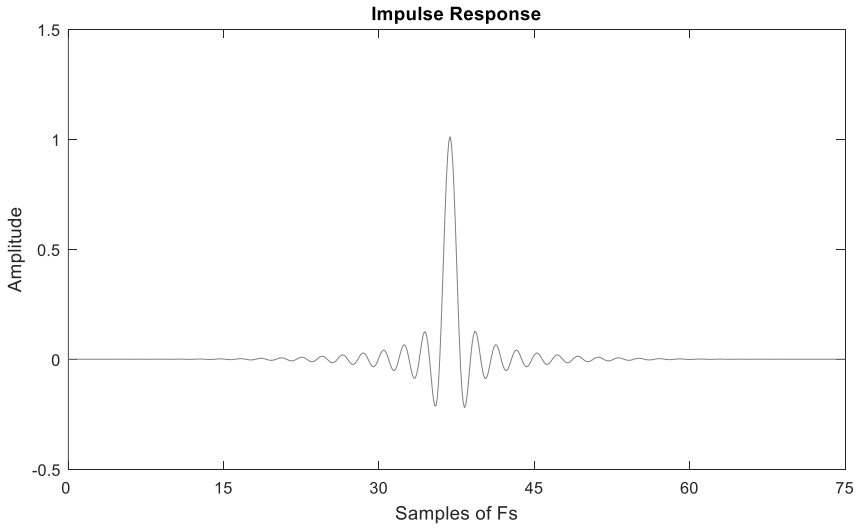
Minimum Phase Slow Roll-Off	
Minimum Phase Slow Roll-Off Low Dispersion	

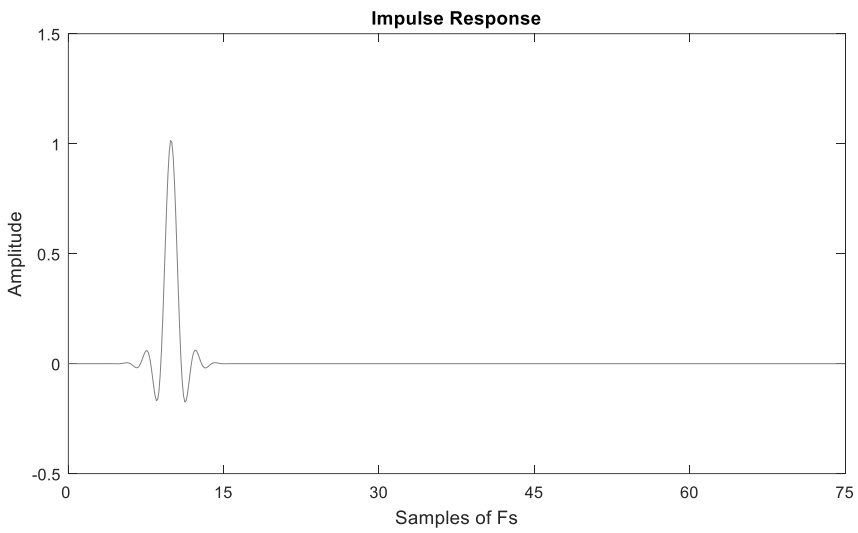
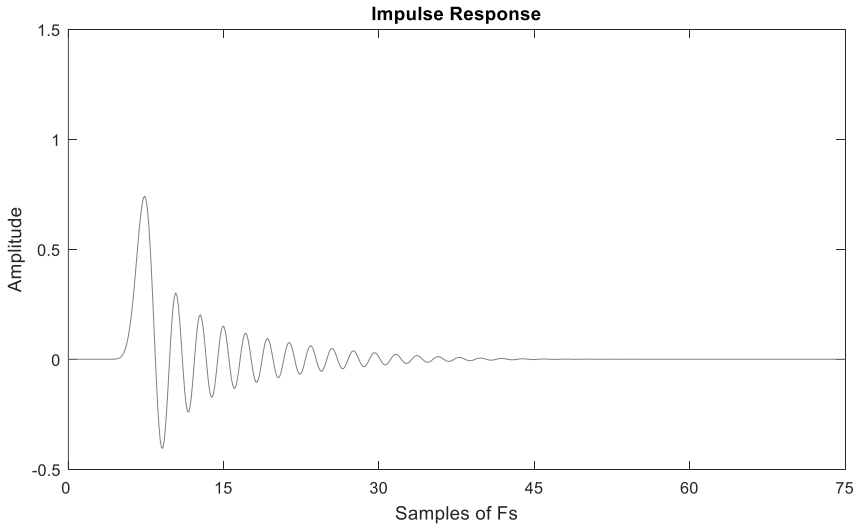
Table 18 - ADC PCM Filter Frequency Response

ADC: PCM Filter Impulse Response

The following impulse responses were obtained from software simulations of these filters. They show the decimation path prior to down-sampling to 1FS and are scaled accordingly. The extra sample delay to get the data encoded accounts for external processing time to serialize data stream.

Filter	Impulse Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-Off	
Linear Phase Fast Roll-Off Low Ripple	

Linear Phase Slow Roll-Off	
Minimum Phase Fast Roll-Off	

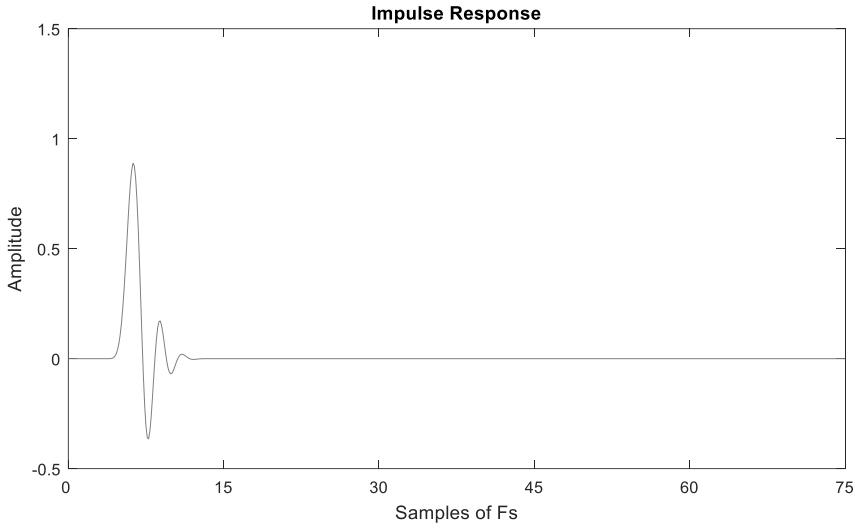
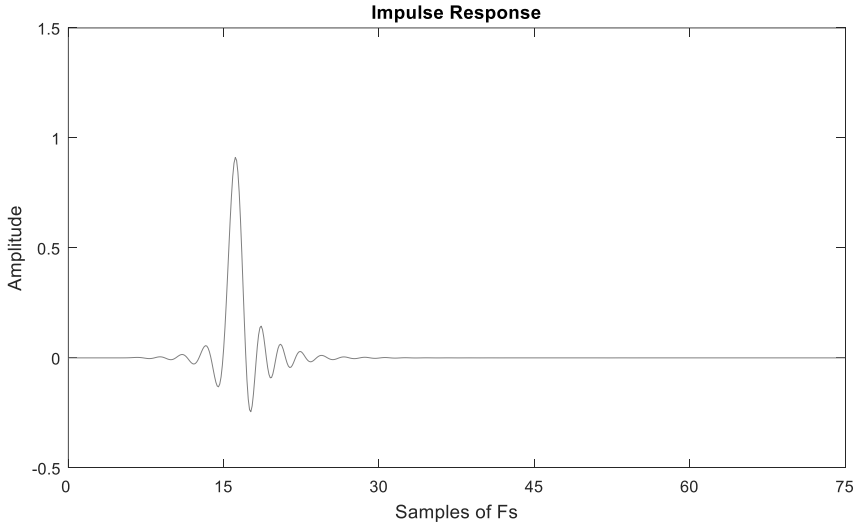
Minimum Phase Slow Roll-Off	
Minimum Phase Slow Roll-Off Low Dispersion	

Table 19 - ADC PCM Filter Impulse Response

ADC: 64FS Mode

ADC: Minimum Phase 64FS Mode Latency

The following table shows the simulated latency at 705.6kHz sampling rate and is very similar at 768kHz. Measurements were taken from the external impulse response prior to being down sampled to 1FS. The extra sample delay to get the data encoded accounts for external processing time to serialize the data stream. Latency delay will reduce (scale) with sampling rate.

Digital Filter	Delay
Minimum Phase Double Rate	6 / FS

Table 20 - ADC Minimum Phase 64FS Latency

ADC: Minimum Phase 64FS Properties

Minimum Phase 64FS Mode					
Parameter	Conditions	MIN	TYP	MAX	UNIT
Pass band	-3 dB			0.44 FS	Hz
Stop band	-68.37 dB	0.68 FS			Hz
Group Delay		1.43/FS		3.45/FS	s
Flatness (ripple)					dB

Table 21 - ADC Minimum Phase 64FS Properties

Note: The ADC Minimum Phase 64FS filter has an additional +0.020dB of gain.

ADC: Minimum Phase 64FS Frequency Response

This filter gets selected automatically when MCLK/FS = 64. The following frequency response was obtained from software simulations with a sample rate of 705.6kHz

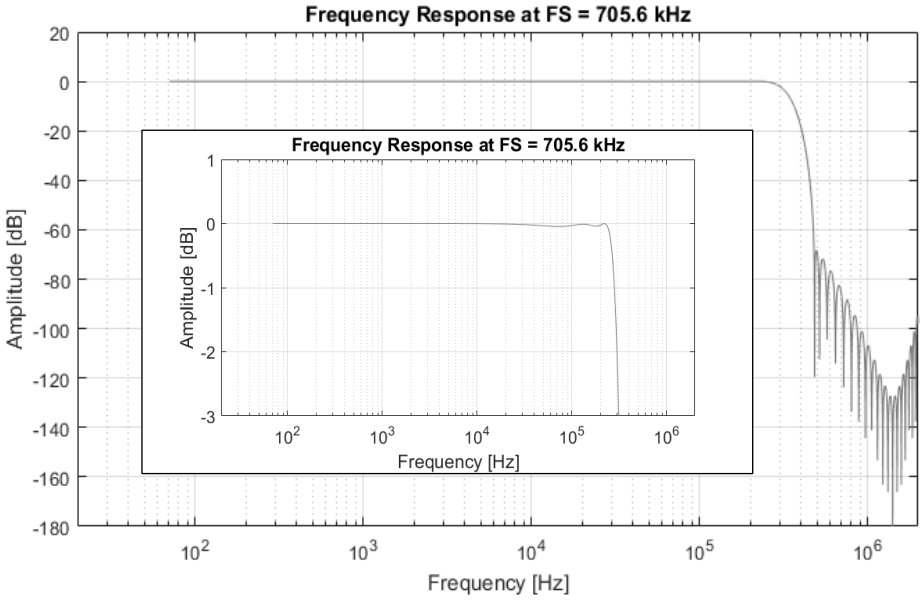


Figure 18 - ADC Minimum Phase 64FS Frequency Response

ADC: Minimum Phase 64FS Impulse Response

The following impulse responses were obtained from software simulations of these filters. They show the decimation path prior to down-sampling to 1FS and are scaled accordingly. The extra sample delay to get the data encoded accounts for external processing time to serialize data stream.

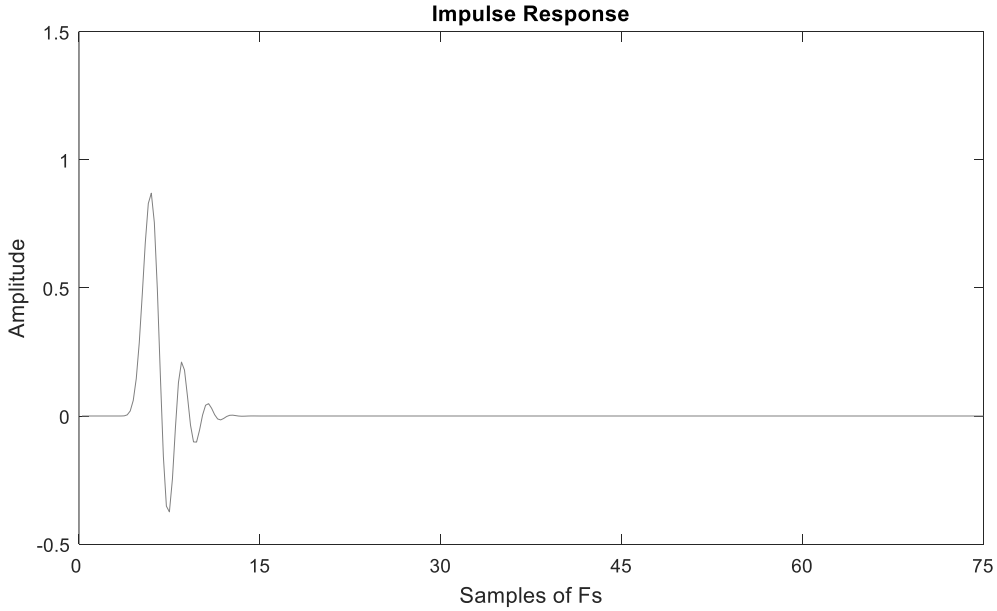


Figure 19 - ADC Minimum Phase 64FS Impulse Response

DAC: PCM Filter Latency

The following table shows the simulated latency of each filter at 44.1kHz sampling rate. Measurements were taken from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize the data stream. Latency will reduce (scale) with sampling rate.

Digital Filter	Delay
Minimum Phase (default)	5.39 / FS
Linear Phase Apodizing Fast Roll-Off	34.76 / FS
Linear Phase Fast Roll-Off	35.38 / FS
Linear Phase Fast Roll-Off Low-Ripple	33.32 / FS
Linear Phase Slow Roll-Off	7.82 / FS
Minimum Phase Fast Roll-Off	5.39 / FS
Minimum Phase Slow Roll-Off	4.42 / FS
Minimum Phase Fast Roll-Off Low Dispersion	11.35 / FS

Table 22 - DAC PCM Filter Latency

DAC: PCM Filter Properties

Minimum Phase					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 x fs	Hz
Stop band	-95 dB	0.55 x fs			Hz
Group Delay		2.91/fs		9.01/fs	s
Flatness (ripple)	0.0012				dB

Linear Phase Apodizing					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.41 x fs	Hz
Stop band	-108 dB	0.50 x fs			Hz
Group Delay			32.81/fs		s
Flatness (ripple)	0.0024				dB

Linear Phase Fast Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.45 x fs	Hz
Stop band	-117 dB	0.55 x fs			Hz
Group Delay			33.43/fs		s
Flatness (ripple)	0.0030				dB

Linear Phase Fast Roll-Off Low Ripple					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 x fs	Hz
Stop band	-88 dB	0.55 x fs			Hz
Group Delay			31.37/fs		s
Flatness (ripple)	0.0012				dB

Linear Phase Slow Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.44 x fs	Hz
Stop band	-90 dB	0.75 x fs			Hz
Group Delay			5.87/fs		s
Flatness (ripple)					dB

Minimum Phase Fast Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 x fs	Hz
Stop band	-98 dB	0.55 x fs			Hz
Group Delay		2.91/fs		9.14/fs	s
Flatness (ripple)	0.0023				dB

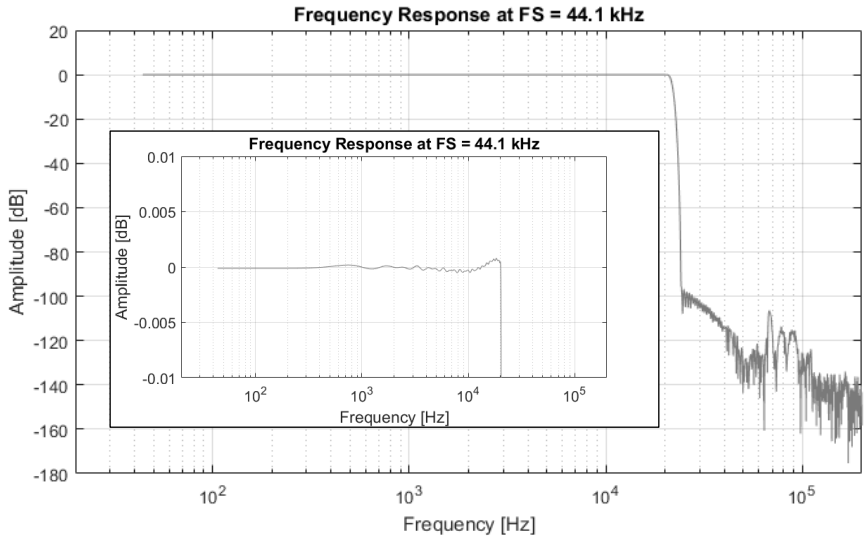
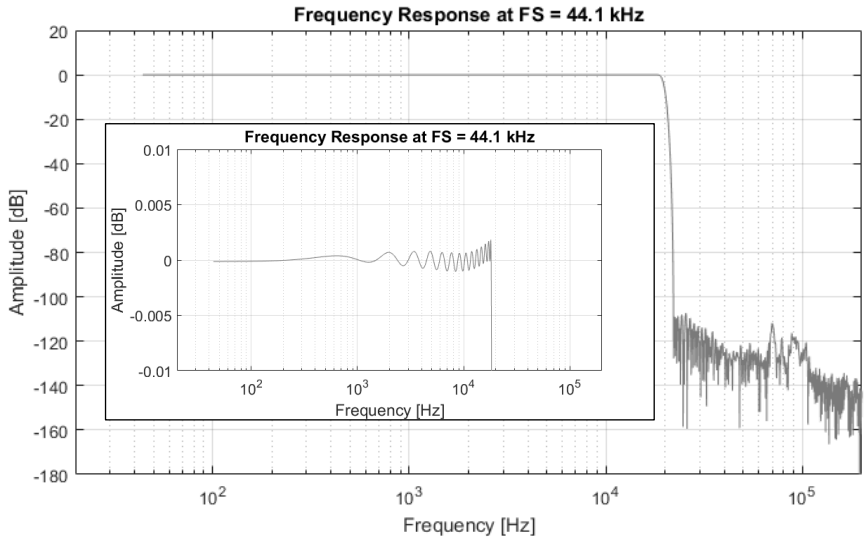
Minimum Phase Slow Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.43 x fs	Hz
Stop band	-91 dB	0.80 x fs			Hz
Group Delay		2.08/fs		3.56/fs	s
Flatness (ripple)					dB

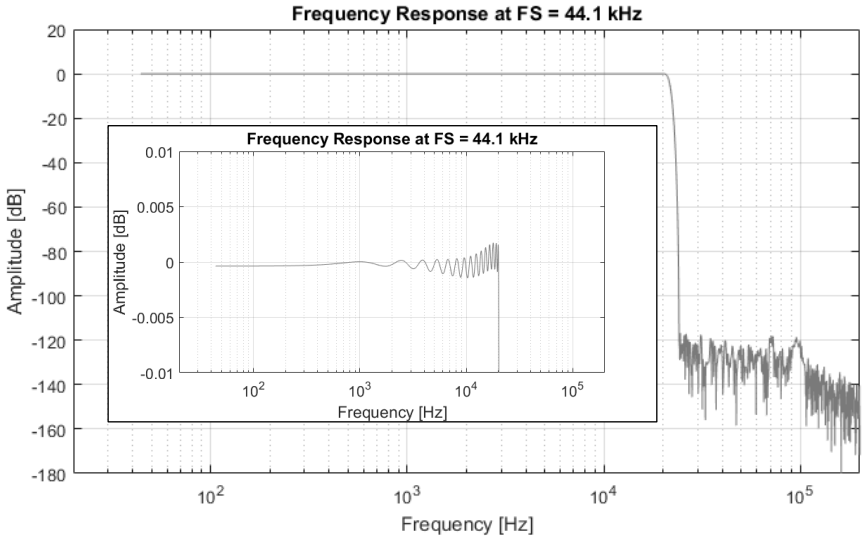
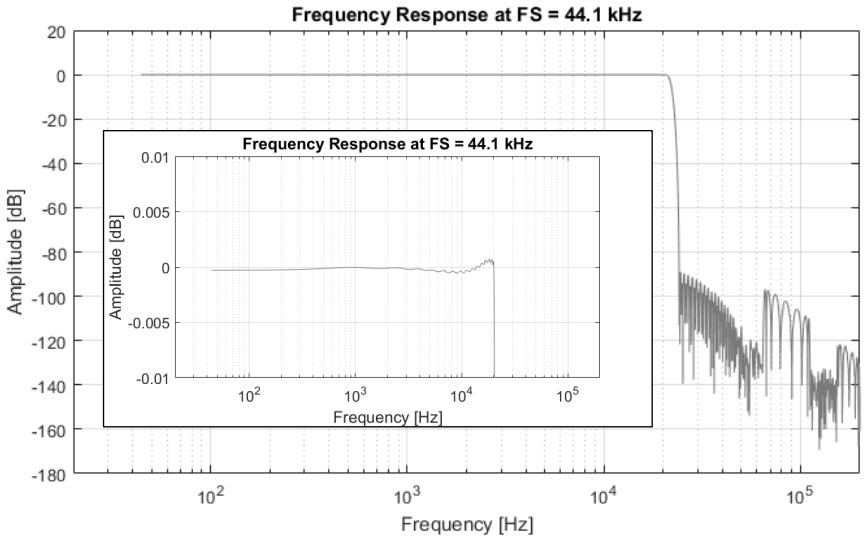
Minimum Phase Slow Roll-Off Low Dispersion					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.43 x fs	Hz
Stop band	-91 dB	0.80 x fs			Hz
Group Delay		9.23/fs		9.75/fs	s
Flatness (ripple)					dB

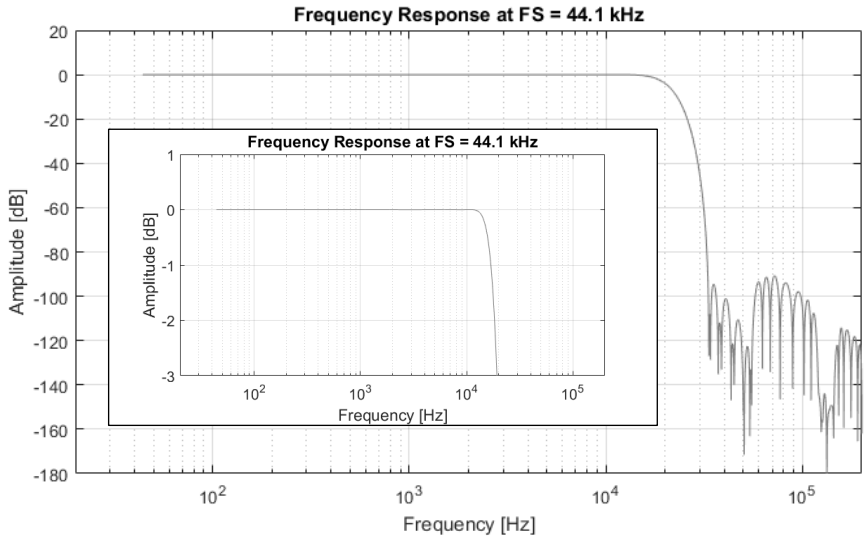
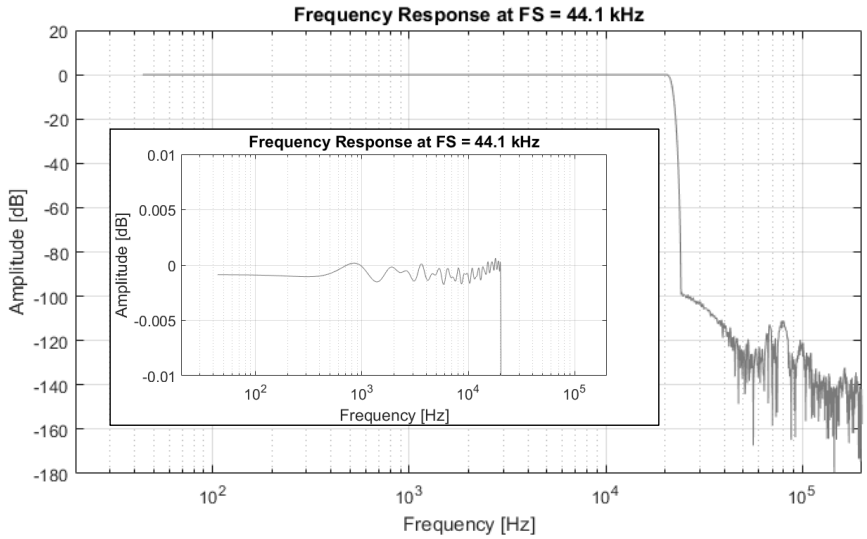
Table 23 - DAC PCM Filter Properties

DAC: PCM Filter Frequency Response

The following frequency responses were obtained from software simulations of these filters. Simulation sample rate is 44.1kHz.

Filter	Frequency Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-Off	
Linear Phase Fast Roll-Off Low Ripple	

Linear Phase Slow Roll-Off	
Minimum Phase Fast Roll-Off	

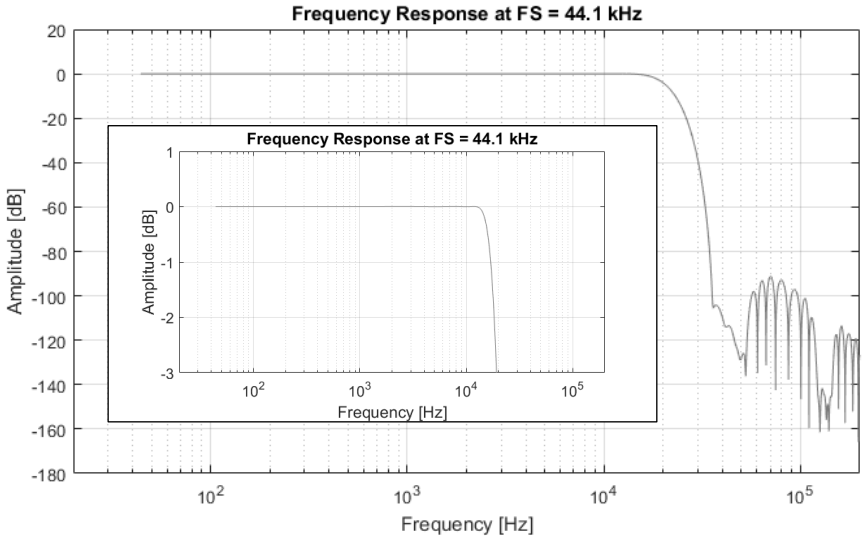
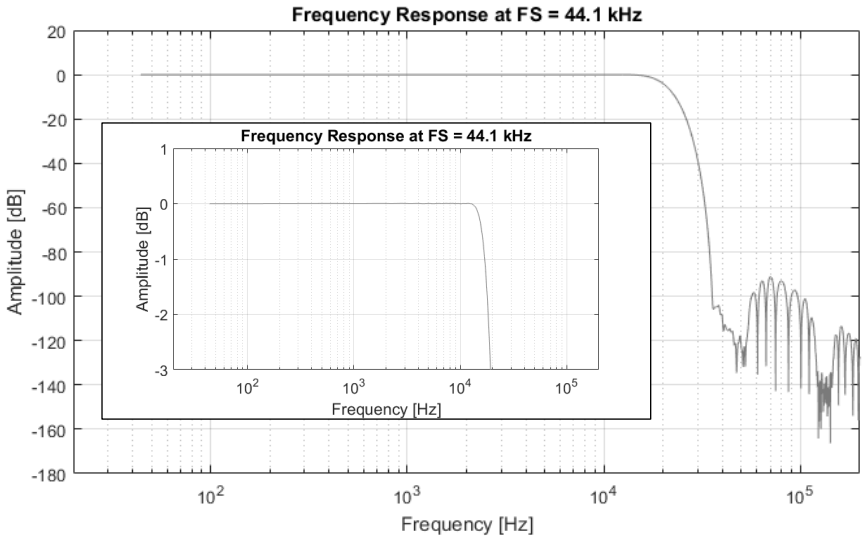
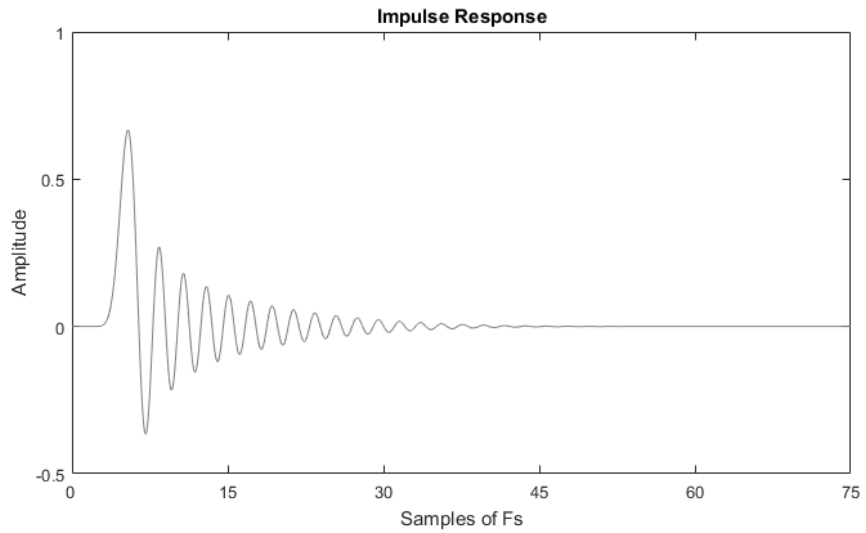
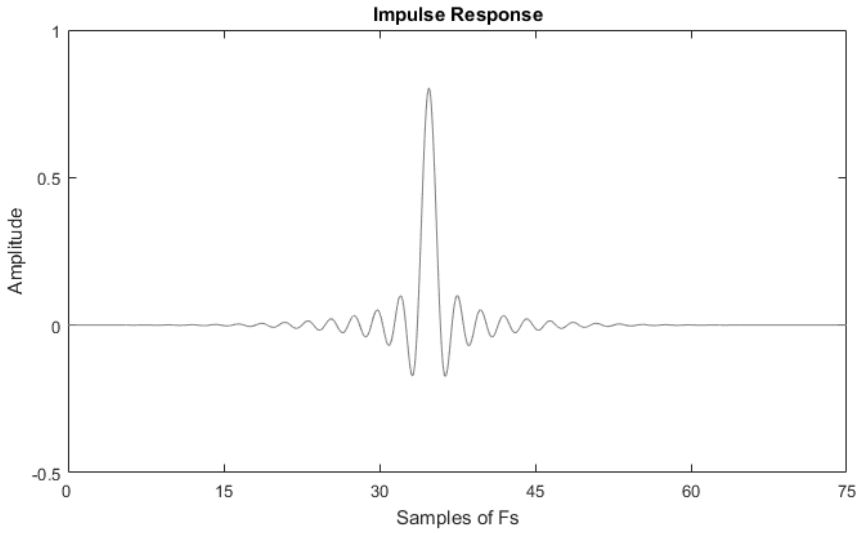
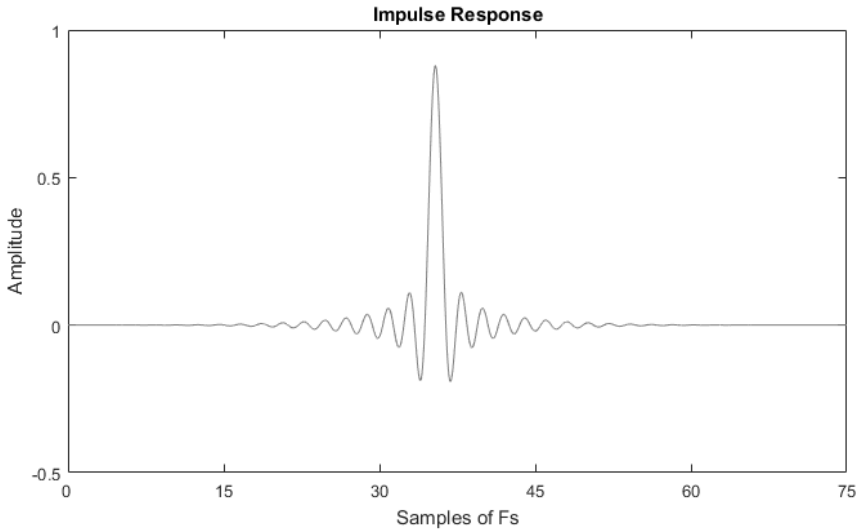
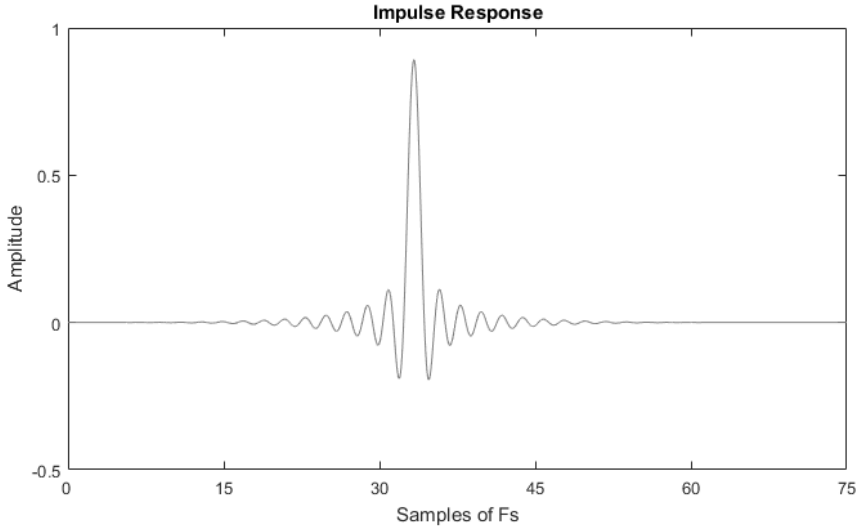
Minimum Phase Slow Roll-Off	
Minimum Phase Slow Roll-Off Low Dispersion	

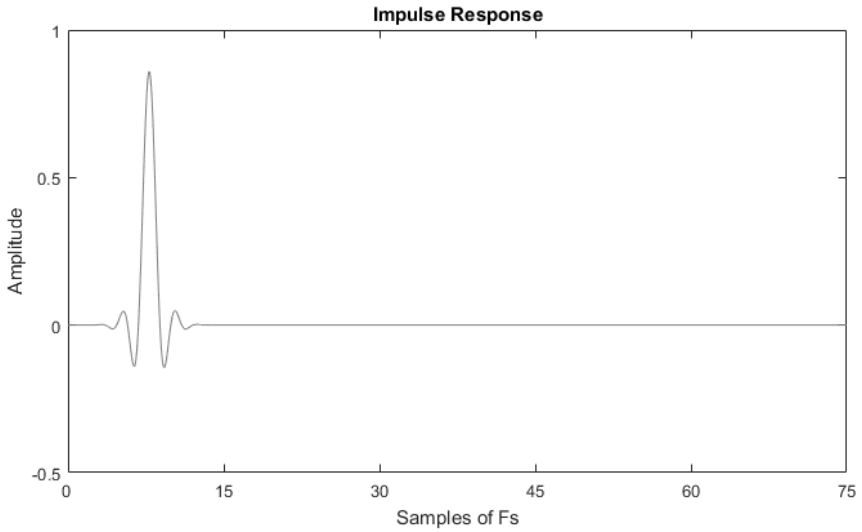
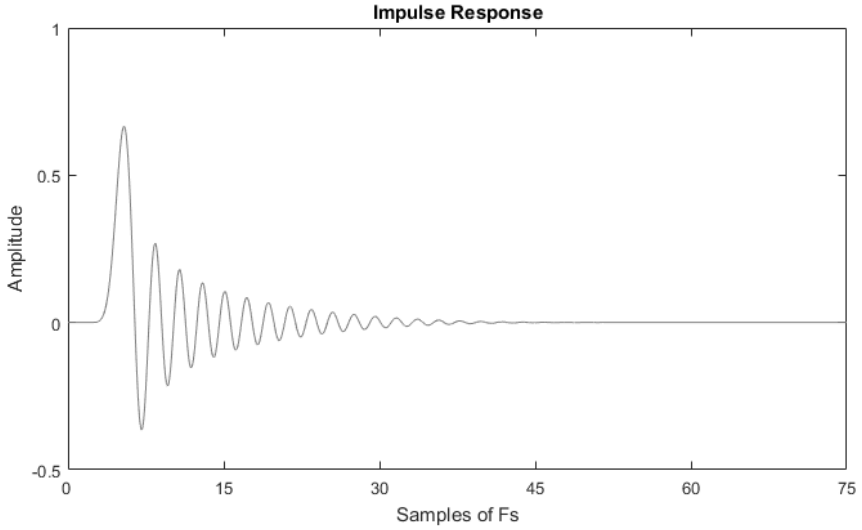
Table 24 - DAC PCM Filter Frequency Response

DAC: PCM Filter Impulse Response

The following impulse responses were obtained from software simulations of these filters. They were measured from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize data stream.

Filter	Impulse Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-Off	
Linear Phase Fast Roll-Off Low Ripple	

Linear Phase Slow Roll-Off	
Minimum Phase Fast Roll-Off	

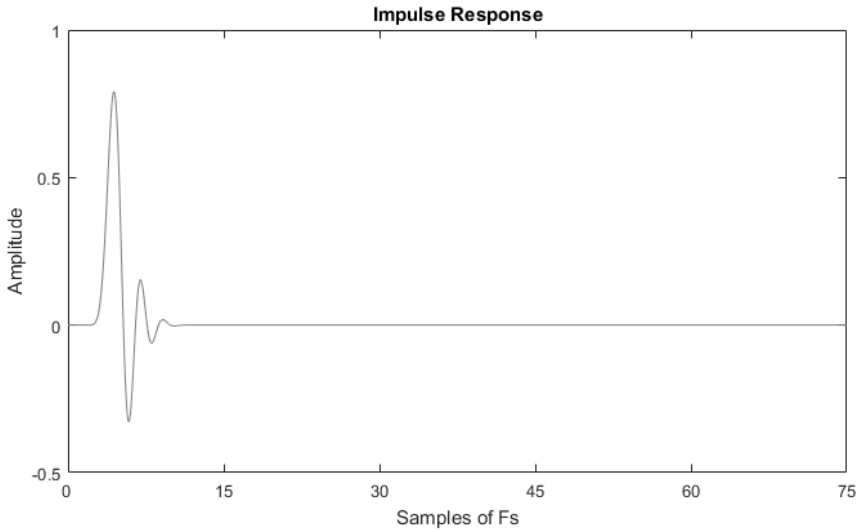
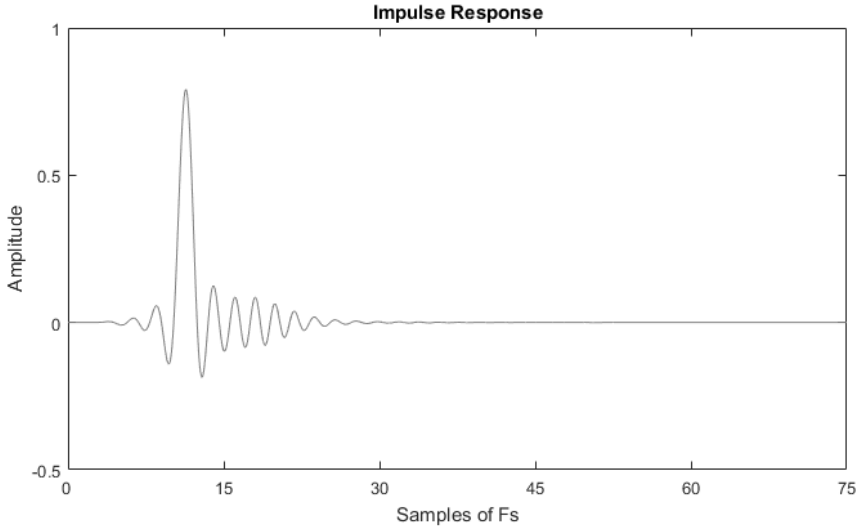
Minimum Phase Slow Roll-Off	
Minimum Phase Slow Roll-Off Low Dispersion	

Table 25 - DAC PCM Filter Impulse Response

DAC: 64FS Mode

DAC: Minimum Phase 64FS Mode Latency

The following table shows the simulated latency at 705.6kHz sampling rate and is very similar at 768kHz. Measurements were taken from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize the data stream. Latency delay will reduce (scale) with sampling rate.

Digital Filter	Delay
Minimum Phase Double Rate	3.83 / FS

Table 26 - DAC Minimum Phase 64FS Latency

DAC: Minimum Phase 64FS Properties

Minimum Phase 64FS Mode					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.45 FS	Hz
Stop band	-61 dB	0.68 FS			Hz
Group Delay		1.54 / FS		2.35 / FS	s
Flatness (ripple)					dB

Table 27 - DAC Minimum Phase 64FS Properties

DAC: Minimum Phase 64FS Frequency Response

This filter gets selected automatically when MCLK/FS = 64. The following frequency response was obtained from software simulations with a sample rate of 705.6kHz

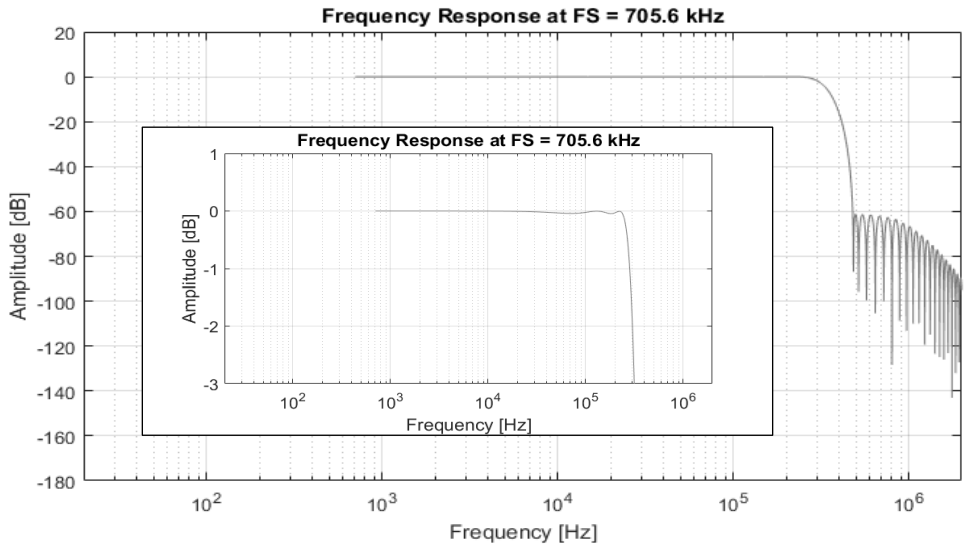


Figure 20 - DAC Minimum Phase 64FS Frequency Response

DAC: Minimum Phase 64FS Impulse Response

The following impulse responses were obtained from software simulations of these filters. They were measured from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize data stream.

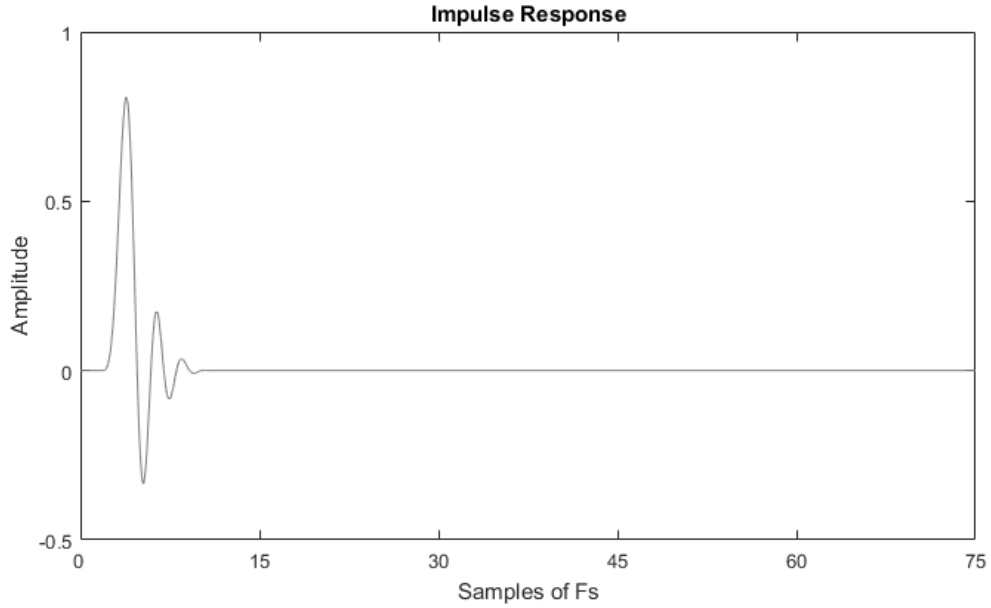


Figure 21 - DAC Minimum Phase 64FS Impulse Response

Pre-Programmed DBQ Filters

The ES9290 has 24 pre-programmed DBQ digital filters, which are second order Butterworth filters with no delay. The cutoff frequency for each filter increases (scales) with increasing sample rates. To manually configure the filters see Register 48[4:0] ADC_DBQ_COEFF_SEL and Register 102[4:0] DAC_DBQ_COEFF_SEL.

The High-pass filters can be automatically set based on the sample rate and clock family. See Register 48[5, 6, 7] ADC_DBQ_120HZ_HPG_EN, ADC_DBQ_80HZ_HPF_EN, ADC_DBQ_CLK_FAMILY_SEL and Register 102[5, 6, 7] DAC_DBQ_120HZ_HPG_EN, DAC_DBQ_80HZ_HPF_EN, DAC_DBQ_CLK_FAMILY_SEL.

The DBQ programmable coefficients are arranged in a Transposed Direct Form II format. See ADC Digital Biquad Filter for more information.

#	Filter	Description
1	Programmable	Program desired filters into the ES9290.
2	Bypass	DBQ filter is bypassed.
3	DC Blocking	High-pass filter with FC = (0.001/48) * FS
4	De-emphasis	Low-pass filter with FC = 3.512kHz, FS = 48kHz
5		Low-pass filter with FC = 3.522kHz, FS = 44.1kHz
6		Low-pass filter with FC = 3.519kHz, FS = 32kHZ
7	RIAA De-emphasis	Standard RIAA De-emphasis filter for FS= 48kHz
8	RIAA Pre-emphasis	Standard RIAA Pre-emphasis filter for FS= 48kHz
9	80Hz High-pass	High-pass filter for FS = 48kHz
10		High-pass filter for FS = 96kHz
11		High-pass filter for FS = 192kHz
12		High-pass filter for FS = 384kHz
13	120Hz High-pass	High-pass filter for FS = 48kHz
14		High-pass filter for FS = 96kHz
15		High-pass filter for FS = 192kHz
16		High-pass filter for FS = 384kHz
17	80Hz High-pass	High-pass filter for FS = 44.1kHz
18		High-pass filter for FS = 88.2kHz
19		High-pass filter for FS = 176.4kHz
20		High-pass filter for FS = 352.8kHz
21	120Hz High-pass	High-pass filter for FS = 44.1kHz
22		High-pass filter for FS = 88.2kHz
23		High-pass filter for FS = 176.4kHz
24		High-pass filter for FS = 352.8kHz

Table 28 - Pre-Programmed DBQ Digital Filter Descriptions

Note: Pre-emphasis filters attenuate lower frequency and boost higher frequencies to improve overall signal to noise ratio. De-emphasis filters redo this process by boosting the lower frequencies and attenuating the higher frequencies. RIAA Pre/De-emphasis filters are specific types of filters used in vinyl record playback systems. It's part of the standard established by the Recording Industry Association of America (RIAA) for phonograph records.

DBQ Filter Properties

DC Blocking					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band		2.1e-5 FS			Hz
Stop band	-32 dB		0 FS		Hz

De-emphasis					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.073 FS	Hz
Stop band	-9.625 dB		0.50 FS		Hz

RIAA De-emphasis					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.001 FS	Hz
Stop band	-40 dB		0.50 FS		Hz

RIAA Pre-emphasis					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band		0.031 FS			Hz
Stop band	-40 dB		0 FS		Hz

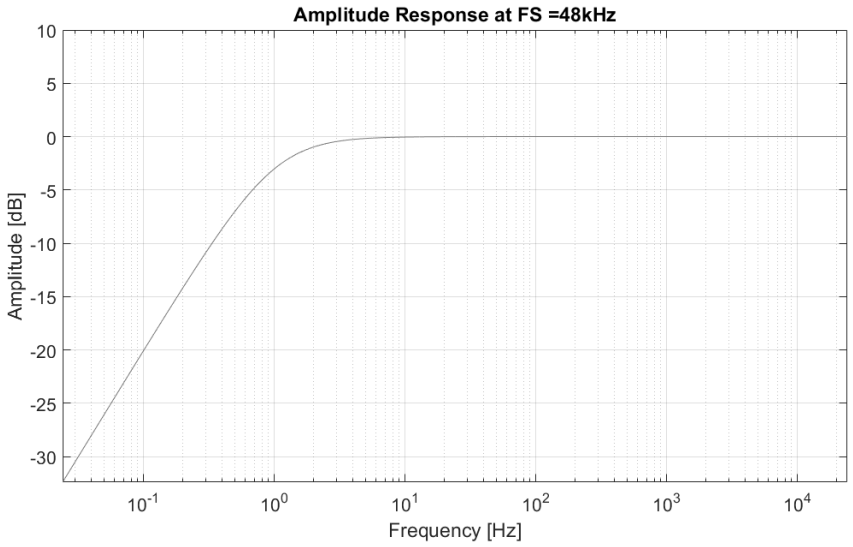
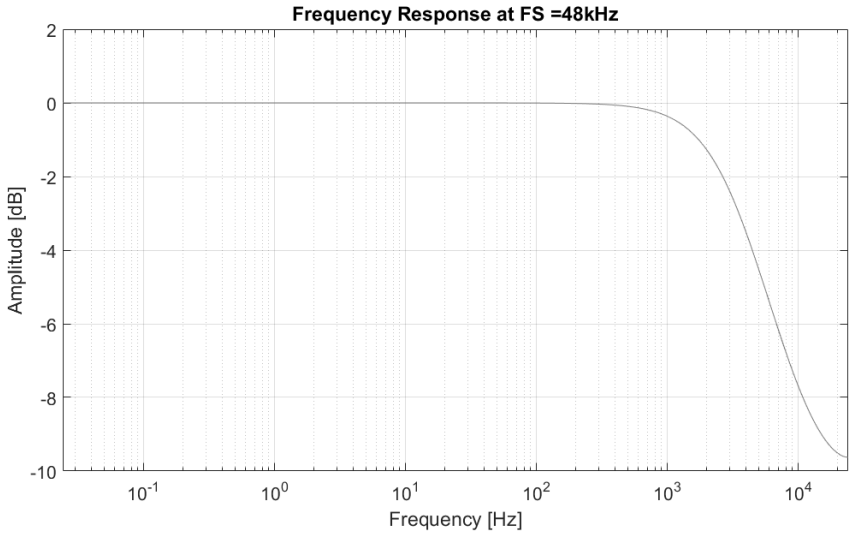
80 Hz High-pass filter (9-12) (17-20)					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				80	Hz
Stop band	-140 dB		0 FS		Hz

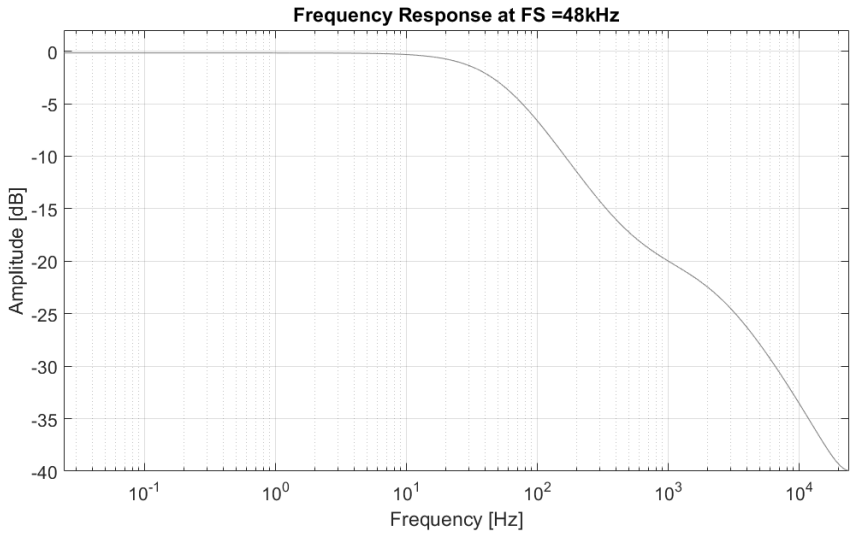
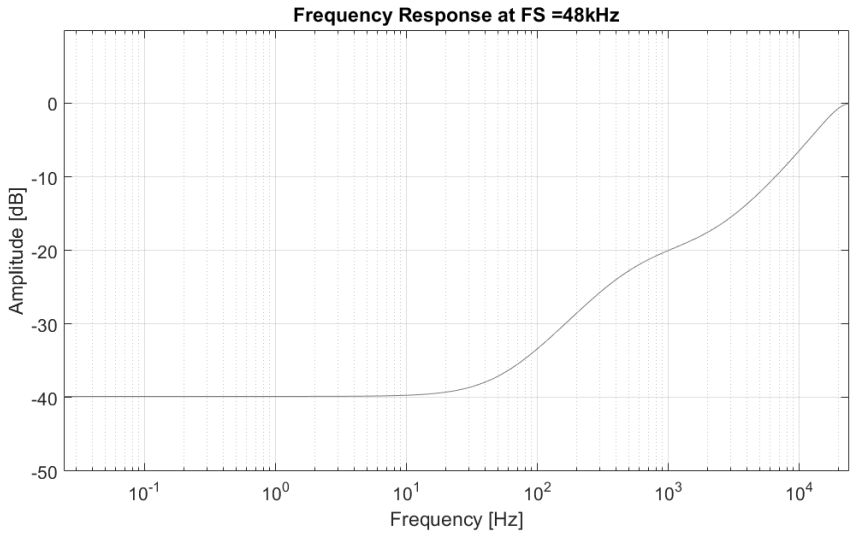
120 Hz High-pass filters (13-16) (21-24)					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				120	Hz
Stop band	-148 dB		0 FS		Hz

Table 29 - DBQ Filter Properties

DBQ Filter Frequency Response

The following frequency responses were obtained from software simulations of these filters.

Filter	Frequency Response
DC Blocking	
De-emphasis	

RIAA De-emphasis	
RIAA Pre-emphasis	

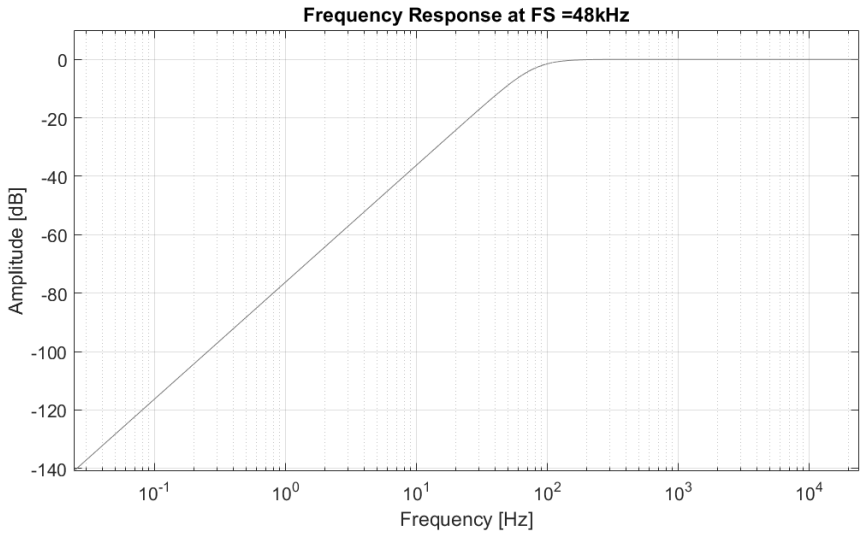
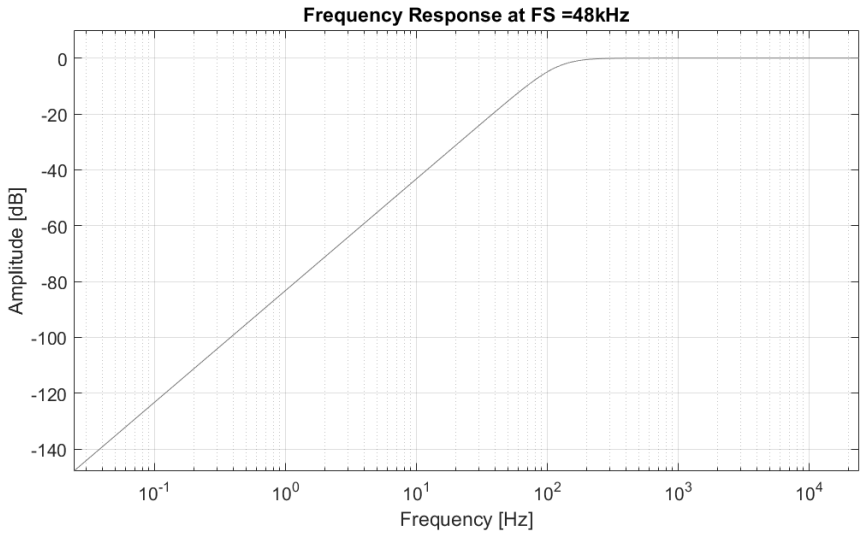
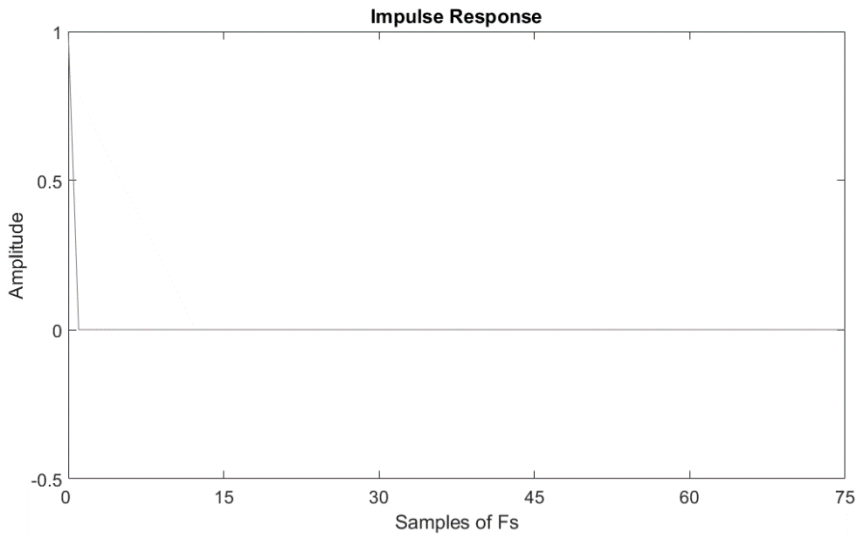
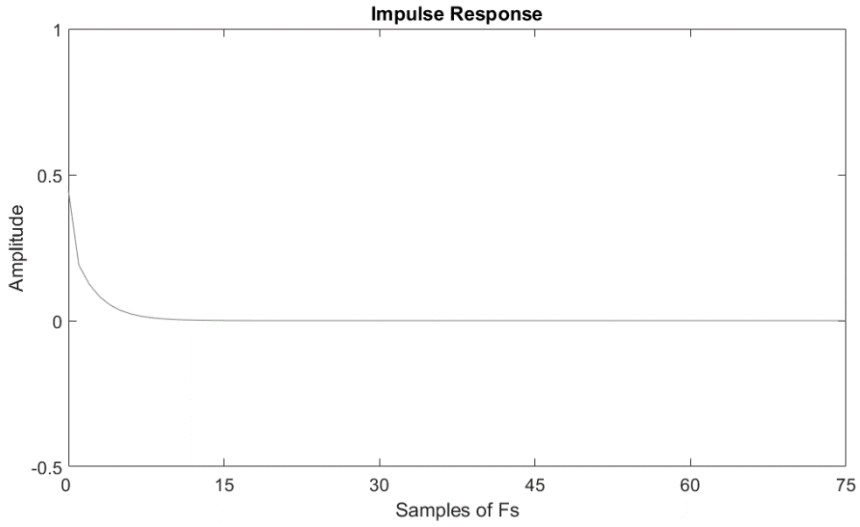
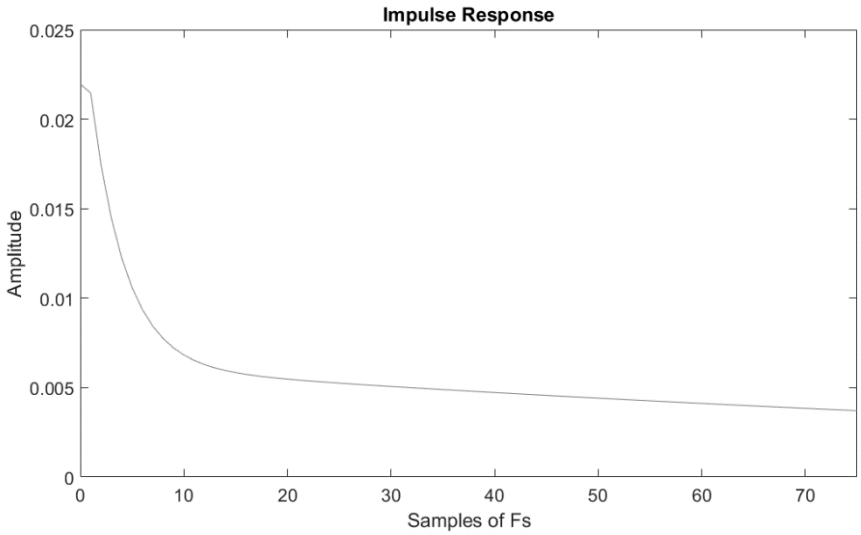
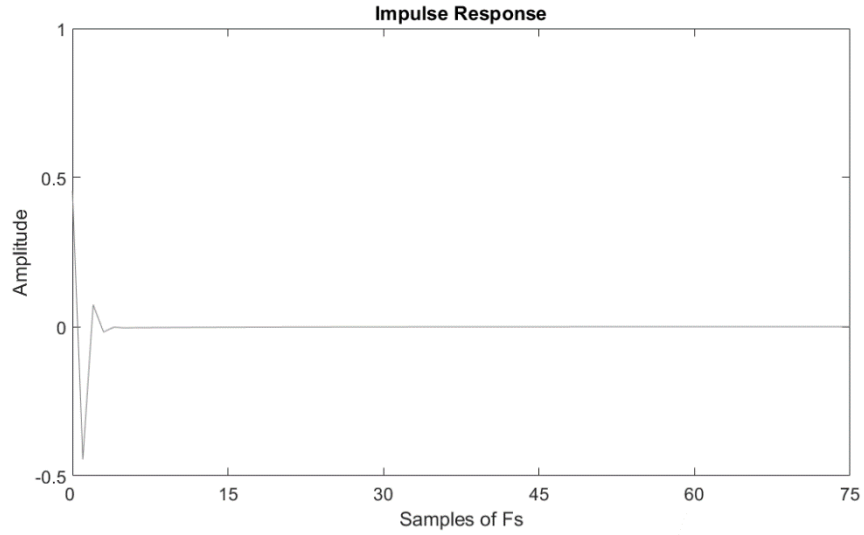
80Hz High-pass filter (9-12) (17-20)	
120Hz High-pass filter (13-16)(21-24)	

Table 30 - DBQ Filter Frequency Response

DBQ Filter Impulse Response

The following impulse responses were obtained from software simulations of these filters. They show the decimation path prior to down-sampling to 1FS and are scaled accordingly. The extra sample delay to get the data encoded accounts for external processing time to serialize data stream.

Filter	Impulse Response
DC Blocking	
De-emphasis	

RIAA De-emphasis	
RIAA Pre-emphasis	

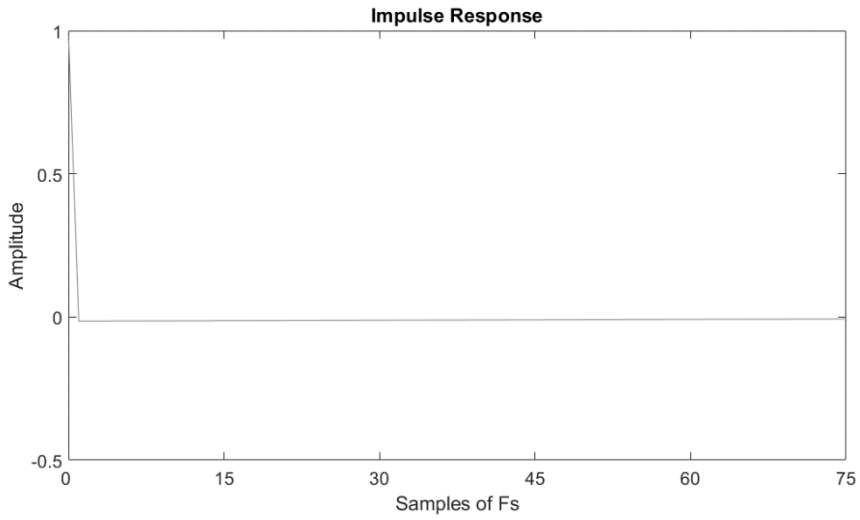
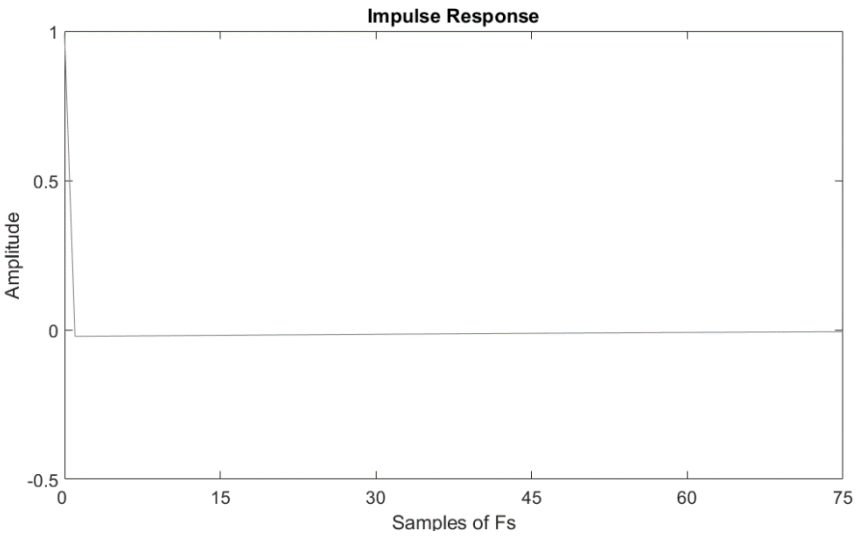
80Hz High-pass filter (9-12) (17-20)	
120Hz High-pass filter (13-16)(21-24)	

Table 31 - DBQ Filter Impulse Response

Daisy Chain

The ES9290 supports connecting multiple devices together in a daisy chain configuration. Up to 16 devices can be daisy chained together to output data onto any of the 32 channels in a TDM data line. The digital input to Chip#1 through DATA3 is output through GPIO1 for the Chip#2 down the chain. At the same time, the digital output from Chip #2's DATA2 is inputted through GPIO2 of Chip #1 to append to its DATA2 digital output. See Application Note for more information.

Note: GPIO2 on the last ES9290 of the Daisy Chain must be set to zero by pulling to ground through a 47Ω resistor.

Note: While operating in 32 or 24bit word widths, TDM must be configured into I²S mode.

Data Path	Output Pin	Input Pin
DAC	GPIO1	DATA3
ADC	DATA2	GPIO2

Table 32 - Daisy Chain Pins

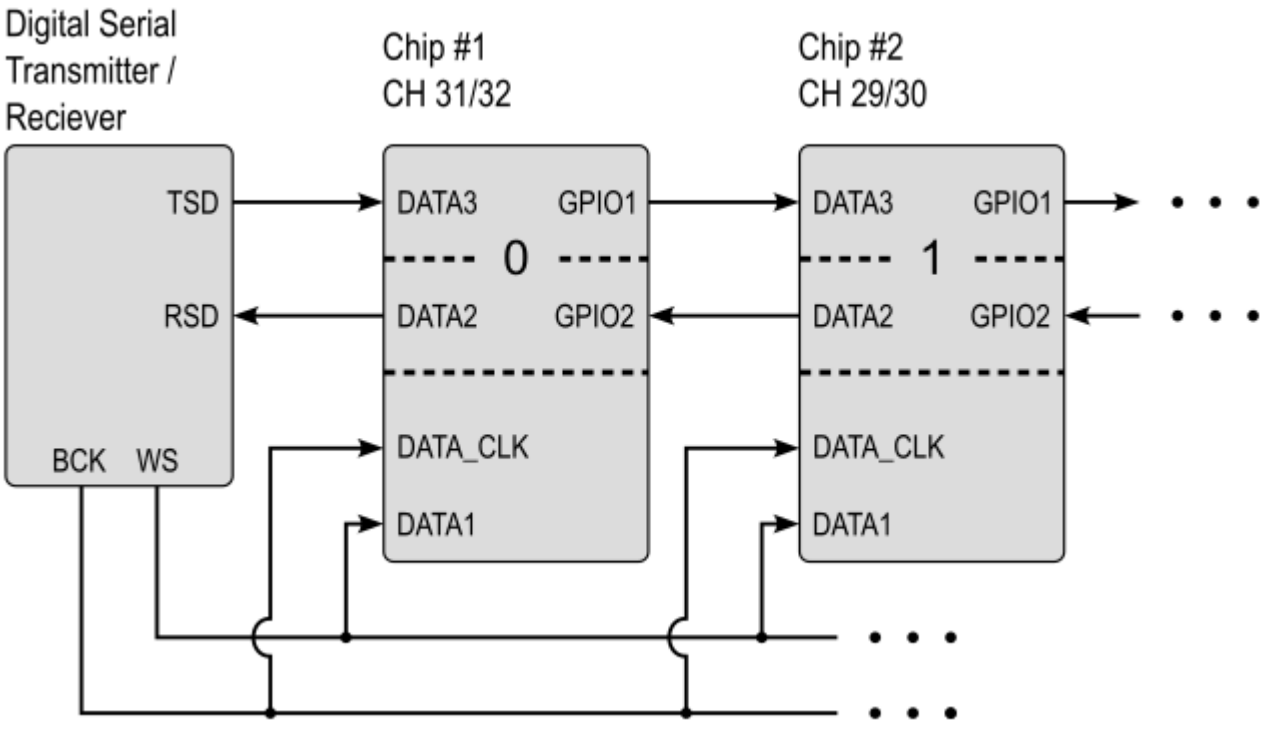


Figure 22 - Daisy Chain Configuration

Sample Rate Calculation

Acquiring the real time sample rate from the ES9290 can be accomplished using Register 230 AUTO FS READ.

Auto fs detect (Register 0[3] AUTO_FS_DETECT = 1'b1) must be set.

The below equation calculates the current auto detected sample rate by using a combination of register readback states.

$$FS\ [Hz] = \frac{Y * MCLK}{(X+1) * \left(\frac{128}{2^Z}\right)}$$

Variables

- {X}: Register 230[5:0] MCLK_128FS_DIV_AUTO
- {Y}: Register 230[6] MCLK_128FS_HALF_DIV_AUTO
  - 1'b0: Y=1
  - 1'b1: Y=2
- {Z}: Register 230[7] EN_64FS_MODE_AUTO
- MCLK: Master Clock rate

Example

For this example, let the variables be as follows:
X = 7, Y = 1, Z = 0, MCLK = 49.152 [MHz]

$$FS\ [Hz] = \frac{1 * 49.152MHz}{(7+1) * \left(\frac{128}{2^0}\right)} = \frac{49.152MHz}{8 * 128} = 48kHz$$

Audio Input and Output Formats

The ES9290 supports PCM or TDM serial input/output data formats along with PDM inputs.

Note: See PDM Decoder for more information on using PDM as an input source.

PCM (I²S, LJ)

PCM includes I²S and LJ with 2 channels/slots per data line. The ADC outputs can be mapped to any slot/channel of the PCM encoder output data (DATA2) using ADC_TDM_SLOT_SEL_CHx. The PCM decoder routes any slot/channel of the PCM input data (DATA3) to the DACs using DAC_TDM_SLOT_SEL_CHx.

Data is latched on the positive edge of BCLK.

Pin Name	Function	Description
DATA_CLK	PCM BCLK	PCM Clock (Bit Clock), Master or Slave
DATA1	PCM WS	PCM WS (Word Select/Frame Select), Master or Slave
DATA2	PCM Output Data	PCM Data Output from ADC
DATA3	PCM Input Data	PCM Data Input for DAC

Table 33 - PCM Pin Connections

Note: The PCM Decoder supports Right Justified (RJ) format in software mode for a single device.

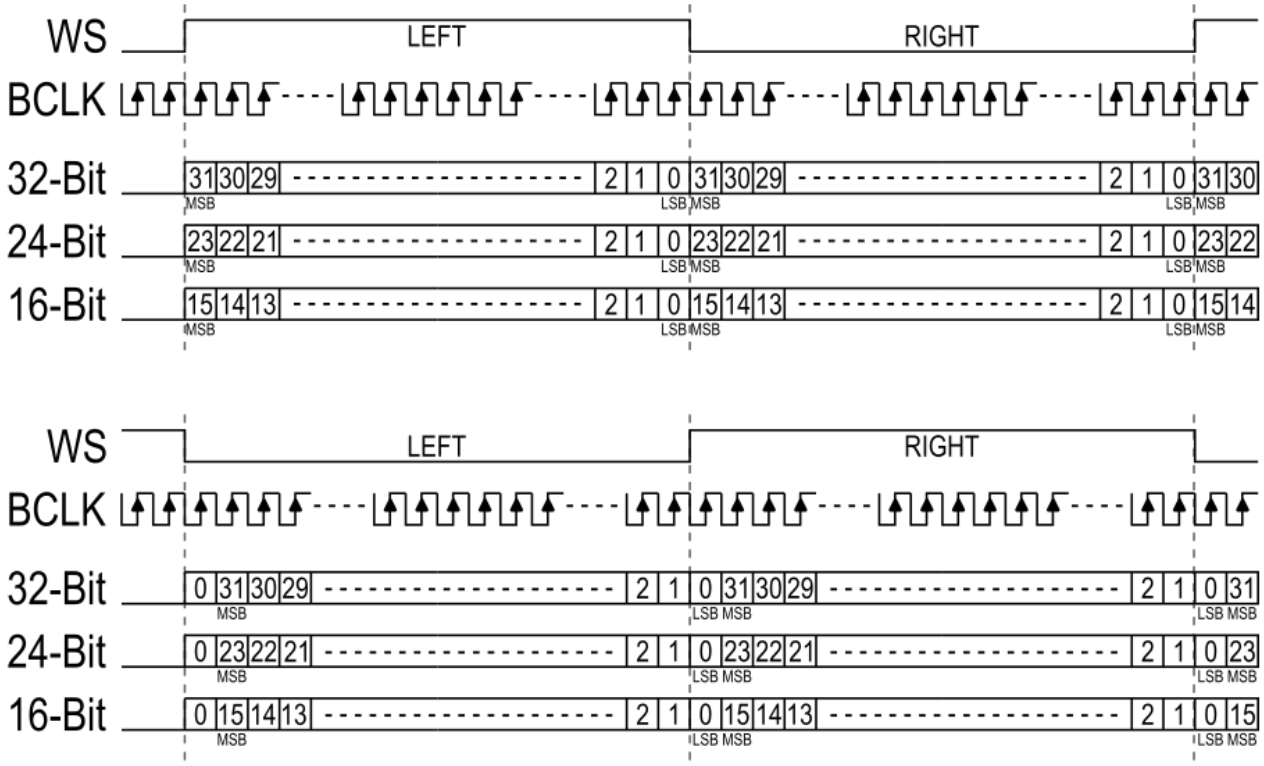


Figure 23 - LJ (top) & I²S (bottom) for 32, 24, and 16-bit Word Widths

TDM (Time Division Multiplexing)

The ES9290 supports TDM format, allowing more than 2 channels/slots to be transmitted and received on each data line, up to a maximum of 32 channels per data line. Supported formats are TDM4 (4ch), TDM8 (8ch), TDM16 (16ch) and TDM32 (32ch). The ADC outputs can be mapped to any slot of the TDM output data (DATA2) using ADC_TDM_SLOT_SEL_CHx. The DACs can choose any slot/channel of the TDM input data (DATA3) using DAC_TDM_SLOT_SEL_CHx.

Data is latched on the positive edge of BCLK.

Pin Name	Function	Description
DATA_CLK	TDM BCLK	TDM Clock, Master or Slave
DATA1	TDM WS	TDM WS, Master or Slave
DATA2	TDM Output Data	TDM Data Output from ADCs
DATA3	TDM Input Data	TDM Data Input for DACs

Table 34 - TDM Pin Connections

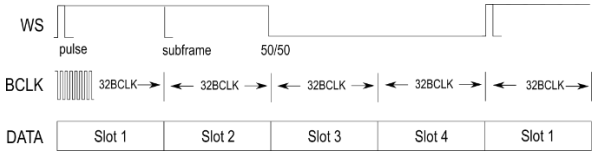


Figure 24 - TDM4 Mode

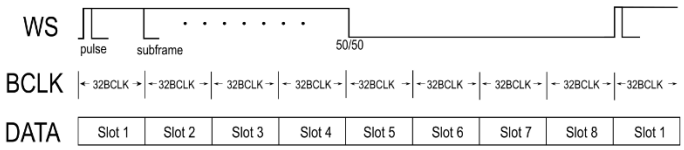


Figure 25 - TDM8 Mode

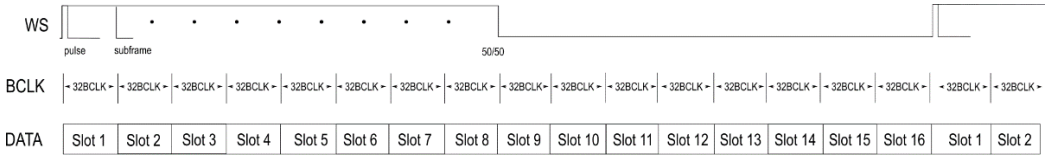


Figure 26 - TDM16 Mode

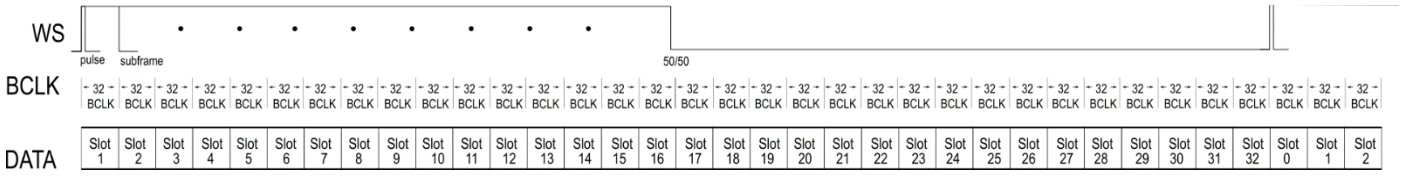


Figure 27 - TDM32 Mode

GPIO Configuration

GPIO_CONFIG	Function	I/O Direction
0	Analog Outputs Off	Shutdown
1	Mute DAC Channels	Input
2	Clock Valid Flag	Output
3	PLL Locked Flag	Output
4	DAC Minimum Volume Flag	Output
5	DAC Automute Status	Output
6	DAC Soft Ramp Done Flag	Output
7	ADC CH1 Peak Flag	Output
8	ADC CH2 Peak Flag	Output
9	PWM Signal	Output
10	OR of Status Bits	Output
11	BCK/WS Monitor	Output
12	MCLK_24M	Output
13	MCLK_128FS	Output
14	Output 1'b0	Output
15	Output 1'b1	Output

Table 35 - GPIO Configuration

GPIOx Default states:

GPIO1-8: Analog Shutdown

Analog Outputs Off

The GPIO is shutdown and has no functionality.

Mute DAC Channels

Mute both DAC channels and Direct Monitor.

Clock Valid Flag

Outputs HIGH if a MCLK source is detected. Outputs LOW when clock is removed or not present.

Relevant Registers

- Register 2[7] EN_CLK_DET must be asserted for the clock valid flag to operate.

PLL Locked Flag

Outputs HIGH if the PLL is locked.

Relevant Registers

- Register 0[5] FORCE_PLL_LOCK must be 1'b0 to see the status of the PLL, else this flag will output HIGH.

DAC Minimum Volume Flag

Outputs HIGH when the DAC is muted. This can occur from manually muting, automuting, and setting volume to 0xFF.

Relevant Registers

- Register 44[0] GPIO_AND_VOL_MIN sets the output to be the logical AND of both channels' mute flags.
- Register 44[3] GPIO_OR_VOL_MIN sets the output to be the logical OR of both channels' mute flags.
- Register 44[6] FLAG_CH_SEL selects which of the individual DAC channel flags to output.

DAC Automute Status

Outputs HIGH when the DACs automute condition is met.

Relevant Registers

- Register 44[1] GPIO_AND_AUTOMUTE sets the output to be the logical AND of both channels' automute flags.
- Register 44[4] GPIO_OR_AUTOMUTE sets the output to be the logical OR of both channels' automute flags.
- Register 44[6] FLAG_CH_SEL selects which of the DAC channel flags to output.

DAC Soft Ramp Done Flag

Outputs HIGH when the DAC is neither ramping up nor down.

Relevant Registers

- Register 44[2] GPIO_AND_SS_RAMP sets the output to be the logical AND of both channels' automute flags.
- Register 44[5] GPIO_OR_SS_RAMP sets the output to be the logical OR of both channels' automute flags.
- Register 44[6] FLAG_CH_SEL selects which of the DAC channel flags to output.

ADC CHx Peak Flag

Outputs the latched peak detector flags. Flags will become HIGH when then channels peak has gone above the peak threshold and will stay high until cleared.

Relevant Registers

- Register 90-91 PEAK_THRESH_CHx sets the peak threshold.
- Register 88[1:0] PEAK_DETECT_CHx_EN is required to be set for the peak detector logic to function.
- Register 18[1:0] STATUS_MASK_CHx_PEAK_LATCH is required to be set for the GPIO output to be active.
- Register 19[1:0] STATUS_CLEAR_CHx_PEAK_LATCH must be toggled HIGH-LOW for the latched flag to clear.

PWM Signal

Outputs a configurable PWM signal. The frequency and duty cycle of the PWM signal can be calculated with the following equations:

$$frequency\ [Hz] = \frac{MCLK}{PWM\_FREQ + 1}$$

$$Duty\ Cycle\ [\%] = \left(\frac{PWM\_COUNT}{PWM\_FREQ + 1}\right) \times 100$$

Relevant Registers

- Register 45 PWM_COUNT
- Register 46-47 PWM_FREQ

OR of all Status Bits

Outputs the logical OR of all the status flags. This includes the PLL Locked Flag, ADC CHx Peak Flag, and ADC CHx Peak Latch Flag.

BCK/WS Monitor

Outputs the status of the BCK and WS monitors. HIGH if either monitor detects an invalid signal.

BCK is considered invalid if the ratio MCLK/BCK > 1024.

WS is considered invalid if the ratio BCK/WS > 1024.

Relevant Registers

- Register 6[7] ENABLE_WS_MONITOR
- Register 6[6] ENABLE_BCK_MONITOR

MCLK_24M

Outputs the MCLK_24M clock. Requires the ADC to be on.

MCLK_128FS

Outputs the MCLK_128FS clock. Requires the ADC or DAC to be on.

Output 1'b0

Outputs a constant 1'b0.

Output 1'b1

Outputs a constant 1'b1.

Analog Features

PGA

The ES9290 features an integrated analog programmable gain amplifier (PGA) that can implement a gain from +0dB to +30dB in configurable steps of +3dB.

PGA Registers

- Register 82[3:0] PGA_GAIN_CTRL_CH1
- Register 82[7:4] PGA_GAIN_CTRL_CH2

APLL

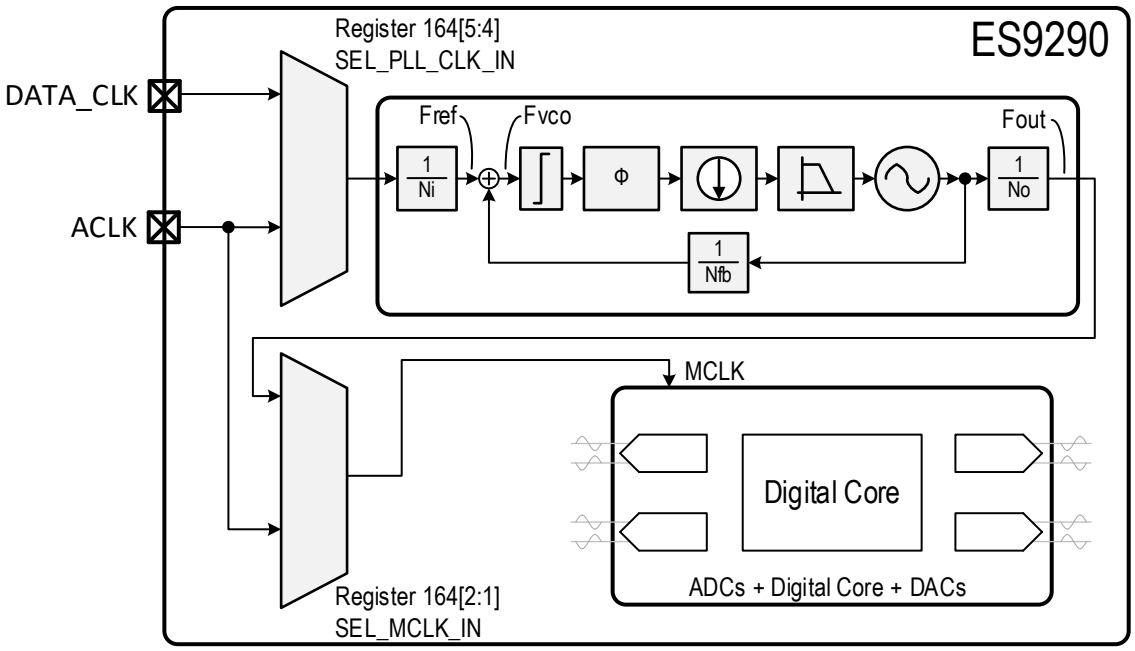


Figure 28 - Functional Block Diagram of ES9290 APLL

The ES9290 has a built in Analog PLL (APLL) for generating frequencies that are unavailable externally. For the application note on the APLL, please ask your FAE or distributor.

For calculation of the PLL frequency output, use the following formulas:

$$F_{ref} = \left(\frac{F_{in}}{N_i}\right) \qquad F_{vco} = \left(\frac{F_{in}}{N_i}\right) * N_{fb} \qquad N_{fb} = \frac{2^{25}}{FBDIV} \qquad F_{out} = \left(\frac{F_{in}}{N_i}\right) * \frac{N_{fb}}{N_o}$$

Where:

a. FBDIV is a 24-bit number
b. PLL frequency range requirements:
    a. Fref requirement: 2.5MHz < Fref < 12 MHz
    b. Fvco requirement: 90MHz < Fvco < 110MHz
    c. Fout requirement: 22.5792/24.576MHz
c. Ni = input divider
    - Accessible from Reg 172-170[8:0], PLL_CLK_IN_DIV
d. No = output divider
    - Accessible from Reg 172-170[15:12], PLL_CLK_OUT_DIV
e. Nfb = feedback divider
    - Accessible from Reg 167-169[23:0], PLL_CLK_FB_DIV

44.1kHz Base Rates (SYNC Slave Mode)							
FS (kHz)	**DATA_CLK (MHz)**	**Ni**	**Fref (MHz)**	**FBDIV**	**Fvco (MHz)**	**No**	**Fout (MHz)**
32-Bit Frame							
352.8	22.5792	2	11.2896	4194304	90.3168	4	22.5792
176.4	11.2896	1	11.2896	4194304	90.3168	4	22.5792
88.2	5.6448	1	5.6448	2097152	90.3168	4	22.5792
44.1	2.8224	1	2.8224	1048576	90.3168	4	22.5792
16-Bit Frame							
352.8	11.2896	1	11.2896	4194304	90.3168	4	22.5792
176.4	5.6448	1	5.6448	2097152	90.3168	4	22.5792
88.2	2.8224	1	2.8224	1048576	90.3168	4	22.5792
44.1	1.4112	1	1.4112	524288	90.3168	4	22.5792

Table 36 - APLL Divider Values for 44.1kHz Base Rates

48kHz Base Rates (SYNC Slave Mode)							
FS (kHz)	**DATA_CLK (MHz)**	**Ni**	**Fref (MHz)**	**FBDIV**	**Fvco (MHz)**	**No**	**Fout (MHz)**
32-Bit Frame							
384	24.576	2	12.288	4194304	98.304	4	24.576
192	12.288	1	12.288	4194304	98.304	4	24.576
96	6.144	1	6.144	2097152	98.304	4	24.576
48	3.072	1	3.072	1048576	98.304	4	24.576
16-Bit Frame							
384	12.288	1	12.288	4194304	98.304	4	24.576
192	6.144	1	6.144	2097152	98.304	4	24.576
96	3.072	1	3.072	1048576	98.304	4	24.576
48	1.536	1	1.536	524288	98.304	4	24.576

Table 37 - APLL Divider Values for 48kHz Base Rates

MICBIAS

The ES9290 integrates a low noise programmable regulator to power or bias external microphones through the MICBIAS pin (Pin 10). The MICBIAS voltage is nominally 2.85V and can be enabled by setting MB_PDB.

In hardware mode, the MICBIAS can be controlled using GPIO2/1, see GPIO Functions in Hardware Mode for more information.

MICBIAS Registers

- Register 94[3] MB_PDB
- Register 94[6] MB_VR_BYPB
    - For enabling voltage select
- Register 94[2:0] MC_VR_SET
    - For selecting voltage

Absolute Maximum Ratings

PARAMETER	RATING
Positive Supply Voltage • AVCC_ADC • AVCC_LD • AVCC_CP • AVDD	 • +3.7V with respect to Ground • +3.7V with respect to Ground • +3.7V with respect to Ground • +3.7V with respect to Ground
Storage Temperature	-65°C to +150°C
Operating Junction Temperature	+125°C
Voltage Range for Digital Input Pins	-0.3V to AVDD (nom) + 0.3V
Maximum/Minimum Input Voltage on IN_P and IN_M Pins	0V to 4.5V

Table 38 - Absolute Maximum Ratings

WARNING: Stresses beyond those listed under here may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied.

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

ESD Ratings

ESD Standard	Rating
Human Body Model (HBM), ANSI/ESDA/JEDEC JS-001	2kV
Charge Device Model (CDM), ANSI/ESDA/JEDEC JS-002	500V

Table 39 - ESD Ratings

I/O Electrical Characteristics

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNIT
High-level Input Voltage	VIH	(AVDD / 2) + 0.4		V
Low-level Input Voltage	VIL		0.4	V
High-level Output Voltage	VOH	AVDD - 0.2		V
Low-level Output Voltage	VOL		0.2	V

Table 40 - I/O Electrical Characteristics

Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Operating Temperature	T_A	-20°C to +85°C
AVCC_ADC		+3.3V
AVCC_LD		+3.3V
AVCC_CP		+3.3V
AVDD		+3.3V
DVDD		Internal
VREF_BUF		Internal
VREF		Internal
MICBIAS		Internal
PLL_REG		Internal
PNEG		Internal
IN_M / IN_P DC Offset		1.4V
IN_M / IN_P Input Voltage		1Vrms (2.8Vpp)

Table 41 - Recommended Operating Conditions

Recommended Power Up/Down Sequence

It is recommended for powering up that AVDD turns on ~200us before AVCC_LD, AVCC_CP and AVCC_ADC turn on.

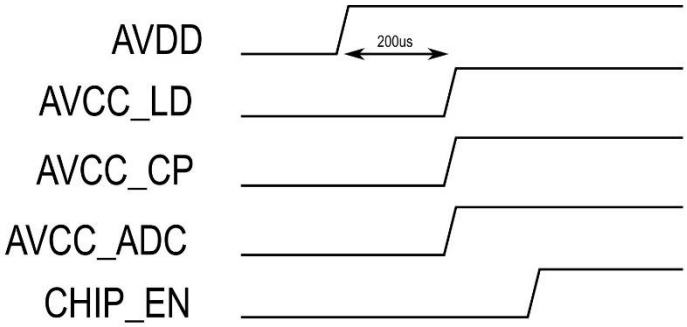


Figure 29 - Recommended Power Up Sequence

For powering down, first make CHIP_EN low, then AVCC_LD, AVCC_CP and AVCC_ADC turn off, then AVDD turns off.

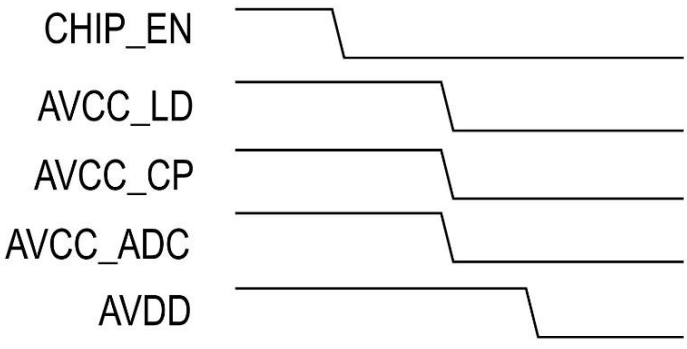


Figure 30 - Recommended Power Down Sequence

Power Consumption

Test Conditions (unless otherwise noted)

T_A = 25ºC, AVCC_ADC = AVCC_LD = AVCC_CP = AVDD = +3.3V, 1.8Vrms differential input, 0dBFS digital input.

AVDD supply includes DVDD current.

Parameter	Min	Typ.	Max	Unit
Standby (CHIP_EN=0)				
AVCC_ADC		0.1		µA
AVCC_LD		0.1		µA
AVCC_CP		0.1		µA
AVDD		0.4		µA
HW Mode 0-2, 4-6 (I²S /LJ Master, 32bit), MCLK = 24.576MHz				
AVCC_ADC		19		mA
AVCC_LD		6.5		mA
AVCC_CP		8		mA
AVDD for HW2/HW6, Fs=48kHz		14		mA
AVDD for HW1/HW5, Fs=96kHz		19		mA
AVDD for HW0/HW4, Fs=192kHz		29		mA
HW Mode 8, 12 (I²S /LJ Slave, 32bit), MCLK = 24.576MHz				
AVCC_ADC		18.5		mA
AVCC_LD		6.5		mA
AVCC_CP		8		mA
AVDD for HW8/HW12, Fs=48kHz		10		mA
AVDD for HW8/HW12, Fs=96kHz		13		mA
AVDD for HW8/HW12, Fs=192kHz		18		mA
AVDD for HW8/HW12, Fs=384kHz		19		mA

Table 42 - Power Consumption

Note: Current consumption can be reduced by externally supplying DVDD with 1.2V to decrease AVDD current.

Performance

Test Conditions 1 (unless otherwise noted)
T_A = 25ºC, AVCC_ADC = AVCC_LD = AVCC_CP = AVDD = +3.3V, fs = 48kHz, HW mode (I^2S Master Mode)

Note: Performance numbers were measured using the ESS ES9290 1v0 evaluation board.

Parameter			Min	Typ.	Max	Unit
ADC Analog Input Characteristics:						
Resolution					32	Bit
Input Voltage		0dBFS		2		V_{rms}
Input DC Common Mode				1.67		V_{dc}
Input Impedance				5		kΩ
Stereo THD+N Ratio (1.8Vrms differential input)	fs=48kHz BW=20Hz-20kHz	-1dBFS		-108		dB
	fs=96kHz BW=20Hz-40kHz	-1dBFS		-106		dB
	fs=192kHz BW=20Hz-80kHz	-1dBFS		-104		dB
	fs=384kHz BW=20Hz-100kHz	-1dBFS		-103		dB
Stereo Dynamic Range (2mVrms differential input)	A-weighted	-60dBFS		116		dB
Mono Dynamic Range (2mVrms differential input)	A-weighted	-60dBFS		119		dB

Table 43 – ES9290 ADC Performance

Parameter			Min	Typ.	Max	Unit
DAC Analog Output Characteristics:						
Resolution					32	Bit
Output Voltage		0dBFS		2		V_{rms}
Output DC Voltage				0		V
Stereo THD+N Ratio (0dBFS input, single ended output)	fs=48kHz BW=20Hz-20kHz	2Vrms		-110		dB
	fs=96kHz BW=20Hz-40kHz	2Vrms		-108		dB
	fs=192kHz BW=20Hz-80kHz	2Vrms		-106		dB
	fs=384kHz BW=20Hz-100kHz	2Vrms		-104		dB
Mono THD+N Ratio (0dBFS input, differential output)	fs=48kHz BW=20Hz-20kHz	4Vrms		-116		dB
Stereo Dynamic Range (-60dBFS input, single ended output)	A-weighted	2mVrms		116		dB
Mono Dynamic Range (-60dBFS input, mono single ended output)	A-weighted	2mVrms		119		dB
Mono Dynamic Range (-60dBFS input, differential output)	A-weighted	4mVrms		122		dB

Table 44 – ES9290 DAC Performance

Register Overview

A system clock is not required to access registers.

Read/Write Register Addresses

Registers 0-178 (0x00 - 0xB2) are read and write registers.

Read-Only Register Addresses

Register 224-251 (0xE0 - 0xFB) are read only registers.

Multi-Byte Registers

Multi-Byte registers must be written from LSB to MSB. Data is latched when MSB is written.
Multi-Byte registers must be read from LSB to MSB. Data is latched when LSB is read.
MSB is always stored in the highest register address.

Register Map

Addr (Hex)	Addr (Dec)	Register	7	6	5	4	3	2	1	0
0x00	0	SYS CONFIG	SOFT_RESET	RESERVED	FORCE_PLL_LOCK	AUTO_FS_DETECT_BLOCK_64FS	AUTO_FS_DETECT	ENABLE_64FS_MODE	ENABLE_DAC	ENABLE_ADC
0x01	1	CODEC CONFIG	RESERVED						ENABLE_TDM_DECODE	ENABLE_TDM_ENCODE
0x02	2	FRONT-END CLOCK CONTROL	EN_CLK_DET	MCLK_128FS_HALF_DIV	MCLK_128FS_DIV					
0x03	3	BACK-END CLOCK CONTROL	DAC_CLK_INV	RESERVED		MCLK_24M_DIV2	RESERVED			
0x04	4	PCM MASTER CLK CONFIG	MASTER_BCK_DIV							
0x05	5	TDM CONFIG 1	TDM_RESYNC	AUTO_CH_DETECT	RESERVED	TDM_CH_NUM				
0x06	6	TDM CONFIG 2	ENABLE_WS_MONITOR	ENABLE_BCK_MONITOR	TDM_WORD_WIDTH		TDM_BIT_DEPTH		TDM_VALID_EDGE	TDM_LJ
0x07	7	ADC TDM CH1 SLOT CONFIG	RESERVED		ADC_16BIT_DITHER_SHAPE	ADC_TDM_SLOT_SEL_CH1				
0x08	8	ADC TDM CH2 SLOT CONFIG	RESERVED			ADC_TDM_SLOT_SEL_CH2				
0x09	9	DAC TDM CH1 SLOT CONFIG	RESERVED			DAC_TDM_SLOT_SEL_CH1				
0x0A	10	DAC TDM CH2 SLOT CONFIG	RESERVED			DAC_TDM_SLOT_SEL_CH2				
0x0B	11	ADC DAISY CHAIN	RESERVED		ADC_TDM_DAISY_CHAIN	ADC_TDM_DATA_LATCH_ADJ				
0x0C	12	DAC DAISY CHAIN	RESERVED		DAC_TDM_DAISY_CHAIN	DAC_TDM_DATA_LATCH_ADJ				
0x0D	13	PCM MASTER MODE CONFIG	SLAVE_BCK_INVERT	RESERVED		MASTER_WS_CLK_PHASE	MASTER_WS_PULSE_MODE	MASTER_WS_INVERT	MASTER_BCK_INVERT	MASTER_MODE_EN
0x0E	14	VOLUME UP RAMP RATE	VOL_RAMP_RATE_UP							
0x0F	15	VOLUME DOWN RAMP RATE	VOL_RAMP_RATE_DOWN							
0x10	16	SYNC CONFIG	RESERVED							
0x11	17	AUTO SYNC CONFIG	RESERVED				AUTO_MCLK_24M_PHASE_SYNC	AUTO_WS_PHASE_SYNC	AUTO_ICG_SYNC	AUTO_FS_CLK_GEN_SYNC
0x12	18	STATUS BITS MASK	RESERVED			STATUS_MASK_PLL_LOCKED	STATUS_MASK_CH2_PEAK_DET	STATUS_MASK_CH1_PEAK_DET	STATUS_MASK_CH2_PEAK_LATCH	STATUS_MASK_CH1_PEAK_LATCH
0x13	19	STATUS BITS CLEAR	RESERVED						STATUS_CLEAR_CH2_PEAK_LATCH	STATUS_CLEAR_CH1_PEAK_LATCH
0x14	20	RESERVED	RESERVED							
0x15	21	CHARGE PUMP CONFIG	RESERVED							CP_PDB_MUTE
0x16	22	RESERVED	RESERVED							
0x17	23	CHARGE PUMP CLOCK DIV	CP_CLK_DIV							
0x18-0x26	24-38	RESERVED	RESERVED							
0x27	39	GPIO1/2 CONFIG	GPIO2_CFG				GPIO1_CFG			
0x28	40	GPIO3/4 CONFIG	GPIO4_CFG				GPIO3_CFG			
0x29	41	GPIO CONTROLS	GPIO4_SDB	GPIO3_SDB	GPIO2_SDB	GPIO1_SDB	GPIO4_OE	GPIO3_OE	GPIO2_OE	GPIO1_OE
0x2A	42		INVERT_GPIO4	INVERT_GPIO3	INVERT_GPIO2	INVERT_GPIO1	GPIO4_WK_EN	GPIO3_WK_EN	GPIO2_WK_EN	GPIO1_WK_EN
0x2B	43	GPIO READ	RESERVED				GPIO4_READ	GPIO3_READ	GPIO2_READ	GPIO1_READ
0x2C	44	GPIO OUTPUT LOGIC	RESERVED	FLAG_CH_SEL	GPIO_OR_SS_RAMP	GPIO_OR_AUTOMUTE	GPIO_OR_VOL_MIN	GPIO_AND_SS_RAMP	GPIO_AND_AUTOMUTE	GPIO_AND_VOL_MIN
0x2D	45	PWM COUNT	PWM_COUNT							
0x2E	46	PWM FREQUENCY	PWM_FREQ							
0x2F	47		PWM_FREQ							
0x30	48	ADC DBQ COEFF SEL	ADC_DBQ_CLK_FAMILY_SEL	ADC_DBQ_80HZ_HPF_EN	ADC_DBQ_120HZ_HPF_EN	ADC_DBQ_COEFF_SEL				
0x31	49	ADC PROG DBQ A2 COEFF	ADC_DBQ_A2							
0x32	50		ADC_DBQ_A2							
0x33	51		ADC_DBQ_A2							
0x34	52	ADC PROG DBQ A1 COEFF	ADC_DBQ_A1							
0x35	53		ADC_DBQ_A1							
0x36	54		ADC_DBQ_A1							
0x37	55	ADC PROG DBQ B2 COEFF	ADC_DBQ_B2							
0x38	56		ADC_DBQ_B2							
0x39	57		ADC_DBQ_B2							
0x3A	58	ADC PROG DBQ B1 COEFF	ADC_DBQ_B1							
0x3B	59		ADC_DBQ_B1							
0x3C	60		ADC_DBQ_B1							
0x3D	61	ADC PROG DBQ B0 COEFF	ADC_DBQ_B0							
0x3E	62		ADC_DBQ_B0							
0x3F	63		ADC_DBQ_B0							
0x40	64	ADC FIR FILTER	ADC_FILTER_SHAPE			RESERVED				
0x41	65	ADC DC BLOCKING	CH2_DC_BLOCK_EN	CH1_DC_BLOCK_EN	RESERVED					
0x42	66	PDM CONFIG	RESERVED	PDM_INPUT_SEL	PDM_SAMPLE_EDGE	PDM_PHASE	RESERVED			
0x43	67	PDM CLK SELECT	RESERVED	MCLK_PDM_DIV						
0x44	68	ADC VOLUME CH1	ADC_VOLUME_CH1							

0x45	69	ADC VOLUME CH2	ADC_VOLUME_CH2						
0x46	70	ADC MIX VOLUME CH1	ADC_MIX_VOL_CH1						
0x47	71	ADC MIX VOLUME CH2	ADC_MIX_VOL_CH2						
0x48	72	ADC DIGITAL GAIN	RESERVED	ADC_DIGITAL_GAIN_CH2			RESERVED	ADC_DIGITAL_GAIN_CH1	
0x49	73	ADC PHASE INVERSION	RESERVED				ADC_MIX_VOL_PHASE_INV_CH2	ADC_MIX_VOL_PHASE_INV_CH1	ADC_VOL_PHASE_INV_CH2	ADC_VOL_PHASE_INV_CH1
0x4A-0x51	74-81	RESERVED	RESERVED						
0x52	82	PGA GAIN CONTROL	PGA_GAIN_CTRL_CH2				PGA_GAIN_CTRL_CH1		
0x53-0x57	83-87	RESERVED	RESERVED						
0x58	88	PEAK DETECT ENABLE	RESERVED					PEAK_DETECT_CH2_EN	PEAK_DETECT_CH1_EN
0x59	89	PEAK DETECT CONFIG	RESERVED	LOCK_PEAK_VALUE	RESERVED	PEAK_DECAY_RATE			
0x5A	90	PEAK THRESHOLDS	PEAK_THRESH_CH1						
0x5B	91		PEAK_THRESH_CH2						
0x5C-0x5D	92-93	RESERVED	RESERVED						
0x5E	94	MIC BIAS	RESERVED	MB_VR_BYPB	RESERVED		MB_PDB	MB_VR_SET	
0x5F-0X63	95-99	RESERVED	RESERVED						
0x64	100	DAC NSMOD SEL	RESERVED						NSMOD_CH2_SEL
0x65	101	RESERVED	RESERVED						
0x66	102	DAC DBQ COEFF SEL	RESERVED		DAC_DBQ_COEFF_SEL				
0x67	103	DAC PROG DBQ A2 COEFF	DAC_DBQ_A2						
0x68	104		DAC_DBQ_A2						
0x69	105		DAC_DBQ_A2						
0x6A	106	DAC PROG DBQ A1 COEFF	DAC_DBQ_A1						
0x6B	107		DAC_DBQ_A1						
0x6C	108		DAC_DBQ_A1						
0x6D	109	DAC PROG DBQ B2 COEFF	DAC_DBQ_B2						
0x6E	110		DAC_DBQ_B2						
0x6F	111		DAC_DBQ_B2						
0x70	112	DAC PROG DBQ B1 COEFF	DAC_DBQ_B1						
0x71	113		DAC_DBQ_B1						
0x72	114		DAC_DBQ_B1						
0x73	115	DAC PROG DBQ B0 COEFF	DAC_DBQ_B0						
0x74	116		DAC_DBQ_B0						
0x75	117		DAC_DBQ_B0						
0x76	118	DAC FILTER CONFIG	RESERVED		BYPASS_IIR	BYPASS_FIR4X	BYPASS_FIR2X	DAC_FILTER_SHAPE	
0x77-0x7A	119-122	RESERVED	RESERVED						
0x7B	123	DAC VOLUME CH1	DAC_VOLUME_CH1						
0x7C	124	DAC VOLUME CH2	DAC_VOLUME_CH2						
0x7D	125	DAC MIX VOLUME CH1	DAC_MIX_VOL_CH1						
0x7E	126	DAC MIX VOLUME CH2	DAC_MIX_VOL_CH2						
0x7F	127	DIRECT MONITOR VOLUME CH1	DIR_MON_VOL_CH1						
0x80	128	DIRECT MONITOR VOLUME CH2	DIR_MON_VOL_CH2						
0x81-0x86	129-134	RESERVED	RESERVED						
0x87	135	DAC DIGITAL GAIN	DIR_MON_MUTE_CH2	DAC_DIGITAL_GAIN_CH2			DIR_MON_MUTE_CH1	DAC_DIGITAL_GAIN_CH1	
0x88	136	DAC PHASE INVERSION	DIR_MON_MONO_CH2	DIR_MON_MONO_CH1	DIR_MON_VOL_PHASE_INV_CH2	DIR_MON_VOL_PHASE_INV_CH1	DAC_MIX_VOL_PHASE_INV_CH2	DAC_MIX_VOL_PHASE_INV_CH1	DAC_VOL_PHASE_INV_CH2	DAC_VOL_PHASE_INV_CH1
0x89	137	DAC MUTE	RESERVED						DAC_MUTE_CH2	DAC_MUTE_CH1
0x8A	138	SOFT RAMP CONFIG	RESERVED		MUTE_RAMP_TO_GROUND	SOFT_RAMP_TIME			
0x8B	139	AUTOMUTE ENABLE	RESERVED						AUTOMUTE_EN_CH2	AUTOMUTE_EN_CH1
0x8C	140	AUTOMUTE TIME	AUTOMUTE_TIME						
0x8D	141		RESERVED					AUTOMUTE_TIME	
0x8E	142	AUTOMUTE LEVEL	AUTOMUTE_LEVEL						
0x8F	143		AUTOMUTE_LEVEL						
0x90	144	AUTOMUTE OFF LEVEL	AUTOMUTE_OFF_LEVEL						
0x91	145		AUTOMUTE_OFF_LEVEL						
0x92-0xA3	146-164	RESERVED	RESERVED						
0xA4	164	PLL CLOCK SELECT	RESERVED	PLL_CLK_PHASE_INV	SEL_PLL_CLK_IN		EN_PLL_CLK_IN	SEL_MCLK_IN		EN_MCLK_IN
0xA5	165	PLL VCO & CP	RESERVED				PLL_CP_PDB	PLL_VCO_PDB	PLL_CLKSMP_PDB	PLL_DIG_RSTB
0xA6	166	PLL REGULATOR	RESERVED				PLL_REG_PDB	RESERVED		
0xA7	167	PLL FEEDBACK DIV	PLL_CLK_FB_DIV						
0xA8	168		PLL_CLK_FB_DIV						
0xA9	169		PLL_CLK_FB_DIV						
0xAA	170	PLL IN & OUT DIV	PLL_CLK_IN_DIV						

0xAB	171		PLL_CLK_OUT_DIV				RESERVED		PLL_FB_DIV_LOAD	PLL_CLK_IN_DIV
0xAC-0xB2	172-178	RESERVED	RESERVED							
0xE0	224	CODEC VALIDITY READ	PLL_LOCKED	DAC_TDM_VALID	ADC_TDM_VALID	AUTO_CH_NUM				
0xE1	225	CHIP ID	CHIP_ID							
0xE2-0xE5	226-229	RESERVED	RESERVED							
0xE6	230	AUTO FS READ	EN_64FS_MODE_AUTO	MCLK_128FS_HALF_DIV_AUTO	MCLK_128FS_DIV_AUTO					
0xE7	231	BCK/WS VALID	RESERVED					RATIO_VALID	BCK_INVALID	WS_INVALID
0xE8	232	GPIO READBACK	RESERVED				GPIO4_R	GPIO3_R	GPIO2_R	GPIO1_R
0xE9	233	PEAK FLAG	PEAK_FLAG_LAT_CH2	PEAK_FLAG_LAT_CH1	PEAK_FLAG_CH2	PEAK_FLAG_CH1	RESERVED			
0xEA-0xED	234-237	RESERVED	RESERVED							
0xEE	238	PEAK CH1 READ	PEAK_CH1							
0xEF	239		PEAK_CH1							
0xF0	240	PEAK CH2 READ	PEAK_CH2							
0xF1	241		PEAK_CH2							
0xF2	242	DAC VOL MIN READ	RESERVED						VOL_MIN_CH2	VOL_MIN_CH1
0xF3	243	DAC AUTOMUTE READ	RESERVED						AUTOMUTE_CH2	AUTOMUTE_CH1
0xF4	244	DAC SOFT RAMP UP READ	RESERVED						SS_RAMP_UP_CH2	SS_RAMP_UP_CH1
0xF5	245	DAC SOFT RAMP DOWN READ	RESERVED						SS_RAMP_DOWN_CH2	SS_RAMP_DOWN_CH1
0xF6-0xFB	246-251	RESERVED	RESERVED							

Table 45 - Register Map

Register Listing

System Registers

Register 0: SYS CONFIG

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b1	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SOFT_RESET	Performs soft reset to digital core, resetting registers to their power-on defaults.
[6]	RESERVED	N/A
[5]	FORCE_PLL_LOCK	Clock locking status control with PLL_LOCKED. • 1'b0: clock locking status is determined by PLL_LOCKED • 1'b1: Ignore PLL_LOCKED signal, set lock status to 1'b1
[4]	AUTO_FS_DETECT_BLOCK_64FS	Block AUTO_FS_DETECT from transitioning to 64FS mode when the detected MCLK/MCLK_128FS ratio is 64. • 1'b0: Disabled (default) • 1'b1: Enabled
[3]	AUTO_FS_DETECT	Automatically determine optimal MCLK/MCLK_128FS ratio, from detected FS. • 1'b0: Disabled, use MCLK_128FS_DIV to set ratio. • 1'b1: Enabled, overrides MCLK_128FS_DIV (default)
[2]	ENABLE_64FS_MODE	Enables 64FS mode for 768k sample rate. • 1'b0: Disabled (default) • 1'b1: Enabled
[1]	ENABLE_DAC	Enables the DAC interpolation path. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	ENABLE_ADC	Enables the ADC decimation path. • 1'b0: Clock disabled (default) • 1'b1: Clock enabled

Register 1: CODEC CONFIG

Bits	[7:2]	[1]	[0]
Default	6'd0	1'b1	1'b1

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1]	ENABLE_TDM_DECODE	Enables I2S/TDM decoding clock. • 1'b0: I2S/TDM clock disabled • 1'b1: I2S/TDM clock enabled (default)
[0]	ENABLE_TDM_ENCODE	Enables I2S/TDM encoding clock. • 1'b0: I2S/TDM clock disabled • 1'b1: I2S/TDM clock enabled (default)

Register 2: FRONT-END CLOCK CONTROL

Bits	[7]	[6]	[5:0]
Default	1'b0	1'b0	6'd3

Bits	Mnemonic	Description
[7]	EN_CLK_DET	Enable the clock detection circuit, sets the CLK_AVALID signal. • 1'b0: Disabled (default) • 1'b1: Enabled
[6]	MCLK_128FS_HALF_DIV	• 1'b0: Divide by SELECT_ADC_NUM + 1 (default) • 1'b1: Divide by half of SELECT_ADC_NUM + 1 Note: Can only produce half of an odd number divide
[5:0]	MCLK_128FS_DIV	Whole number divide value + 1 for MCLK_128FS (MCLK/divide_value). • 6'd0: Whole number divide value + 1 = 1 • 6'd3: Whole number divide value + 1 = 4 (default)

Register 3: BACK-END CLOCK CONTROL

Bits	[7]	[6:5]	[4]	[3:0]
Default	1'b0	2'b00	1'b0	4'b1000

Bits	Mnemonic	Description
[7]	DAC_CLK_INV	Inverts the phase of the analog DAC_CLK. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[6:5]	RESERVED	N/A
[4]	MCLK_24M_DIV2	Sets the rate of MCLK_24M as well as the analog ADC_CLK, relative to MCLK. Both clocks must be running at 22.5792 MHz or 24.576 MHz. • 1'b0: Rate = MCLK (default) • 1'b1: Rate = MCLK/2
[3:0]	RESERVED	N/A

Register 4: PCM MASTER CLK CONFIG

Bits	[7:0]
Default	8'd7

Bits	Mnemonic	Description
[7:0]	MASTER_BCK_DIV	Master mode DCLK and WS generation clock divider. Whole number divide value + 1 for CLK_BCK_WS_GEN (MCLK/divide_value).

Register 5: TDM CONFIG 1

Bits	[7]	[6]	[5]	[4:0]
Default	1'b0	1'b0	1'b0	5'd1

Bits	Mnemonic	Description
[7]	TDM_RESYNC	Force TDM encoder & decoder to resync. • 1'b0: Enable TDM codec synchronization (default) • 1'b1: Force TDM codec to desynchronize.
[6]	AUTO_CH_DETECT	Automatically determine the number of TDM channels in a sample, based on the BCK/WS ratio. • 1'b0: Disabled, use TDM_CH_NUM to set channels (default) • 1'b1: Enabled, overrides TDM_CH_NUM Note: Only active in TDM slave mode.
[5]	RESERVED	N/A
[4:0]	TDM_CH_NUM	Sets number of channels in each frame. • 5'd0: 1 channel • 5'd1: 2 channels (default) • 5'd31: 32 channels

Register 6: TDM CONFIG 2

Bits	[7]	[6]	[5:4]	[3:2]	[1]	[0]
Default	1'b1	1'b1	2'b00	2'b00	1'b0	1'b0

Bits	Mnemonic	Description
[7]	ENABLE_WS_MONITOR	Enable WS monitor, used to detect the validity of the WS signal. WS is considered invalid if BCK/WS > 1024. • 1'b0: Disabled • 1'b1: Enabled (default)
[6]	ENABLE_BCK_MONITOR	Enable BCK monitor, used to detect the validity of the BCK signal. BCK is considered invalid if MCLK/BCK > 256. • 1'b0: Disabled • 1'b1: Enabled (default)
[5:4]	TDM_WORD_WIDTH	Sets the width, in bits, of one data word / subframe. A subframe is a frame divided by the number of channels. • 2'b00: 32-bits (default) • 2'b01: 24-bits • 2'b10: 16-bits
[3:2]	TDM_BIT_DEPTH	Sets the bit depth, number of data bits, in one data word / subframe. • 2'b00: 32-bit (default) • 2'b01: 24-bit • 2'b10: 16-bit
[1]	TDM_VALID_EDGE	Sets which WS edge the frame starts on. • 1'b0: Frame starts on negedge of WS (default) • 1'b1: Frame starts on posedge of WS
[0]	TDM_LJ	Sets left-justified mode. • 1'b0: One BCK period delay (default) • 1'b1: Left-justified

Register 7: ADC TDM CH1 SLOT CONFIG

Bits	[7:6]	[5]	[4:0]
Default	2'd0	1'b0	5'd0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	ADC_16BIT_DITHER_SHAPE	Sets the shape of the 16-bit data output dither. • 1'b0: 1st order noise shaped (default) • 1'b1: Flat noise shaped
[4:0]	ADC_TDM_SLOT_SEL_CH1	Selects which TDM channel slot is filled by ADC CH1 data. • 5'd0: Slot 1 (default) • 5'd31: Slot 32

Register 8: ADC TDM CH2 SLOT CONFIG

Bits	[7:5]	[4:0]
Default	3'd0	5'd1

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4:0]	ADC_TDM_SLOT_SEL_CH2	Selects which TDM channel slot is filled by ADC CH2 data. • 5'd0: Slot 1 • 5'd1: Slot 2 (default) • 5'd31: Slot 32

Register 9: DAC TDM CH1 SLOT CONFIG

Bits	[7:5]	[4:0]
Default	3'd0	5'd0

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4:0]	DAC_TDM_SLOT_SEL_CH1	Selects which TDM channel slot is latched into DAC CH1. • 5'd0: Slot 1 (default) • 5'd31: Slot 32

Register 10: DAC TDM CH2 SLOT CONFIG

Bits	[7:5]	[4:0]
Default	3'd0	5'd1

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4:0]	DAC_TDM_SLOT_SEL_CH2	Selects which TDM channel slot is latched into DAC CH2. • 5'd0: Slot 1 • 5'd1: Slot 2 (default) • 5'd31: Slot 32

Register 11: ADC DAISY CHAIN

Bits	[7:6]	[5]	[4:0]
Default	2'd0	1'b0	5'd0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	ADC_TDM_DAISY_CHAIN	ADC TDM daisy chain mode. • 1'b0: Disabled (default) • 1'b1: Enabled
[4:0]	ADC_TDM_DATA_LATCH_ADJ	Adjusts the position of the MSB within each TDM slot by TDM_DATA_LATCH_ADJ clock cycles. ADC data is placed ahead of the normal position. • 5'd0: Normal position • 5'd1-31: Data is placed ADC_TDM_DATA_LATCH_ADJ BCKs ahead

Register 12: DAC DAISY CHAIN

Bits	[7:6]	[5]	[4:0]
Default	2'd0	1'b0	5'd0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	DAC_TDM_DAISY_CHAIN	DAC TDM daisy chain mode. • 1'b0: Disabled (default) • 1'b1: Enabled
[4:0]	DAC_TDM_DATA_LATCH_ADJ	Adjusts the position of the MSB within each TDM slot by TDM_DATA_LATCH_ADJ clock cycles. DAC data sampling is delayed from the normal position. • 5'd0: Normal position • 5'd1-31: DAC_TDM_DATA_LATCH_ADJ BCKs delay before sampling data

Register 13: PCM MASTER MODE CONFIG

Bits	[7]	[6:5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	2'd0	1'b1	1'b0	1'b0	1'b1	1'b0

Bits	Mnemonic	Description
[7]	SLAVE_BCK_INVERT	Inverts the BCK input on DATA_CLK. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[6:5]	RESERVED	N/A
[4]	MASTER_WS_CLK_PHASE	Determines the CLK_BCK edge DATA_WS (GPIO2) is output on, in master mode. • 1'b0: Negative edge • 1'b1: Positive edge (default) Note: MASTER_BCK_INVERT inverts this logic.
[3]	MASTER_WS_PULSE_MODE	When enabled, master WS is a 1 BCK pulse signal instead of a 50% duty cycle signal. • 1'b0: 50% duty cycle WS signal (default) • 1'b1: Pulse WS signal
[2]	MASTER_WS_INVERT	Inverts master WS output on DATA1. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[1]	MASTER_BCK_INVERT	Inverts master BCK output on DATA_CLK. • 1'b0: Non-inverted • 1'b1: Inverted (default)
[0]	MASTER_MODE_EN	Enables I2S/TDM master mode and generates master BCK and master WS. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 14: VOLUME UP RAMP RATE

Bits	[7:0]
Default	8'h04

Bits	Mnemonic	Description
[7:0]	VOL_RAMP_RATE_UP	Linear step size from current volume to target volume, represented as a fraction of full-scale. $\text{ramp\_step [inc/sample]} = \frac{\text{VOL\_RAMP\_RATE\_UP}}{2^{12}}$ • 8'h00: Instant change • 8'h01: Slowest change • 8'h04: Default • 8'hFF: Fastest change

Register 15: VOLUME DOWN RAMP RATE

Bits	[7:0]
Default	8'h04

Bits	Mnemonic	Description
[7:0]	VOL_RAMP_RATE_DOWN	Linear step size from current volume to target volume, represented as a fraction of full-scale. $\text{ramp\_step [dec/sample]} = \frac{\text{VOL\_RAMP\_RATE\_DOWN}}{2^{12}}$ • 8'h00: Instant change • 8'h01: Slowest change • 8'h04: Default • 8'hFF: Fastest change

Register 16: RESERVED

Register 17: AUTO SYNC CONFIG

Bits	[7:4]	[3]	[2]	[1]	[0]
Default	4'b0000	1'b1	1'b1	1'b1	1'b1

Bits	Mnemonic	Description
[7:4]	RESERVED	N/A
[3]	AUTO_MCLK_24M_PHASE_SYNC	Allows phase of MCLK_24M to be tuned automatically according to ADC input data. Only used when MCLK is faster than MCLK_24M. • 1'b0: MCLK_24M phase tuning disabled (default) • 1'b1: Auto MCLK_24M phase tuning
[2]	AUTO_WS_PHASE_SYNC	Uses WS input (DATA1) as the sync reference. • 1'b0: WS is not the sync reference • 1'b1: WS is the sync reference
[1]	AUTO_ICG_SYNC	Allows programmable clock dividers to auto sync to the reference. • 1'b0: Auto sync disabled • 1'b1: Auto sync enabled (default)
[0]	AUTO_FS_CLK_GEN_SYNC	Allows FS signals to auto sync to the reference. • 1'b0: Auto sync disabled • 1'b1: Auto sync enabled (default)

Register 18: STATUS BITS MASK

Bits	[7:5]	[4]	[3]	[2]	[1]	[0]
Default	3'b000	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4]	STATUS_MASK_PLL_LOCKED	Masks the PLL_LOCK status bit. • 1'b0: Status bit masked (default) • 1'b1: Status bit enabled
[3]	STATUS_MASK_CH2_PEAK_DET	Masks the PEAK_FLAG status bit on ADC CH2. • 1'b0: Status bit masked (default) • 1'b1: Status bit enabled
[2]	STATUS_MASK_CH1_PEAK_DET	Masks the PEAK_FLAG status bit on ADC CH1. • 1'b0: Status bit masked (default) • 1'b1: Status bit enabled
[1]	STATUS_MASK_CH2_PEAK_LATCH	Masks the latched PEAK_FLAG status bit on ADC CH2. • 1'b0: Status bit masked (default) • 1'b1: Status bit enabled
[0]	STATUS_MASK_CH1_PEAK_LATCH	Masks the latched PEAK_FLAG status bit on ADC CH1. • 1'b0: Status bit masked (default) • 1'b1: Status bit enabled

Register 19: STATUS BITS CLEAR

Bits	[7:2]	[1]	[0]
Default	6'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1]	STATUS_CLEAR_CH2_PEAK_LATCH	Clears the latched PEAK_FLAG status bit on ADC CH2. • 1'b0: Status bit held if asserted (default) • 1'b1: Status bit cleared
[0]	STATUS_CLEAR_CH1_PEAK_LATCH	Clears the latched PEAK_FLAG status bit on ADC CH1. • 1'b0: Status bit held if asserted (default) • 1'b1: Status bit cleared

Register 20: RESERVED

Register 21: CHARGE PUMP CONFIG

Bits	[7:1]	[0]
Default	7'b0000000	1'b1

Bits	Mnemonic	Description
[7:1]	RESERVED	N/A
[0]	CP_PDB_MUTE	Charge pump state control when the DAC mutes. • 1'b0: Keep charge pump on when DAC mutes • 1'b1: Turn off charge pump when DAC mutes (default)

Register 22: RESERVED

Register 23: CHARGE PUMP CLOCK DIV

Bits	[7:0]
Default	8'd31

Bits	Mnemonic	Description
[7:0]	CP_CLK_DIV	Specifies the clock divider for the charge pump clock. $\text{CP\_CLK [Hz]} = \frac{\text{MCLK} \cdot 2^{\sim \text{MCLK\_24M\_DIV2}}}{2 \cdot (\text{CP\_CLK\_DIV} + 1)}$

Register 38-24: RESERVED

GPIO Registers

Register 39: GPIO1/2 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO2_CFG	Configure GPIO2 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Mute DAC Channels – input • 4'd2: Clock valid flag – output • 4'd3: PLL locked flag – output • 4'd4: DAC Minimum Volume flag – output • 4'd5: DAC Automute status – output • 4'd6: DAC Soft Ramp Done flag – output • 4'd7: ADC CH1 Peak flag – output • 4'd8: ADC CH2 Peak flag – output • 4'd9: PWM Signal – output • 4'd10: OR of Status Bits – output • 4'd11: BCK/WS monitor – output • 4'd12: MCLK_24M – output • 4'd13: MCLK_128FS – output • 4'd14: Output 0 – output • 4'd15: Output 1 – output
[3:0]	GPIO1_CFG	Configure GPIO1 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Mute DAC Channels – input • 4'd2: Clock valid flag – output • 4'd3: PLL locked flag – output • 4'd4: DAC Minimum Volume flag – output • 4'd5: DAC Automute status – output • 4'd6: DAC Soft Ramp Done flag – output • 4'd7: ADC CH1 Peak flag – output • 4'd8: ADC CH2 Peak flag – output • 4'd9: PWM Signal – output • 4'd10: OR of Status Bits – output • 4'd11: BCK/WS monitor – output • 4'd12: MCLK_24M – output • 4'd13: MCLK_128FS – output • 4'd14: Output 0 – output • 4'd15: Output 1 – output

Register 40: GPIO3/4 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO4_CFG	Configure GPIO4 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Mute DAC Channels – input • 4'd2: Clock valid flag – output • 4'd3: PLL locked flag – output • 4'd4: DAC Minimum Volume flag – output • 4'd5: DAC Automute status – output • 4'd6: DAC Soft Ramp Done flag – output • 4'd7: ADC CH1 Peak flag – output • 4'd8: ADC CH2 Peak flag – output • 4'd9: PWM Signal – output • 4'd10: OR of Status Bits – output • 4'd11: BCK/WS monitor – output • 4'd12: MCLK_24M – output • 4'd13: MCLK_128FS – output • 4'd14: Output 0 – output • 4'd15: Output 1 – output
[3:0]	GPIO3_CFG	Configure GPIO3 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Mute DAC Channels – input • 4'd2: Clock valid flag – output • 4'd3: PLL locked flag – output • 4'd4: DAC Minimum Volume flag – output • 4'd5: DAC Automute status – output • 4'd6: DAC Soft Ramp Done flag – output • 4'd7: ADC CH1 Peak flag – output • 4'd8: ADC CH2 Peak flag – output • 4'd9: PWM Signal – output • 4'd10: OR of Status Bits – output • 4'd11: BCK/WS monitor – output • 4'd12: MCLK_24M – output • 4'd13: MCLK_128FS – output • 4'd14: Output 0 – output • 4'd15: Output 1 – output

Register 42-41: GPIO CONTROLS

Bits	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15]	INVERT_GPIO4	Invert the GPIO4 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[14]	INVERT_GPIO3	Invert the GPIO3 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[13]	INVERT_GPIO2	Invert the GPIO2 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[12]	INVERT_GPIO1	Invert the GPIO1 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[11]	GPIO4_WK_EN	• 1'b0: GPIO4 weak keeper disabled (default) • 1'b1: GPIO4 weak keeper enabled
[10]	GPIO3_WK_EN	• 1'b0: GPIO3 weak keeper disabled (default) • 1'b1: GPIO3 weak keeper enabled
[9]	GPIO2_WK_EN	• 1'b0: GPIO2 weak keeper disabled (default) • 1'b1: GPIO2 weak keeper enabled
[8]	GPIO1_WK_EN	• 1'b0: GPIO1 weak keeper disabled (default) • 1'b1: GPIO1 weak keeper enabled
[7]	GPIO4_SDB	• 1'b0: GPIO4 input disabled (default) • 1'b1: GPIO4 input enabled
[6]	GPIO3_SDB	• 1'b0: GPIO3 input disabled (default) • 1'b1: GPIO3 input enabled
[5]	GPIO2_SDB	• 1'b0: GPIO2 input disabled (default) • 1'b1: GPIO2 input enabled
[4]	GPIO1_SDB	• 1'b0: GPIO1 input disabled (default) • 1'b1: GPIO1 input enabled
[3]	GPIO4_OE	• 1'b0: Tristate GPIO4 output (default) • 1'b1: GPIO4 output enabled
[2]	GPIO3_OE	• 1'b0: Tristate GPIO3 output (default) • 1'b1: GPIO3 output enabled
[1]	GPIO2_OE	• 1'b0: Tristate GPIO2 output (default) • 1'b1: GPIO2 output enabled
[0]	GPIO1_OE	• 1'b0: Tristate GPIO1 output (default) • 1'b1: GPIO1 output enabled

Register 43: GPIO READ

Bits	[7:4]	[3]	[2]	[1]	[0]
Default	4'd0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:4]	RESERVED	N/A
[3]	GPIO4_READ	• 1'b0: GPIO4 readback disabled (default) • 1'b1: Allows readback of GPIO4 input
[2]	GPIO3_READ	• 1'b0: GPIO3 readback disabled (default) • 1'b1: Allows readback of GPIO3 input
[1]	GPIO2_READ	• 1'b0: GPIO2 readback disabled (default) • 1'b1: Allows readback of GPIO2 input
[0]	GPIO1_READ	• 1'b0: GPIO1 readback disabled (default) • 1'b1: Allows readback of GPIO1 input

Register 44: GPIO OUTPUT LOGIC

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b1	1'b1	1'b1

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	FLAG_CH_SEL	Outputs a specific channel's flag if the corresponding GPIO_AND and GPIO_OR are not set. • 1'b0: Outputs status/flag from CH1 • 1'b1: Outputs status/flag from CH2
[5]	GPIO_OR_SS_RAMP	Sets the GPIO_CFG "Soft Ramp Done" flag output as the bitwise OR of both channel's flags. • 1'b0: Disabled (default) • 1'b1: Enabled, GPIO_CFG output is |(ss_full_ramp[CHx])
[4]	GPIO_OR_AUTOMUTE	Sets the GPIO_CFG "Automute Status" output as the bitwise OR of both channel's statuses. • 1'b0: Disabled (default) • 1'b1: Enabled, GPIO_CFG output is |(automute[CHx])
[3]	GPIO_OR_VOL_MIN	Sets the GPIO_CFG "Minimum Volume" flag output as the bitwise OR of both channel's flags. • 1'b0: Disabled (default) • 1'b1: Enabled, GPIO_CFG output is |(vol_min[CHx])
[2]	GPIO_AND_SS_RAMP	Sets the GPIO_CFG "Soft Ramp Done" flag output as the bitwise AND of both channel's flags. • 1'b0: Disabled • 1'b1: Enabled, GPIO_CFG output is &(ss_full_ramp[CHx]) (default) Note: Overridden by GPIO_OR_SS_RAMP.
[1]	GPIO_AND_AUTOMUTE	Sets the GPIO_CFG "Automute Status" output as the bitwise AND of both channel's statuses. • 1'b0: Disabled • 1'b1: Enabled, GPIO_CFG output is &(automute[CHx]) (default) Note: Overridden by GPIO_OR_AUTOMUTE.
[0]	GPIO_AND_VOL_MIN	Sets the GPIO_CFG "Minimum Volume" flag output as the bitwise AND of both channel's flags. • 1'b0: Disabled • 1'b1: Enabled, GPIO_CFG output is &(vol_min[CHx]) (default) Note: Overridden by GPIO_OR_VOL_MIN.

Register 45: PWM COUNT

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	PWM_COUNT	8-bit value for the number of MCLK periods the PWM signal is high. • 8'h00: Disabled (default) • 8'h01: Minimum • 8'hFF: Maximum

Register 47-46: PWM FREQUENCY

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	PWM_FREQ	16-bit value for the frequency of the PWM signal. • 16'h0000: Disabled (default) • 16'h0001: Minimum • 16'hFFFF: Maximum $$\text{frequency [Hz]} = \frac{\text{MCLK}}{\text{PWM\_FREQ} + 1}$$ $$\text{Duty Cycle [\%]} = \left(\frac{\text{PWM\_COUNT}}{\text{PWM\_FREQ} + 1}\right) \cdot 100$$

ADC Registers

Register 48: ADC DBQ COEFF SEL

Bits	[7]	[6]	[5]	[4:0]
Default	1'b0	1'b0	1'b0	5'd1

Bits	Mnemonic	Description
[7]	ADC_DBQ_CLK_FAMILY_SEL	Selects the clock family for the automatic DBQ selection. • 1'b0: 48kHz clock family (default) • 1'b1: 44.1kHz clock family
[6]	ADC_DBQ_80HZ_HPF_EN	Sets the DBQ to one of the 80Hz HPFs, based on sample rate. • 1'b0: Disabled (default) • 1'b1: Enabled
[5]	ADC_DBQ_120HZ_HPF_EN	Sets the DBQ to one of the 120Hz HPFs, based on sample rate. • 1'b0: Disabled (default) • 1'b1: Enabled
[4:0]	ADC_DBQ_COEFF_SEL	Select the filter coefficients used by the ADC DBQ filter. • 5'd0: Use programmable coeffs • 5'd1: Bypass DBQ Filter (default) • 5'd2: 1st order DC blocking filter • 5'd3: 48kHz de-emphasis filter • 5'd4: 44.1kHz de-emphasis filter • 5'd5: 32kHz de-emphasis filter • 5'd6: RIAA de-emphasis filter • 5'd7: RIAA pre-emphasis filter • 5'd8: 80Hz high-pass filter, FS = 48kHz • 5'd9: 80Hz high-pass filter, FS = 96kHz • 5'd10: 80Hz high-pass filter, FS = 192kHz • 5'd11: 80Hz high-pass filter, FS = 384kHz • 5'd12: 120Hz high-pass filter, FS = 48kHz • 5'd13: 120Hz high-pass filter, FS = 96kHz • 5'd14: 120Hz high-pass filter, FS = 192kHz • 5'd15: 120Hz high-pass filter, FS = 384kHz • 5'd16: 80Hz high-pass filter, FS = 44.1kHz • 5'd17: 80Hz high-pass filter, FS = 88.2kHz • 5'd18: 80Hz high-pass filter, FS = 176.4kHz • 5'd19: 80Hz high-pass filter, FS = 352.8kHz • 5'd20: 120Hz high-pass filter, FS = 44.1kHz • 5'd21: 120Hz high-pass filter, FS = 88.2kHz • 5'd22: 120Hz high-pass filter, FS = 176.4kHz • 5'd23: 120Hz high-pass filter, FS = 352.8kHz • Others: Reserved

Register 51-49: ADC PROG DBQ A2 COEFF

Bits	[23:0]
Default	24'h000000

Bits	Mnemonic	Description
[23:0]	ADC_DBQ_A2	A 24-bit signed value for the ADC DBQ filter a2 coefficient. Note: Assign -1*a2 value to the register.

Register 54-52: ADC PROG DBQ A1 COEFF

Bits	[23:0]
Default	24'h000000

Bits	Mnemonic	Description
[23:0]	ADC_DBQ_A1	A 24-bit signed value for the ADC DBQ filter a1 coefficient. Note: Assign -1*a1 value to the register.

Register 57-55: ADC PROG DBQ B2 COEFF

Bits	[23:0]
Default	24'h000000

Bits	Mnemonic	Description
[23:0]	ADC_DBQ_B2	A 24-bit signed value for the ADC DBQ filter b2 coefficient.

Register 60-58: ADC PROG DBQ B1 COEFF

Bits	[23:0]
Default	24'h000000

Bits	Mnemonic	Description
[23:0]	ADC_DBQ_B1	A 24-bit signed value for the ADC DBQ filter b1 coefficient.

Register 63-61: ADC PROG DBQ B0 COEFF

Bits	[23:0]
Default	24'h000000

Bits	Mnemonic	Description
[23:0]	ADC_DBQ_B0	A 24-bit signed value for the ADC DBQ filter b0 coefficient.

Register 64: ADC FIR FILTER

Bits	[7:5]	[4:0]
Default	3'd0	5'd0

Bits	Mnemonic	Description
[7:5]	ADC_FILTER_SHAPE	Selects the 8x decimation FIR filter shape. • 3'd0: Minimum phase (default) • 3'd1: Linear phase fast roll-off apodizing • 3'd2: Linear phase fast roll-off • 3'd3: Linear phase fast roll-off low ripple • 3'd4: Linear phase slow roll-off • 3'd5: Minimum phase fast roll-off • 3'd6: Minimum phase slow roll-off • 3'd7: Minimum phase slow roll-off low dispersion
[4:0]	RESERVED	N/A

Register 65: ADC DC BLOCKING

Bits	[7]	[6]	[5:0]
Default	1'b1	1'b1	6'b111111

Bits	Mnemonic	Description
[7]	CH2_DC_BLOCK_EN	Enable the CH2 DC blocking filter on audio datapath. • 1'b0: Bypass DC blocking filter • 1'b1: Use DC blocking filter (default)
[6]	CH1_DC_BLOCK_EN	Enable the CH1 DC blocking filter on audio datapath. • 1'b0: Bypass DC blocking filter • 1'b1: Use DC blocking filter (default)
[5:0]	RESERVED	N/A

Register 66: PDM CONFIG

Bits	[7]	[6]	[5]	[4]	[3:0]
Default	1'b0	1'b0	1'b1	1'b0	4'b1010

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	PDM_INPUT_SEL	Select between PCM and PDM input streams. • 1'b0: Enable PCM input stream (default) • 1'b1: Enable PDM input stream
[5]	PDM_SAMPLE_EDGE	Sets the edge of PDM_CLK where the PDM sample increments. • 1'b0: Rising edge • 1'b1: Falling edge (default)
[4]	PDM_PHASE	• 1'b0: CH1 on the rising edge of PDM clock, CH2 on the falling edge (default) • 1'b1: CH2 on the rising edge of PDM clock, CH1 on the falling edge
[3:0]	RESERVED	N/A

Register 67: PDM CLK SELECT

Bits	[7]	[6:0]
Default	1'b0	7'd3

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:0]	MCLK_PDM_DIV	Whole number divide value + 1 for MCLK_PDM (MCLK/divide_value). • 7'd0: Whole number divide value + 1 = 1 • 7'd3: Whole number divide value + 1 = 4 (default)

Register 68: ADC VOLUME CH1

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	ADC_VOLUME_CH1	ADC CH1 volume. -0dB to -127dB, 0.5dB steps. • 8'h00: 0dB (default) • 8'hFE: -127dB • 8'hFF: Mute

Register 69: ADC VOLUME CH2

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	ADC_VOLUME_CH2	ADC CH2 volume. -0dB to -127dB, 0.5dB steps. • 8'h00: 0dB (default) • 8'hFE: -127dB • 8'hFF: Mute

Register 70: ADC MIX VOLUME CH1

Bits	[7:0]
Default	8'hFF

Bits	Mnemonic	Description
[7:0]	ADC_MIX_VOL_CH1	Volume of ADC_CH2 mixed into ADC_CH1. -0dB to -127dB, 0.5dB steps. • 8'h00: 0dB • 8'hFE: -127dB • 8'hFF: -inf dB (default)

Register 71: ADC MIX VOLUME CH2

Bits	[7:0]
Default	8'hFF

Bits	Mnemonic	Description
[7:0]	ADC_MIX_VOL_CH2	Volume of ADC_CH1 mixed into ADC_CH2. -0dB to -127dB, 0.5dB steps. • 8'h00: 0dB • 8'hFE: -127dB • 8'hFF: -inf dB (default)

Register 72: ADC DIGITAL GAIN

Bits	[7]	[6:4]	[3]	[2:0]
Default	1'b0	3'd0	1'b0	3'd0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:4]	ADC_DIGITAL_GAIN_CH2	ADC CH2 gain boost. +0dB to +42dB, +6dB steps. • 3'd0: +0dB (default) • 3'd1: +6dB • 3'd2: +12dB • 3'd3: +18dB • 3'd4: +24dB • 3'd5: +30dB • 3'd6: +36dB • 3'd7: +42dB
[3]	RESERVED	N/A
[2:0]	ADC_DIGITAL_GAIN_CH1	ADC CH1 gain boost. +0dB to +42dB, +6dB steps. • 3'd0: +0dB (default) • 3'd1: +6dB • 3'd2: +12dB • 3'd3: +18dB • 3'd4: +24dB • 3'd5: +30dB • 3'd6: +36dB • 3'd7: +42dB

Register 73: ADC PHASE INVERSION

Bits	[7:4]	[3]	[2]	[1]	[0]
Default	4'd0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:4]	RESERVED	N/A
[3]	ADC_MIX_VOL_PHASE_INV_CH2	Inverts the phase of ADC_MIX_VOL_CH2. • 1'b0: Non-inverted, ADC_CH1 added into ADC_CH2 (default) • 1'b1: Inverted, ADC_CH1 subtracted from ADC_CH2
[2]	ADC_MIX_VOL_PHASE_INV_CH1	Inverts the phase of ADC_MIX_VOL_CH1. • 1'b0: Non-inverted, ADC_CH2 added into ADC_CH1 (default) • 1'b1: Inverted, ADC_CH2 subtracted from ADC_CH1
[1]	ADC_VOL_PHASE_INV_CH2	Inverts the phase of ADC_VOLUME_CH2. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[0]	ADC_VOL_PHASE_INV_CH1	Inverts the phase of ADC_VOLUME_CH1. • 1'b0: Non-inverted (default) • 1'b1: Inverted

Register 81-74: RESERVED

Register 82: PGA GAIN CONTROL

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	PGA_GAIN_CTRL_CH2	Sets the gain applied to the PGA (+0dB to +30dB, 3dB steps). Valid from 4'd0 to 4'd10.
[3:0]	PGA_GAIN_CTRL_CH1	Sets the gain applied to the PGA (+0dB to +30dB, 3dB steps). Valid from 4'd0 to 4'd10.

Register 87-83: RESERVED

Register 88: PEAK DETECT ENABLE

Bits	[7:2]	[1]	[0]
Default	6'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1]	PEAK_DETECT_CH2_EN	Enables the ADC CH2 peak detector. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	PEAK_DETECT_CH1_EN	Enables the ADC CH1 peak detector. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 89: PEAK DETECT CONFIG

Bits	[7]	[6]	[5]	[4:0]
Default	1'd0	1'b0	1'b0	5'd10

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	LOCK_PEAK_VALUE	Locks the current peak detector values, for reading back. • 1'b0: Peak detector value can update (default) • 1'b1: Peak detector value locked
[5]	RESERVED	N/A
[4:0]	PEAK_DECAY_RATE	Sets the speed at which the peak detector value will decay when greater than the input signal. • 5'd0: Instant decay • 5'd1: Fastest decay • 5'd10: Default value • 5'd22: Slowest decay • Others: Reserved

Register 91-90: PEAK THRESHOLDS

Bits	[15:8]	[7:0]
Default	8'hFF	8'hFF

Bits	Mnemonic	Description
[15:8]	PEAK_THRESH_CH2	Threshold value to trigger the PEAK_FLAG in the CH2 peak detector. Triggers if the input signal > PEAK_THRESH_CH2. • 8'h01: -48dB • 8'hFF: 0dB (default) $\text{threshold [dB]} = 20 \cdot \log10\left(\frac{\text{PEAK\_THRESH\_CH2}}{2^8 - 1}\right)$
[7:0]	PEAK_THRESH_CH1	Threshold value to trigger the PEAK_FLAG in the CH1 peak detector. Triggers if the input signal > PEAK_THRESH_CH1. • 8'h01: -48dB • 8'hFF: 0dB (default) $\text{threshold [dB]} = 20 \cdot \log10\left(\frac{\text{PEAK\_THRESH\_CH1}}{2^8 - 1}\right)$

Register 93-92: RESERVED

Register 94: MIC BIAS

Bits	[7]	[6]	[5:4]	[3]	[2:0]
Default	1'b0	1'b0	2'b00	1'b0	3'b010

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	MB_VR_BYPB	Bypass the MICBIAS reference voltage select. • 1'b0: 2.85V (default) • 1'b1: Determined by MB_VR_SET
[5:4]	RESERVED	N/A
[3]	MB_PDB	Enables the MICBIAS. • 1'b0: Disabled (default) • 1'b1: Enabled
[2:0]	MB_VR_SET	Set mic bias voltage. • 3'b000: 1.45V • 3'b001: 2.55V • 3'b010: 2.65V (default) • 3'b011: 2.75V • 3'b100: 1.65V • 3'b101: 1.75V • 3'b110: 1.85V • 3'b111: 1.95V

Register 99-95: RESERVED

DAC Registers

Register 100: DAC NSMOD SEL

Bits	[7:1]	[0]
Default	6'd0	1'b0

Bits	Mnemonic	Description
[7:1]	RESERVED	N/A
[0]	NSMOD_CH2_SEL	Selects CH2 nsmod input. 1'b0: Input from CH2 interpolation path (default) 1'b1: Input from CH1 interpolation path

Register 101: RESERVED

Register 102: DAC DBQ COEFF SEL

Bits	[7:5]	[4:0]
Default	3'd0	5'd1

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4:0]	DAC_DBQ_COEFF_SEL	Select the filter coefficients used by the DAC DBQ filter. 5'd0: Use programmable coeffs 5'd1: Bypass DBQ Filter (default) 5'd2: 1st order DC blocking filter 5'd3: 48kHz de-emphasis filter 5'd4: 44.1kHz de-emphasis filter 5'd5: 32kHz de-emphasis filter 5'd6: RIAA de-emphasis filter 5'd7: RIAA pre-emphasis filter 5'd8: 80Hz high-pass filter, FS = 48kHz 5'd9: 80Hz high-pass filter, FS = 96kHz 5'd10: 80Hz high-pass filter, FS = 192kHz 5'd11: 80Hz high-pass filter, FS = 384kHz 5'd12: 120Hz high-pass filter, FS = 48kHz 5'd13: 120Hz high-pass filter, FS = 96kHz 5'd14: 120Hz high-pass filter, FS = 192kHz 5'd15: 120Hz high-pass filter, FS = 384kHz 5'd16: 80Hz high-pass filter, FS = 44.1kHz 5'd17: 80Hz high-pass filter, FS = 88.2kHz 5'd18: 80Hz high-pass filter, FS = 176.4kHz 5'd19: 80Hz high-pass filter, FS = 352.8kHz 5'd20: 120Hz high-pass filter, FS = 44.1kHz 5'd21: 120Hz high-pass filter, FS = 88.2kHz 5'd22: 120Hz high-pass filter, FS = 176.4kHz 5'd23: 120Hz high-pass filter, FS = 352.8kHz Others: Reserved

Register 105-103: DAC PROG DBQ A2 COEFF

Bits	[23:0]
Default	24'h000000

Bits	Mnemonic	Description
[23:0]	DAC_DBQ_A2	A 24-bit signed value for the DAC DBQ filter a2 coefficient. Note: Assign -1*a2 value to the register.

Register 108-106: DAC PROG DBQ A1 COEFF

Bits	[23:0]
Default	24'h000000

Bits	Mnemonic	Description
[23:0]	DAC_DBQ_A1	A 24-bit signed value for the DAC DBQ filter a1 coefficient. Note: Assign -1*a1 value to the register.

Register 111-109: DAC PROG DBQ B2 COEFF

Bits	[23:0]
Default	24'h000000

Bits	Mnemonic	Description
[23:0]	DAC_DBQ_B2	A 24-bit signed value for the DAC DBQ filter b2 coefficient.

Register 114-112: DAC PROG DBQ B1 COEFF

Bits	[23:0]
Default	24'h000000

Bits	Mnemonic	Description
[23:0]	DAC_DBQ_B1	A 24-bit signed value for the DAC DBQ filter b1 coefficient.

Register 117-115: DAC PROG DBQ B0 COEFF

Bits	[23:0]
Default	24'h000000

Bits	Mnemonic	Description
[23:0]	DAC_DBQ_B0	A 24-bit signed value for the DAC DBQ filter b0 coefficient.

Register 118: DAC FILTER CONFIG

Bits	[7:6]	[5]	[4]	[3]	[2:0]
Default	2'd0	1'b0	1'b0	1'b0	3'd0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	BYPASS_IIR	Bypass the IIR filter. 1'b0: Non-bypassed (default) 1'b1: Bypassed
[4]	BYPASS_FIR4X	Bypass the 4X FIR filter. 1'b0: Non-bypassed (default) 1'b1: Bypassed
[3]	BYPASS_FIR2X	Bypass the 2X FIR filter. 1'b0: Non-bypassed (default) 1'b1: Bypassed
[2:0]	DAC_FILTER_SHAPE	Selects the 8x interpolation FIR filter shape. 3'd0: Minimum phase (default) 3'd1: Linear phase fast roll-off apodizing 3'd2: Linear phase fast roll-off 3'd3: Linear phase fast roll-off low ripple 3'd4: Linear phase slow roll-off 3'd5: Minimum phase fast roll-off 3'd6: Minimum phase slow roll-off 3'd7: Minimum phase slow roll-off low dispersion

Register 122-119: RESERVED

Register 123: DAC VOLUME CH1

Bits	[7:0]
Default	8'h02

Bits	Mnemonic	Description
[7:0]	DAC_VOLUME_CH1	DAC CH1 volume. +1dB to -126dB, 0.5dB steps. 8'h00: +1dB 8'h02: 0dB (default) 8'hFE: -126dB 8'hFF: Mute

Register 124: DAC VOLUME CH2

Bits	[7:0]
Default	8'h02

Bits	Mnemonic	Description
[7:0]	DAC_VOLUME_CH2	DAC CH2 volume. +1dB to -126dB, 0.5dB steps. 8'h00: +1dB 8'h02: 0dB (default) 8'hFE: -126dB 8'hFF: Mute

Register 125: DAC MIX VOLUME CH1

Bits	[7:0]
Default	8'hFF

Bits	Mnemonic	Description
[7:0]	DAC_MIX_VOL_CH1	Volume of DAC_CH2 mixed into DAC_CH1. -0dB to -127dB, 0.5dB steps. 8'h00: 0dB 8'hFE: -127dB 8'hFF: -inf dB (default)

Register 126: DAC MIX VOLUME CH2

Bits	[7:0]
Default	8'hFF

Bits	Mnemonic	Description
[7:0]	DAC_MIX_VOL_CH2	Volume of DAC_CH1 mixed into DAC_CH2. -0dB to -127dB, 0.5dB steps. 8'h00: 0dB 8'hFE: -127dB 8'hFF: -inf dB (default)

Register 127: DIRECT MONITOR VOLUME CH1

Bits	[7:0]
Default	8'hFF

Bits	Mnemonic	Description
[7:0]	DIR_MON_VOL_CH1	Volume of ADC CH1 direct monitor signal added into DAC CH1. +1dB to -126dB, 0.5dB steps. 8'h00: +1dB 8'h02: 0dB 8'hFE: -126dB 8'hFF: -inf dB (default)

Register 128: DIRECT MONITOR VOLUME CH2

Bits	[7:0]
Default	8'hFF

Bits	Mnemonic	Description
[7:0]	DIR_MON_VOL_CH2	Volume of ADC CH2 direct monitor signal added into DAC CH2. +1dB to -126dB, 0.5dB steps. 8'h00: +1dB 8'h02: 0dB 8'hFE: -126dB 8'hFF: -inf dB (default)

Register 134-129: RESERVED

Register 135: DAC DIGITAL GAIN

Bits	[7]	[6:4]	[3]	[2:0]
Default	1'b0	3'd0	1'b0	3'd0

Bits	Mnemonic	Description
[7]	DIR_MON_MUTE_CH2	Mutes the CH2 ADC direct monitor signal. 1'b0: Normal operation (default) 1'b1: Direct monitor signal muted
[6:4]	DAC_DIGITAL_GAIN_CH2	DAC CH2 gain boost. +0dB to +42dB, +6dB steps. 3'd0: +0dB (default) 3'd1: +6dB 3'd2: +12dB 3'd3: +18dB 3'd4: +24dB 3'd5: +30dB 3'd6: +36dB 3'd7: +42dB
[3]	DIR_MON_MUTE_CH1	Mutes the CH1 ADC direct monitor signal. 1'b0: Normal operation (default) 1'b1: Direct monitor signal muted
[2:0]	DAC_DIGITAL_GAIN_CH1	DAC CH1 gain boost. +0dB to +42dB, +6dB steps. 3'd0: +0dB (default) 3'd1: +6dB 3'd2: +12dB 3'd3: +18dB 3'd4: +24dB 3'd5: +30dB 3'd6: +36dB 3'd7: +42dB

Register 136: DAC PHASE INVERSION

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	DIR_MON_MONO_CH2	Adds both ADC direct monitor signals onto the CH2 DAC datapath. Both signals are controlled by the CH2 volume and mute controls. 1'b0: Disabled, CH2 ADC monitored on CH2 DAC (default) 1'b1: Enabled, CH1 ADC & CH2 ADC monitored on CH2 DAC
[6]	DIR_MON_MONO_CH1	Adds both ADC direct monitor signals onto the CH1 DAC datapath. Both signals are controlled by the CH1 volume and mute controls. 1'b0: Disabled, CH1 ADC monitored on CH1 DAC (default) 1'b1: Enabled, CH1 ADC & CH2 ADC monitored on CH1 DAC
[5]	DIR_MON_VOL_PHASE_INV_CH2	Inverts the phase of DIR_MON_VOL_CH2. 1'b0: Non-inverted (default) 1'b1: Inverted
[4]	DIR_MON_VOL_PHASE_INV_CH1	Inverts the phase of DIR_MON_VOL_CH1. 1'b0: Non-inverted (default) 1'b1: Inverted
[3]	DAC_MIX_VOL_PHASE_INV_CH2	Inverts the phase of DAC_MIX_VOL_CH2. 1'b0: Non-inverted, DAC_CH1 added into DAC_CH2 (default) 1'b1: Inverted, DAC_CH1 subtracted from DAC_CH2
[2]	DAC_MIX_VOL_PHASE_INV_CH1	Inverts the phase of DAC_MIX_VOL_CH1. 1'b0: Non-inverted, DAC_CH2 added into DAC_CH1 (default) 1'b1: Inverted, DAC_CH2 subtracted from DAC_CH1
[1]	DAC_VOL_PHASE_INV_CH2	Inverts the phase of DAC_VOLUME_CH2. 1'b0: Non-inverted (default) 1'b1: Inverted
[0]	DAC_VOL_PHASE_INV_CH1	Inverts the phase of DAC_VOLUME_CH1. 1'b0: Non-inverted (default) 1'b1: Inverted

Register 137: DAC MUTE

Bits	[7:2]	[1]	[0]
Default	6'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1]	DAC_MUTE_CH2	Mutes the CH2 DAC datapath, will not mute the monitor signal. 1'b0: Normal CH2 operation (default) 1'b1: Mute CH2 DAC
[0]	DAC_MUTE_CH1	Mutes the CH1 DAC datapath, will not mute the monitor signal. 1'b0: Normal CH1 operation (default) 1'b1: Mute CH1 DAC

Register 138: SOFT RAMP CONFIG

Bits	[7:6]	[5]	[4:0]
Default	2'd0	1'b1	5'd3

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	MUTE_RAMP_TO_GROUND	1'b0: When ramped to min volume during normal mute, do not soft ramp to ground 1'b1: When ramped to min volume during normal mute, soft ramp to ground for power saving (default) normal mute includes: automute, mute by register, mute by GPIO
[4:0]	SOFT_RAMP_TIME	Sets the amount of time that it takes to perform a soft start ramp. This time affects both "ramp to ground" and "ramp to AVCC/2". Valid from 0 to 20 (inclusive). $\text{Time [s]} = \frac{2^{15} \cdot 2^{\text{SOFT\_RAMP\_TIME}} \cdot 2^{\text{MCLK\_24M\_DIV2}}}{MCLK}$

Register 139: AUTOMUTE ENABLE

Bits	[7:2]	[1]	[0]
Default	6'd0	1'b1	1'b1

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1]	AUTOMUTE_EN_CH2	Enables CH2 automute. 1'b0: Disabled 1'b1: Enabled (default) Note: Automute will not engage if the ADC monitor is running.
[0]	AUTOMUTE_EN_CH1	Enables CH1 automute. 1'b0: Disabled 1'b1: Enabled (default) Note: Automute will not engage if the ADC monitor is running.

Register 141-140: AUTOMUTE TIME

Bits	[15:11]	[10:0]
Default	5'd0	11'h0F

Bits	Mnemonic	Description
[15:11]	RESERVED	N/A
[10:0]	AUTOMUTE_TIME	Configures the amount of time in seconds the audio must remain below AUTOMUTE_LEVEL before an automute condition is flagged. 11'h000: Disabled 11'h001: Slowest 11'h00F: Default 11'h7FF: Fastest $\text{Time [s]} = \frac{2^{25}}{\text{AUTOMUTE\_TIME} \cdot \text{MCLK\_128FS} \cdot 2^{\text{64FS\_MODE}}}$

Register 143-142: AUTOMUTE LEVEL

Bits	[15:0]
Default	16'h0008

Bits	Mnemonic	Description
[15:0]	AUTOMUTE_LEVEL	The threshold which the audio must be below before an automute condition is flagged. 16'h0001: -138dB 16'h0008: -120dB (default) 16'hFFFF: -42dB $\text{Level [dB]} = 20 \cdot \log10\left(\frac{\text{AUTOMUTE\_LEVEL}}{(2^{16}-1)\cdot 2^{7}}\right)$

Register 145-144: AUTOMUTE OFF LEVEL

Bits	[15:0]
Default	16'h000A

Bits	Mnemonic	Description
[15:0]	AUTOMUTE_OFF_LEVEL	The threshold which the audio must be above before the automute condition is immediately cleared. 16'h0001: -138dB 16'h000A: -118dB (default) 16'hFFFF: -42dB $\text{Level [dB]} = 20 \cdot \log10\left(\frac{\text{AUTOMUTE\_OFF\_LEVEL}}{(2^{16}-1)\cdot 2^{7}}\right)$

Register 163-146: RESERVED

PLL Registers

Register 164: PLL CLOCK SELECT

Bits	[7]	[6]	[5:4]	[3]	[2:1]	[0]
Default	1'b0	1'b0	2'b10	1'b0	2'b00	1'b1

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	PLL_CLK_PHASE_INV	Inverts the phase of the PLL output clock. 1'b0: Non-inverted (default) 1'b1: Inverted
[5:4]	SEL_PLL_CLK_IN	Selects PLL input clock source when EN_PLL_CLK_IN is set. 2'b00: ACLK 2'b10: BCK (default) Others: Reserved
[3]	EN_PLL_CLK_IN	Allows SEL_PLL_CLK_IN to select PLL input clocks. 1'b0: Disables SEL_PLL_CLK_IN (default) 1'b1: Enables SEL_PLL_CLK_IN
[2:1]	SEL_MCLK_IN	Selects digital core and ADC clock source when EN_MCLK_IN is set. 2'b00: ACLK (default) 2'b10: PLL Others: Reserved
[0]	EN_MCLK_IN	Enables clock inputs to the digital core. 1'b0: Disabled 1'b1: Enabled (default)

Register 165: PLL VCO & CP

Bits	[7:4]	[3]	[2]	[1]	[0]
Default	4'b0011	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:4]	RESERVED	N/A
[3]	PLL_CP_PDB	Enables/disables the PLL charge pump. 1'b0: Disabled (default) 1'b1: Enabled
[2]	PLL_VCO_PDB	Enables/disables the PLL voltage-controlled oscillator (VCO). 1'b0: Disabled (default) 1'b1: Enabled
[1]	PLL_CLKSMP_PDB	Power Down the PLL circuitry. 1'b0: PLL Block disabled (default) 1'b1: PLL Block enabled
[0]	PLL_DIG_RSTB	Resets the Digital core of the PLL.

Register 166: PLL REGULATOR

Bits	[7:4]	[3]	[2:0]
Default	4'd0	1'b0	3'b010

Bits	Mnemonic	Description
[7:4]	RESERVED	N/A
[3]	PLL_REG_PDB	Power down the PLL regulator. 1'b0: Disable the PLL regulator (default) 1'b1: Enable the PLL regulator
[2:0]	RESERVED	N/A

Register 169-167: PLL FEEDBACK DIV

Bits	[23:0]
Default	24'h100000

Bits	Mnemonic	Description
[23:0]	PLL_CLK_FB_DIV	Sets the PLL clock feedback divider (Nfb). 24'h000000: Reserved 24'h100000: Default 24'hn: Divide by 2^25/n

Register 172-170: PLL IN & OUT DIV

Bits	[23:16]	[15:12]	[11:10]	[9]	[8:0]
Default	8'b00010000	4'd3	2'd0	1'b1	9'd0

Bits	Mnemonic	Description
[23:16]	RESERVED	N/A
[15:12]	PLL_CLK_OUT_DIV	Sets the PLL clock output divider (No). 4'd0: Reserved 4'd3: Divide by 4. (default) 4'dn: Divide by (n + 1).
[11:10]	RESERVED	N/A
[9]	PLL_FB_DIV_LOAD	Write 1'b1 then write 1'b0 to load CLK_FB_DIV.
[8:0]	PLL_CLK_IN_DIV	Sets the PLL clock input divider (Ni). 9'd0: Reserved (default) 9'dn: Divide by (n + 1).

Register 178-173: RESERVED

Readback Registers

Register 224: CODEC VALIDITY READ

Bits	[7]	[6]	[5]	[4:0]
Default	-	-	-	-

Bits	Mnemonic	Description
[7]	PLL_LOCKED	PLL locked flag.
[6]	DAC_TDM_VALID	TDM decoder valid flag.
[5]	ADC_TDM_VALID	TDM encoder valid flag.
[4:0]	AUTO_CH_NUM	Automatic TDM channel number tuning result.

Register 225: CHIP ID

Bits	[7:0]
Default	8'hAA

Bits	Mnemonic	Description
[7:0]	CHIP_ID	Chip ID. • ES9290: 0xAA

Register 229-226: RESERVED

Register 230: AUTO FS READ

Bits	[7]	[6]	[5:0]
Default	-	-	-

Bits	Mnemonic	Description
[7]	EN_64FS_MODE_AUTO	Result {Z} of the automatic sample rate detect (reg0[3] AUTO_FS_DETECT) logic, running the device in 64FS mode. • 1'b0: 64FS disabled • 1'b1: 64FS enabled
[6]	MCLK_128FS_HALF_DIV_AUTO	Result {Y} of the automatic sample rate detect (reg0[3] AUTO_FS_DETECT) logic. • 1'b0: MCLK_128FS is an integer multiple of MCLK, Y = 1. • 1'b1: MCLK_128FS is a (X+1)*0.5 multiple of MCLK, Y = 2.
[5:0]	MCLK_128FS_DIV_AUTO	Result {X} of the automatic sample rate detect (reg0[3] AUTO_FS_DETECT) logic. $$FS[Hz] = \frac{Y \cdot MCLK}{(X+1) \cdot \left(\frac{128^Z}{2}\right)}$$

Register 231: BCK/WS VALID

Bits	[7:3]	[2]	[1]	[0]
Default		-	-	-

Bits	Mnemonic	Description
[7:3]	RESERVED	N/A
[2]	RATIO_VALID	Validity of the MCLK/MCLK_128FS ratio. • 1'b0: Invalid ratio • 1'b1: Valid ratio
[1]	BCK_INVALID	Validity of the BCK signal, requires BCK_MONITOR to be enabled.
[0]	WS_INVALID	Validity of the WS signal, requires WS_MONITOR to be enabled.

Register 232: GPIO READBACK

Bits	[7:4]	[3]	[2]	[1]	[0]
Default		-	-	-	-

Bits	Mnemonic	Description
[7:4]	RESERVED	N/A
[3]	GPIO4_R	GPIO4 input readback.
[2]	GPIO3_R	GPIO3 input readback.
[1]	GPIO2_R	GPIO2 input readback.
[0]	GPIO1_R	GPIO1 input readback.

Register 233: PEAK FLAG

Bits	[7]	[6]	[5]	[4]	[3:0]
Default	-	-	-	-	

Bits	Mnemonic	Description
[7]	PEAK_FLAG_LAT_CH2	ADC CH2 latched peak detector flag. • 1'b0: CH2 input signal ≤ PEAK_THRESH_CH2 • 1'b1: CH2 input signal > PEAK_THRESH_CH2 Note: Requires reg19[1] INT_CLEAR_CH2_PEAK_LATCH to clear flag.
[6]	PEAK_FLAG_LAT_CH1	ADC CH1 latched peak detector flag. • 1'b0: CH1 input signal ≤ PEAK_THRESH_CH2 • 1'b1: CH1 input signal > PEAK_THRESH_CH2 Note: Requires reg19[0] INT_CLEAR_CH1_PEAK_LATCH to clear flag.
[5]	PEAK_FLAG_CH2	ADC CH2 peak detector flag. • 1'b0: CH2 input signal ≤ PEAK_THRESH_CH2 • 1'b1: CH2 input signal > PEAK_THRESH_CH2
[4]	PEAK_FLAG_CH1	ADC CH1 peak detector flag. • 1'b0: CH1 input signal ≤ PEAK_THRESH_CH2 • 1'b1: CH1 input signal > PEAK_THRESH_CH2
[3:0]	RESERVED	N/A

Register 237-234: RESERVED

Register 239-238: PEAK CH1 READ

Bits	[15:0]
Default	-

Bits	Mnemonic	Description
[15:0]	PEAK_CH1	Channel 1 peak detector value readback. $$Peak[\mathrm{dB}] = 20 \cdot \log10\left(\frac{\mathrm{PEAK\_CH1}}{2^{16}-1}\right)$$

Register 241-240: PEAK CH2 READ

Bits	[15:0]
Default	-

Bits	Mnemonic	Description
[15:0]	PEAK_CH2	Channel 2 peak detector value readback. $$Peak[\mathrm{dB}] = 20 \cdot \log10\left(\frac{\mathrm{PEAK\_CH2}}{2^{16}-1}\right)$$

Register 242: DAC VOL MIN READ

Bits	[7:2]	[1]	[0]
Default		-	-

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1]	VOL_MIN_CH2	CH2 minimum volume flag.
[0]	VOL_MIN_CH1	CH1 minimum volume flag.

Register 243: DAC AUTOMUTE READ

Bits	[7:2]	[1]	[0]
Default		-	-

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1]	AUTOMUTE_CH2	CH2 automute status flag.
[0]	AUTOMUTE_CH1	CH1 automute status flag.

Register 244: DAC SOFT RAMP UP READ

Bits	[7:2]	[1]	[0]
Default		-	-

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1]	SS_RAMP_UP_CH2	CH2 soft ramped up flag.
[0]	SS_RAMP_UP_CH1	CH1 soft ramped up flag.

Register 245: DAC SOFT RAMP DOWN READ

Bits	[7:2]	[1]	[0]
Default		-	-

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1]	SS_RAMP_DOWN_CH2	CH2 soft ramped down flag.
[0]	SS_RAMP_DOWN_CH1	CH1 soft ramped down flag.

Register 251-246: RESERVED

ES9290 Reference Schematics

Software (SW) Mode

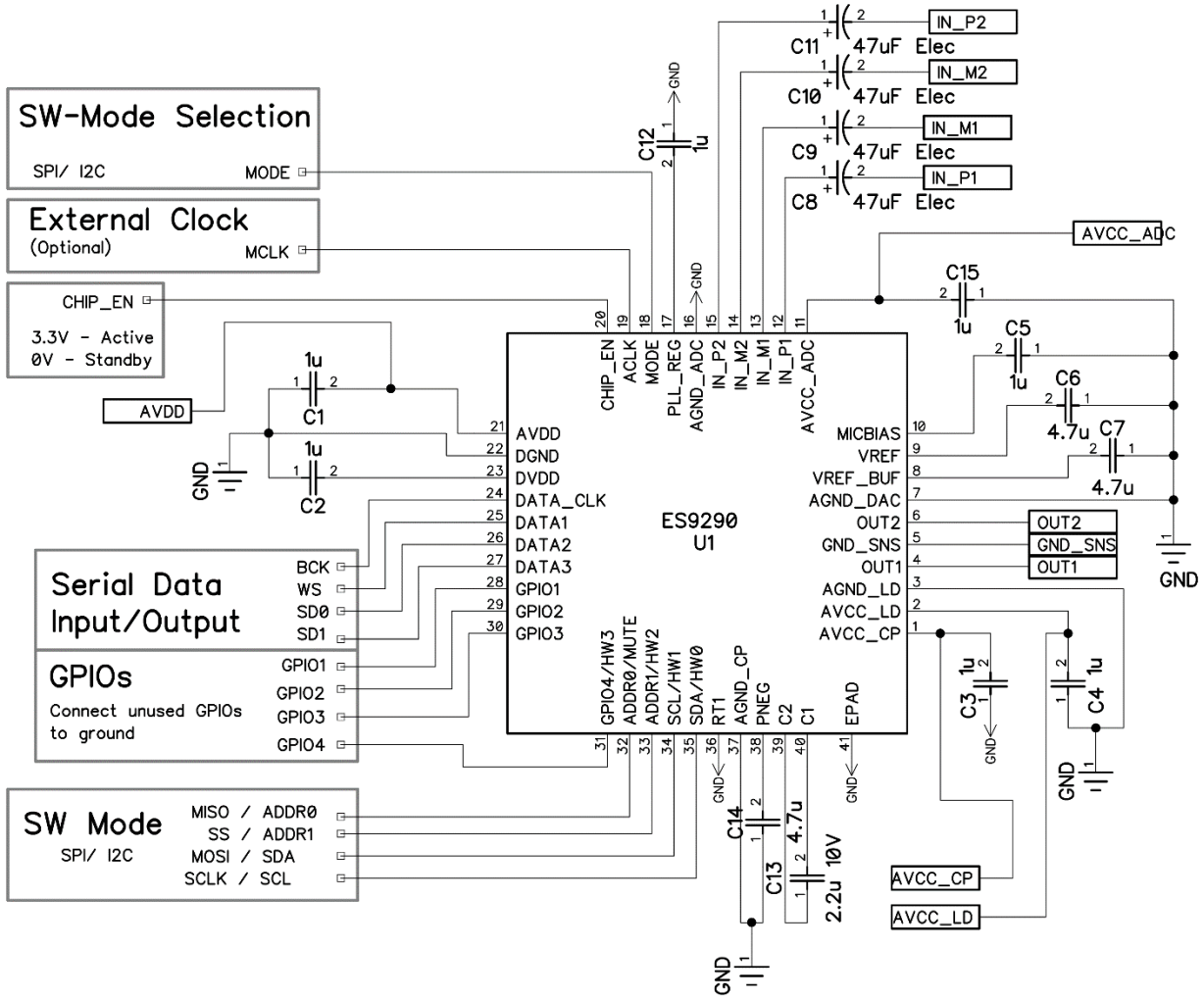


Figure 31 - ES9290 Software Mode Reference Schematic

Hardware (HW) Mode

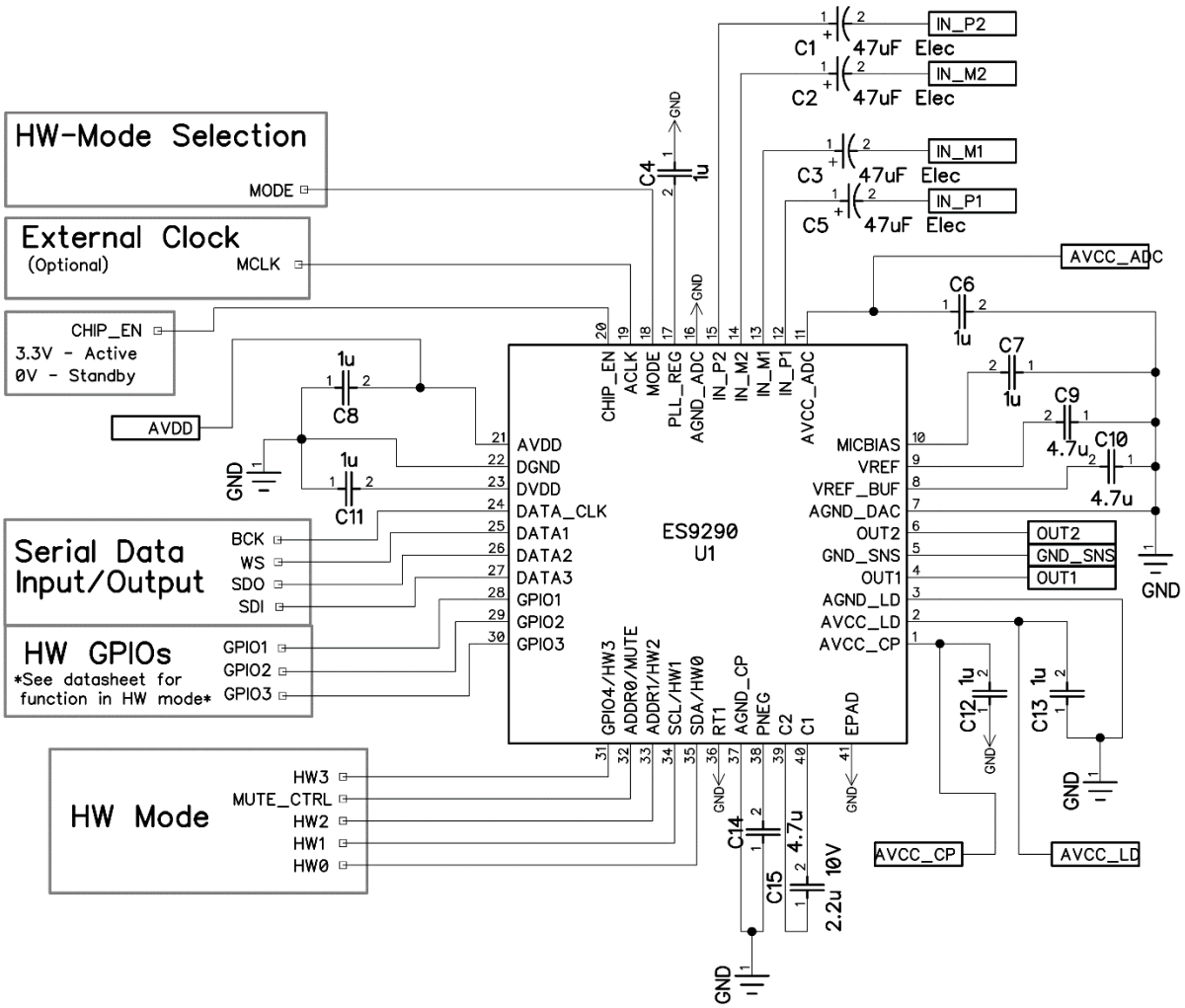
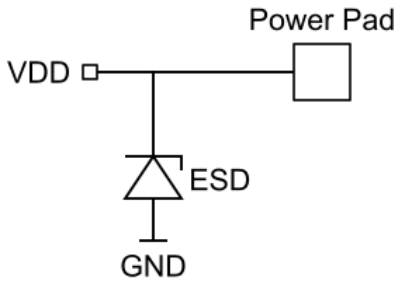
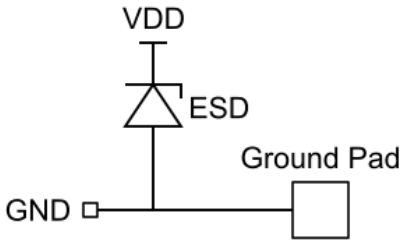
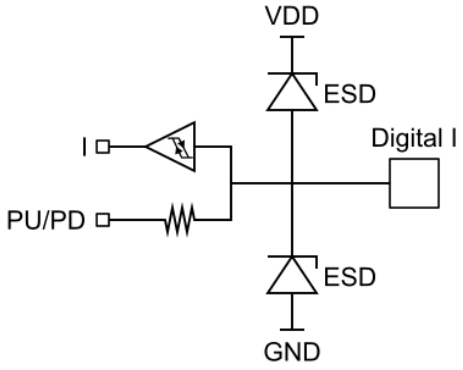
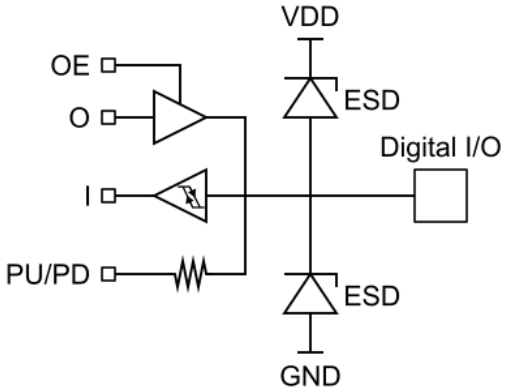
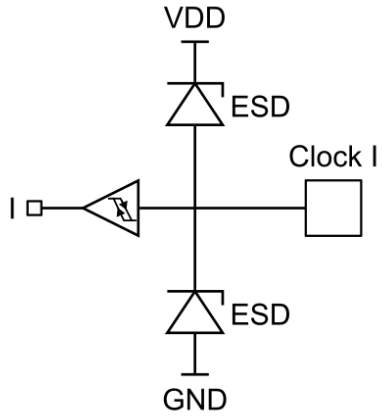
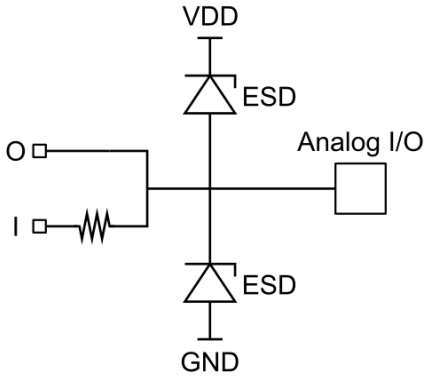
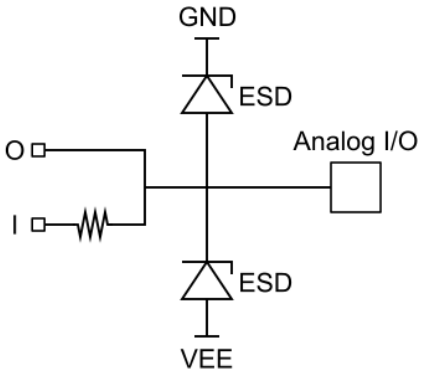
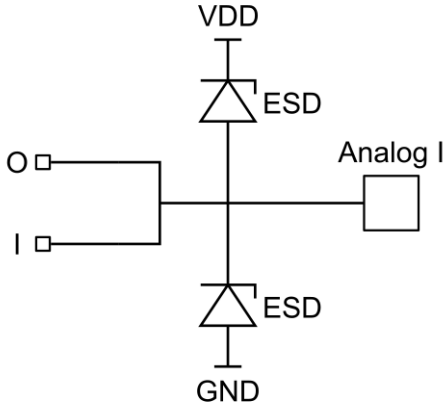


Figure 32 - ES9290 Hardware Mode Reference Schematic

Internal Pad Circuitry

Pin Name	Type	Pin	Equivalent Circuit
AVCC_CP AVCC_LD AVCC_ADC AVDD	Power	1 2 11 21	
AGND_LD AGND_DAC AGND_ADC DGND AGND_CP	Ground	3 7 16 22 37	
CHIP_EN	Reset	20	
MODE DATA_CLK DATA1 DATA2 DATA3 GPIO1 GPIO2 GPIO3 GPIO4/HW3 MISO/ADDR0/MUTE_MCLK_CTRL SS/ADDR1/HW2 SCLK/SCL/HW1 MOSI/SDA/HW0 RT1	Digital I/O	18 24 25 26 27 28 29 30 31 32 33 34 35 36	

ACLK	Clock I	19	
VREF_BUF VREF MICBIAS PLL_REG C1	Analog I/O	8 9 10 17 40	
C2	Analog I/O Neg	39	
IN_P1 IN_M1 IN_M2 IN_P2	Analog I	12 13 14 15	

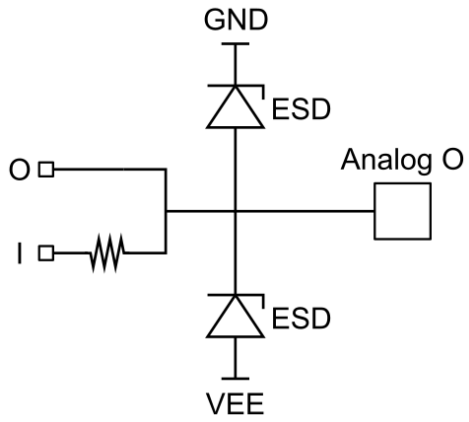
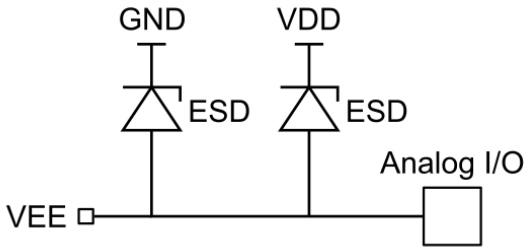
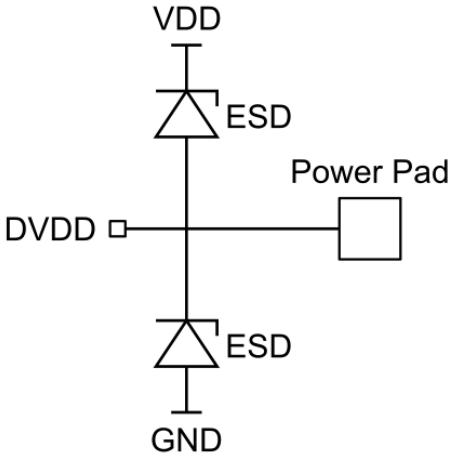
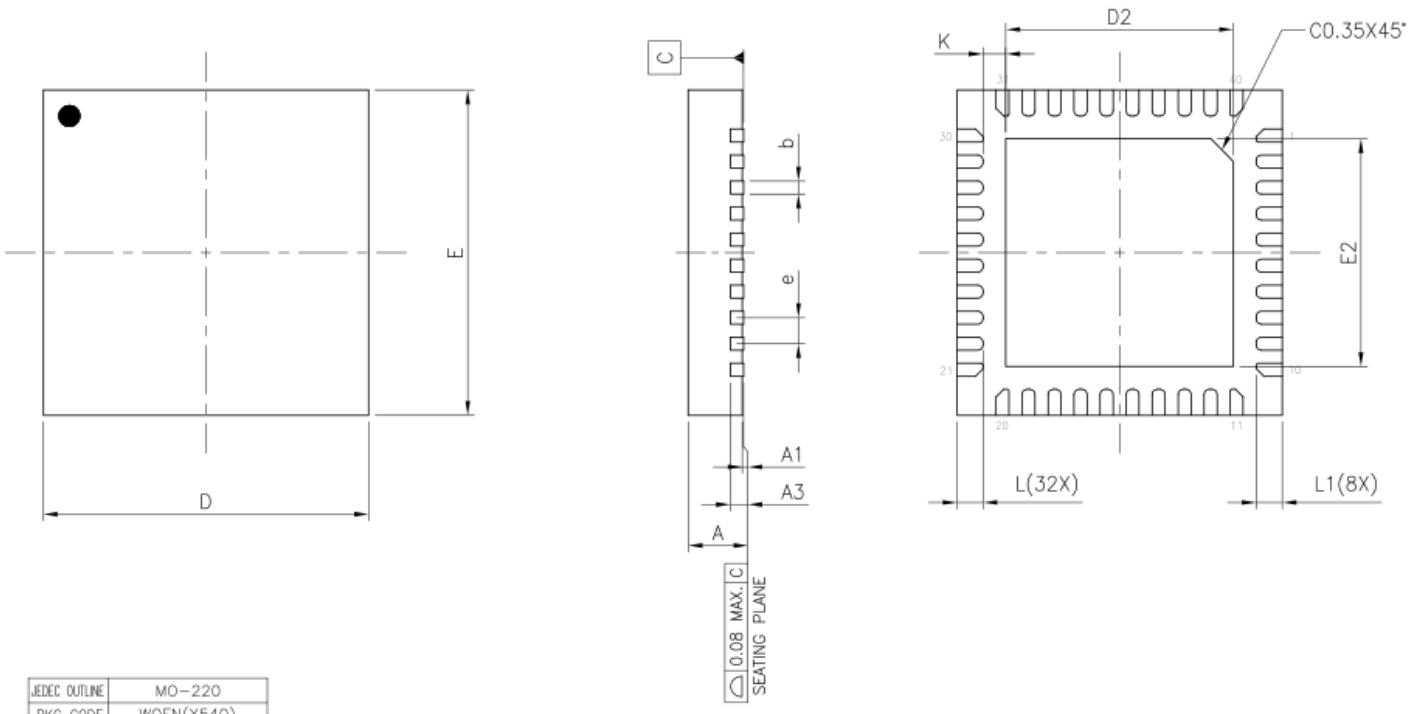
OUT_1 OUT_2	Analog O	4 6	
PNEG	Analog I/O Neg	38	
DVDD	Analog I/O	23	

Table 46 - Internal Pad Circuitry

40 QFN Package Dimensions



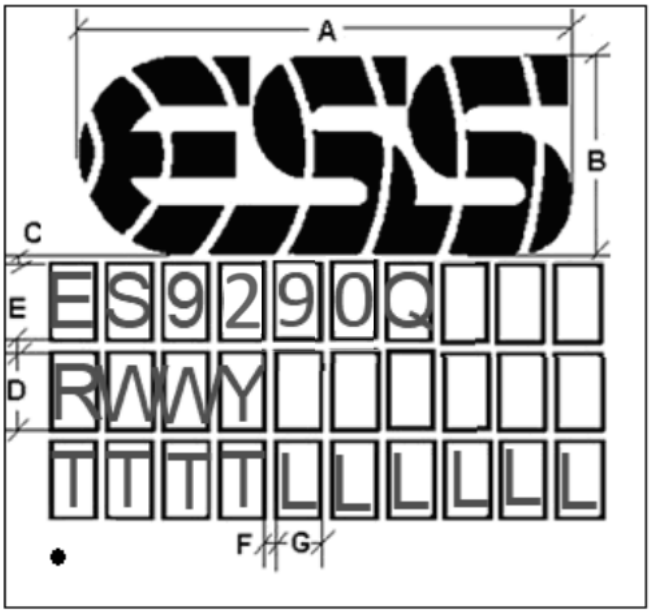
JEDEC OUTLINE	MO-220		
PKG CODE	WQFN(X540)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	5.00 BSC		
E	5.00 BSC		
e	0.40 BSC		
L	0.35	0.40	0.45
L1	0.33	0.38	0.43
K	0.20	–	–

PAD SIZE	D2			E2			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
A150X15R MIL	3.40	3.50	3.60	3.40	3.50	3.60	V	X	W(V)HHE-1

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 33 - ES9290 40 QFN Package Dimensions

40 QFN Top View Marking



	Dimension in mm						
Package Type	A	B	C	D	E	F	G
QFN 5mm x 5mm	4.0	1.6	0.2	0.4	0.2	0.1	0.3

T	Tracking number
W	Work week
Y	Last digit of year
L	Lot number
R	Silicon Revision

Marking is subject to change. This drawing is not to scale.

Figure 34 - ES9290 40 QFN Top View Markings

Reflow Process Considerations

Temperature Controlled

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor to consider.

The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size (RPC-2-Pb-Free Process - Classification Temperatures (Tc)). This narrows the process window for lead-free soldering to 10°C to 20°C.

The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used.

Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits (Table RPC-2).

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

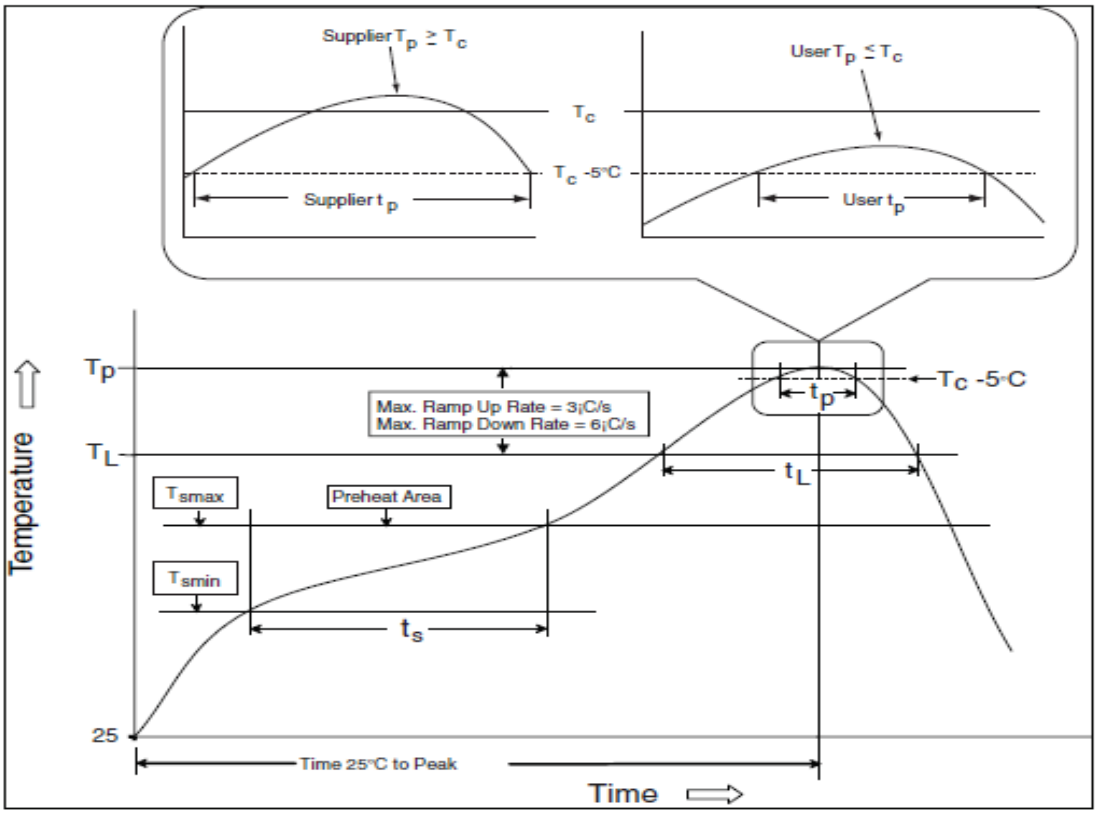


Figure 35 - IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)

Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time bake the board according to the moisture sensitivity label instructions.

Manual

Allowed up to 2 times with maximum temperature of 350ºC no longer than 3 seconds.

RPC-1 Classification Reflow Profile

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150°C 200°C 60-120 seconds
Ramp-up rate (TL to Tp)	3°C / second maximum
Liquidous temperature (TL) Time (tL) maintained above TL	217°C 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the classification temp in Table RPC-2. For suppliers Tp must equal or exceed the Classification temp in Table RPC-2.
Time (tp)* within 5°C of the specified classification temperature (Tc)	30* seconds
Ramp-down rate (Tp to TL)	6°C / second maximum
Time 25°C to peak temperature	8 minutes maximum
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.	

Table 47 - RPC-1 Classification Reflow Profile

All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp shall be within ±2°C of the live-bug Tp and still meet the Tc requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures, refer to JEP140 for recommended thermocouple use.

Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.

For example, if Tc is 260°C and time tp is 30 seconds, this means the following for the supplier and the user.
For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.
For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

All components in the test load shall meet the classification profile requirements.

RPC-2-Pb-Free Process - Classification Temperatures (Tc)

Package Thickness	Volume mm3, <350	Volume mm3, 350 to 2000	Volume mm3, >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm - 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Table 48 - RPC-2 Pb Free Classification Temperature

At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).

Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.

The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

Ordering Information

Part Number	Description	Package
ES9290Q	SABRE 32-bit 2 Channel ADC/DAC CODEC with built-in digital filters, and multiple input-output formats.	5mm x 5mm 40 QFN

Table 49 - Ordering Information

Revision History

Current Version 0.3.2

Rev.	Date	Notes
0.3.1	June, 2024	Initial Release
0.3.2	September, 2024	• Added note to daisy chain section about 32 & 24 bit daisy chain • Updated DAC performance table • Updated CLOCK VALID flag description • Updated APLL divider value tables • Corrected reference schematic titles

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