Analog Reinvented

ES9219

32-bit Stereo Low Power DAC with Headphone Amplifier, Analog Volume Control, and Output Switch

The ***ES9219*** is a high-performance 32-bit, 2-channel audio **SABRE HiFi®** D/A converter with QUAD DAC+™ technology, headphone amplifier, analog volume control, dynamic range enhancement (DRE) and output switch designed for audiophile-grade portable power sensitive applications such as digital music players, consumer applications such as USB DACs and A/V receivers, as well as professional applications such as mixer consoles and digital audio workstations.

Using critically acclaimed QUAD DAC+™ technology, patented 32-bit HyperStream III® DAC architecture and Time Domain Jitter Eliminator, the ***ES9219*** delivers up to 121dB DNR and –114dB THD+N in HiFi mode, a performance level that will satisfy the most demanding audio enthusiasts.

The ***ES9219's*** integrated SABRE DAC supports up to 32-bit 384kHz PCM and DSD256 audio data via master/slave I²S/DSD interface in synchronous and asynchronous sampling modes. A user-programmable FIR filter with user presets is included for customizable sound signature. Additionally, the ***ES9219's*** integrated SABRE Headphone Amp supports up to 2.0Vrms output with analog gain control to reduce output noise at real-life listening levels. An integrated output switch allows an auxiliary source such as voice to bypass the ***ES9219*** for lowest power consumption in non-HiFi mode. Residual distortion from suboptimal PCB components and layout can be minimized using ***ES9219's*** unique THD compensation circuit, while PCB footprint and bill-of-material are minimized via the ***ES9219's*** integrated feedback resistors and low-noise DAC reference LDO.

The ***ES9219*** sets the standard for HD audio performance enabling **SABRE HiFi®** experience all the way from the DAC to headphones for today's most demanding digital-audio applications in an easy-to-use 42-CSP package.

FEATURE	DESCRIPTION
Patented 32-bit HyperStream® III DAC/HPA QUAD DAC+™ technology +130dB SNR, +121dB DNR -114 dB THD+N, 1.0Vrms into 100kΩ -112 dB THD+N, 2.0Vrms into 300Ω -106 dB THD+N, 300mVrms into 32Ω	Industry's highest performance 32-bit mobile audio DAC/HPA with unprecedented dynamic range & ultra-low distortion Support synchronous and asynchronous sampling modes Enable SABRE HiFi® experience all the way to headphones
Patented Time Domain Jitter Eliminator	Unmatched audio clarity free from input clock jitter
64-bit accumulator & 32-bit processing	Distortion free signal processing
Versatile digital input	Support master/slave PCM (I2S, LJ 16-32-bit), DSD or DoP, MQA Renderer
Customizable filter characteristics	Preset filters and a User-programmable filter for custom sound signature
Output Switch for Auxiliary Source	Voice mode bypass with ultra-low power consumption
Integrated Low Noise AVCC LDO	Eliminate external LDO and reduce PCB size
Adjustable Analog Gain with Dynamic Range Enhancement, Integrated HPA Feedback Resistors	Reduce noise at real-life listening levels Eliminate external thin film resistors and reduce PCB size
THD Compensation + Analog THD Removal (ATR)	Minimize DAC non-linearity
42-CSP Package	Minimize PCB footprint
< 45 mW quiescent power < 10uW standby power	Maximize battery life
Integrated Analog PLL	Allow BOM reduction, Crystal not required.

APPLICATIONS

- Mobile phones / Tablets / Digital music players / Portable multimedia players
- Consumer and Audiophile USB DAC headphone amplifiers and A/V receivers
- Professional digital audio workstations and mixer consoles

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Functional Block Diagram

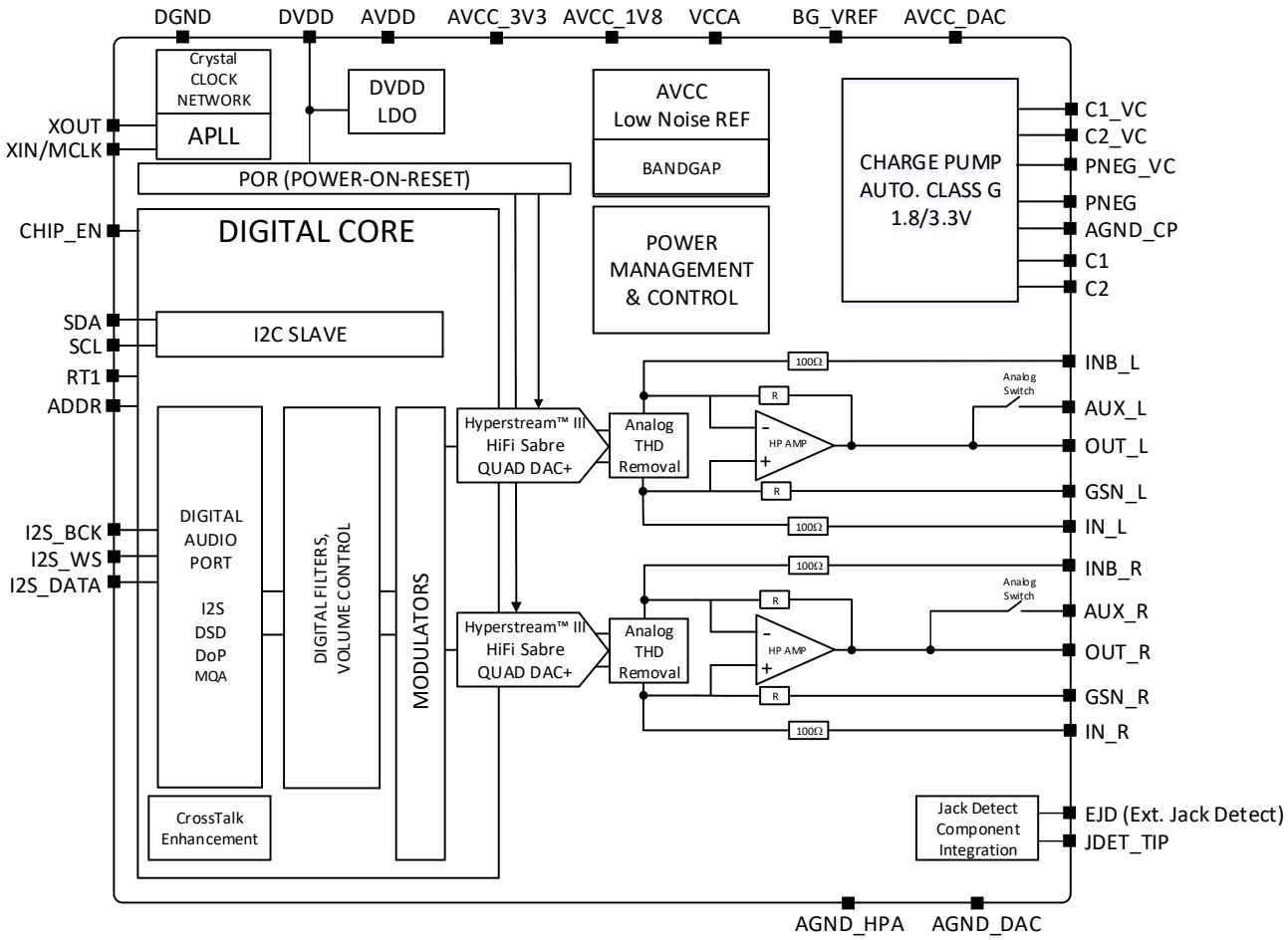


Figure 1. ES9219 Block Diagram

Typical Application

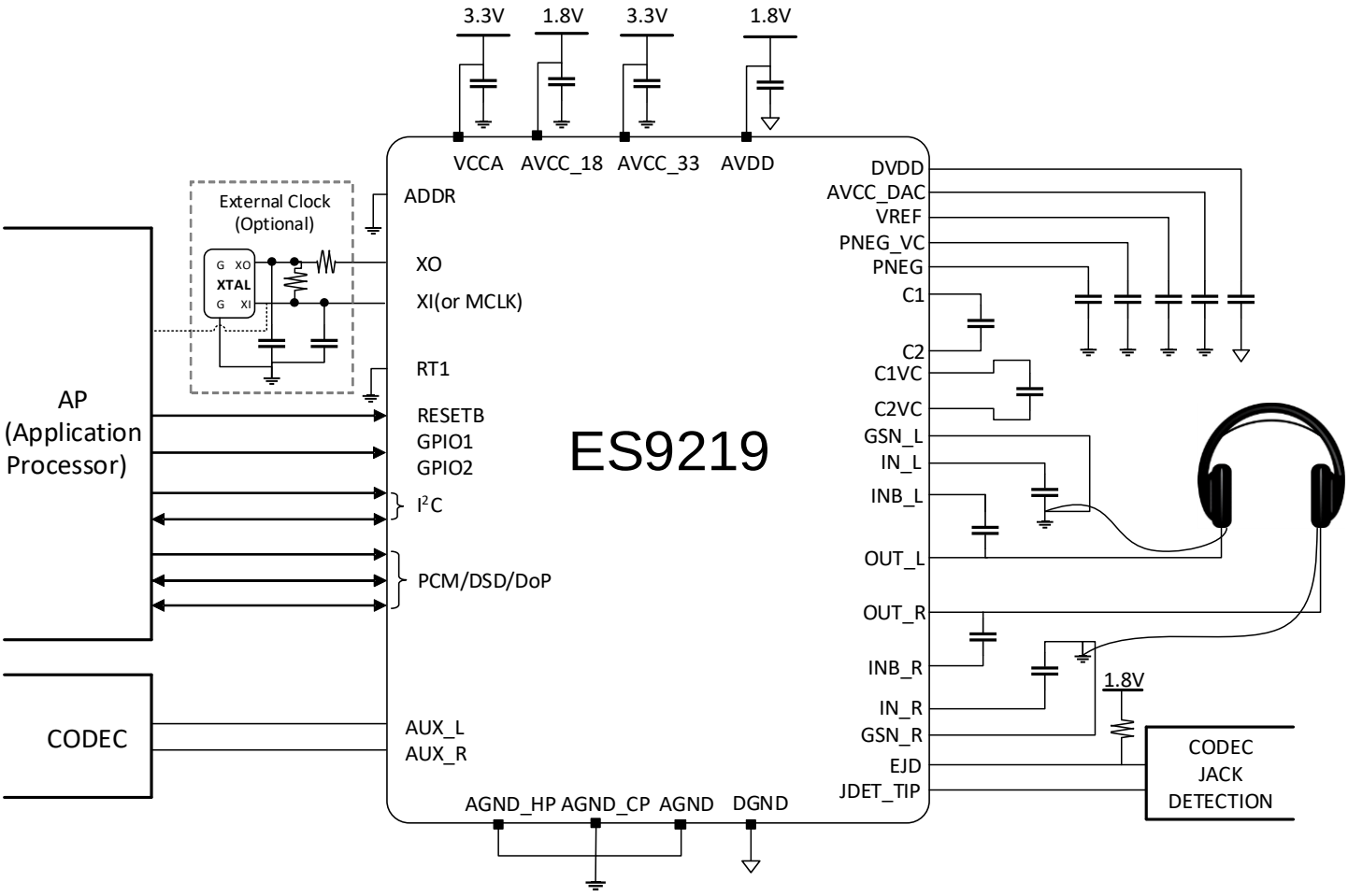


Figure 2. Typical Application Diagram

42 CSP Pinout

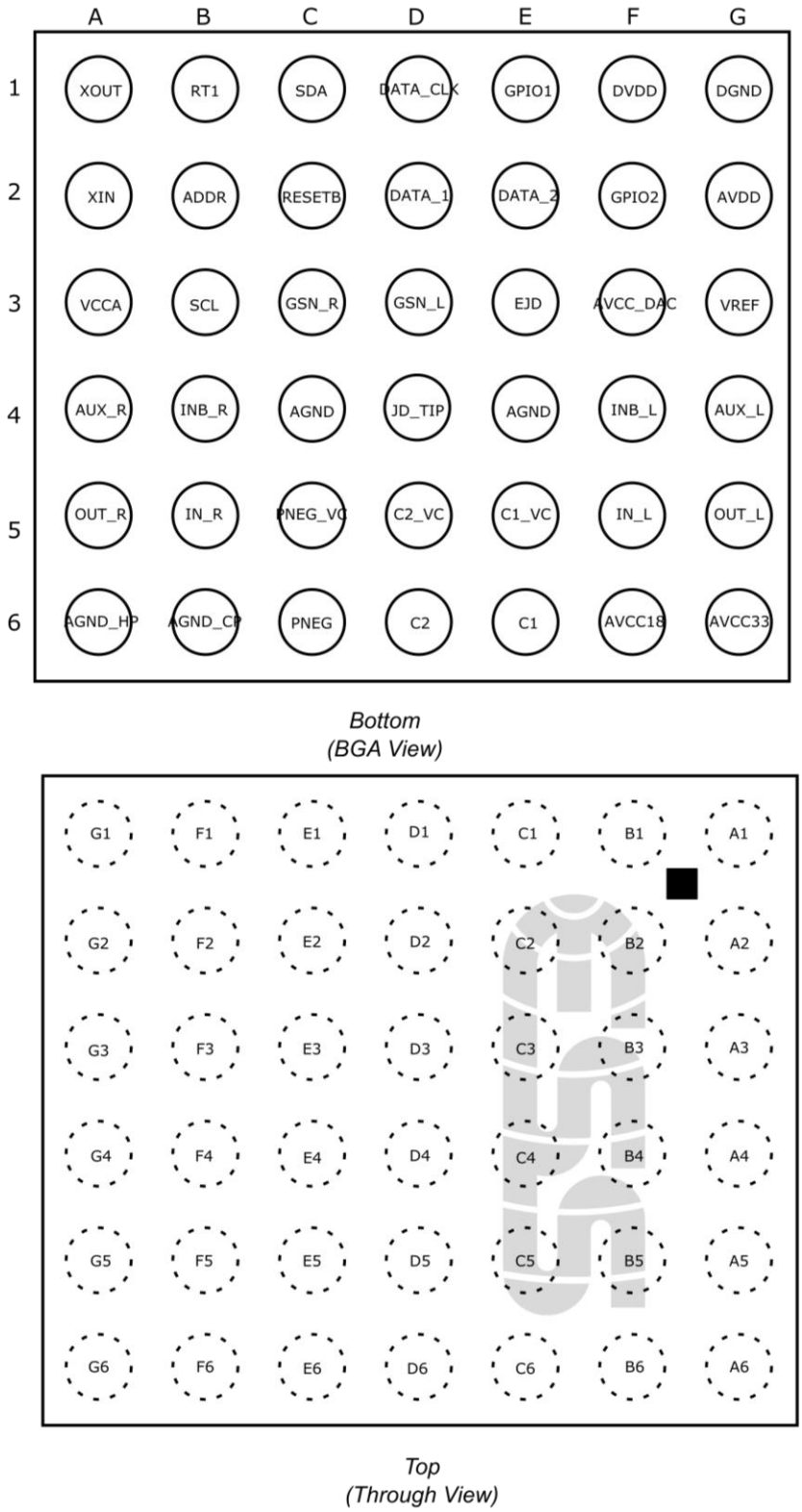


Figure 3: Pin Layout of ES9219C

42 CSP Pin Descriptions

Pin	Name	Pin Type	Reset State	Pin Description
A1	XOUT	AO	Floating	XTAL output
A2	XIN	AI	Floating	XTAL / MCLK input
A3	VCCA	Power	Power	Analog 1.8V/3.3V for OSC and on-chip AVCC_DAC regulator.
A4	AUX_R	AI	-	Auxiliary analog input (Right Channel)
A5	OUT_R	AO	-	Amplifier output (Right Channel)
A6	AGND_HP	Ground	Ground	Amplifier analog ground
B1	RT1	I	Tri-stated	Reserved. Must be connected to DGND for normal operation.
B2	ADDR	I	Tri-stated	I²C address select.
B3	SCL	I	Tri-stated	I²C serial clock input.
B4	INB_R	AI	-	Amplifier differential inverting input (Right Channel)
B5	IN_R	AI	-	Amplifier differential non-inverting input (Right Channel)
B6	AGND_CP	Ground	Ground	Charge pump analog ground.
C1	SDA	I/O	Tri-stated	I²C serial data input/output.
C2	RESETB	I	1'b0	Power down. Active low.
C3	GSN_R	-	-	Amplifier load ground sense. Right Channel
C4	AGND	Ground	Ground	DAC analog ground
C5	PNEG_VC	Power	Power	AVC negative supply. Internally supplied.
C6	PNEG	Power	Power	Amplifier negative supply. Internally supplied.
D1	DATA_CLK	I/O	Tri-stated	Slave Mode: Input for PCM Bit Clock or DSD Bit Clock, Master Mode: Output for PCM Bit Clock
D2	DATA1	I/O	Tri-stated	Slave Mode: Input for PCM Frame Clock or Input for DSD Data1 (Left Channel) Master Mode: Output for PCM Frame Clock
D3	GSN_L	-	-	Amplifier load ground sense. Left channel.
D4	JDET_TIP	AI		Audio Jack Tip connection for Jack detection
D5	C2_VC	-	-	AVC charge pump negative flying capacitor pin.
D6	C2	-	-	Amplifier charge pump negative flying capacitor pin.
E1	GPIO1	I/O	Tri-stated	GPIO 1
E2	DATA_2	I	Tri-stated	PCM Data Ch1+Ch2 or DSD Data2 (Right Channel)
E3	EJD	AI		External Jack Detection Connection
E4	AGND	Ground	Ground	DAC analog ground
E5	C1_VC	-	-	AVC charge pump positive flying capacitor pin.
E6	C1	-	-	Amplifier charge pump positive flying capacitor pin.
F1	DVDD	Power	Power	Digital core supply. Internally supplied.
F2	GPIO2	I/O	Tri-stated	GPIO 2 *special function in standby* (Aux. Path)
F3	AVCC_DAC	Power	Power	DAC analog supply. Internally supplied.
F4	INB_L	AI	-	Amplifier differential inverting input (Left Channel)
F5	IN_L	AI	-	Amplifier differential non-inverting input (Left Channel)
F6	AVCC18	Power	Power	Analog 1.8V supply for Amplifier, switch, AVC and charge pumps.
G1	DGND	Ground	Ground	Digital ground.
G2	AVDD	Power	Power	Digital 1.8V/3.3V supply for I/O and on-chip DVDD regulator.
G3	VREF	Power	Power	Low Noise reference for on-chip AVCC_DAC regulator.
G4	AUX_L	AI	-	Auxiliary analog input (Left Channel)
G5	OUT_L	AO	-	Amplifier output (Left Channel).
G6	AVCC33	Power	Power	Analog 3.3V supply for Amplifier, switch, AVC and charge pumps.

Functional Description

Sample Rate Notation

Mode	fs (target sample rate)	FSR (raw sample rate)
PCM Normal Mode	Frame Clock Rate	Frame Clock Rate
PCM OSF Bypass Mode	Frame Clock Rate / 8	Frame Clock Rate
DSD Mode	DSD Clock (DATA_CLK)	DSD data rate

PCM Pin Connections

The clock requirements in System Clock XI/MCLK must be met for proper operation in PCM mode.

Pin Name	Description
DATA_2	2-channel PCM serial data
DATA_1	Frame clock
DATA_CLK	Bit clock

DSD Pin Connections

The clock requirements in System Clock XI/MCLK must be met for proper operation in DSD mode.

Pin Name	Description
DATA_2	DSD Data mapped to Left Channel by default.
DATA_1	DSD Data mapped to Right Channel by default.
DATA_CLK	Bit clock

DoP Pin Connections

The clock requirements in System Clock XI/MCLK must be met for proper operation in DoP mode.

Pin Name	Description
DATA_2	2-channel DSD data encoded into PCM frames according to the DoP standard.
DATA_1	Frame clock
DATA_CLK	Bit clock

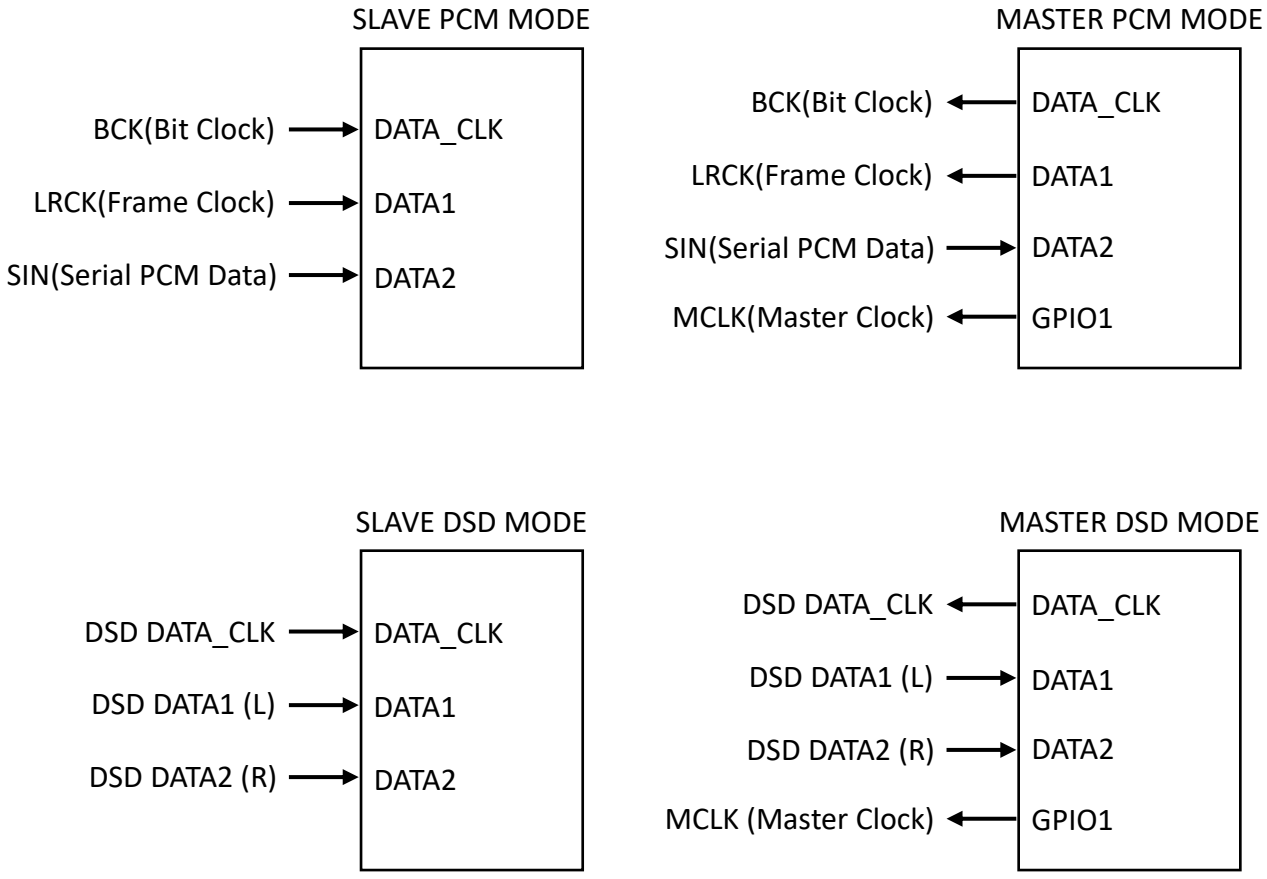
Master Mode

The DAC can be configured for master mode operation using Register 10: MASTER MODE AND SYNC CONFIGURATION.
Register 1: Input selections (0x01) *input_select* must also be set to either DSD or Serial mode. Auto Select will not work correctly in master mode.

DATA_CLK frequency can be configured using one of the following methods:

1. Set the desired *master_div* in Register 10: MASTER MODE AND SYNC CONFIGURATION.
   OR
2. Use NCO mode to set CLK/FSR ratio with Register 34-37: Programmable NCO (0x22 – 0x25). When NCO mode is enabled it has precedence and the *master_div* setting will be ignored.

An available GPIO pin can be configured to output CLK using Register 8: GPIO1-2 CONFIGURATION. GPIO1 is recommended for this purpose since GPIO2 is used to control Low Power Bypass mode.



Contact your local FAE for DoP master mode support.

Functional Description – Digital Features

Digital Audio Path

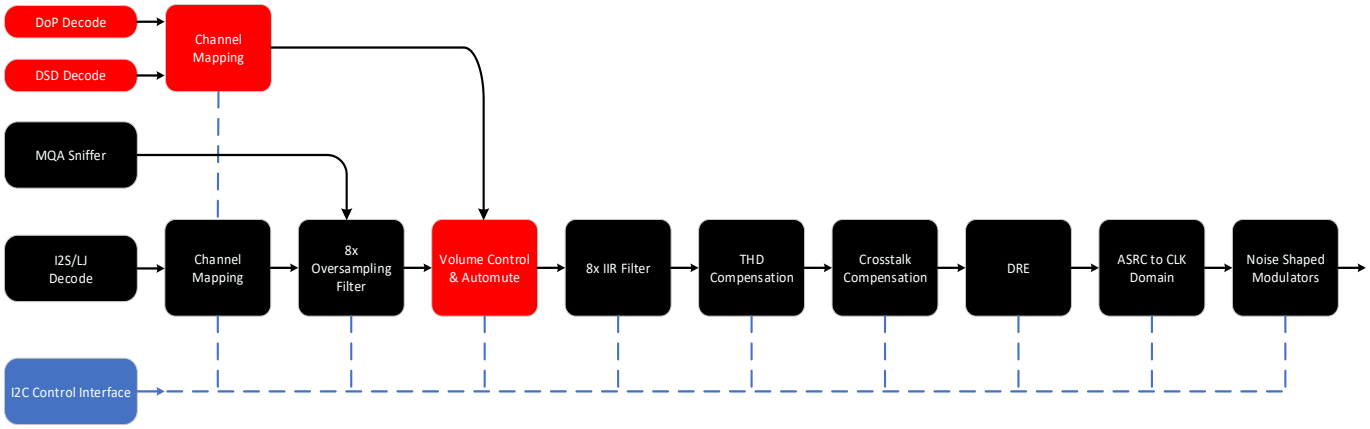


Figure 4 - Digital audio path

Soft Mute

When Mute is asserted the output signal will be ramped to the –∞ level. When Mute is reset the attenuation level will ramp back up to the previous level set by the volume control register. Asserting Mute will not change the value of the volume control register. The ramp rate is set by Register 6: DOP AND VOLUME RAMP RATE according to the following relationship:

$$\frac{2^{\text{vol\_rate}} * \text{FS}}{512} \text{ dB/s}$$

Mute can be triggered by any of the following settings:

- GPIO. See Register 8: GPIO1-2 CONFIGURATION.
- Explicit register setting. See Register 7: FILTER SHAPE AND SYSTEM MUTE.
- Automute. See Automute.

Automute

Automute must be enabled and configured using Register 2: MIXING AND AUTOMUTE CONFIGURATION. It is disabled by default. Automute is triggered when any one of the following conditions are met:

Mode	Detection Condition	Time
PCM	Data is lower than *automute_level* for the specified time	2096896 / (*automute_time* x 64 x fs)
DSD	Equal number of 1s and 0s in every 8 bits of data	2096896 / (*automute_time*) x DATA_CLK)

Automute_time can be set using Register 4: AUTOMUTE TIME.
Automute_level can be set using Register 5: AUTOMUTE LEVEL.

Volume Control

Each output channel has its own attenuation circuit. The attenuation for each channel is controlled independently. Each channel can be attenuated from 0dB to –127dB in 0.5dB steps. Each 0.5dB step transition takes up to 64 intermediate levels, depending on the *vol_rate* setting in Register 6: DOP AND VOLUME RAMP RATE. The result being that the level changes are done using small enough steps so that no switching noise occurs during the transition of the volume control. When a new volume level is set, the attenuation circuit will ramp softly to the new level.

The volume control can be either channel independent or synchronized using Register 27: GENERAL CONFIGURATION *ch1_volume*.

Master Trim

The master trim sets the 0dB reference level for the digital volume control of each DAC. The master trim is programmable via Register 17-20: MASTER TRIM. The master trim registers store a 32bit signed number.

This register value should never exceed the full scale signed value 32'h7FFFFFFF

Example: Setting the reference value to -1dB (from full-scale) = 32'h721482BF

System Clock XI/MCLK & BCK

A system clock is required for proper operation of the digital filters and modulation circuitry. It can be generated using an appropriate crystal, MCLK, or BCK in combination with the Analog PLL.

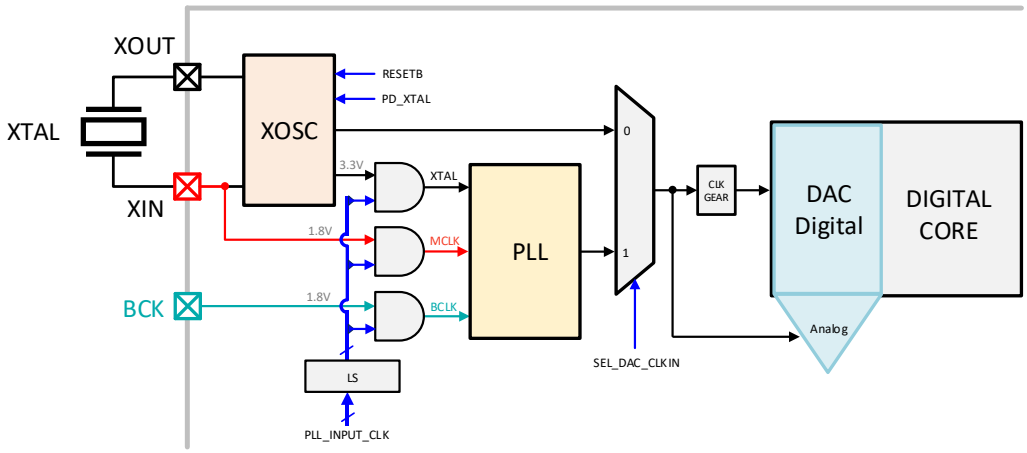


Figure 5: ES9219 MCLK & BCK Routing

MCLK Path in RED, BCK Path in Green, both will use the Analog PLL

Automatic clock gearing is supported to save power with the full XI (or MCLK) clock rate is not required.

$$\mathrm{CLK} = \frac{\mathrm{XI}}{clock\_div}$$

The minimum XI(MCLK) frequency must satisfy the following conditions:

Data Type	Minimum MCLK Frequency
DSD Data	CLK > 3 x FSR , FSR = 2.8224MHz (x 1, 2, or 4)
Serial Normal Mode	CLK > 128 x FSR, FSR ≤ 384kHz CLK = 128 x FSR (synchronous MCLK) with FSR ≤ 384kHz
Serial OSF Bypass Mode	CLK > 24 x FSR, FSR ≤ 768kHz

Data Clock

DATA_CLOCK must be (2 x *i2s_length*) x FSR for PCM mode, and FSR for DSD modes. This pin should be pulled low if not used.

Built-in Digital Filters

Two built-in digital filters are included for PCM mode. A programmable FIR filter is also included.
See PCM Filter Frequency Response for filter characteristics and Register 7: FILTER SHAPE AND SYSTEM MUTE for available filter settings.

Programmable FIR filter

A two stage interpolating FIR design is used. The interpolating FIR filter is generated using MATLAB, and can then be downloaded using a custom C code.

Example Source Code for Loading a Filter

```
// only accept 128 or 16 coefficients
// Note:  The coefficients must be quantized to 24 bits for this method!
// Note:  Stage 1 consists of 128 values (0-127 being the coefficients)
// Note:  Stage 2 consists of 16 values (0-13 being the coefficients, 14-15 are zeros)
// Note:  Stage 2 is symmetric about coefficient 13.  See the example filters for more information.
byte reg40 = (byte)(coeffs.Count == 128 ? 0 : 128);
for (int i = 0; i < coeffs.Count; i++)
{
    // stage 1 contains 128 coefficients, while stage 2 contains 16 coefficients
    registers.WriteRegister(40, (byte)(reg26 + i));

    // write the coefficient data
    registers.WriteRegister(41, (byte)(coeffs[i] & 0xff));
    registers.WriteRegister(42, (byte)((coeffs[i] >> 8) & 0xff));
    registers.WriteRegister(43, (byte)((coeffs[i] >> 16) & 0xff));

    registers.WriteRegister(44, 0x02);   // set the write enable bit
}
// disable the write enable bit when we're done
registers.WriteRegister(44, (byte)(setEvenBit ? 0x04 : 0x00));
```

For more information on programming a custom filter, contact your local FAE.

Standby Mode

For lowest power consumption, the following should be performed to enter stand-by mode:
Shut down the amplifier portion of the chip with Register 32: AMPLIFIER CONFIGURATION.

1. Pull RESETB low. This will:
    a. Shut off the DACs, oscillator and internal regulators.
    b. Force all digital I/O pins into tri-state mode
2. If XI is supplied externally, it should be stopped at a logic low level
3. Disable any power supplies connected to the chip

To resume from standby mode:

1. Enable all power supplies
2. Pull RESETB up
3. Reinitialize all registers

To resume from standby mode, bring RESETB to a logic-high and reinitialize all registers.

OPERATION Mode	RESETB	GPIO2
HiFi Mode **(DAC & HPA: ON, AUX SW: OFF)**	H	X
AUX Mode **(DAC & HPA: OFF, AUX SW: ON)**	L	H
Standby(Shutdown) Mode **(DAC, HPA, AUX SW: OFF)**	L	L

DVDD Supply

The ES9219 is equipped with a regulated DVDD supply powered from AVDD. The internal DVDD regulator should be decoupled to DGND with a capacitor that maintains a minimum value of 1μF at 1.2V over the target operating temperature range.
External 1.2V can be supplied if the customer would prefer to do so but setting the SEL1V in Register 46: ANALOG CONTROL OVERRIDE

OSF Bypass

The oversampling FIR filter can be bypassed using *bypass_osf* in Register 7: FILTER SHAPE AND SYSTEM MUTE, sourcing data directly into the IIR filter. The audio input should be oversampled at 8 x fs rate when OSF is bypassed to have the same IIR filter bandwidth as PCM audio sampled at fs rate. For example, an external signal at 44.1kHz can be oversampled externally to 8 x 44.1kHz = 352.8kHz and then applied to the serial decoder in either I^2S or LJ format. The maximum sample rate that can be applied is 768kHz (8 x 96kHz).

DSD Filter

A DSD filter with cutoff at 47kHz scaled by fs/44100 is available. See DSD FILTER Characteristics for more information.

THD Compensation

THD Compensation minimizes the non-linearity of the DAC output resistors and to a lesser degree the non-linearity of passive components in the output stage.

Non-linearity of the DAC output resistors can lead to output distortion in two ways:

1. Amplitude modulation of the output current from the DAC
2. Gain modulation of the output stage as the output impedance of the DAC swings with the audio signal

The ES9219 includes models for its output resistors and can compensate for their characteristic curve by finely adjusting the DAC codes for large and small signal amplitudes.

THD compensation can be enabled via *bypass_thd* in Register 13: THD BYPASS & MONO_MODE
The coefficient for manipulating second harmonic distortion is stored in Register 22-23: THD COMPENSATION C2
The coefficient for manipulating third harmonic distortion is stored in Register 24-25: THD COMPENSATION C3
Left and right channels use the same compensation coefficients unless enable_seperate_thd_comp in Register 48: ANALOG CONTROL SIGNALS is used.

CrossTalk Compensation

The ES9219 has registers built in to add (or subtract) a signed number from Ch1 to Ch2 and vice versa. This is to help mitigate the crosstalk between channels induced by the device or system.

See Register 128: CROSSTALK COMPENSATION CONFIG & Register 130-131: CROSSTALK SCALE CH1 for more details.

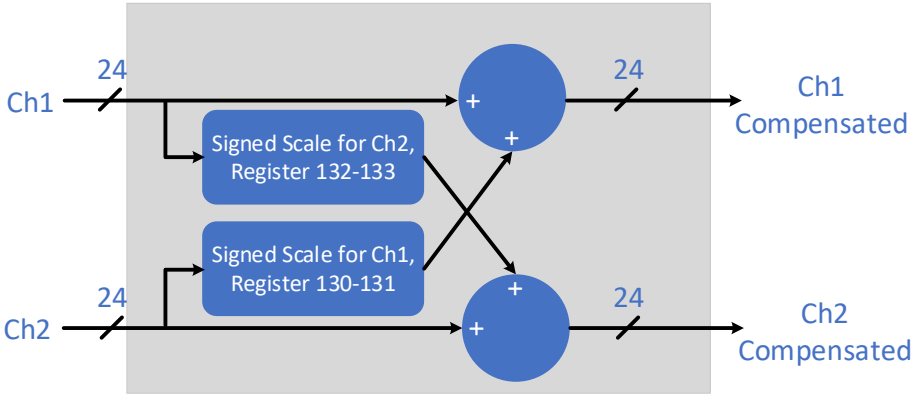


Figure 6: Diagram shows crosstalk compensation configuration

MQA Rendering

The ES9219 is a licensed MQA hardware renderer.

Enabling the MQA renderer is from Register 146: MQA CONFIG, and to check if the stream is locked query Register 77: READ LOCK STATUS.

Functional Description – Analog Features

Charge Pump

The ES9219 includes two charge pumps.

The main low noise charge pump uses a 500kHz switching frequency, which is outside the audio band and therefore does not interfere with audio signals. The chargepump switches are sequence controlled to minimize pops and clicks. This supply requires a 2.2μF (minimum) ceramic flying capacitor between pins C1 and C2 and a 22μF (recommended) ceramic hold capacitor from PNEG to AGND_CP. See ES9219C Reference Schematic.

The auxiliary charge pump uses the same switching frequency as the main chargepump, so no intermodulation frequencies are generated. It requires a 1μF (recommended) ceramic flying capacitor across pins C1_VC and C2_VC and a 1μF (recommended) ceramic hold capacitor from PNEG_VC to AGND_CP. See ES9219C Reference Schematic.

Use capacitors with an Equivalent Series Resistance (ESR) of less than 100mΩ for optimum performance. Low-ESR ceramic capacitors minimize the output resistance of the main charge pump. For best performance over the extended temperature range select capacitors with a minimum X5R dielectric, the X7R dielectric is preferred.

Analog Volume Control

ES9219

Analog volume control (AVC) provides improved noise performance as the gain is reduced. The hardware default programmable analog gain is -24dB with 1dB steps up to 0dB. See Register 3: ANALOG VOLUME CONTROL.

The AVC is forced to minimum gain until the transition to HiFi mode is complete. The ES9219 follows a programmed timing sequence to enter HiFi mode. Enabling the AVC is one of the last steps in that sequence. This procedure will not change the value of the analog volume control register.

See Register 32: AMPLIFIER CONFIGURATION.

Compensation Components

For optimum performance, matched feedback capacitors should be installed between OUT_L and INB_L, IN_L and GSN_L, OUT_R and INB_R, IN_R and GSN_R. These components set the bandwidth of the headphone amplifier. These capacitors should have a low temperature coefficient, NP0/C0G type are recommended. See ES9219C Reference Schematic

The ES9219 includes internal feedback resistors for reduced part-count. 2.2nF NP0/C0G feedback capacitors are recommended to filter out-of-band noise. (2.2nF equals 70KHz bandwidth @ 0dB analog gain, 2.0nF equals 80KHz bandwidth, and 1.5nF equals 100KHz bandwidth).

Output Switch

The output signal is selected by an ultra-low THD analog switch that connects either to the HiFi audio headphone amplifier or to an alternate audio source. A typical alternate source may be voice or another DAC. There are two different ways to use the output switch:

LowFi Mode

The ultra-low THD analog switch may be controlled using Register 32: AMPLIFIER CONFIGURATION. This allows audio to pass from an alternate source to the output. The digital core remains powered on and ready for a quick transition back to HiFi mode. All supplies must be enabled.

Low Power Bypass Mode

The ultra-low THD analog switch may be controlled using GPIO2 after RESETb is asserted and the chip is in standby. This allows audio to pass from an alternate source to the output without the use of the digital core. AVCC_HP and AVCC_CP supplies must be enabled.

This mode is activated when RESETB = pulled down and GPIO2=pulled up.

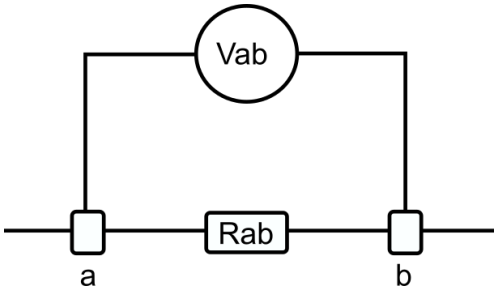
Analog THD Removal (ATR)

The ESS Sabre DAC's can be operated in 2 fundamental modes of operation, Voltage Mode and Current Mode.

Voltage mode

The Sabre DAC is connected to a single OPAMP operating in the Differential to Single Ended mode. This mode is cost efficient, however it exposes the 2nd and 3rd order voltage coefficients of the on die poly-silicon resistors used in the D/A conversion interface. There are 64 poly-silicon unit weight resistors that sum together to make the analog representation of the digital value. Each resistor contributes 1/64th of the output, and each resistor is exposed to a signal dependent voltage across it. The 2nd and 3rd order terms create 2nd and 3rd order harmonics from this simplified equation of the resistor.

$$Rab = Rnom + (Rnom * Vab * Vc2^2) + (Rnom * Vab * Vc3^3)$$



Where:
Rab: Resistance across the resistor terminals
Rnom: The Nominal value of the resistor.
Vab: Voltage across the resistor terminals
Vc2: Squared Voltage coefficient term
Vc3: Cubed Voltage coefficient term

Current mode

In this mode of operation of the Sabre DAC, the output of the DAC is held at a virtual ground, therefore the current going though each of the has only 2 states, either sourcing our sinking. Even though the resistors still have the 2nd and 3rd order voltage coefficients, there is only ever 2 voltages applied across the resistor, which means that the 2nd and 3rd order terms end up being a DC offset instead of harmonic distortion. This is typically done by connecting the Sabre DAC to an I/V convertor stage, then to a Differential to Single Ended stage, which requires 3 opamps to implement.

The ES9219 Implements analog circuitry that puts the Sabre DAC's into "Current Mode" by integrating the I/V stage. This allows the Sabre DAC's to achieve the best possible linearity.

Overcurrent Protection

Overcurrent Protection (OCP) protects the amplifier output stage by independently sensing the positive and negative output current on the OUT_R and OUT_L pins. Once the current exceeds a built-in threshold for a cumulative user programmable timeout period, an OCP event will be triggered and both DAC channels will be muted.

OCP must be enabled and configured using *oc_sd_en* and *oc_sd_gain* in Register 11: OVERCURRENT PROTECTION; it is disabled by default.

When an overcurrent event is triggered, *oc_sd_mute* Register 72: READ INPUT SELECTION AND AUTOMUTE STATUS will be set and latched to indicate which channel triggered the event.

OCP does not automatically reset when the overcurrent condition is removed. After an OCP event occurs, the state of the OCP circuit needs to be manually cleared. This is accomplished by toggling OCP disabled-enabled with *oc_sd_en*.

Once enabled, the OCP status can be monitored in one of two ways:

1. Poll the *oc_sd_mute* flags in Register 72: READ INPUT SELECTION AND AUTOMUTE STATUS
2. Configure Register 8: GPIO1-2 CONFIGURATION to set the desired GPIO pin to Interrupt mode and set Register 33: INTERRUPT MASK appropriately.

Analog PLL

The Fractional-N (Frac-N) Analog PLL supports high-frequency clock generation from one of three clock sources (See Register 201: PLL CONFIG5). It can be configured without the need for any additional system clock. Write-only access to the PLL configuration registers is available via a synchronous I2C interface.

The PLL registers may be written using the I²C Synchronous Slave Interface. No system clock is required. These registers are write-only.

The PLL registers may be read back using the I2C Slave Interface. A system clock is required for readback. These PLL registers are read-only by default. If a system clock is already present, write access for the PLL registers may be enabled with *mcu_configure_pll*.

External Jack Detection Integration

This is a new feature of the ES9219. Feature description to be added in next revision.

Absolute Maximum Ratings

PARAMETER	RATING
Positive Supply Voltage • AVDD, VCCA • AVCC_33 • AVCC_18 • DVDD	 +4.0V with respect to GND +4.0V with respect to GND +4.0V with respect to GND +1.8V with respect to GND
Negative Supply Voltage (PNEG & PNEG_VC)	–4.0V with respect to GND
Output Short-Circuit to GND (OUT_L, OUT_R)	Default Disable (Register setting)
Storage temperature	–65°C to +150°C
Operating Junction Temperature	+125°C
Voltage range for digital input pins	–0.3V to AVDD+ 0.3V
ESD Protection Human Body Model (HBM) Charge Device Model (CDM)	 2000V 500V

WARNING: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Operating temperature	T_A	–20°C to +70°C

Power Consumption

Power Supply	Symbol	Voltage	Nominal Current / Power Consumption (Note 1)			
			HiFi 2V mode	HiFi 1V mode	LPB mode (Note 2)	Standby (Note 3)
Digital I/O	AVDD	+1.8V ±5%	5.5mA	8.5mA	0	<<1 uA
Analog core	VCCA	+3.3V ±5%	8mA	2mA	4uA	<<1uA
Analog power	AVCC_18 AVCC_33	+1.8V ±5% +3.3V ±5%	40uA 9.8mA	3.4mA 5mA	40uA	<<1 uA <<1 uA
Internally Generated	DVDD AVCC_DAC PNEG PNEG_VC	+1.2V ±5% +1.25, 1.4, 2.5 or 2.8V ±5% -1.8V or -3.3V ±5% -3.3V ±5%	-	-	-	-
Total			69mW	44.5mW	0.5mW	1uW

Notes:

1) fs = 44.1kHz, external XI = 27MHz, auto clock gearing, I^2S input, output unloaded, internal DVDD, all external supply voltages at nominal values, ATR (Analog THD Removal) is off.
2) LPB = Low power Bypass Mode
3) RSTb = 0, GPIO2 = 0

DC Electrical Characteristics

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNIT	COMMENTS
High-level input voltage	VIH	AVDD / 2 + 0.4		V	
Low-level input voltage	VIL		0.4	V	
High-level output voltage	VOH	AVDD – 0.2		V	IOH = 1.5mA
Low-level output voltage	VOL		0.2	V	IOL = 7.5mA

Analog Performance

Test Conditions (unless otherwise stated)

1. T_A = 25ºC, VCCA =+3.3V, AVDD = +1.8V, internal DVDD with 1.0µF ±20% decoupling, fs = 48kHz, XI(MCLK) = 49.152MHz & 32-bit data
2. SNR/DNR: A-weighted over 20Hz-20kHz in averaging mode, Reference 2.0Vrms, HiFi2V mode.
   THD+N: un-weighted over 20Hz-20kHz bandwidth

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			32		Bits
CLK (PCM normal mode)	Note *1	128FSR		50M	Hz
CLK (PCM OSF bypass mode)		24FSR			
CLK (DSD mode)		3FSR			
DYNAMIC PERFORMANCE (digital input to headphone amplifier output @ HiFi Mode)					
Full Scale Output	0dBFS 600Ω		2.0	2.06	Vrms
SNR	Zero input 600Ω (Note *3)		135		dB-A
DNR	–60dBFS 600Ω		121		dB-A
DNR (w/DRE enabled)			123		dB-A
THD+N	2Vrms into 300Ω		-114		dB
OUTPUT AMPLIFIER					
Output offset voltage	Note *2		<-0.5	0.15	mV
AUXILIARY ANALOG INPUTS					
Input voltage				1.0	Vrms
Digital Filter Performance					
Mute Attenuation			127		dB
PCM Filter Characteristics (Linear Phase Fast Roll Off)					
Pass band	±0.002dB			0.453 x fs	Hz
	–3dB			0.484 x fs	Hz
Stop band	< –120dB	0.55 x fs			Hz
Group Delay			35 / fs		s
PCM Filter Characteristics (Hybrid Fast Roll-off)					
Pass band	±0.01dB			0.404 x fs	Hz
	–3dB			0.430 x fs	Hz
Stop band	< -94.5dB < -106dB	0.504 x fs 0.512 x fs			Hz
Group Delay			18.5 / fs		s

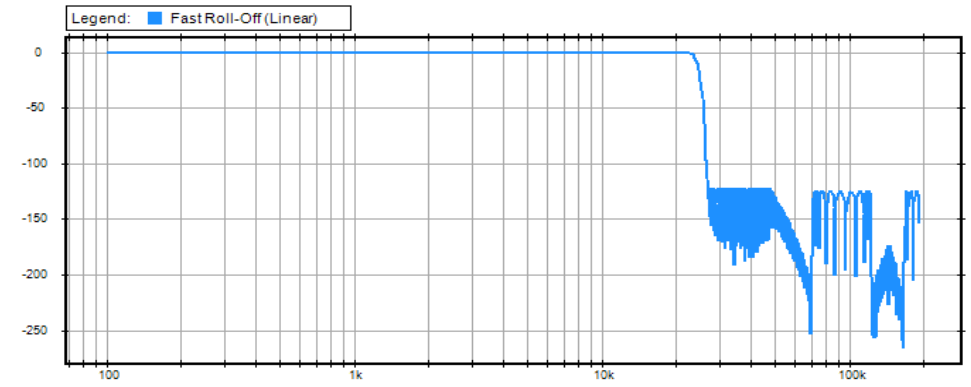
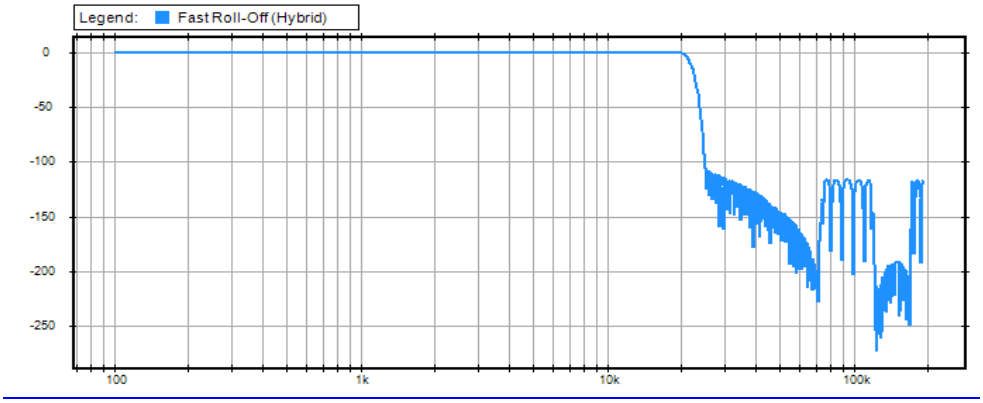
Notes:

*1. CLK at 128FSR is also supported in Synchronous Mode

*2. Measured between OUT_L and GND, and OUT_R and GND, DAC outputs set to DAC output set to 50/50.

*3. Automute Enabled, Automute configured for Mute + Ramp-to-ground, Analog Automute, Amp_pdb_ss

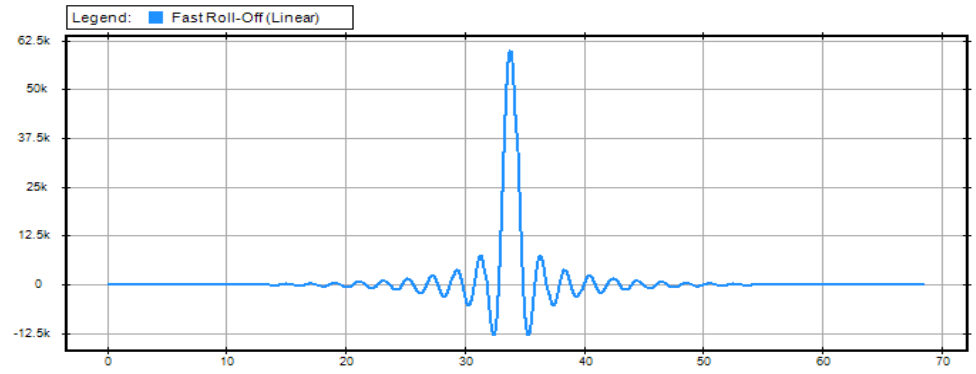
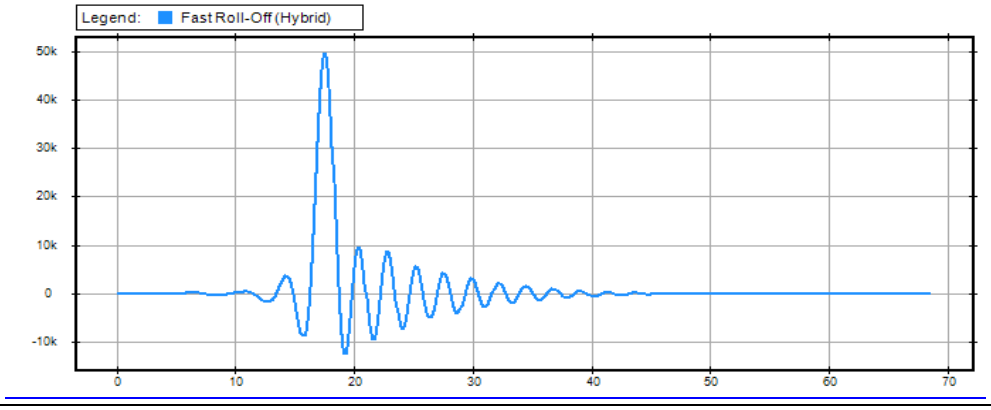
PCM Filter Frequency Response

Filter	Response Curve
Linear phase fast roll-off filter (dB)	
Hybrid fast roll-off filter (dB)	

Unit: fs (Hz) / 48000

Figure 3. PCM Filter Frequency Response

PCM Filter Impulse Response

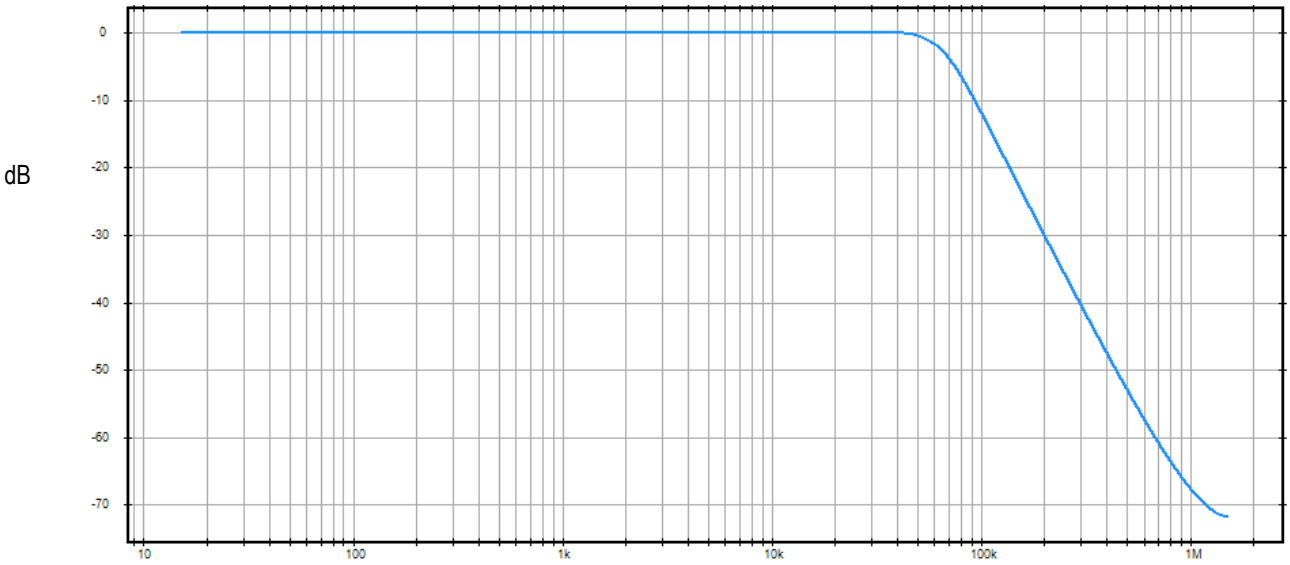
Filter	Response Curve
Linear phase fast roll-off filter	
Hybrid fast roll-off filter	

Unit: 1/fs (s)

Figure 4. PCM Filter Impulse Response

DSD Filter Characteristics

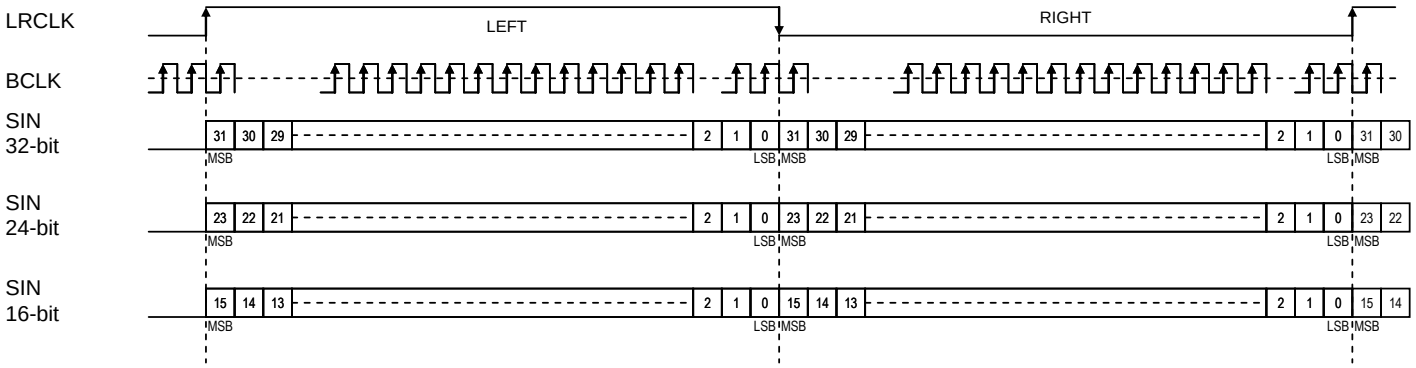
DSD Filter Frequency Response



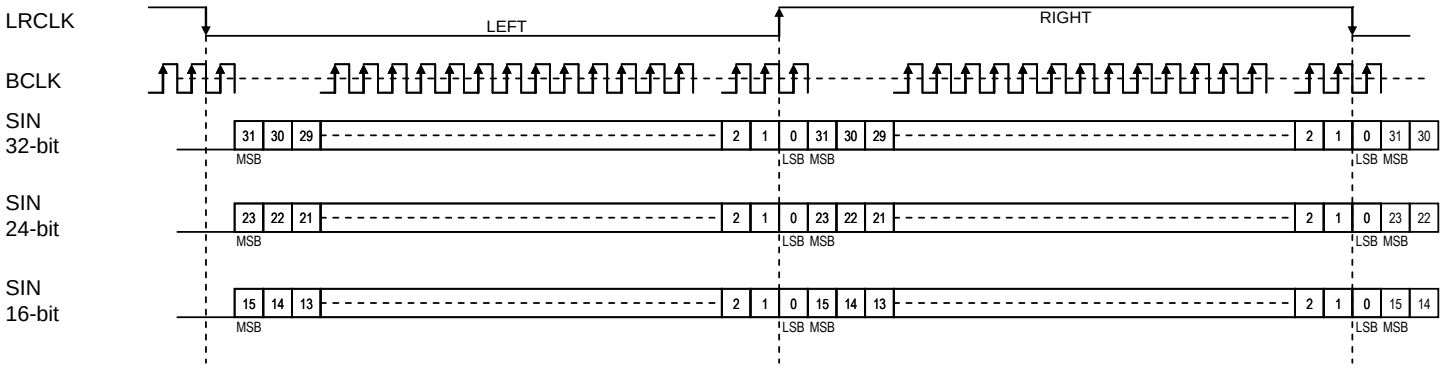
Unit: DATA_CLK (Hz) / 2822400

Audio Interface Formats

Several interface formats are provided so that direct connection to common audio processors is possible. The available formats are shown in the following diagrams. The audio interface format can be set by programming the registers.



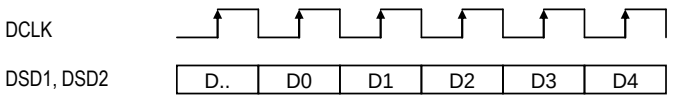
LEFT JUSTIFIED FORMAT



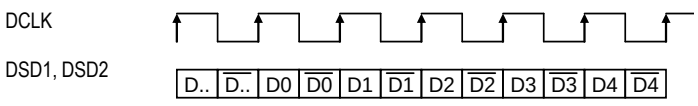
I2S FORMAT

Note: for Left-Justified and I²S formats, the following number of BCLKs is present per (left plus right) frame:

- 16-bit mode: 32 BCLKs
- 24-bit mode: 48 BCLKs
- 32-bit mode: 64 BCLKs



DSD NORMAL MODE



DSD PHASE MODE

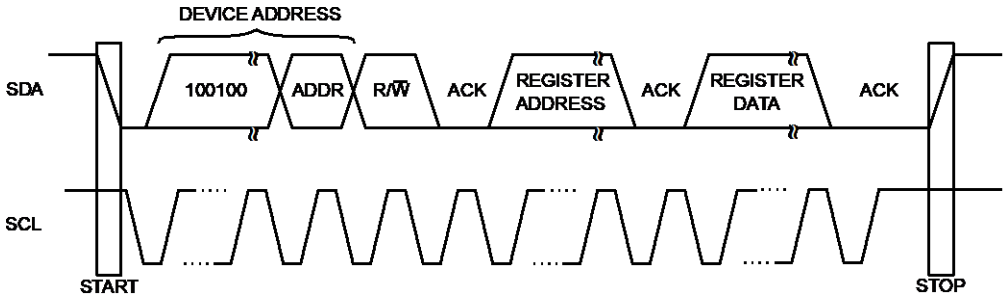
Figure 5. Audio Interface Format

Serial Control Interface

I²C Slave Interface

This interface is only available when a system clock is present. 2 device addresses are selectable using the ADDR pin.

ADDR	DEVICE ADDRESS
0	0x90
1	0x92

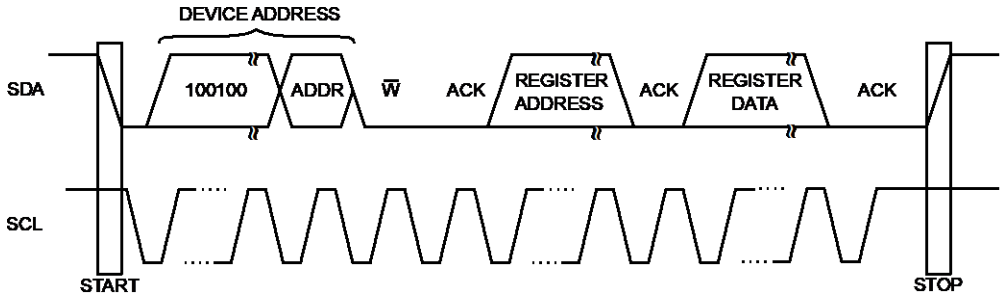


I²C Synchronous Slave Interface

This I²C interface is Write-Only. A system clock is not required to write to this interface. 2 device addresses are selectable using the ADDR pin. This interface is available if the ES9219 is enabled (RESETb). This interface allows the PLL, and several other clock-related registers to be configured without the need for a system clock.

The registers on this interface are mirrored by registers on the I2C Slave Interface.

ADDR	DEVICE ADDRESS
0	0x94
1	0x96



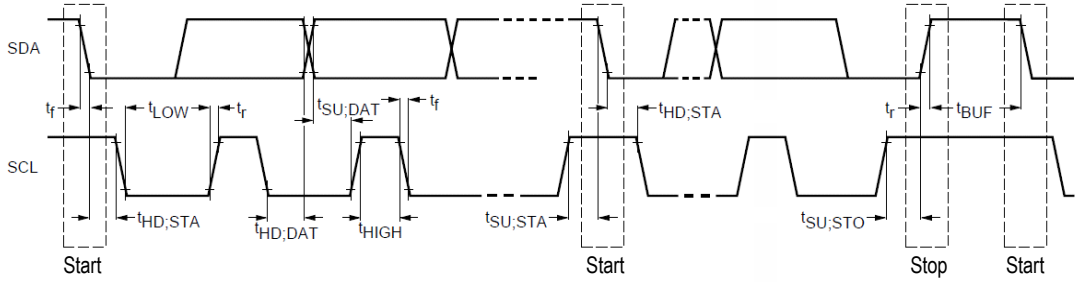


Figure 6. I2C Control Interface

Parameter	Symbol	CLK Constraint	Standard-Mode		Fast-Mode		Unit
			MIN	MAX	MIN	MAX	
SCL Clock Frequency	f_{SCL}	< CLK/20	0	100	0	400	kHz
START condition hold time	$t_{HD,STA}$		4.0	-	0.6	-	µs
LOW period of SCL	t_{LOW}	>10/CLK	4.7	-	1.3	-	µs
HIGH period of SCL (>10/CLK)	t_{HIGH}	>10/CLK	4.0	-	0.6	-	µs
START condition setup time (repeat)	$t_{SU,STA}$		4.7	-	0.6	-	µs
SDA hold time from SCL falling - All except NACK read - NACK read only	$t_{HD,DAT}$		0 2/CLK	-	0 2/CLK	-	µs s
SDA setup time from SCL rising	$t_{SU,DAT}$		250	-	100	-	ns
Rise time of SDA and SCL	t_r		-	1000		300	ns
Fall time of SDA and SCL	t_f		-	300		300	ns
STOP condition setup time	$t_{SU,STO}$		4	-	0.6	-	µs
Bus free time between transmissions	t_{BUF}		4.7	-	1.3	-	µs
Capacitive load for each bus line	C_b		-	400	-	400	pF

The I2C master clock is affected by the clock gearing. If the auto clock gearing lowers CLK by too much it can cause I2C transactions to fail. See Register 29: GPIO CONFIGURATION AND AUTO CLOCK GEAR for clock gearing options.

CLK Requirement	t(SCL high) >=10*t(Clock Gear(CLK)) t(SCL low) >=10*t(Clock Gear(CLK))

The system must ensure this condition can still be met when enabling automatic clock gearing. If the criterion cannot be met for all clock gear settings, then the clock gearing must be limited using Register 29: GPIO CONFIGURATION AND AUTO CLOCK GEAR.

XIN/MCLK Timing

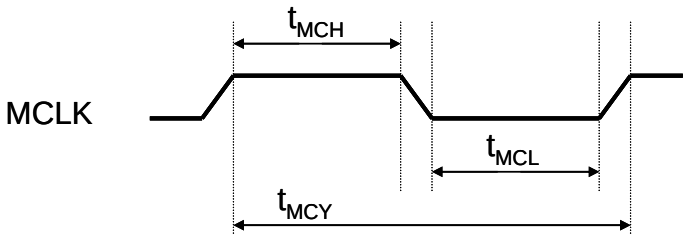
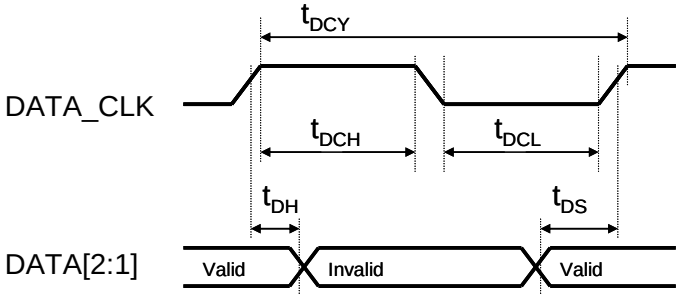


Figure 7. Clock Timing

Parameter	Symbol	Min	Max	Unit
MCLK pulse width high	T_{MCH}	9.0	90	ns
MCLK pulse width low	T_{MCL}	9.0	90	ns
MCLK cycle time	T_{MCY}	20	200	ns
MCLK duty cycle		45:55	55:45	

$$5MHz \leq MCLK \leq 50MHz$$

Audio Interface Timing



Parameter	Symbol	Min	Max	Unit
DATA_CLK pulse width high	t_{DCH}	9.0		ns
DATA_CLK pulse width low	t_{DCL}	9.0		ns
DATA_CLK cycle time	t_{DCY}	20		ns
DATA_CLK duty cycle		45:55	55:45	
DATA set-up time to DATA_CLK rising edge	t_{DS}	4.1		ns
DATA hold time to DATA_CLK rising edge	t_{DH}	2		ns

Figure 8. Audio Interface Timing

Notes:

- Audio data on DATA[2:1] are sampled at the rising edges of DATA_CLK and must satisfy the setup and hold time requirements relative to the rising edge of DATA_CLK
- For DSD Phase mode, the normal data (D0, D1, D2) must satisfy the setup and hold time requirements relative to the rising edge of DATA_CLK. The complimentary data (D0, D1, etc.) will be ignored.

Recommended Power-up Sequence

External Powered Oscillator / MCLK

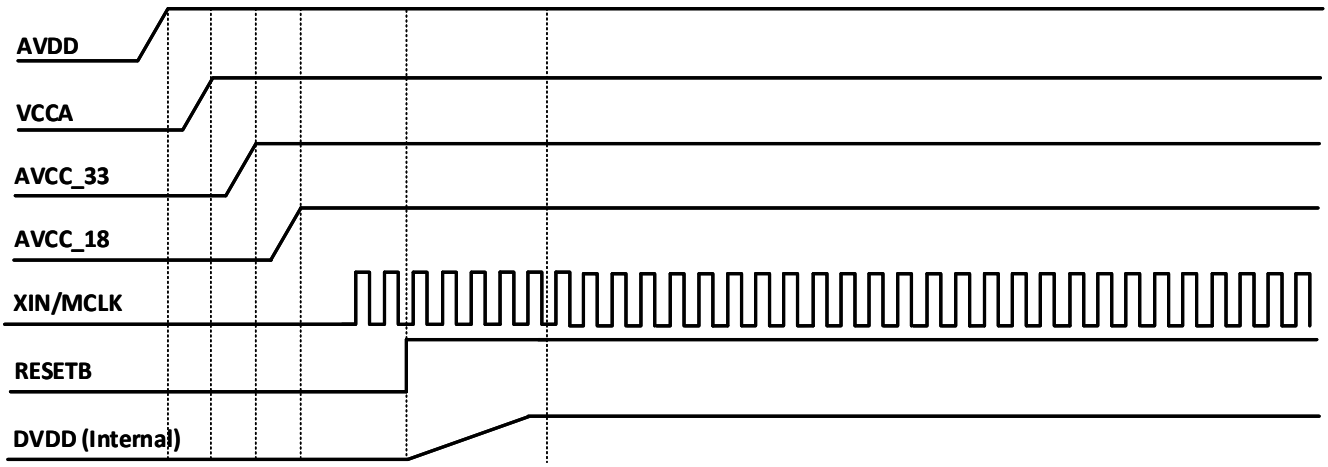


Figure 9. Using external powered oscillator or MCLK

Crystal

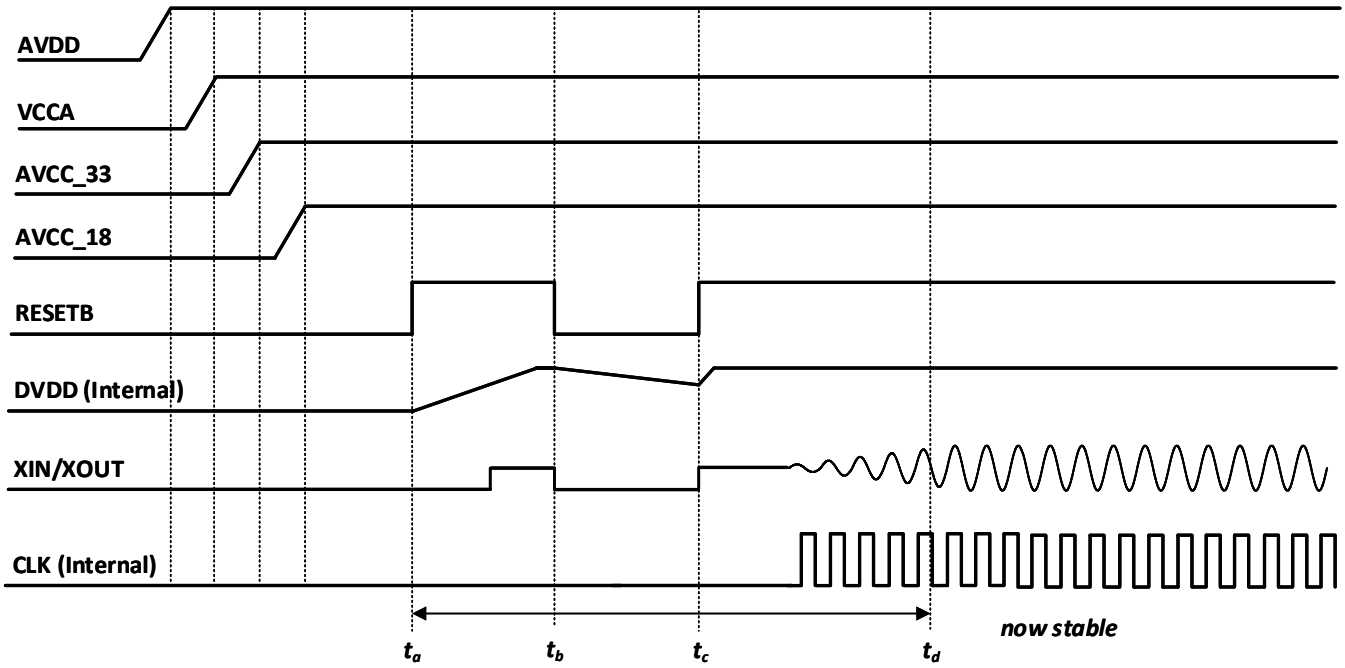


Figure 10. Crystal with internal oscillator

When a crystal is used with internal DVDD, it is possible for core timing requirements to be violated during chip startup. The following measures should be taken to ensure default register values are loaded correctly:

1. Use a small decoupling capacitor at the DVDD pin. 1µF maximum is recommended.
2. Consult the crystal vendor to optimize crystal circuitry. The chip has a 2-stage reset pipeline. If the oscillator starts slowly for any reason, more than two runt-pulses may occur and the reset pipeline will not be sufficient to prevent invalid core timing.

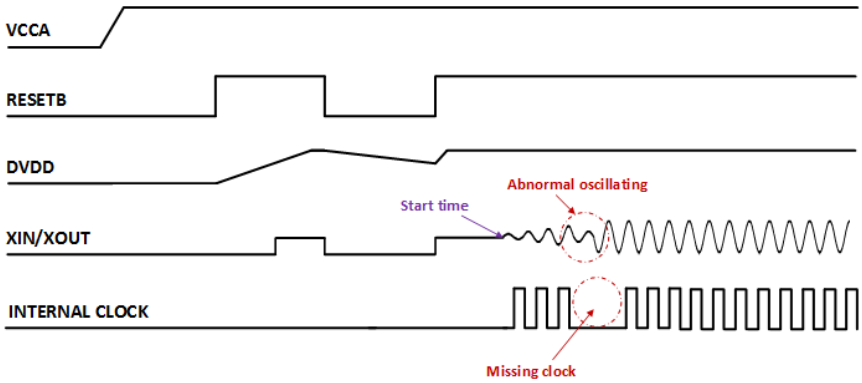


Figure 11. Non-optimal crystal circuitry

3. Perform two hardware resets (RESETB is de-asserted), followed by a software reset.
   For a 1µF DVDD de-coupling capacitor:

$$70\mu s \leq t_b - t_a \leq 100\mu s$$

$$50\mu s \leq t_c - t_b \leq 150\mu s$$ DVDD should not fall below 1V during $t_c - t_b$.

$$t_d - t_a \approx 1.5ms$$

Device Register Map

Address (Hex)	Address (Dec)	Register	7	6	5	4	3	2	1	0
0x0	0	SYSTEM REGISTERS	OSC_DRV				CLK_GEAR		RESERVED	SOFT_RESET
0x1	1	INPUT SELECTION	SERIAL_LENGTH		SERIAL_MODE		AUTO_SELECT		INPUT_SELECT	
0x2	2	MIXING AND AUTOMUTE CONFIGURATION	AUTOMUTE_CONFIG		ANALOG_AUTOMUTE	AUTOMUTE_TIMER_FAST	CH2_MIX_SEL		CH1_MIX_SEL	
0x3	3	ANALOG VOLUME CONTROL	RESERVED		RESERVED	ANALOG_VOLUME_MAIN				
0x4	4	AUTOMUTE TIME	AUTOMUTE_TIME							
0x5	5	AUTOMUTE LEVEL	RESERVED	AUTOMUTE_LEVEL						
0x6	6	DOP AND VOLUME RAMP RATE	RESERVED				DOP_ENABLE	VOLUME_RATE		
0x7	7	FILTER SHAPE AND SYSTEM MUTE	FILTER_SHAPE			RESERVED	BYPASS_OSF	RESERVED		MUTE
0x8	8	GPIO1-2 CONFIGURATION	GPIO2_CFG				GPIO1_CFG			
0x9	9	RESERVED	RESERVED							
0xA	10	MASTER MODE AND SYNC CONFIGURATION	MASTER_MODE	MASTER_DIV		128fs_MODE	LOCK_SPEED			
0xB	11	ANALOG SWAP	OC_SD_EN	OC_SD_GAIN			RESERVED			
0xC	12	DPLL BANDWIDTH	DPLL_BW_SERIAL				DPLL_BW_DSD			
0xD	13	THD BYPASS & MONO MODE	RESERVED	BYPASS_THD	RESERVED	MONO_MODE	RESERVED			
0xE	14	SOFT START CONFIGURATION	SOFT_START	RESERVED	SOFT_START_TYPE	SOFT_START_TIME				
0xF-0x10	15-16	VOLUME CONTROL	VOLUME_2							
0x11-0x14	17-20	MASTER TRIM	MASTER_TRIM							
0x15	21	GPIO INPUT SELECTION	GPIO_INPUT_SEL2		GPIO_INPUT_SEL1		RESERVED			
0x16-0x17	22-23	THD COMPENSATION C2	THD_COMP_C2							
0x18-0x19	24	THD COMPENSATION C3	THD_COMP_C3							
0x1A	26	CHARGE PUMP SOFT START DELAY	CP_SS_DELAY							
0x1B	27	GENERAL CONFIGURATION	ASRC_EN	RESERVED			CH1_VOLUME	RESERVED		
0x1C	28	RESERVED	RESERVED							
0x1D	29	GPIO CONFIGURATION AND AUTO CLOCK GEAR	INVERT_GPIO		RESERVED			AUTO_CLK_GEAR	MAX_CLK_GEAR	
0x1E	30	CHARGE PUMP CLOCK	CP_CLK_DIV							
0x1F	31	CHARGE PUMP CLOCK	CP_CLK_SEL		CP_CLK_EN		CP_CLK_DIV			
0x20	32	AMPLIFIER CONFIGURATION	AMP_PDB_SS	RESERVED	RESERVED	AMP_MODE_GPIO		RESERVED		
0x21	33	INTERRUPT MASK	OCR_SD_MASK	OCL_SD_MASK	OCR_MASK		OCL_MASK		AUTOMUTE_MASK	LOCK_MASK
0x22-0x26	34-37	PROGRAMMABLE NCO	NCO_NUM							
0x26	38	I/O WEAK KEEPERS	RESERVED							
0x27	39	reserved	RESERVED							
0x28	40	PROGRAMMABLE FIR RAM ADDRESS	COEFF_STAGE	COEFF_ADDR						

0x29-0x2B	41-43	PROGRAMMABLE FIR RAM DATA	PROG_COEFF_DATA							
0x2C	44	PROGRAMMABLE FIR CONFIGURATION	RESERVED					EVEN_STAGE2_COEFF	PROG_COEFF_WE	PROG_COEFF_EN
0x2D	45	ANALOG CONTROL OVERRIDE 1	ENAUX	AREG_PDB	ENHPA	CPH_ENS	CPH_ENW	APDB	CP_CLK_SEL	RESERVED
0x2E	46	ANALOG CONTROL OVERRIDE 2	DIG_OVER_EN	RESERVED		RESERVED		SEL1V	SHTOUTb	SHTINb
0x2F	47	ANALOG CONTROL OVERRIDE 3	ENFCB	ENCP_OE	ENAUX_OE	CPL_ENS	CPL_ENW	SEL3V3_PS	ENSM_PS	SEL3V3_CPH
0x30	48	ANALOG CONTROL SIGNALS	RESERVED	ENHPA_OUT	RESERVED		HPA_HIQ	ENABLE_SEPARATE_THD_COMP	RESERVED	
0x31	49	AUTOMATIC CLOCK GEARING THRESHOLDS	CLK_GEAR_MIN_THRESH							
0x32	50	AUTOMATIC CLOCK GEARING THRESHOLDS	CLK_GEAR_MAX_THRESH				CLK_GEAR_MIN_THRESH			
0x33	51	AUTOMATIC CLOCK GEARING THRESHOLDS	CLK_GEAR_MAX_THRESH							
0x34	52	CHARGE PUMP SOFT START 2	RESERVED							
0x35-0x36	53-54	THD COMPENSATION C2 -CH2	THD_COMP_C2_Ch2							
0x37-0x38	55-56	THD COMPENSATION C3 - CH2	THD_COMP_C3_Ch2							
0x39-0x3C	57-60	RESERVED	RESERVED							
0x40	64	CHIP STATUS	CHIP_ID						AUTOMUTE_STATUS	LOCK_STATUS
0x41	65	GPIO Readback	ocbr_pos	ocbl_pos	ocbr_neg	obcl_neg	clk_gear_rb		gpio2	gpio1
0x42-0x45	66-69	DPLL Number	DPLL_NUM							
0x46	70	RESERVED	RESERVED							
0x47	71	RESERVED	RESERVED							
0x48	72	READ INPUT SELECTION AND AUTOMUTE STATUS	OCR_SD_MUTE	OCL_SD_MUTE	AMR	AML	INPUT_SELECTION			
0x49-0x4B	73-75	READ PROGRAMMABLE FIR RAM DATA	PROG_COEFF_OUT							
0x4C	76	READ DRE STATUS	RESERVED		CHANNEL_GAIN2	CHANNEL_GAIN1	DRE_SELECT2	DRE_SELECT1	DRE_DETECT2	DRE_DETECT1
0x4D	77	READ LOCK STATUS	RESERVED					MQA_LOCKED	PLL_LOCKED	LOCK_STATUS_ASRC
0x4E-0x55	78-85	RESERVED	RESERVED							
0x80	128	CROSSTALK COMPENSATION	BYPASS_CT	ENABLE_PLL_LOCK	RESERVED					
0x81	129	RESERVED	RESERVED							
0x82-0x83	130-131	CROSSTALK SCALE CH1	CH1_CROSSTALK_SCALE							
0x84-0x85	132-133	CROSSTALK SCALE CH2	CH2_CROSSTALK_SCALE							
0x86	134	ANALOG CONTROL & I2S MONITOR CONFIG	RESERVED		DVDD_SHUNT_ENB	RESERVED	CH2_ANALOG_SWAP	CH1_ANALOG_SWAP	ENABLE_BCK_DETECT	ENABLE_WS_DETECT

0x87	135	ANALOG CONTROL OVERRIDES & CMP/ATR CONTROL	DISABLE_ENCMP	DISABLE_ATR_CH2	DISABLE_ATR_CH1	ENCMP_ALWAYS_ON	SEL_PSD_1V2	ENCMP	PDB_ATR_R	PDB_ATR_L
0x88	136	DRE CONFIG	DRE_FORCE2	DRE_FORCE1	DRE_ENABLE_PEAK_FILTER	DRE_VOLUME_CTRL	DRE_ATR_DISABLE	RESERVED	RESERVED	ENABLE_DRE
0x89-0x8A	137-138	DRE GAIN CH1	DRE_GAIN1							
0x8B-0x8C	139-140	DRE GAIN CH2	DRE_GAIN2							
0x8D-0x90	141-144	DRE ON THRESHOLD	DRE_ON_THRESH							
0x91	145	DRE DECAY RATE	RESERVED			DRE_DECAY_RATE				
0x92	146	MQA CONFIG	MQA_ENABLE	RESERVED						
0x93	147-151	RESERVED	RESERVED							
0xC0	192	SOFT_RESET	RESERVED							AO_SOFT_RESET
0xC1	193	PLL CONFIG1	PLL_CP_PDB	PLL_VCO_PDB	RESERVED	PLL_VCO_BIAS_SEL				
0xC2	194	PLL CONFIG2	PLL_CLK_FB_DIV[19:0]							
0xC3	195	PLL CONFIG2	PLL_CLK_FB_DIV[19:0]							
0xC4	196	PLL CONFIG2	PLL_CLK_IN_DIV[8:0]				PLL_CLK_FB_DIV[19:0]			
0xC5	197	PLL CONFIG2	PLL_BYPASS	PLL_LOW_BW	RESERVED	PLL_CLK_IN_DIV[8:0]				
0xC6	198	PLL CONFIG3	PLL_CLK_OUT_DIV[8:0]							
0xC7	199	PLL CONFIG3	PLL_PFD_DELAY_SEL		RESERVED		PLL_CP_BIAS_SEL			PLL_CLK_OUT_DIV[8:0]
0xC8	200	PLL CONFIG4	RESERVED		PLL_HV_REG_BYPASS	PLL_LV_REG_BYPASS	PLL_HV_REG_PDB	PLL_LV_REG_PDB	PLL_VREF_SEL	
0xC9	201	PLL CONFIG5	RESERVED			SEL_DAC_CLKIN	PD_XTAL	PLL_INPUT_CLK		

Table 1. Register Map

Register Settings

Read-Write Registers

Register 0: SYSTEM REGISTERS

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7:4]	[3:2]	[1]	[0]
Mnemonic	Reserved	CLK_GEAR	RESERVED	SOFT_RESET

Bits	Mnemonic	Description
[7:4]	RESERVED	NA
[3:2]	CLK_GEAR	Configures a clock divider network that can reduce the power consumption of the chip by reducing the clock frequency supplied to both the digital core and analog stages 2'b00: uses MCLK (default) 2'b01: divides MCLK by 2 2'b10: divides MCLK by 4 2'b11: divides MCLK by 8
[1]	RESERVED	NA
[0]	SOFT_RESET	Software configurable hardware reset with the ability to reset the design to its initial power-on configuration 1'b0: normal operation (default) 1'b1: resets the Sabre to its power-on defaults Note: This register will always read as "1'b0" as the power-on default for this register is "1'b0" A reset can be verified by checking the status of other modified registers.

Register 1: INPUT SELECTION

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7:6]	[5:4]	[3:2]	[1:0]
Mnemonic	SERIAL_LENGTH	SERIAL_MODE	AUTO_SELECT	INPUT_SELECT

Bits	Mnemonic	Description
[7:6]	SERIAL_LENGTH	Selects how many DATA_CLK pulses exist per data word. 2'b00: 16-bit data words 2'b01: 24-bit data words 2'b10: 32-bit data words (default) 2'b11: 32-bit data words
[5:4]	SERIAL_MODE	Configures the type of serial data. 2'b00: I2S mode (default) 2'b01: Left-justified mode 2'b11 or 2'b10: reserved
[3:2]	AUTO_SELECT	Allows the Sabre ES9219 to automatically select between either serial (I2S), or DSD input formats. 2'b00: Disable automatic input decoder and instead use the information provided by register 1[1:0] 2'b01: Automatically select between DSD or serial data 2'b10: Reserved 2'b11: Automatically select between DSD or serial (I2S) data (default)
[1:0]	INPUT_SELECT	Configures the ES9219 to use a particular input decoder if auto_select is disabled. 2'b00: Serial (default) 2'b01: reserved 2'b10: Auto Select

		2'b11: DSD Note: Register 1[3:2] must be set to 2'b00 for input_select to function.

Register 2: MIXING AND AUTOMUTE CONFIGURATION

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7:6]	[5]	[4]	[3:2]	[1:0]
Mnemonic	AUTOMUTE_CONFIG	ANALOG_AUTOMUTE	AUTOMUTE_TIMER_FAST	CH2_MIX_SEL	CH1_MIX_SEL

Bits	Mnemonic	Description
[7:6]	AUTOMUTE_CONFIG	Configures the automute state machine, which allows the Sabre to perform different power saving and sound optimizations. 2'b00: Normal operation (default). 2'b01: Perform a mute when an automute condition is asserted. 2'b10: Ramp all channels to ground when an automute condition is asserted. 2'b11: Perform a mute and then ramp all channels to ground when an automute condition is asserted. Note: Ramping DAC outputs to ground can reduce the power consumption of the Sabre in some situations. Note: This process can be sped up by using the automute_time, volume_rate and soft_start_rate registers.
[5]	ANALOG_AUTOMUTE	Allows the analog volume control to be driven to -22dB when an automute condition occurs. 1'b0: Analog volume control is left 'as programmed' when an automute occurs. 1'b1: Analog volume control is pushed to -22dB when an automute occurs (default).
[4]	AUTOMUTE_TIMER_FAST	If disabled, the automute time is multiplied by 8, resulting in a longer delay before an automute event is triggered. 1'b0: Automute time is calculated by the regular formula (see automute_time) multiplied by 8. 1'b1: Automute time is calculated by the regular formula (default).
[3:2]	CH2_MIX_SEL	Selects which data is mapped to DAC 2. 2'b00: ch1 2'b01: ch2 (default) 2'b10-2'b11: reserved
[1:0]	CH1_MIX_SEL	Selects which data is mapped to DAC 1. 2'b00: ch1 (default) 2'b01: ch2 2'b10-2'b11: reserved

Register 3: ANALOG VOLUME CONTROL

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7:5]	[4:0]
Mnemonic	RESERVED	ANALOG_VOLUME_MAIN

Bits	Mnemonic	Description
[7:5]	RESERVED	NA
[4:0]	ANALOG_VOLUME_MAIN	This register controls the analog volume which ranges from +2dB to -22dB in 2dB steps This register is only valid from 5'd0 to 5'd24. 1dB steps can be enabled via analog_1db_en. By default, this register controls both channel 1 and channel 2 analog volume controls. However, it is possible to enable independent analog volume control via analog_use_secondary. Note: This feature is only active when in HiFi mode.

Register 4: AUTOMUTE TIME

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7:0]
Mnemonic	AUTOMUTE_TIME

Bits	Mnemonic	Description
[7:0]	AUTOMUTE_TIME	Configures the amount of time the audio data must remain below the automute_level before an automute condition is flagged. Defaults to 0 which disables automute. Note: DATA_CLK should be provided with a unit of Hz $Time\ in\ Seconds\ = \frac{2096896}{automute_{time} * DATA_{CLK}}$

Register 5: AUTOMUTE LEVEL

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7]	[6:0]
Mnemonic	RESERVED	AUTOMUTE_LEVEL

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6:0]	AUTOMUTE_LEVEL	Configures the threshold which the audio must be below before an automute condition is flagged. The level is measured in decibels (dB) and defaults to -104dB. Note: This register works in tandem with automute_time to create the automute condition.

Register 6: DOP AND VOLUME RAMP RATE

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7:4]	[3]	[2:0]
Mnemonic	RESERVED	DOP_ENABLE	VOLUME_RATE

Bits	Mnemonic	Description
[7:4]	RESERVED	NA
[3]	DOP_ENABLE	Selects whether the DSD over PCM (DoP) logic is enabled. 1'b0: disables the DoP logic (default). 1'b1: enables the DoP logic.
[2:0]	VOLUME_RATE	Selects a volume ramp rate to use when transitioning between different volume levels. The volume ramp rate is measured in decibels per second (dB/s). $Rate\ \left(\frac{dB}{s}\right) = \frac{0.0078125 * FS}{2^{(2-volume_{rate})}}$

Register 7: FILTER SHAPE AND SYSTEM MUTE

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7:5]	[4]	[3]	[2:1]	[0]
Mnemonic	FILTER_SHAPE	RESERVED	BYPASS_OSF	RESERVED	MUTE

Bits	Mnemonic	Description
[7:5]	FILTER_SHAPE	Selects the type of filter to use during the 8x FIR interpolation phase. 3'b110: Hybrid fast roll-off 3'b000: Linear phase fast roll-off filter. All other modes are reserved
[4]	RESERVED	NA
[3]	BYPASS_OSF	Allows the use of an external 8x upsampling filter, bypassing the internal interpolating FIR filter. Overrides the bypass_stage1 option. 1'b0: uses the built-in oversampling filter (default) 1'b1: uses an external upsampling filter, which requires data oversampled by 8x externally
[2:1]	RESERVED	NA
[0]	MUTE	Mutes both channels of the Sabre. 1'b0: normal operation (default) 1'b1: mute both channels

Register 8: GPIO1-2 CONFIGURATION

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7:4]	[3:0]
Mnemonic	GPIO2_CFG	GPIO1_CFG

Bits	Mnemonic	Description
[7:4]	GPIO2_CFG	GPIO 2 configuration bits, value 4'b0 – 4'd15 4'd13: shutdown (default) See GPIO Modes for all configuration options
[3:0]	GPIO1_CFG	GPIO 1 configuration bits, value 4'b0 – 4'd15 4'd13: shutdown (default) See GPIO Modes for all configuration options

Register 9: RESERVED

Register 10: MASTER MODE AND SYNC CONFIGURATION

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7]	[6:5]	[4]	[3:0]
Mnemonic	MASTER_MODE	MASTER_DIV	128fs_MODE	LOCK_SPEED

Bits	Mnemonic	Description
[7]	MASTER_MODE	Enables master mode which causes the Sabre to drive the DATA_CLK and DATA1 signals when in I2S mode Can also be enabled when in DSD mode to enable DATA_CLK only. 1'b0: Disables master mode (default). 1'b1: Enables master mode.
[6:5]	MASTER_DIV	Sets the frame clock (DATA1) and DATA_CLK frequencies when in master mode. This register is used when in normal synchronous operation. 2'b00: DATA_CLK frequency = MCLK/2 (default). 2'b01: DATA_CLK frequency = MCLK/4. 2'b10: DATA_CLK frequency = MCLK/8. 2'b11: DATA_CLK frequency = MCLK/16.
[4]	128fs_MODE	Enables operation of the DAC while in synchronous mode with a 128*fs MCLK. 1'b0: Disables MCLK = 128*fs mode (default). 1'b1: Enables MCLK = 128*fs mode.
[3:0]	LOCK_SPEED	Sets the number of audio samples required before the DPLL and ASRC lock to the incoming signal. More audio samples give a better initial estimate of the MCLK/FS ratio at the expense of a longer locking interval. 4'd0: 16384 FS edges 4'd1: 8192 FS edges 4'd2: 5461 FS edges (default) 4'd3: 4096 FS edges 4'd4: 3276 FS edges 4'd5: 2730 FS edges 4'd6: 2340 FS edges 4'd7: 2048 FS edges 4'd8: 1820 FS edges 4'd9: 1638 FS edges 4'd10: 1489 FS edges 4'd11: 1365 FS edges 4'd12: 1260 FS edges 4'd13: 1170 FS edges 4'd14: 1092 FS edges 4'd15: 1024 FS edges

Register 11: OVERCURRENT PROTECTION

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7]	[6:4]	[3:0]
Mnemonic	OC_SD_EN	OC_SD_GAIN	RESERVED

Bits	Mnemonic	Description
[7]	OC_SD_EN	Enable an automatic detection circuit to mute the DAC (and disable the headphone amplifier) when an overcurrent event is detected. 1'b0: Automatic overcurrent shutdown is disabled (default).

		1'b1: Automatic overcurrent shutdown is enabled and will mute the DAC if an overcurrent event exists for the timeout period (defined by oc_sd_gain).
[6:4]	OC_SD_GAIN	Configures a timeout period before the automatic overcurrent detection circuit triggers a DAC mute. 3'd0: A timeout will never occur, which disables the overcurrent shutdown logic (default). 3'd1-3'd7: Selects the amount of time (MCLK dependent) before an overcurrent flag triggers an automatic shutdown.
[3:0]	RESERVED	NA

Register 12: DPLL BANDWIDTH

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7:4]	[3:0]
Mnemonic	DPLL_BW_SERIAL	DPLL_BW_DSD

Bits	Mnemonic	Description
[7:4]	DPLL_BW_SERIAL	Sets the bandwidth of the DPLL when operating in I2S/SPDIF mode. 4'd0: DPLL Off 4'd1: Lowest Bandwidth 4'd2: 4'd3: 4'd4: 4'd5: (default) 4'd6: 4'd7: 4'd8: 4'd9: 4'd10: 4'd11: 4'd12: 4'd13: 4'd14: 4'd15: Highest Bandwidth
[3:0]	DPLL_BW_DSD	Sets the bandwidth of the DPLL when operating in DSD mode. 4'd0: DPLL Off 4'd1: Lowest Bandwidth 4'd2: 4'd3: 4'd4: 4'd5: 4'd6: 4'd7: 4'd8: 4'd9: 4'd10: (default) 4'd11: 4'd12: 4'd13: 4'd14: 4'd15: Highest Bandwidth

Register 13: THD BYPASS & MONO_MODE

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7]	[6]	[5]	[4]	[3:0]
Mnemonic	RESERVED	BYPASS_THD	RESERVED	MONO_MODE	RESERVED

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6]	BYPASS_THD	Selects whether to disable the THD compensation logic. THD compensation is disabled by default and can be configured to correct for second and third harmonic distortion. 1'b0: Enable THD compensation. 1'b1: Disable THD compensation (default).
[5]	RESERVED	NA
[4]	MONO_MODE	Selects whether mono mode is enabled. Mono mode disables the channel 2 datapath and routes the channel 1 output to both DAC_L and DAC_R. This mode will consume less power as nearly half of the datapath is disabled. 1'b0: Disable mono mode (default). 1'b1: Enable mono mode.
[3:0]	RESERVED	NA

Register 14: SOFT START CONFIGURATION

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7]	[6]	[5]	[4:0]
Mnemonic	SOFT_START	RESERVED	SOFT_START_TYPE	SOFT_START_TIME

Bits	Mnemonic	Description
[7]	SOFT_START	Allows a register override for the soft start/stop ramp circuitry when in dig_override mode. 1'b0: Ramps the output to ground (soft stop) when the dig_override bit is enabled (default). 1'b1: Ramps the output to AVCC/2, which allows the DAC to produce an output. Only functions when the dig_override bit is enabled.
[6]	RESERVED	NA
[5]	SOFT_START_TYPE	Sets whether the soft start ramp is linear or a quadratic function. 1'b0: Uses the standard soft start ramp. 1'b1: Uses a quadratic function for the soft start ramp.
[4:0]	SOFT_START_TIME	Sets the amount of time that it takes to perform a soft start ramp. This time affects both ramp to ground and ramp to AVCC/2. This value is valid from 0 to 20 (inclusive). $time\ (s) = 4096 * \frac{2^{(soft_{start_{time}}+1)}}{MCLK\ (Hz)}$

Register 15-16: VOLUME CONTROL

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[15:8]	[7:0]
Mnemonic	VOLUME_1	VOLUME_2

Bits	Mnemonic	Description
[15:8]	VOLUME_1	Default of 8'd80 (-40dB).

		-0dB to -127.5dB with 0.5dB steps.
[7:0]	VOLUME_2	Default of 8'd80 (-40dB). -0dB to -127.5dB with 0.5dB steps.

Register 17-20: MASTER TRIM

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[31:0]
Mnemonic	MASTER_TRIM

Bits	Mnemonic	Description
[31:0]	MASTER_TRIM	A 32-bit signed value that sets the 0dB level for all volume controls. Defaults to full-scale (32'h7FFFFFFF).

Register 21: GPIO INPUT SELECTION

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7:6]	[5:4]	[3:0]
Mnemonic	GPIO_INPUT_SEL2	GPIO_INPUT_SEL1	RESERVED

Bits	Mnemonic	Description
[7:6]	GPIO_INPUT_SEL2	Selects which input type will be selected when GPIOX = 1'b1 2'd0: Serial data (I2S/LJ) (default). 2'd3: DSD data.
[5:4]	GPIO_INPUT_SEL1	Selects which input type will be selected when GPIOX = 1'b0 2'd0: Serial data (I2S/LJ) (default). 2'd3: DSD data.
[3:0]	RESERVED	NA

Register 22-23: THD COMPENSATION C2

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[15:0]
Mnemonic	THD_COMP_C2

Bits	Mnemonic	Description
[15:0]	THD_COMP_C2	A 16-bit signed coefficient for correcting for the second harmonic distortion.

Register 24-25: THD COMPENSATION C3

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[15:0]
Mnemonic	THD_COMP_C3

Bits	Mnemonic	Description
[15:0]	THD_COMP_C3	A 16-bit signed coefficient for correcting for the third harmonic distortion.

Register 26: CHARGE PUMP SOFT START DELAY

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7:0]
Mnemonic	CP_SS_DELAY

Bits	Mnemonic	Description
[7:0]	CP_SS_DELAY	Sets the delay between when weak mode is enabled and when strong mode is enabled during the fixed charge pump soft start. $$delay(s) = \frac{2048 * cps_{delay} - 2}{f_{MCLK}}$$

Register 27: GENERAL CONFIGURATION

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7]	[6:4]	[3]	[2:0]
Mnemonic	ASRC_EN	RESERVED	CH1_VOLUME	RESERVED

Bits	Mnemonic	Description
[7]	ASRC_EN	Selects whether the ASRC is enabled. 1'b0: ASRC is disabled and the output from the THD compensation block is piped directly into the modulators. 1'b1: The ASRC is used as normal, providing a first order correction on the sample rate converted data (default).
[6:4]	RESERVED	NA
[3]	CH1_VOLUME	Allows channel 2 to share the channel 1 volume control. This allows for perfectly syncing up the two channel gains. 1'b0: Allow independent control of both channel 1 and channel volume controls (default). 1'b1: Use the channel 1 volume control for both channel 1 and channel 2.
[2:0]	RESERVED	NA

Register 28: RESERVED

Register 29: GPIO CONFIGURATION AND AUTO CLOCK GEAR

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7:6]	[5:3]	[2]	[1:0]
Mnemonic	INVERT_GPIO	RESERVED	AUTO_CLK_GEAR	MAX_CLK_GEAR

Bits	Mnemonic	Description
[7:6]	INVERT_GPIO	Allows each GPIO output to be inverted independently. 2'b00: Normal GPIO operation (default). 2'b01: Invert GPIO1 output only. 2'b10: Invert GPIO2 output only. 2'b11: Invert both GPIO outputs.
[5:3]	RESERVED	NA
[2]	AUTO_CLK_GEAR	Allows the digital core to automatically adjust the clock gear setting by counting the number of MCLK pulses per 1fs. If the number of MCLK pulses exceeds a threshold, then the clock gear will decrease (get faster) and if the number of MCLK pulses is below a threshold then the clock gear will increase (get slower). This allows the Sabre to automatically save power when running at lower sample rates. 1'b0: Automatic clock gearing is disabled (default). 1'b1: Automatic clock gearing is enabled. See Register 49-51: Automatic Clock Gearing Thresholds for threshold setting
[1:0]	MAX_CLK_GEAR	Selects the maximum amount of clock gearing that the automatic clock gearing circuitry can implement. This is useful when running at slow clock rates where a clock gear could slow the MCLK down below the I2C programming constraints. 2'b00: Sets MCLK/1 as the maximum clock gearing ratio (effectively disabling the automatic clock gearing) (default). 2'b01: Sets MCLK/2 as the maximum clock gearing ratio. 2'b10: Sets MCLK/4 as the maximum clock gearing ratio. 2'b11: Sets MCLK/8 as the maximum clock gearing ratio.

Register 30-31: CHARGE PUMP CLOCK

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[15:14]	[13:12]	[11:0]
Mnemonic	CP_CLK_SEL	CP_CLK_EN	CP_CLK_DIV

Bits	Mnemonic	Description
[15:14]	CP_CLK_SEL	Selects which clock will be used as the reference clock for the charge pump clock. 2'b00: Use MCLK as the reference clock (default). 2'b01: Use 128*fs as the reference clock. 2'b10: Use 64*fs as the reference clock. 2'b11: Use 1*fs as the reference clock.
[13:12]	CP_CLK_EN	Sets the state of the charge pump clock. 2'b00: Tristate output (default). 2'b01: Tied to GND. 2'b10: Tied to DVDD. 2'b11: cp_clk_sel/ cp_clk_div.
[11:0]	CP_CLK_DIV	Sets the divider ratio for the charge pump clock. F_CLK is the frequency of the clock selected by cp_clk_sel. $f_{cp} = f_{CLK\left(cp_{clk_{div}}+1\right)} * 2$

Register 32: AMPLIFIER CONFIGURATION

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7]	[6:5]	[4:3]	[2]
Mnemonic	AMP_PDB_SS	RESERVED	AMP_MODE_GPIO	RESERVED

Bits	Mnemonic	Description
[7]	AMP_PDB_SS	Powers the amplifier down when the DAC ramps to ground. Useful for powering down the amplifier when using automute 1'b0: Amplifier shutdown is controlled by the amp_mode (default) 1'b1: Shuts down the amplifier when the DAC is ramped to ground.
[7:5]	RESERVED	NA
[4:3]	AMP_MODE_GPIO	Configures the amplifier mode based on inputs from gpio1 and gpio2 3'd0: Core on (default). 3'd1: LowFi. 2'd2: HiFi 1V. 3'd3: HiFi 2V. Note: GPIO1 or GPIO2 must be high and gpio1_cfg or gpio2_cfg must be configured to Amp Mode Select (4'd11) for this to be selected for amp_mode
[2:0]	RESERVED	NA

Register 33: INTERRUPT MASK

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	OCR_SD_MASK	OCL_SD_MASK	OCR_MASK	OCR_MASK	OCL_MASK	OCL_MASK	AUTOMUTE_MASK	LOCK_MASK

Bits	Mnemonic	Description
[7]	OCR_SD_MASK	Masks the overcurrent shutdown bits from flagging an interrupt.
[6]	OCL_SD_MASK	Masks the overcurrent shutdown bits from flagging an interrupt.
[5]	OCR_MASK	Masks the right channel p/n overcurrent bits from flagging an interrupt.
[4]	OCR_MASK	Masks the right channel p/n overcurrent bits from flagging an interrupt.
[3]	OCL_MASK	Masks the left channel p/n overcurrent bits from flagging an interrupt.
[2]	OCL_MASK	Masks the left channel p/n overcurrent bits from flagging an interrupt.
[1]	AUTOMUTE_MASK	Masks the automute bit from flagging an interrupt.
[0]	LOCK_MASK	Masks the lock status bit from flagging an interrupt.

Register 34-37: PROGRAMMABLE NCO

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[31:0]
Mnemonic	NCO_NUM

Bits	Mnemonic	Description
[31:0]	NCO_NUM	An unsigned 32-bit quantity that provides the ratio between MCLK and DATA_CLK. This value can be used to generate arbitrary DATA_CLK frequencies in master mode. A value of 0 disables this operating mode.

		Note: Master mode must still be enabled for the Sabre to drive the DATA_CLK and DATA1 pins. You must also select either serial mode or DSD mode in the input_select register to determine whether DATA_CLK should be driven alone (DSD mode) or both DATA_CLK and DATA1 should be driven (serial mode). 32'd0: disables NCO mode (default). 32'd0: disables NCO mode (default) 32'd?: enables NCO mode

Register 38-39: RESERVED

Register 40: PROGRAMMABLE FIR RAM ADDRESS

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7]	[6:0]
Mnemonic	COEFF_STAGE	COEFF_ADDR

Bits	Mnemonic	Description
[7]	COEFF_STAGE	Selects which stage of the filter to write. 1'b0: selects stage 1 of the oversampling filter (default). 1'b1: selects stage 2 of the oversampling filter.
[6:0]	COEFF_ADDR	Selects the coefficient address when writing custom coefficients for the oversampling filter.

Register 41-43: PROGRAMMABLE FIR RAM DATA

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[23:0]
Mnemonic	PROG_COEFF_DATA

Bits	Mnemonic	Description
[23:0]	PROG_COEFF_DATA	

Register 44: PROGRAMMABLE FIR CONFIGURATION

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7:3]	[2]	[1]	[0]
Mnemonic	RESERVED	EVEN_STAGE2_COEFF	PROG_COEFF_WE	PROG_COEFF_EN

Bits	Mnemonic	Description
[7:3]	RESERVED	NC
[2]	EVEN_STAGE2_COEFF	Selects the symmetry of the stage 2 oversampling filter. 1'b0: Uses a sine symmetric filter (27 coefficients) (default). 1'b1: Uses a cosine symmetric filter (28 coefficients).
[1]	PROG_COEFF_WE	Enables writing to the programmable coefficient RAM. 1'b0: Disables write signal to the coefficient RAM (default). 1'b1: Enables write signal to the coefficient RAM.
[0]	PROG_COEFF_EN	Enables the custom oversampling filter coefficients. 1'b0: Uses a built-in filter selected by filter_shape (default). 1'b1: Uses the coefficients programmed via prog_coeff_data.

Register 45: ANALOG CONTROL OVERRIDE 1

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	ENAUX	AREG_PDB	ENHPA	CPH_ENS	CPH_ENW	APDB	CP_CLKIO_SEL	RESERVED

Bits	Mnemonic	Description
[7]	ENAUX	Sets the state of the output switch when the digital core has taken control of the switch. The switch can be controlled by the digital by setting ENAUX_OE to 1'b1. 1'b0: The switch is disengaged, allowing the DAC and headphone amplifier to drive the output (default). 1'b1: The switch is engaged, allowing the auxiliary input to drive the output. Note: The switch should not be engaged when the headphone amplifier is enabled.
[6]	AREG_PDB	Enables the analog regulator, which uses the reference voltage enabled by the apdb signal. 1'b0: The analog regulator is disabled (default). 1'b1: The analog regulator is enabled. Note: apdb must be set to 1'b1 for the analog regulator to work correctly.
[5]	ENHPA	Enables the pre-amplifier for the headphone amplifier. 1'b0: The pre-amplifier is disabled (default). 1'b1: The pre-amplifier is enabled.
[4]	CPH_ENS	Enables the main charge pump and places it into strong mode. The main charge pump powers the output stage of the headphone amplifier. 1'b0: The main charge pump (strong mode) is disabled (default). 1'b1: The main charge pump (strong mode) is enabled. Note: encp_oe must be set to 1'b1 for the digital core to control the charge pump.
[3]	CPH_ENW	Enables the main charge pump and places it into weak mode. The main charge pump powers the output stage of the headphone amplifier. 1'b0: The main charge pump is disabled (default). 1'b1: The main charge pump is enabled. Note: encp_oe must be set to 1'b1 for the digital core to control the charge pump.
[2]	APDB	Enables the analog reference voltage, which is derived by a bandgap. 1'b0: The analog reference is disabled (default). 1'b1: The analog reference is enabled, which supplies a reference voltage for the analog regulator. This bit must be set prior to enabling the analog regulator (AREG_PDB).
[1]	CP_CLK_SEL_IO	Disables the internal oscillator for the charge pump and uses a digitally generated clock signal instead. The digitally generated clock signal can be configured via register 30-31. 1'b0: Use the internal oscillator as the charge pump clock (default). 1'b1: Use the digitally generated clock as the charge pump clock.
[0]	RESERVED	NA

Register 46: ANALOG CONTROL OVERRIDE 2

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7]	[6:3]	[2]	[1]	[0]
Mnemonic	DIG_OVER_EN	RESERVED	SEL1V	SHTOUTb	SHTINb

Bits	Mnemonic	Description
[7]	DIG_OVER_EN	Allows the digital core to override the amp_mode settings via the contents of register 45, 46 and 47. 1'b0: Uses the amp_mode setting to control the analog sections (default). 1'b1: Allows the digital core to override the amp_mode settings.
[6:3]	RESERVED	NA
[2]	SEL1V	Drops the digital power supply to 1V, which allows the supply to be driven externally. 1'b0: Use the internal digital power supply regulator (default).

		1'b1: Disable the internal digital power supply generator.
[1]	SHTOUTb	Disengages the shunt on the output of the amplifier. 1'b0: Shunt on the output of the amplifier is engaged, allowing for protection against clicks while configuring the amplifier (default). 1'b1: Shunt on the output of the amplifier is disengaged, allowing the amplifier to drive an audio signal.
[0]	SHTINb	Disngages the shunt on the input of the amplifier. 1'b0: Shunt on the input of the amplifier is engaged, allowing for protection against clicks while configuring the amplifier (default). 1'b1: Shunt on the input of the amplifier is disengaged.

Register 47: ANALOG CONTROL OVERRIDE 3

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	ENFCB	ENCP_OE	ENAUX_OE	CPL_ENS	CPL_ENW	SEL3V3_PS	ENSM_PS	SEL3V3_CPH

Bits	Mnemonic	Description
[7]	ENFCB	Enables the fast charge of the analog reference. 1'b0: The analog reference will be charged as quickly as possible (default). 1'b1: The analog reference will be charged at a slower rate.
[6]	ENCP_OE	Allows the digital core to override the charge pump settings. 1'b0: The charge pump settings are controlled via the GPIO2 pin (default). 1'b1: The charge pump settings are controlled via the digital override bits.
[5]	ENAUX_OE	Allows the digital core to override the output switch settings. 1'b0: The output switch is controlled via the GPIO2 pin (default). 1'b1: The output switch is controlled via the enaux register.
[4]	CPL_ENS	Enables the small charge pump and places it into strong mode. The small charge pump powers the pre-amplifier of the headphone amp. 1'b0: The small charge pump (strong mode) is disabled (default). 1'b1: The small charge pump (strong mode) is enabled. Note: encp_oe must be set to 1'b1 for the digital core to control the charge pump.
[3]	CPL_ENW	Enables the small charge pump and places it into weak mode. The small charge pump powers the pre-amplifier of the headphone amp. 1'b0: The small charge pump (weak mode) is disabled (default). 1'b1: The small charge pump (weak mode) is enabled. Note: encp_oe must be set to 1'b1 for the digital core to control the charge pump.
[2]	SEL3V3_PS	Configures the voltage of the positive power supply of the output stage. 1'b0: Uses 1.8V for the positive power supply of the output stage (default). 1'b1: Uses 3.3V for the positive power supply of the output stage.
[1]	ENSM_PS	Allows for a smooth transition between 1.8V and 3.3V on the positive power supply. This bit should be configured to 1'b0 immediately before changing the sel3v3_ps bit. Once sel3v3_ps has been set to the required value, then ensm_ps can be set back to 1'b1 for normal operation. 1'b0: Configure the positive supply for a transition between 1.8V and 3.3V (default). 1'b1: Normal operation.
[0]	SEL3V3_CPH	Configures the voltage of the negative power supply of the output stage. 1'b0: Uses 1.8V for the negative power supply of the output stage (default). 1'b1: Uses 3.3V for the negative power supply of the output stage.

Register 48: ANALOG CONTROL SIGNALS

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7]	[6]	[5:4]	[3]	[2]	[1:0]
Mnemonic	RESERVED	ENHPA_OUT	RESERVED	HPA_HIQ	ENABLE_SEPARATE_THD_COMP	RESERVED

Bits	Mnemonic	Description
[7]	RESERVED	NC
[6]	ENHPA_OUT	Enable the headphone amplifier output stage, active high. 1'b0: Disable the headphone output stage (default). 1'b1: Enable the headphone output stage. Note: To reduce clicks/pops during power sequencing ENHPA_OUT should be delayed at least 100us after issuing the ENHPA signal.
[5:4]	RESERVED	NA
[3]	HPA_HIQ	Selects the quiescent current of the headphone amp. This may be useful for adjusting the crossover distortion between the left and right channel. 1'b0: Low output quiescent current (default). 1'b1: High output quiescent current.
[2]	ENABLE_SEPARATE_THD_COMP	Selects which bank of THD coefficients to use for channel 2 compensation. 1'b0: One set of coefficients (registers 22-25) are used for both channel 1 and channel 2 (default). 1'b1: A separate set of coefficients (registers 53-56) are used for channel 2.
[1:0]	RESERVED	NA

Register 49-51: AUTOMATIC CLOCK GEARING THRESHOLDS

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[23:12]	[11:0]
Mnemonic	CLK_GEAR_MAX_THRESH	CLK_GEAR_MIN_THRESH

Bits	Mnemonic	Description
[23:12]	CLK_GEAR_MAX_THRESH	Selects the maximum number of MCLK/2 pulses per 1fs that must be counted before the clock gear is automatically increased (MCLK is slowed down).
[11:0]	CLK_GEAR_MIN_THRESH	Selects the minimum number of MCLK/2 pulses per 1fs that must be counted before the clock gear is automatically decreased (MCLK is sped up). This value should always be 98 or larger so that the minimum MCLK oversampling factor is achieved.

Register 52: RESERVED

Register 53-54: THD COMPENSATION C2 -CH2

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[15:0]
Mnemonic	THD_COMP_C2_Ch2

Bits	Mnemonic	Description
[15:0]	THD_COMP_C2_Ch2	A 16-bit signed coefficient for correcting for the second harmonic distortion. Used only in the channel 2 THD compensation block when enable_seperate_thd_comp is selected.

Register 55-56: THD COMPENSATION C3 – CH2

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[15:0]
Mnemonic	THD_COMP_C3_Ch2

Bits	Mnemonic	Description
[15:0]	THD_COMP_C3_Ch2	A 16-bit signed coefficient for correcting for the third harmonic distortion. Used only in the channel 2 THD compensation block when enable_seperate_thd_comp is selected.

Register 57-60: RESERVED

Read-Only Registers

Register 64: CHIP STATUS

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7:2]	[1]	[0]
Mnemonic	CHIP_ID	AUTOMUTE _STATUS	LOCK_STATUS

Bits	Mnemonic	Description
[7:2]	CHIP_ID	6'b100011: ES9219
[1]	AUTOMUTE _STATUS	Indicator for when automute has become active. 1'b0: automute condition is inactive 1'b1: automute condition has been flagged and is active
[0]	LOCK_STATUS	Indicator for when DPLL is locked (when in slave mode) or 1'b1 when the ES9219 is the master. 1'b0: DPLL is not locked to the incoming audio sample rate (which could mean that no audio input is present, the lock has not completed, or the ES9219 is unable to lock due to clock jitter or drift) 1'b1: DPLL is locked to the incoming audio sample rate, or the ES9219 is in master or 128*fs mode

Register 65: GPIO Readback

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7]	[6]	[5]	[4]	[3:2]	[1]	[0]
Mnemonic	ocbr_pos	ocbl_pos	ocbr_neg	obcl_neg	clk_gear_rb	gpio2	gpio1

Bits	Mnemonic	Description
[7]	ocbr_pos	Indicates instantaneous positive overcurrent condition on the right channel. 1'b0 No positive overcurrent condition (default) 1'b1 Positive overcurrent condition at the amplifier output
[6]	ocbl_pos	Indicates instantaneous positive overcurrent condition on the left channel. 1'b0 No positive overcurrent condition (default) 1'b1 Positive overcurrent condition at the amplifier output
[5]	ocbr_neg	Indicates instantaneous negative overcurrent condition on the right channel 1'b0 No negative overcurrent condition (default) 1'b1 Negative overcurrent condition at the amplifier output
[4]	obcl_neg	Indicates instantaneous negative overcurrent condition on the right channel 1'b0 No negative overcurrent condition (default) 1'b1 Negative overcurrent condition at the amplifier output
[3:2]	clk_gear_rb	Clock gear readback. This register will reflect changes from both manual and automatic clock gearing 2'b00: indicates CLK = XI(MCLK) (default) 2'b01: indicates CLK = XI(MCLK) / 2 2'b10: indicates CLK = XI(MCLK) / 4 2'b11: indicates CLK = XI(MCLK) / 8
[1]	gpio2	Contains the state of the GPIO2 pin
[0]	gpio1	Contains the state of the GPIO1 pin

Register 66-69: DPLL Number

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[31:0]
Mnemonic	DPLL_NUM

Bits	Mnemonic	Description
[31:0]	DPLL_NUM	Contains the ratio between the CLK and the audio clock rate once the DPLL has acquired lock. This value is latched on reading the LSB, so register 66 must be read first to acquire the latest DPLL value and avoid data tearing. The value is latched on LSB because the DPLL number can change as the I2C transactions are performed. $FSR = \frac{dpll_{num} * CLK}{2^{32}}$

Register 70-71: RESERVED

Register 72: READ INPUT SELECTION AND AUTOMUTE STATUS

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7]	[6]	[5]	[4]	[3:0]
Mnemonic	OCR_SD_MUTE	OCL_SD_MUTE	AMR	AML	INPUT_SELECTION

Bits	Mnemonic	Description
[7]	OCR_SD_MUTE	Indicates when the OCP timeout has expired and an overcurrent event has occurred on the right channel. 1'b0: No overcurrent condition (default) 1'b1: Overcurrent condition detected at amplifier output OUT_R.
[6]	OCL_SD_MUTE	Indicates when the oc_sd_gain OCP timeout has expired and an overcurrent event has occurred on the left channel. 1'b0: No overcurrent condition (default) 1'b1: Overcurrent condition detected at amplifier output OUT_L
[5]	AMR	Automute status of right channel.
[4]	AML	Automute status of left channel.
[3:0]	INPUT_SELECTION	Indicates which input data source is selected. 2'b00: Serial (default) 2'b11: DSD 2'b01/2'b10: Reserved

Register 73-75: READ PROGRAMMABLE FIR RAM DATA

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[23:0]
Mnemonic	PROG_COEFF_OUT

Bits	Mnemonic	Description
[23:0]	PROG_COEFF_OUT	A 24bit signed filter coefficient that has been written to the address defined in PROG_COEFF_ADDR.

Register 76: READ DRE STATUS

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7:6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	RESERVED	CHANNEL_GAIN2	CHANNEL_GAIN1	DRE_SELECT2	DRE_SELECT1	DRE_DETECT2	DRE_DETECT1

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5]	CHANNEL_GAIN2	DRE gain is applied on channel 2
[4]	CHANNEL_GAIN1	DRE gain is applied on channel 1
[3]	DRE_SELECT2	DRE engaged on channel 2
[2]	DRE_SELECT1	DRE engaged on channel 1
[1]	DRE_DETECT2	DRE condition detected on channel 2
[0]	DRE_DETECT1	DRE condition detected on channel 1

Register 77: READ LOCK STATUS

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7:3]	[2]	[1]	[0]
Mnemonic	RESERVED	MQA_LOCKED	PLL_LOCKED	LOCK_STATUS_ASRC

Bits	Mnemonic	Description
[7:3]	RESERVED	NA
[2]	MQA_LOCKED	1'b0: MQA stream is not locked 1'b1: MQA stream is locked
[1]	PLL_LOCKED	1'b0: the analog PLL is unlocked 1'b1: the analog PLL is locked
[0]	LOCK_STATUS_ASRC	1'b0: when in async mode and the asrc is unlocked 1'b1: when in sync mode, or async mode and the asrc is locked

Register 78-85: RESERVED

Extended Read-Write Registers

Register 128: CROSSTALK COMPENSATION CONFIG

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7]	[6]	[5:0]
Mnemonic	BYPASS_CT	ENABLE_PLL_LOCK	RESERVED

Bits	Mnemonic	Description
[7]	BYPASS_CT	Selects whether to disable the crosstalk compensation logic. The crosstalk compensation logic aims to compensate the crosstalk issue in each channel by adding in a scaled signal from the other channel. 1'b0: Enable Crosstalk compensation. 1'b1: Disable Crosstalk compensation (default).
[6]	ENABLE_PLL_LOCK	Enables analog PLL lock indicator, which indicates whether the analog PLL is locked and stable or not. 1'b0: LOCK_STATUS is only controlled by the DPLL lock indicator (default). 1'b1: LOCK_STATUS is controlled by both DPLL lock indicator and analog PLL lock indicator. LOCK_STATUS is set when both DPLL and analog PLL are locked.
[5:0]	RESERVED	NA

Register 129: RESERVED

Register 130-131: CROSSTALK SCALE CH1

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[15:0]
Mnemonic	CH1_CROSSTALK_SCALE

Bits	Mnemonic	Description
[15:0]	CH1_CROSSTALK_SCALE	A 16-bit signed scale factor for Ch1 crosstalk compensation. Ch2 signal is scaled by this factor and added into Ch1. See CrossTalk Compensation

Register 132-133: CROSSTALK SCALE CH2

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[15:0]
Mnemonic	CH2_CROSSTALK_SCALE

Bits	Mnemonic	Description
[15:0]	CH2_CROSSTALK_SCALE	A 16-bit signed scale factor for Ch2 crosstalk compensation. Ch1 signal is scaled by this factor and added into Ch2. See CrossTalk Compensation

Register 134: ANALOG CONTROL & I2S MONITOR CONFIG

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7:6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	RESERVED	DVDD_SHUNT_ENB	RESERVED	CH2_ANALOG_SWAP	CH1_ANALOG_SWAP	ENABLE_BCK_DETECT	ENABLE_WS_DETECT

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5]	DVDD_SHUNT_ENB	Enables the output shunt of the internal DVDD regulator. 1'b0: Shunt disabled 1'b1: Enable output shunt
[4]	RESERVED	NA
[3]	CH2_ANALOG_SWAP	1'b0: Normal polarity of DAC2 and DAC2B (default). 1'b1: Swaps DAC2 and DAC2B (180 degree phase shift).
[2]	CH1_ANALOG_SWAP	1'b0: Normal polarity of DAC1 and DAC1B (default). 1'b1: Swaps DAC1 and DAC1B (180 degree phase shift).
[1]	ENABLE_BCK_DETECT	1'b0: Disable BCK monitor (default). 1'b1: Enable BCK monitor (assume normal MCLK exists). If BCK is lost (no pulses after 1024 MCLK clock cycles), set LOCK_STATUS to 0 until normal BCK resumes.
[0]	ENABLE_WS_DETECT	1'b0: Disable WS monitor (default). 1'b1: Enable WS monitor (assume normal BCK exists). If WS is lost (no pulses after 256 BCK clock cycles), set LOCK_STATUS to 0 until normal WS resumes.

Register 135: ANALOG CONTROL OVERRIDES & CMP/ATR CONTROL

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	RESERVED	DISABLE_ATR_CH2	DISABLE_ATR_CH1	RESERVED	SEL_PSD_1V2	ENCMP	PDB_ATR_R	PDB_ATR_L

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6]	DISABLE_ATR_CH2	1'b0: Ch2 Analog THD removal (ATR) is enabled (default). 1'b1: Ch2 Analog THD removal (ATR) is disabled.
[5]	DISABLE_ATR_CH1	1'b0: Ch1 Analog THD removal (ATR) is enabled (default). 1'b1: Ch1 Analog THD removal (ATR) is disabled.
[4]	RESERVED	NA
[3]	SEL_PSD_1V2	Over current protection setting. 1'b0: set HPA output stage supply to 1.8V (default) 1'b1: set HPA output stage supply to 3.3V
[2]	ENCMP	Jack detection comparator enable 1'b0: Power down the comparator. (default) 1'b1: Comparator is enabled.
[1]	PDB_ATR_R	Analog THD Removal (ATR) power down control in the HPA for right channel. 1'b0: Power down the ATR. (default) 1'b1: ATR is enabled.
[0]	PDB_ATR_L	Analog THD Removal (ATR) power down control in the HPA for left channel. 1'b0: Power down the ATR. (default) 1'b1: ATR is enabled.

Register 136: DRE CONFIG

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	DRE_FORCE2	DRE_FORCE1	DRE_ENABLE_PEAK_FILTER	DRE_VOLUME_CTRL	DRE_ATR_DISABLE	RESERVED	RESERVED	ENABLE_DRE

Bits	Mnemonic	Description
[7]	DRE_FORCE2	Force Channel 2 into DRE mode even if zero cross has not occurred. 1'b1: Enable 1'b0: Disable
[6]	DRE_FORCE1	Force Channel 1 into DRE mode even if zero cross has not occurred. 1'b1: Enable 1'b0: Disable
[5]	DRE_ENABLE_PEAK_FILTER	Low Pass filter the input to the DRE peak detector, for use with DSD inputs. 1'b1: Enable 1'b0: Disable
[4]	DRE_VOLUME_CTRL	When enabled, the analog volume control and digital gain will be adjusted to optimize output performance in DRE mode. 1'b0: The analog volume control will not be affected by the DRE (default). 1'b1: The analog volume control will be set to its minimum value when the DRE mode is engaged. A digital gain will be applied in this mode of operation to ensure the total gain of the DAC is nominal at 0dB.
[3]	DRE_ATR_DISABLE	1'b0: Analog THD removal (ATR) will not be disabled by the DRE block (default). 1'b1: Disable analog THD removal (ATR) when DRE is engaged.
[2]	RESERVED	NA
[1]	RESERVED	NA
[0]	ENABLE_DRE	Selects whether the DRE module is enabled. 1'b0: DRE module is disabled and DRE mode will never be engaged (default). 1'b1: DRE module is enabled and DRE mode will be engaged if the stored value in the peak detector falls below the specified DRE threshold.

Register 137-138: DRE GAIN CH1

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[15:0]
Mnemonic	DRE_GAIN1

Bits	Mnemonic	Description
[15:0]	DRE_GAIN1	Sets the DRE gain for channel 1. Shifting right 1 bit corresponds to -6dB Valid from 16'h7FFF (30dB) to 16'h03FF (0dB)

Register 139-140: DRE GAIN CH2

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[15:0]
Mnemonic	DRE_GAIN2

Bits	Mnemonic	Description
[15:0]	DRE_GAIN2	Sets the DRE gain for channel 2. Shift right 1 bit corresponds to -6dB Valid from 16'h7FFF (30dB) to 16'h03FF (0dB)

Register 141-142: DRE ON THRESHOLD

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[15:0]
Mnemonic	DRE_ON_THRESH

Bits	Mnemonic	Description
[15:0]	DRE_ON_THRESH	DRE on threshold. Shift right 1 bit corresponds to -6dB 16'hFFFF corresponds to -24dB

Register 143-144: DRE OFF THRESHOLD

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[15:0]
Mnemonic	DRE_OFF_THRESH

Bits	Mnemonic	Description
[15:0]	DRE_OFF_THRESH	DRE off threshold. Shifting right 1 bit corresponds to -6dB 16'hFFFF corresponds to -24dB

Register 145: DRE DECAY RATE

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7:5]	[4:0]
Mnemonic	RESERVED	DRE_DECAY_RATE

Bits	Mnemonic	Description
[7:5]	RESERVED	NA
[4:0]	DRE_DECAY_RATE	Sets the speed at which the stored value of the DRE peak detector will decay when the input signal is below the stored value. 4'd31: slowest decay 4'd0: instant decay

Register 146: MQA CONFIG

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7]	[6:0]
Mnemonic	MQA_ENABLE	RESERVED

Bits	Mnemonic	Description
[7]	MQA_ENABLE	This allows the Sabre to decode MQA streams 1'b0: disabled (default) 1'b1: enabled
[6:0]	RESERVED	NA

Register 147-151: RESERVED

Synchronous I2C Interface (0x94 or 0x96)

These registers are write only.

Register 192: SOFT_RESET

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7:1]	[0]
Mnemonic	RESERVED	AO_SOFT_RESET

Bits	Mnemonic	Description
[7:1]	RESERVED	NA
[0]	AO_SOFT_RESET	Software configurable hardware reset with the ability to reset the design to its initial power-on configuration. 1'b0: normal operation (default) 1'b1: resets the Sabre to its power-on defaults Note: This register will always read as "1'b0" as the power-on default for this register is "1'b0". A reset can be verified by checking the status of other modified registers.

Register 193: PLL CONFIG1

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7]	[6]	[5]	[4:0]
Mnemonic	PLL_CP_PDB	PLL_VCO_PDB	RESERVED	PLL_VCO_BIAS_SEL

Bits	Mnemonic	Description
[7]	PLL_CP_PDB	Enables/disables the PLL charge pump. 1'b0: Disabled (default) 1'b0: Enabled Enable **BEFORE** PLL_VCO_PDB
[6]	PLL_VCO_PDB	Enables/disables the PLL voltage-controlled oscillator (VCO). 1'b0: Disabled (default) 1'b0: Enabled Enable **AFTER** PLL_CP_PDB
[5]	RESERVED	NA
[4:0]	PLL_VCO_BIAS_SEL	Sets the VCO output and op-amp bias currents. VCO V2I Op-Amp Bias Current: 5'b000xx: Vtune/45kΩ (default) 5'b001xx: Vtune/40kΩ 5'b010xx: Vtune/35kΩ 5'b011xx: Vtune/30kΩ 5'b100xx: Vtune/80kΩ 5'b101xx: Vtune/70kΩ 5'b110xx: Vtune/60kΩ 5'b111xx: Vtune/50kΩ VCO V2I Output Current: 5'bxxx00: 2.0uA (default) 5'bxxx01: 1.5uA 5'bxxx10: 1.0uA 5'bxxx11: 0.5uA

Register 194-197: PLL CONFIG2

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[31]	[30]	[29]	[28:20]	[19:0]
Mnemonic	PLL_BYPASS	PLL_LOW_BW	RESERVED	PLL_CLK_IN_DIV[8:0]	PLL_CLK_FB_DIV[19:0]

Bits	Mnemonic	Description
[31]	PLL_BYPASS	PLL bypass mode
[30]	PLL_LOW_BW	PLL low bandwidth mode
[29]	RESERVED	NA
[28:20]	PLL_CLK_IN_DIV[8:0]	Sets the PLL clock input divider: 9'd0: Reserved 9'd1: Divide by 1 9'd2: Divide by 2 9'dn: Divide by n
[19:0]	PLL_CLK_FB_DIV[19:0]	Sets the PLL clock feedback divider: 20'd0: Reserved 20'dn: Divide by 2^21/n

Register 198-199: PLL CONFIG3

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[15:14]	[13:12]	[11:9]	[8:0]
Mnemonic	PLL_PFD_DELAY_SEL	RESERVED	PLL_CP_BIAS_SEL	PLL_CLK_OUT_DIV[8:0]

Bits	Mnemonic	Description
[15:14]	PLL_PFD_DELAY_SEL	Indicates the PFD minimum pulse. 2'b00: 8.5ns (default) 2'b01: 5.5ns 2'b10: 3.5ns 2'b11: 1.5ns
[13:12]	RESERVED	NA
[11:9]	PLL_CP_BIAS_SEL	Sets the PLL charge pump bias current. 3'b000: 1uA (default) 3'b001: 2uA 3'b010: 3uA 3'b011: 4uA 3'b111: 8uA
[8:0]	PLL_CLK_OUT_DIV[8:0]	Indicates the PLL clock output divider. 9'd0: Reserved 9'dn: Divide by n

Register 200: PLL CONFIG4

I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

Bits	[7:6]	[5]	[4]	[3]	[2]	[1:0]
Mnemonic	RESERVED	PLL_HV_REG_BYPASS	PLL_LV_REG_BYPASS	PLL_HV_REG_PDB	PLL_LV_REG_PDB	PLL_VREF_SEL

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5]	PLL_HV_REG_BYPASS	High Voltage PLL Regulators Bypass. 1'b0: Normal operating mode (default). 1'b1: HV regulator in bypass mode; the output of HV regulator = AVDD
[4]	PLL_LV_REG_BYPASS	Low Voltage PLL Regulator Bypass 1'b0: Normal operating mode (default). 1'b1: LV regulator in bypass mode; the output of LV regulator = DVCC
[3]	PLL_HV_REG_PDB	High Voltage PLL regulator power down. 1'b0: PLL HV regulator is powered down. Output is shunted to ground (default). 1'b1: Normal operating mode
[2]	PLL_LV_REG_PDB	Low Voltage PLL regulator power down 1'b0: PLL LV regulator is powered down. Output is shunted to ground (default). 1'b1: Normal operating mode
[1:0]	PLL_VREF_SEL	PLL HV regulator output voltage select. 2'b00: 2V (default) 2'b01: 1.9V 2'b10: 1.8V 2'b11: 1.7V

Register 201: PLL CONFIG5

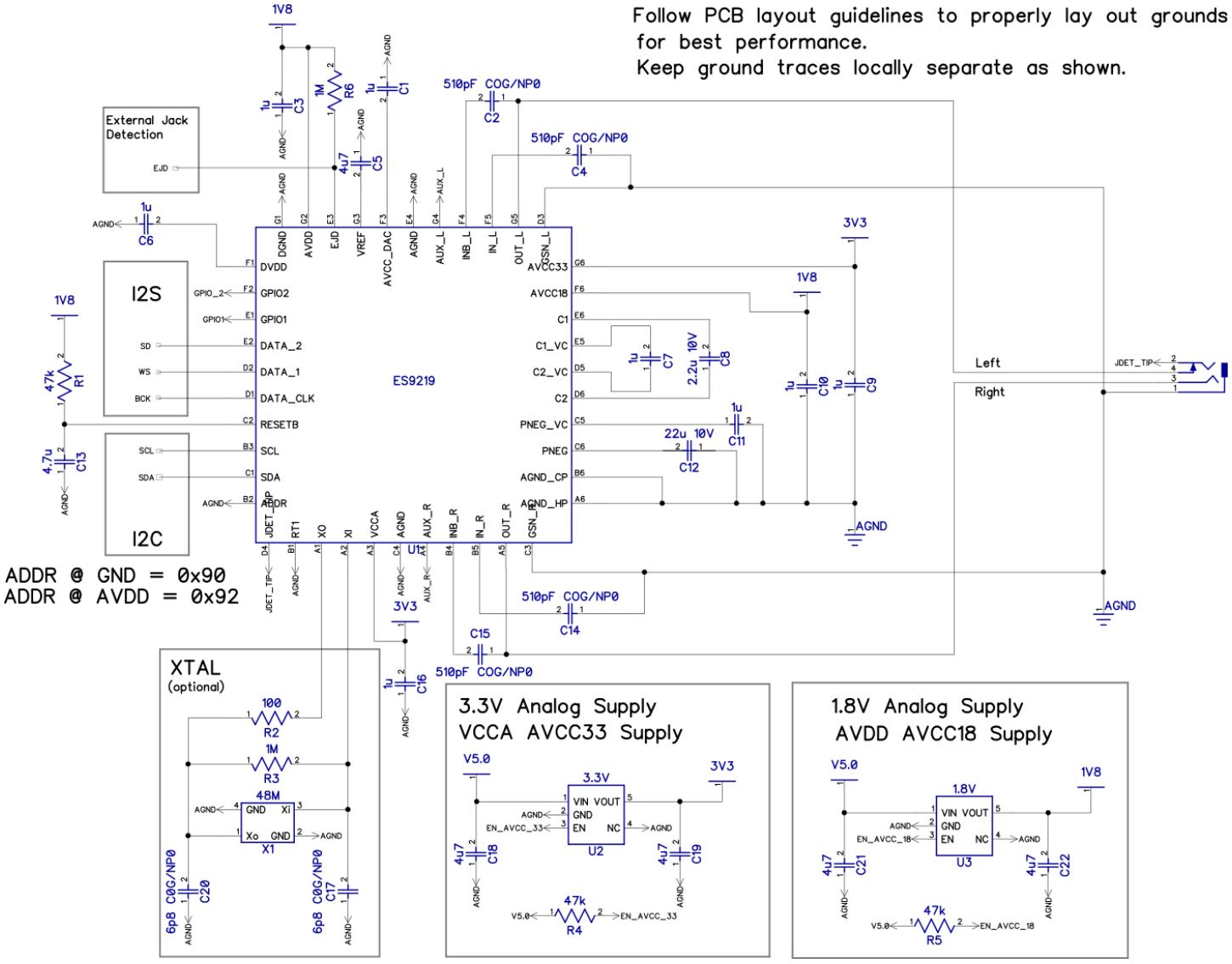
I2C Slave Access:
I2S Sync Slave Access:

Clock Domain:

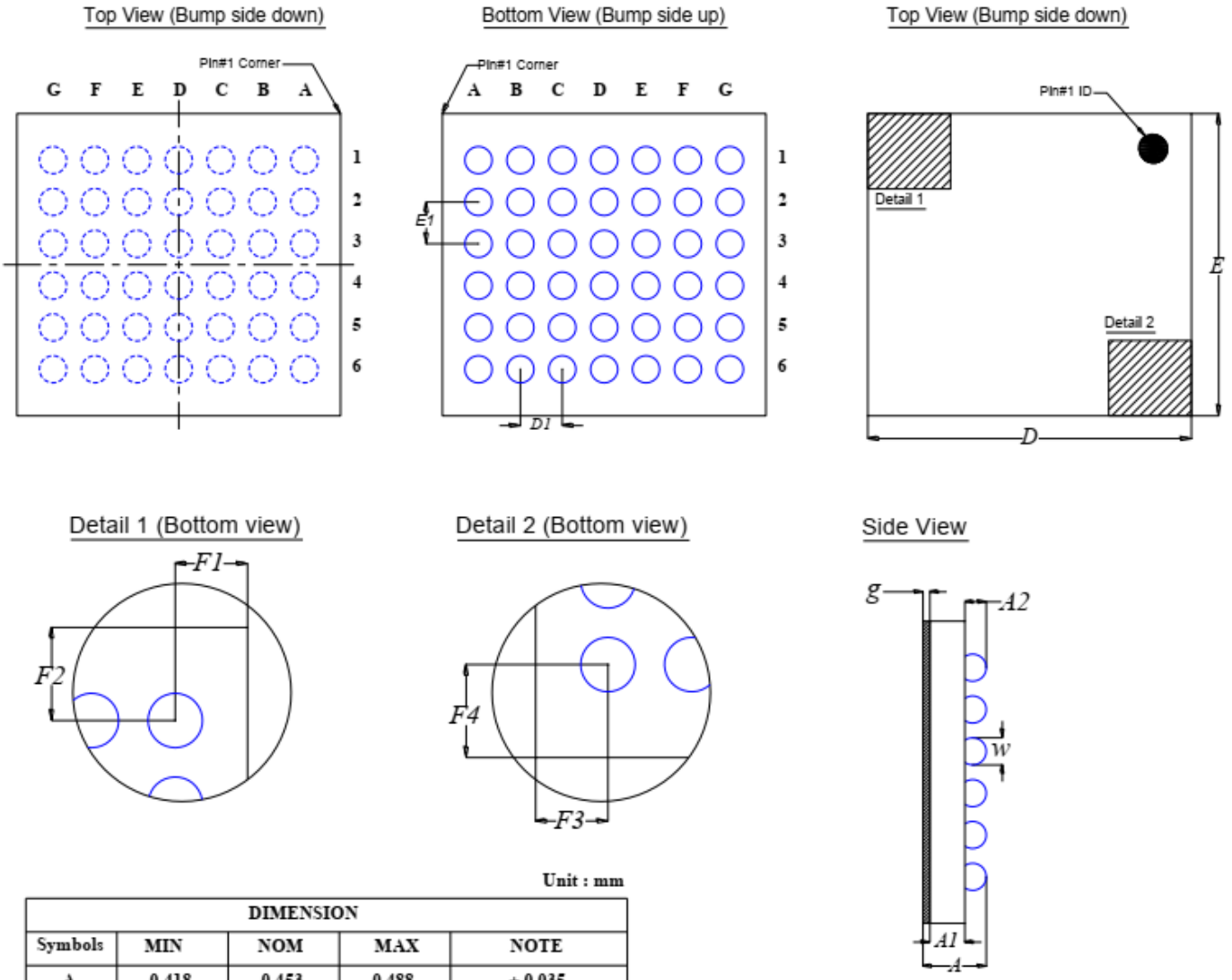
Bits	[7:5]	[4]	[3]	[2:0]
Mnemonic	RESERVED	SEL_DAC_CLKIN	PD_XTAL	PLL_INPUT_CLK

Bits	Mnemonic	Description
[7:5]	RESERVED	NA
[4]	SEL_DAC_CLKIN	Select which clock is used for the DAC 1'b0: XTAL is selected as the DAC clock (default). 1'b1: PLL clock is selected as the DAC clock.
[3]	PD_XTAL	XTAL circuit power down 1'b0: Normal operating mode (default). 1'b1: XTAL circuit is powered down.
[2:0]	PLL_INPUT_CLK	Selects the input clock to the PLL 3'b:000 No clock is selected 3'b:001 MCLK is selected as PLL input clock 3'b:010 BCK is selected as PLL input clock 3'b:100 XTAL is selected as PLL input clock All other values are invalid, not allowed See System Clock XI/MCLK & BCK for more information

ES9219C Reference Schematic



42-Ball CSP Mechanical Dimensions



Unit : mm

DIMENSION				
Symbols	MIN	NOM	MAX	NOTE
A	0.418	0.453	0.488	± 0.035
A 1	0.208	0.223	0.238	± 0.015
A 2	0.188	0.205	0.222	± 0.017
D		3.090		± 0.030
E		2.890		± 0.030
D1		0.400		
E1		0.400		
F1		0.345		Ball center to die edge
F2		0.445		Ball center to die edge
F3		0.345		Ball center to die edge
F4		0.445		Ball center to die edge
g	0.022	0.025	0.028	± 0.003
w	0.234	0.260	0.286	± 0.026

Remark

. POD designed base on die size with sealing size
. Die stepping pitch : 3.120mm * 2.920mm
. Sawing street width : 0.080mm * 0.080mm

Comment

. POD be designed base on LBS design rule

Figure 13. ES9219C Mechanical Dimensions

42-Ball CSP Top View Marking

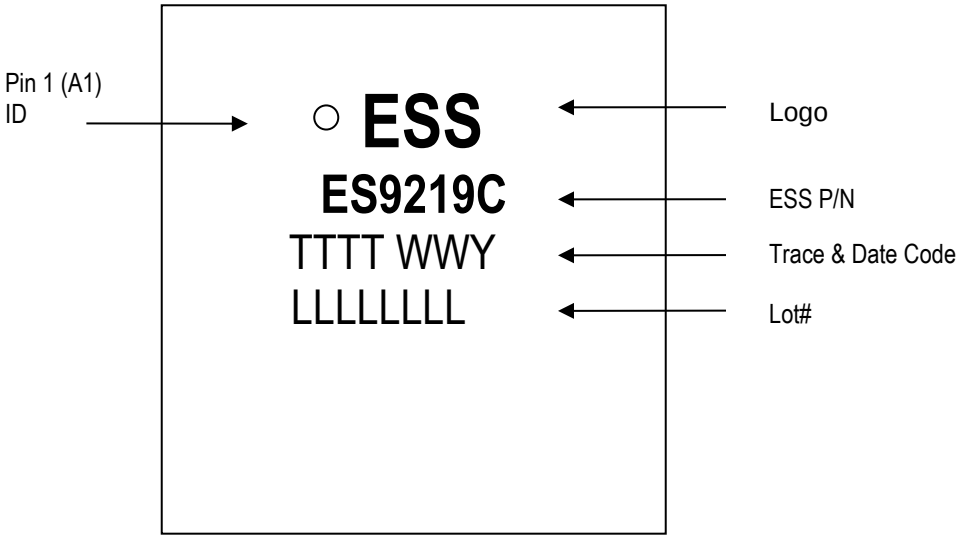


Figure 14. ES9219C Marking

Marking is subject to change. This drawing is not to scale.

Reflow Process Considerations

Temperature Controlled

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor to consider.
The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size (RPC-2 Pb-Free Process – Classification Temperatures (Tc)). This narrows the process window for lead-free soldering to 10°C to 20°C.
The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used. Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits (Table RPC-2).

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

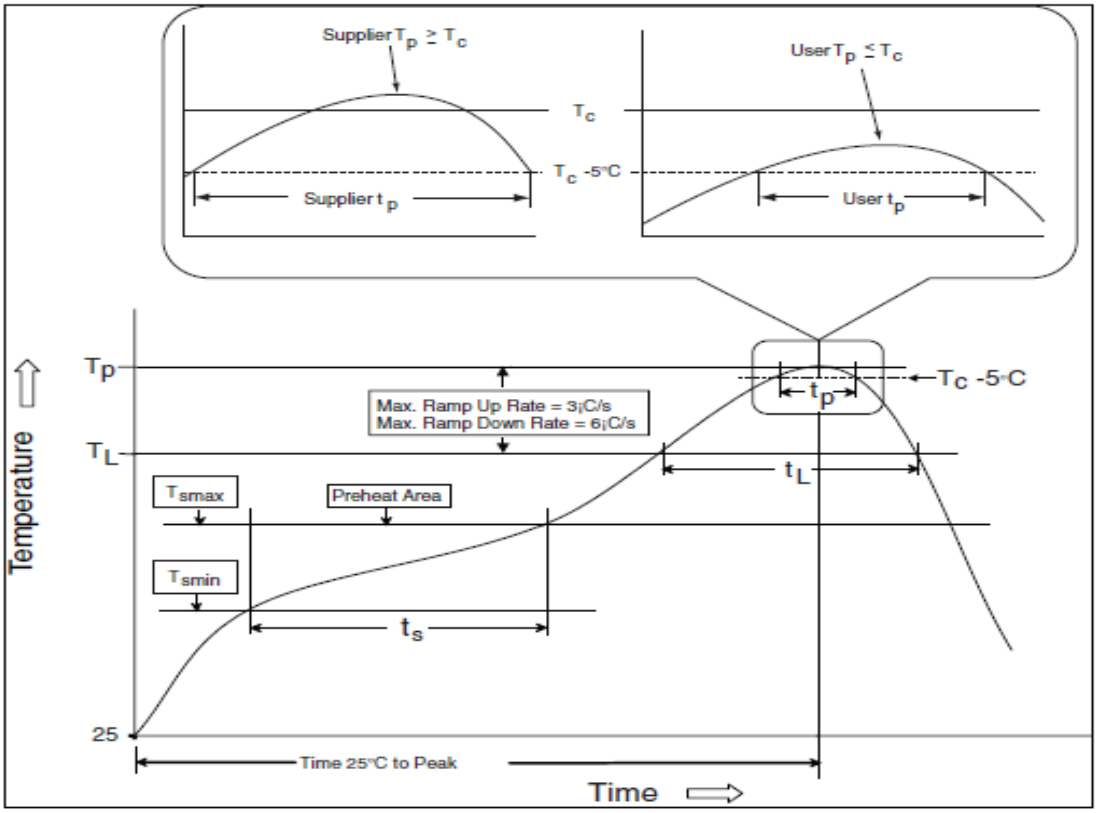


Figure 16. IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)

Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time bake the board according to the moisture sensitivity label instructions.

Manual

Allowed up to 2 times with maximum temperature of 350°C no longer than 3 seconds.

RPC-1 Classification reflow profile

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150°C 200°C 60-120 seconds
Ramp-up rate (TL to Tp)	3°C / second maximum
Liquidous temperature (TL) Time (tL) maintained above TL	217°C 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the classification temp in Table RPC-2. For suppliers Tp must equal or exceed the Classification temp in Table RPC-2.
Time (tp)* within 5°C of the specified classification temperature (Tc), see Figure	30* seconds
Ramp-down rate (Tp to TL)	6°C / second maximum
Time 25°C to peak temperature	8 minutes maximum
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.	

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp shall be within ±2°C of the live-bug Tp and still meet the Tc requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures, refer to JEP140 for recommended thermocouple use.

Note 2: Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.

For example, if Tc is 260°C and time tp is 30 seconds, this means the following for the supplier and the user.
For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.
For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

Note 3: All components in the test load shall meet the classification profile requirements.

RPC-2 Pb-Free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm3, <350	Volume mm3, 350 to 2000	Volume mm3, >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Note 1: At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).
Note 2: Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.
Note 3: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

Ordering Information

Part Number	Description	Package
ES9219C	SABRE 32-bit Low Power Stereo DAC with Headphone Amplifier, Analog Volume Control, APLL, and Output Switch, on-chip feedback resistors	42-ball CSP

Revision History

Current Version 1.0.4

Rev.	Date	Notes
1.0	Dec 5, 2019	Initial release
1.0.1	Dec 9, 2019	Changed name of Register 45 [1] “CP_CLKIO_SEL” due to naming conflict
1.0.2	Dec 10, 2019	Changed PLL_CP_BIAS_SEL, Register 199 Values Changed Registers 45-47 Naming for clarity Modified instructions for Register 193 [7] & [6]
1.0.3	Jan 7, 2020	Updated reference schematic & typical application diagram with pullup on EJD pin
1.0.4	Mar 3, 2020	Changed Built in Filter type to Hybrid fast roll-off (Reg 7) & Settings

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