Analog Reinvented

ES9033

32-bit High-Performance 2-Channel DAC with Line Drivers

Product Datasheet

The Sabre ES9033 High Performance Audio DAC is a 32-Bit, 2-channel audio DAC that brings professional, digital audio quality to the consumer home entertainment market.

Using ESS' patented HyperStream ® II architecture, the Sabre ES9033 delivers studio quality audio with 122dB DNR (w / DRE) and -108dB THD+N.

With the integrated line drivers, the ES9033 reduces BOM costs by eliminating the need for external amplifier to produce a line level 2Vrms output.

The Sabre ES9033 flexible input architecture accepts up to serial 32-bit serial PCM data to 768kHz sample rate & DSD512.

The Sabre DAC sets a new standard for high-quality audio performance in a cost-effective, compact, easy to use form factor for today's most demanding digital audio applications.

FEATURE	DESCRIPTION
+122dB DNR (w/ DRE) per channel -108dB THD+N per channel	Unprecedented dynamic range and ultra-low distortion
High Sample Rates	Support for up to PCM 768kHz & DSD512
2-channel DAC + Line Driver in 28-QFN	Reduced footprint and simplifies board layout
Multiple formats available	PCM, TDM, DSD, DoP input data formats.
Customizable filter characteristics	8 preset filters
I²C, SPI, and Hardware interface control	Configured by microcontroller or other I²C /SPI source, or pins through Hardware Mode
Integrated low noise DAC reference regulators	Reduced BOM cost, PCB area and improved DNR.
Low Pin Count Standardized Packaging	5mm x 5mm, 28 pin QFN
2Vrms Integrated Line Driver	Reduces BOM costs w/o required external op-amp required for line driver levels
Analog PLL (APLL)	Simplifies clocking requirements and reduces PCB size and BOM cost

Applications

- Media Streamer Applications
- Gaming Motherboards
- Audio Receivers
- Professional audio Equipment
- Active Speakers

Table of Contents

List of Figures

List of Tables

Functional Block Diagram

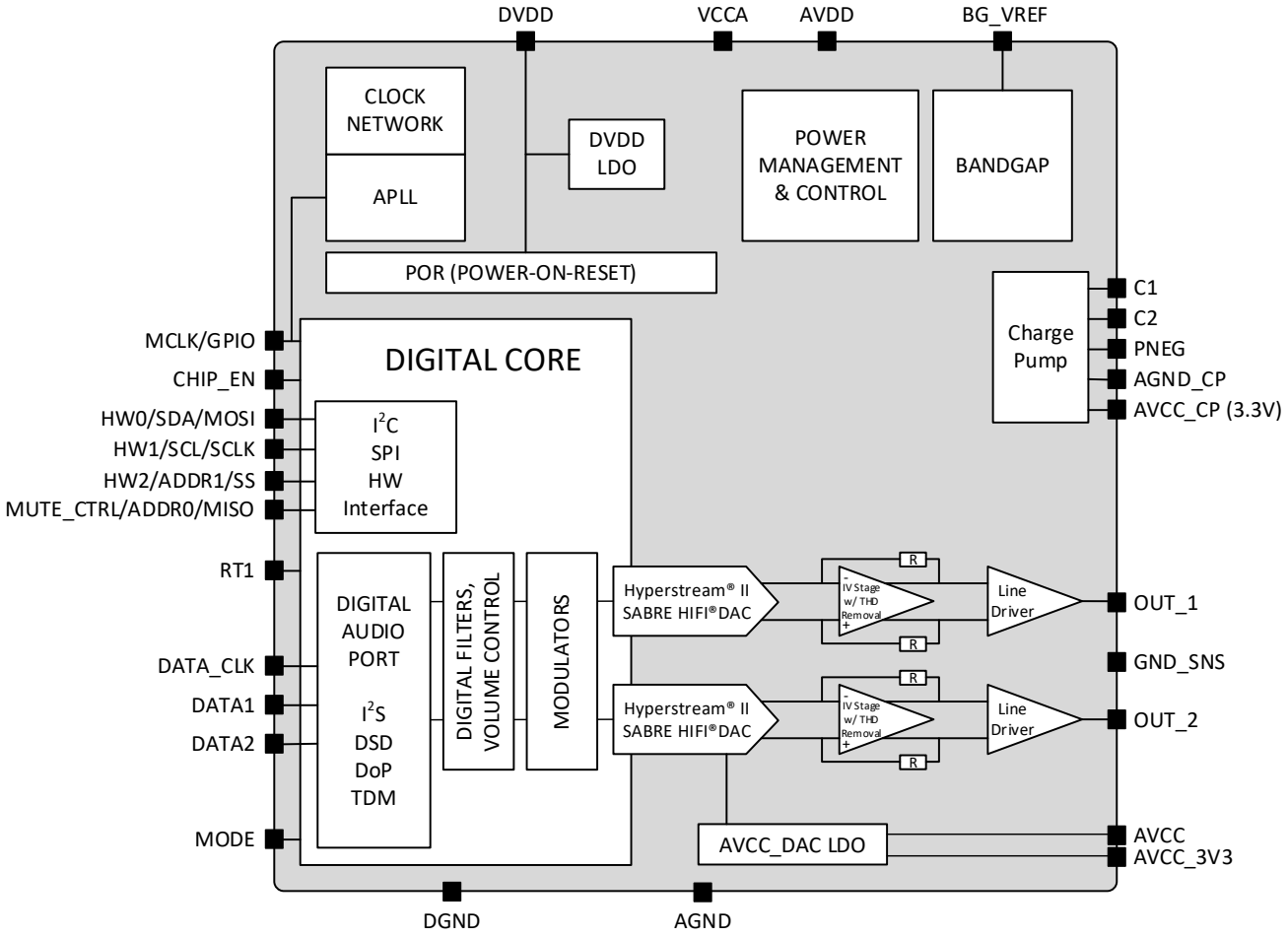


Figure 1 - ES9033 Block Diagram

ES9033Q Package

28 QFN Pinout

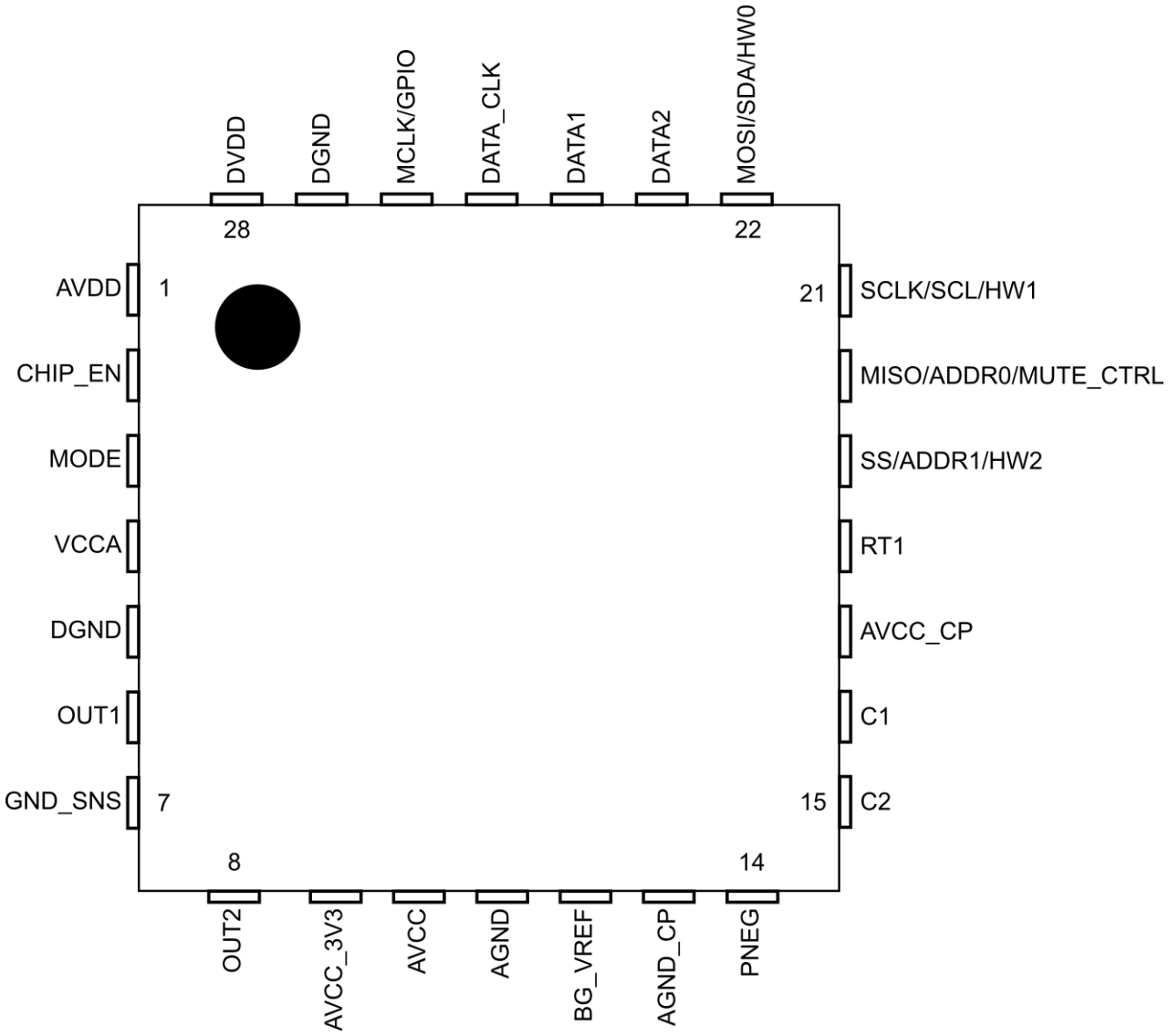


Figure 2 - 28 QFN Pinout

28 QFN Pin Descriptions

Pin	Name	Pin Type	Reset State	Pin Description
1	AVDD	Power	Power	3.3V I/O supply
2	CHIP_EN	I/O	HiZ	Active-high chip enable.
3	MODE	I/O	HiZ	Control for SPI/I²C/HW modes
4	VCCA	Power	Power	Analog Supply
5	DGND	Ground	Ground	Digital ground
6	OUT1	AO	Ground	Output channel 1
7	GND_SNS	AI	Ground	Line driver load ground voltage sense
8	OUT2	AO	Ground	Output channel 2
9	AVCC_3V3	Power	Power	Analog Regulator 3.3V Supply
10	AVCC	A I/O	P/D	Analog Regulator Output, internally supplied
11	AGND	Ground	Ground	Analog ground
12	BG_VREF	A I/O	P/D	Bandgap Voltage reference
13	AGND_CP	Ground	Ground	Analog Ground for charge pump
14	PNEG	A I/O	P/D	Integrated charge pump output. Line driver negative supply.
15	C2	-	-	Line driver negative flying capacitor
16	C1	-	-	Line driver positive flying capacitor
17	AVCC_CP	Power	Power	Analog Supply for charge Pump
18	RT1	I	HiZ	Reserved. Must be connected to DGND for normal operation.
19	SS	I/O	HiZ	SPI Slave Select pin, controlled by MODE
	ADDR1			I²C Address 1 pin, controlled by MODE
	HW2			Hardware 2 interface pin, controlled by MODE
20	MISO	I/O	HiZ	SPI Main In Sub Out pin, controlled by MODE
	ADDR0			I²C Address 0 pin, controlled by MODE
	MUTE_CTRL			Hardware Mute Control pin, controlled by MODE
21	SCLK	I/O	HiZ	SPI Serial Clock pin, controlled by MODE
	SCL			I²C Serial Clock pin, controlled by MODE
	HW1			Hardware 1 interface pin, controlled by MODE
22	MOSI	I/O	HiZ	SPI Main Out Sub In pin, controlled by MODE
	SDA			I²C Serial Data pin, controlled by MODE

	HW0			Hardware 0 interface pin, controlled by MODE
23	DATA2	I/O	HiZ	Serial DATA2
24	DATA1	I/O	HiZ	Serial DATA1
25	DATA_CLK	I	HiZ	Serial data clock
26	MCLK/GPIO	I/O	HiZ	MCLK input
	GPIO			General I/O
27	DGND	Ground	Ground	Digital core ground
28	DVDD	A I/O	P/D	Digital core supply, internally supplied
29	Package PAD[1]	-	-	Not electrically connected, used for heat dissipation

Table 1 - 28 QFN Pin Descriptions

[1] Pin 29 is the package pad. See 28 QFN package dimensions for sizing.

Configuration Modes

Hardware Mode

The ES9033 has 31 pre-configured modes that can be set with external pin configuration. These modes configure the DAC for different input serial data rates and set the DAC muting.

These modes are set with pins:

- MODE (Pin 3)
- HW0 (Pin 22)
- HW1 (Pin 21)
- HW2 (Pin 19)
- MUTE_CTRL (Pin 20)

Each hardware mode pin has 4 states:

- 0 - Pin directly connected to GND
- 1 - Pin directly connected to AVDD
- Pull 0 - Pin pulled to GND through 47kΩ resistor
- Pull 1 - Pin pulled to AVDD through 47kΩ resistor

Design Information

Each hardware mode pin can be configured with either a pull-up or pull-down resistor. Therefore, it is important that the pin is configured to allow for the desired hardware modes. Some guidelines include the following:

- By placing a pull-down resistor on the MODE pin, the device is limited to hardware modes with DRE. Alternatively, if a pull-up resistor is placed on the MODE pin, the device is limited to non-DRE modes.
- By placing a pull-down resistor on the HW2 pin, the device can no longer access modes 8-11 or modes 24-27. Alternatively, if a pull-up resistor is placed on the HW2 pin, the device can no longer use LJ Master mode with an external MCLK.
- The HW0 and HW1 pins never require a pull up or pull-down resistor.

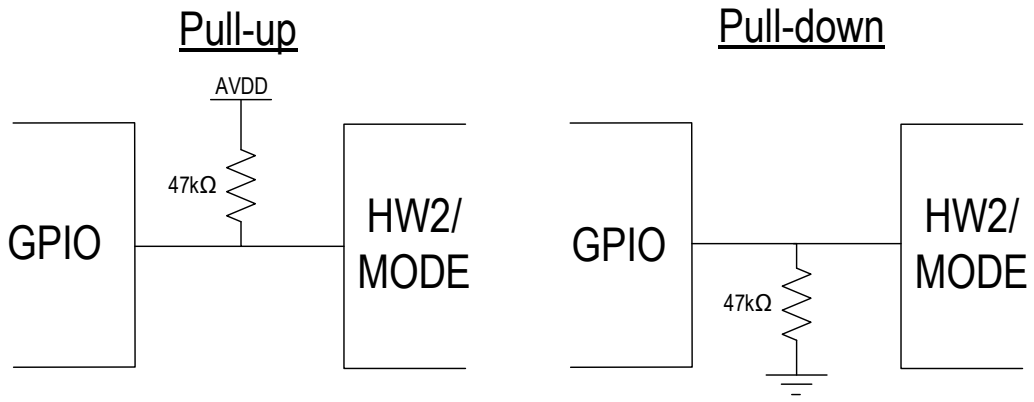


Figure 3 - Hardware Mode Pin Configuration

Hardware Mode Pin Configurations

HW #	Description	DRE	FS [kHz]	BCK [MHz]	MCLK [MHz]	MODE	HW2	HW1	HW0
0	I²S Master	Yes	MCLK / 128	MCLK / 2	5 < MCLK < 50	Pull 0	0	0	0
1	I²S Master	Yes	MCLK / 256	MCLK / 4	5 < MCLK < 50	Pull 0	0	0	1
2	I²S Master	Yes	MCLK / 512	MCLK / 8	5 < MCLK < 50	Pull 0	0	1	0
3	I²S Master	Yes	MCLK / 1024	MCLK / 16	5 < MCLK < 50	Pull 0	0	1	1
4	LJ Master	Yes	MCLK / 128	MCLK / 2	5 < MCLK < 50	Pull 0	Pull 0	0	0
5	LJ Master	Yes	MCLK / 256	MCLK / 4	5 < MCLK < 50	Pull 0	Pull 0	0	1
6	LJ Master	Yes	MCLK / 512	MCLK / 8	5 < MCLK < 50	Pull 0	Pull 0	1	0
7	LJ Master	Yes	MCLK / 1024	MCLK / 16	5 < MCLK < 50	Pull 0	Pull 0	1	1
8	I²S Slave (Ext MCLK)	Yes	Auto (8 < FS < 384)	64FS	128FS < MCLK < 50	Pull 0	Pull 1	0	0
9	I²S Slave (PLL from BCK)	Yes	48	3.072	49.152 from PLL	Pull 0	Pull 1	0	1
10	I²S Slave (PLL from BCK)	Yes	96	6.144	49.152 from PLL	Pull 0	Pull 1	1	0
11	I²S Slave (PLL from BCK)	Yes	192	12.288	49.152 from PLL	Pull 0	Pull 1	1	1
12	DSD Slave (EXT MCLK)	Yes	64FS	64FS	5 < MCLK < 50	Pull 0	1	0	0
13	LJ Slave (PLL from BCK)	Yes	48	3.072	49.152 from PLL	Pull 0	1	0	1
14	LJ Slave (PLL from BCK)	Yes	96	6.144	49.152 from PLL	Pull 0	1	1	0
15	LJ Slave (PLL from BCK)	Yes	192	12.288	49.152 from PLL	Pull 0	1	1	1
16	I²S Master	No	MCLK / 128	MCLK / 2	5 < MCLK < 50	Pull 1	0	0	0
17	I²S Master	No	MCLK / 256	MCLK / 4	5 < MCLK < 50	Pull 1	0	0	1
18	I²S Master	No	MCLK / 512	MCLK / 8	5 < MCLK < 50	Pull 1	0	1	0
19	I²S Master	No	MCLK / 1024	MCLK / 16	5 < MCLK < 50	Pull 1	0	1	1
20	LJ Master	No	MCLK / 128	MCLK / 2	5 < MCLK < 50	Pull 1	Pull 0	0	0
21	LJ Master	No	MCLK / 256	MCLK / 4	5 < MCLK < 50	Pull 1	Pull 0	0	1
22	LJ Master	No	MCLK / 512	MCLK / 8	5 < MCLK < 50	Pull 1	Pull 0	1	0
23	LJ Master	No	MCLK / 1024	MCLK / 16	5 < MCLK < 50	Pull 1	Pull 0	1	1
24	I²S Slave (Ext MCLK)	No	Auto (8 < FS < 384)	64FS	128FS < MCLK < 50	Pull 1	Pull 1	0	0
25	I²S Slave (PLL from BCK)	No	48	3.072	49.152 from PLL	Pull 1	Pull 1	0	1
26	I²S Slave (PLL from BCK)	No	96	6.144	49.152 from PLL	Pull 1	Pull 1	1	0
27	I²S Slave (PLL from BCK)	No	192	12.288	49.152 from PLL	Pull 1	Pull 1	1	1

28	DSD Slave (EXT MCLK)	No	64FS	64FS	5 < MCLK < 50	Pull 1	1	0	0
29	LJ Slave (PLL from BCK)	No	48	3.072	49.152 from PLL	Pull 1	1	0	1
30	LJ Slave (PLL from BCK)	No	96	6.144	49.152 from PLL	Pull 1	1	1	0
31	LJ Slave (PLL from BCK)	No	192	12.288	49.152 from PLL	Pull 1	1	1	1

Table 2 - Hardware Pin Configurations

Muting

MUTE_CTRL (Pin 20) is used to control the muting of the output and enabling of the Automute feature while in Hardware Mode:

- 0 - Output Muted
- 1 - Output Unmuted
- Pull 0 - Output Muted
- Pull 1 - Output Unmuted, Automute Enabled

Recommended Hardware Mode Setup Sequence

The hardware mode setup sequence is shown below with all hardware pins being defined before and after CHIP_EN is asserted.

Note: It is recommended that MUTE_CTRL is set low until the HW mode and CHIP_EN is finalized, then asserted last.

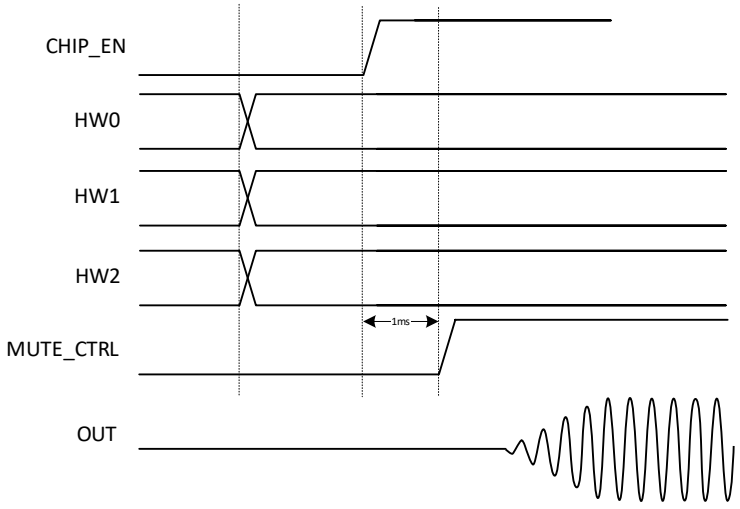


Figure 4 - Hardware Mode Startup Sequence

Software Mode

To configure the ES9033 registers manually over I²C or SPI, connect the following pins:

I²C

- Mode (Pin 3) - GND
- Connect per I²C standard
  - SDA (Pin 22)
  - SCL (Pin 21)
  - ADDR0 (Pin 20)
  - ADDR1 (Pin 19)

I²C Address	ADDR1	ADDR0
0x90	GND	GND
0x92	GND	AVDD
0x94	AVDD	GND
0x96	AVDD	AVDD

Table 3 - I²C Addresses

SPI

- Mode (Pin 3) - AVDD
- Connect per SPI standard
  - SCLK (Pin 21)
  - SS (Pin 19)
  - MOSI (Pin 22)
  - MISO (Pin 20)

SPI Command	First Byte
Write	3
Read	1

Table 4 - SPI Commands

Digital Features

Digital Signal Path

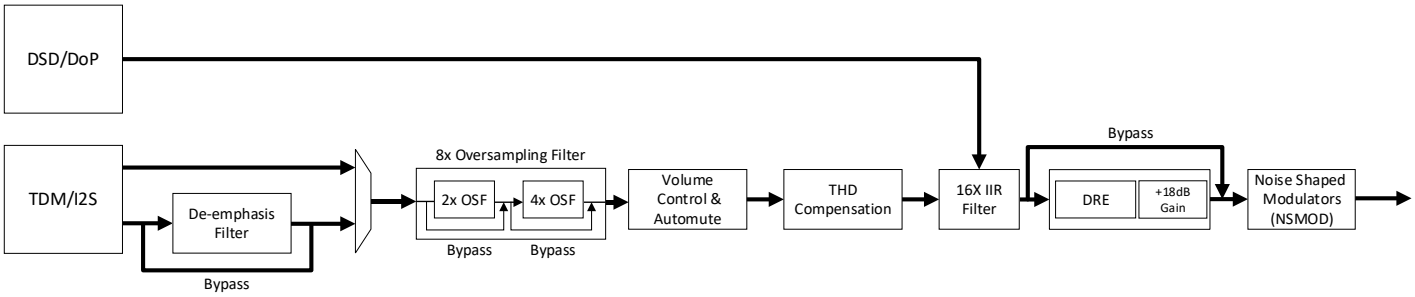


Table 5 - Digital Signal Path

GPIO Configuration

GPIO_CONFIG	Function	I/O Direction
0	1'b0	Output
1	1'b0	Output
2	1'b1	Output
3	128 FS Block	Output
4	Interrupt Output	Output
5	Mute all channel	Input
6	System mode Control	Input
7	Reserved	Output
8	CLK_VALID flag	Output
9	PWM1	Output
10	PWM2	Output
11	PWM3	Output
12	Volume min	Output
13	Automute status	Output
14	Soft Ramp finished	Output
15	1'b0	Output

Figure 5 - Standard GPIO Functions

For GPIO_CONFIG 12, 13, 14:

Register 26[0] GPIO_SEL selects which channel determines the flag status when the corresponding bits in Register 25[7:2] are set to 1'b0. See register listing for more details.

Soft Mute

When Mute is asserted the digital signal level will be smoothly ramped to minimum. When Mute is de-asserted the digital signal level will ramp back up to the level set by the volume control register. Asserting Mute will not change the value stored in the volume control register. The volume ramp rate is controlled through registers 48-50.

Mute can be engaged through either the automute feature or by setting the mute bits for any individual channel through Register 51: MUTE CTRL.

Automute

Automute is disabled by default and is triggered when any one of the following conditions are met:

Mode	Detection Condition	Time
PCM	The absolute value of the signal is lower than automute_level for longer than the calculated time.	$\frac{2^{25}}{automute\_time * CLK\_IDAC * 2^{64fs\_mode}}$
DSD	In one byte of data there is either all 1's, all 0's or an equal amount both for longer than the calculated time.	
DoP		

Table 6 - Automute Conditions

The automute feature is enabled for both channels individually through the AUTOMUTE_EN_CH2 and AUTOMUTE_EN_CH1 bits (Register 64-63[12:11]). The thresholds that trigger and disable automute can be configured through registers 65-66 AUTOMUTE LEVEL and 67-68 AUTOMUTE OFF LEVEL.

Note: Register 63-64[14] AUTOMUTE_WAIT_ON_DRE must be set to 1'b0 if not using DRE as the automute will be waiting for the DRE to trigger indefinitely.

Volume Control

This volume control is intended for use during audio playback. Each channel can be digitally attenuated from 0dB to –127.5dB. When a new volume level is set, the attenuation circuit will ramp softly to the new level.

Volume of both channels is individually configured through Registers 46-47.

By default, channel volumes are updated as soon as the volume registers are written. However, the volume control can be configured to only change once Register 51[5] RUN_VOLUME is set. This feature can be enabled or disabled by setting Register 51[7] FORCE_VOLUME.

Both output channels have an independent volume control. The attenuation for the channels can be independent or synchronized in pairs by setting Register 51[6] DAC_USE_MONO_VOLUME.

THD Compensation

THD Compensation can be used to minimize distortion from external PCB components and layout through the generation of inverse second and third harmonic components matching the target system distortion profile.

The coefficients are stored in Registers 56 – 61.

THD Configuration Registers

- Register 56-55: THD COMP C2 CH1
- Register 58-57: THD COMP C3 CH1
- Register 60-59: THD COMP C2 CH2
- Register 62-61: THD COMP C3 CH2

Dynamic Range Enhancement (DRE)

The DRE controller is composed of a peak detector with a programmable rate. If the input audio stream peak level decays below the DRE ON THRESHOLD value, the controller will attenuate the analog gain by 16.33 dB, while simultaneously increasing the digital gain by the value of DRE GAIN CHx. DRE will remain engaged until the input audio stream peak level rises above the DRE OFF THRESHOLD value. The rate at which the peak level decay is determined by DRE DECAY RATE.

Control over various device functions is given to the DRE peak filter through the DRE_ATR_EN and DRE_GAIN_EN registers. Once configured, the DRE_ZC_CHx registers may be configured to enable DRE on the desired channels.

The DRE peak filter is disabled by default and is enabled by setting the PEAK_FILTER bit.

DRE Configuration Registers:

- Register 73[7:6]: DRE_ZC_CHx
- Register 73[1]: DRE_ATR_EN
- Register 73[0]: DRE_GAIN_EN
- Register 74-75: DRE GAIN CH1
- Register 76-77: DRE GAIN CH2
- Register 78-79: DRE ON THRESHOLD
- Register 80-81: DRE OFF THRESHOLD
- Register 82[7]: DRE_ZC_LEVEL
- Register 82[5]: MIN_PEAK
- Register 82[4:0]: DRE_DECAY_RATE
- Register 52[5]: PEAK_FILTER

Audio Input Formats

For configuring TDM and I²S, use Register 36-40.

TDM (Time Division Multiplexing)

The ES9033 supports up to 32 channel TMD modes.

I²S

Data is latched on the positive edge of BCK.

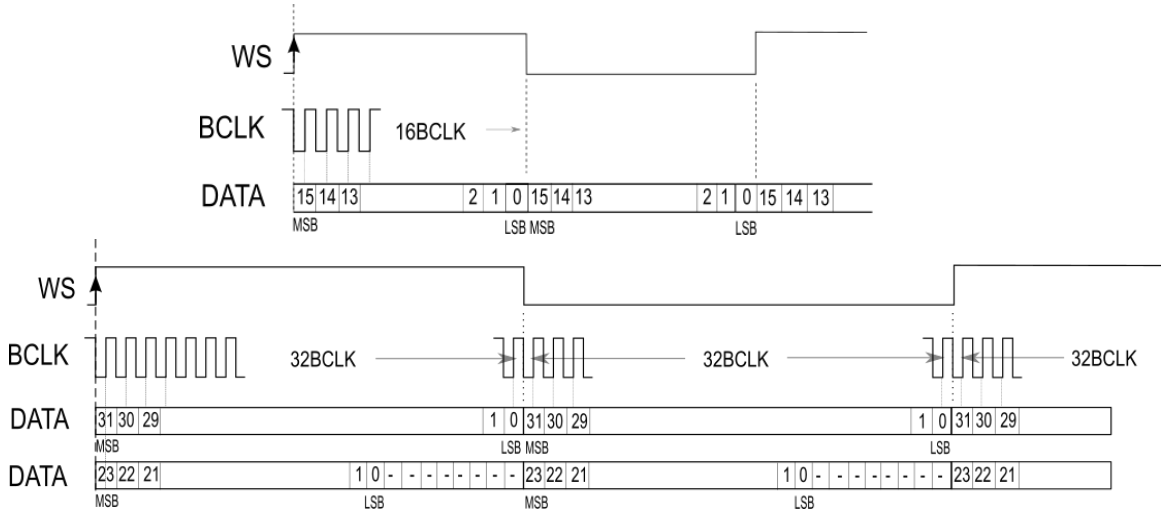


Figure 6 - LJ Input Format for 16 and 32bit Word Depths

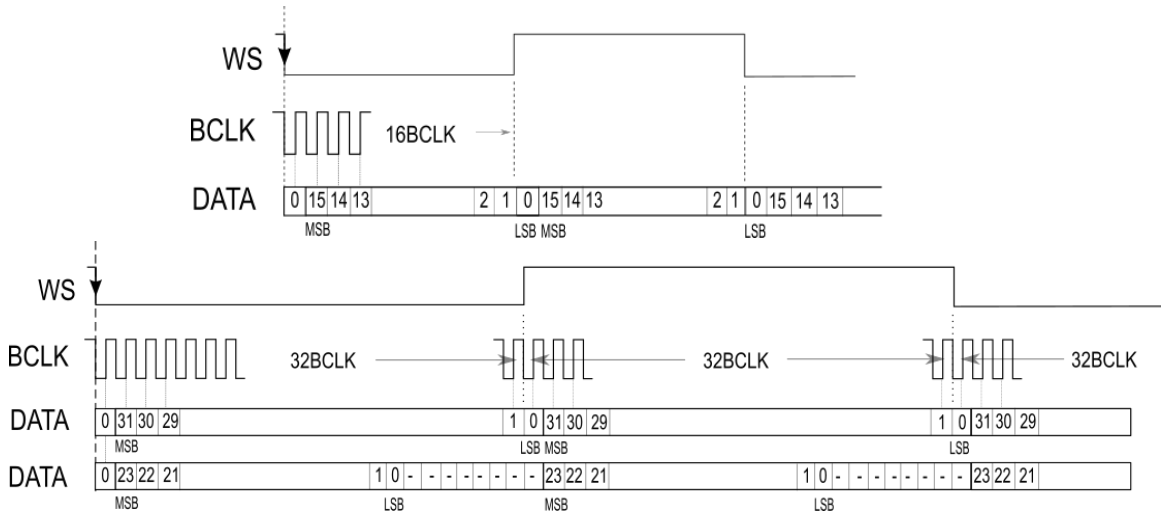


Figure 7 - I²S Input Format for 16bit and 32bit Work Depths

DSD

Data is latched on the positive edge of DCLK.

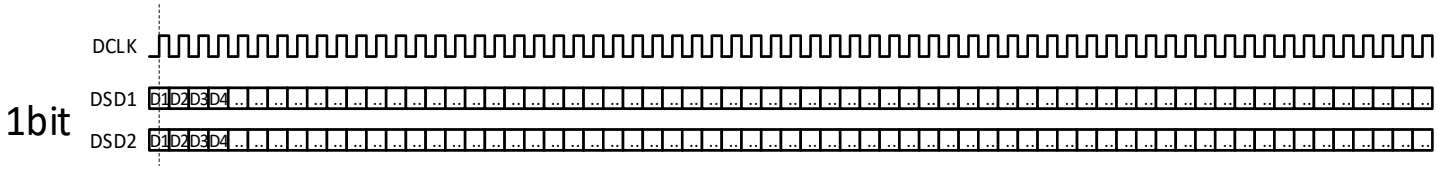


Figure 8 - DSD Format

Note: Automatic sample rate detection is not available for DSD inputs.

Clock Distribution

The ES9033 includes features for selecting and manipulating the input clock source.

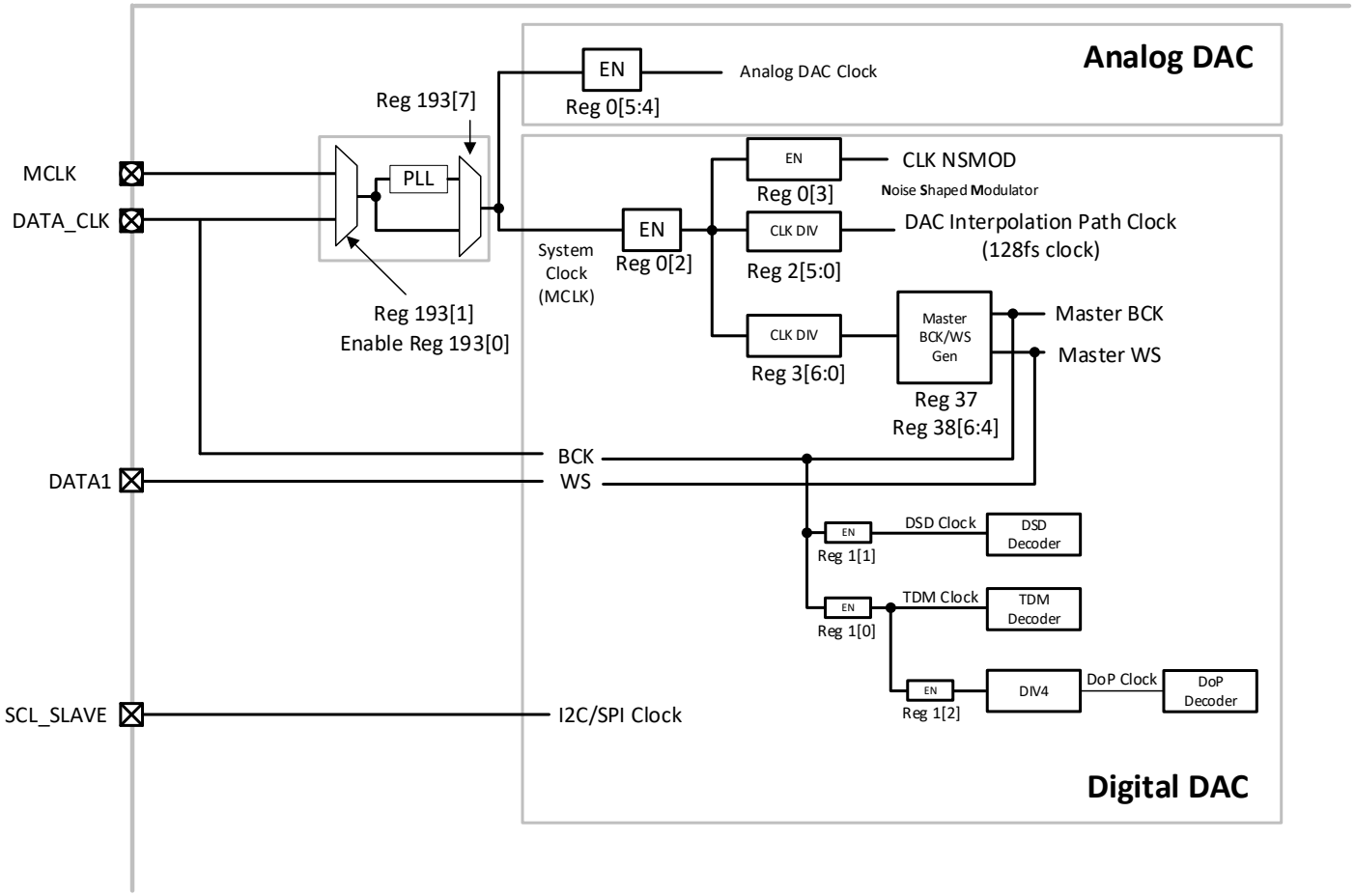


Figure 9 - ES9033 Clock Distribution

The following list shows the various clocks of the ES9033 and the associated registers for configuration.

Analog DAC Clock

- Reg 0[5:4] ENABLE_ANALOG_DAC_CHx
- Reg 193[7] PLL_BYP
- Reg 193[1] SEL_PLL_IN
- Reg 193[0] EN_PLL_CLKIN

NSMOD Clock

The NSMOD clock is utilized by the HyperStream® II Noise Shaped Modulators

- Reg 0[3] ENABLE_NSMOD
- Reg 0[2] ENABLE_DAC
- Reg 193[7] PLL_BYP
- Reg 193[1] SEL_PLL_IN
- Reg 193[0] EN_PLL_CLKIN

DAC Interpolation Path Clock

- Reg 2[5:0] SELECT_IDAC_NUM
- Reg 0[2] ENABLE_DAC
- Reg 193[7] PLL_BYP
- Reg 193[1] SEL_PLL_IN
- Reg 193[0] EN_PLL_CLKIN

Master BCK and WS

- Reg 37 MASTER MODE CONFIG
- Reg 38[6:4] MASTER_WS_SCALE
- Reg 3[6:0] SELECT_MENC_NUM
- Reg 0[2] ENABLE_DAC
- Reg 193[7] PLL_BYP
- Reg 193[1] SEL_PLL_IN
- Reg 193[0] EN_PLL_CLKIN

DSD Clock

- Reg 1[1] ENABLE_DSD_DECODE

TDM Clock

- Reg 1[0] ENABLE_TDM_DECODE

DoP Clock

- Reg 1[2] ENABLE_DOP_DECODE
- Reg 1[0] ENABLE_TDM_DECODE

I²S Master Clock Rate Configurations

WS can be scaled down further than shown via Register 38 [6:4] MASTER_WS_SCALE

MCLK Frequency	WS [kHz]	BCK [MHz]	Bits	Channels	Register 2 [5:0] SELECT_IDAC_NUM		Register 3 [6:0] SELECT_MENC_NUM		Register 40 [4:0] TDM_BIT_WIDTH	
					Value	Divider	Value	Divider	Value	Length
22.579 MHz	44.1	2.822	32	2	5'd3	4	7'd3	4	1'b0	32
	88.2	5.645		2	5'd1	2	7'd1	2	1'b0	32
	176.4	11.290		2	5'd0	1	7'd0	1	1'b0	32
	44.1	1.411	16	2	5'd3	4	7'd3	4	1'b1	16
	88.2	2.822		2	5'd1	2	7'd1	2	1'b1	16
	176.4	5.645		2	5'd0	1	7'd0	1	1'b1	16
24.576 MHz	48	3.072	32	2	5'd3	4	7'd3	4	1'b0	32
	96	6.144		2	5'd1	2	7'd1	2	1'b0	32
	192	12.288		2	5'd0	1	7'd0	1	1'b0	32
	48	1.536	16	2	5'd3	4	7'd3	4	1'b1	16
	96	3.072		2	5'd1	2	7'd1	2	1'b1	16
	192	6.144		2	5'd0	1	7'd0	1	1'b1	16
45.158 MHz	44.1	2.822	32	2	5'd7	8	7'd7	8	1'b0	32
	88.2	5.645		2	5'd3	4	7'd3	4	1'b0	32
	176.4	11.290		2	5'd1	2	7'd1	2	1'b0	32
	352.8	22.579		2	5'd0	1	7'd0	1	1'b0	32
	44.1	1.411	16	2	5'd7	8	7'd7	8	1'b1	16
	88.2	2.822		2	5'd3	4	7'd3	4	1'b1	16
	176.4	5.645		2	5'd1	2	7'd1	2	1'b1	16
	352.8	11.290		2	5'd0	1	7'd0	1	1'b1	16
49.152 MHz	48	3.072	32	2	5'd7	8	7'd7	8	1'b0	32
	96	6.144		2	5'd3	4	7'd3	4	1'b0	32
	192	12.288		2	5'd1	2	7'd1	2	1'b0	32
	384	24.576		2	5'd0	1	7'd0	1	1'b0	32
	48	1.536	16	2	5'd7	8	7'd7	8	1'b1	16
	96	3.072		2	5'd3	4	7'd3	4	1'b1	16
	192	6.144		2	5'd1	2	7'd1	2	1'b1	16
	384	12.288		2	5'd0	1	7'd0	1	1'b1	16

Table 7 - I²S Master Clock Rate Configurations

I²S Slave Clock Rate Configurations

MCLK Frequency	WS [kHz]	BCK	Channels	Register 2 [5:0] SELECT_IDAC_NUM		Register 0 [6] ENABLE_2X_MODE	
				Value	Divider	Value	Multiplier
22.579 MHz	44.1	64FS	2	7'd3	4	1'b0	1x
	88.2		2	7'd1	2	1'b0	1x
	176.4		2	7'd0	1	1'b0	1x
	352.8		2	7'd0	1	1'b1	2x
24.576 MHz	48		2	7'd3	4	1'b0	1x
	96		2	7'd1	2	1'b0	1x
	192		2	7'd0	1	1'b0	1x
	384		2	7'd0	1	1'b1	2x
45.158 MHz	44.1		2	7'd7	8	1'b0	1x
	88.2		2	7'd3	4	1'b0	1x
	176.4		2	7'd1	2	1'b0	1x
	352.8		2	7'd0	1	1'b0	1x
49.152 MHz	48		2	7'd7	8	1'b0	1x
	96		2	7'd3	4	1'b0	1x
	192		2	7'd1	2	1'b0	1x
	384		2	7'd0	1	1'b0	1x

Table 8 - I²S Slave Clock Rate Configurations

TDM Master Clock Rate Configurations

MCLK Frequency	WS [kHz]	BCK [MHz]	TDM Mode	Chan-nels	Register 2 [5:0] SELECT_ IDAC_NUM		Register 3 [6:0] SELECT_ MENC_NUM		Register 38 [6:4] MASTER_ WS_SCALE		Register 37 [6] MASTER_ BCK_DIV1	
					Value	Div.	Value	Div.	Value	Div.	Value	Div.
22.579 MHz	44.1	5.645	TDM 128	4	5'd3	4	7'd1	2	3'd1	2	1'b0	2
	88.2	11.290		4	5'd1	2	7'd0	1	3'd1	2	1'b0	2
	176.4	22.579		4	5'd0	1	7'd0	1	3'd0	1	1'b1	1
	44.1	11.290	TDM 256	8	5'd3	4	7'd0	1	3'd2	4	1'b0	2
	88.2	22.579		8	5'd1	2	7'd0	1	3'd1	2	1'b1	1
	44.1	22.579	TDM 512	16	5'd3	4	7'd0	1	3'd2	4	1'b1	1
24.576 MHz	48	6.144	TDM 128	4	5'd3	4	7'd1	2	3'd1	2	1'b0	2
	96	12.288		4	5'd1	2	7'd0	1	3'd1	2	1'b0	2
	192	24.576		4	5'd0	1	7'd0	1	3'd0	1	1'b1	1
	48	12.288	TDM 256	8	5'd3	4	7'd0	1	3'd2	4	1'b0	2
	96	24.576		8	5'd1	2	7'd0	1	3'd1	2	1'b1	1
	48	24.576	TDM 512	16	5'd3	4	7'd0	1	3'd2	4	1'b1	1
45.158 MHz	44.1	5.645	TDM 128	4	5'd7	8	7'd3	4	3'd1	2	1'b0	2
	88.2	11.290		4	5'd3	4	7'd1	2	3'd1	2	1'b0	2
	176.4	22.579		4	5'd1	2	7'd0	1	3'd1	2	1'b0	2
	44.1	11.290	TDM 256	8	5'd7	8	7'd1	2	3'd2	4	1'b0	2
	88.2	22.579		8	5'd3	4	7'd0	1	3'd2	4	1'b0	2
	44.1	22.579	TDM 512	16	5'd7	8	7'd0	1	3'd3	8	1'b0	2
49.152 MHz	48	6.144	TDM 128	4	5'd7	8	7'd3	4	3'd1	2	1'b0	2
	96	12.288		4	5'd3	4	7'd1	2	3'd1	2	1'b0	2
	192	24.576		4	5'd1	2	7'd0	1	3'd1	2	1'b0	2
	48	12.288	TDM 256	8	5'd7	8	7'd1	2	3'd2	4	1'b0	2
	96	24.576		8	5'd3	4	7'd0	1	3'd2	4	1'b0	2
	48	24.576	TDM 512	16	5'd7	8	7'd0	1	3'd3	8	1'b0	2

Table 9 - TDM Master Clock Rate Configurations

TDM Slave Clock Rate Configurations

All configurations are 32-bit.

MCLK Frequency	WS [kHz]	BCK [MHz]	TDM Mode	Chan-nels	Register 2 [5:0] SELECT_IDAC_NUM	
					Value	Divider
22.579 MHz	44.1	5.645	TDM 128	4	5'd3	4
	88.2	11.290		4	5'd1	2
	176.4	22.579		4	5'd0	1
	44.1	11.290	TDM 256	8	5'd3	4
	88.2	22.579		8	5'd1	2
	44.1	22.579	TDM 512	16	5'd3	4
24.576 MHz	48	6.144	TDM 128	4	5'd3	4
	96	12.288		4	5'd1	2
	192	24.576		4	5'd0	1
	48	12.288	TDM 256	8	5'd3	4
	96	24.576		8	5'd1	2
	48	24.576	TDM 512	16	5'd3	4
45.158 MHz	44.1	5.645	TDM 128	4	5'd7	8
	88.2	11.290		4	5'd3	4
	176.4	22.579		4	5'd1	2
	44.1	11.290	TDM 256	8	5'd7	8
	88.2	22.579		8	5'd3	4
	44.1	22.579	TDM 512	16	5'd7	8
49.152 MHz	48	6.144	TDM 128	4	5'd7	8
	96	12.288		4	5'd3	4
	192	24.576		4	5'd1	2
	48	12.288	TDM 256	8	5'd7	8
	96	24.576		8	5'd3	4
	48	24.576	TDM 512	16	5'd7	8

Table 10 - TDM Slave Slock Rate Configurations

Audio Interface Timing

Audio data on DATA1-2 are sampled at the rising edges of DATA_CLK and must satisfy the setup and hold time requirements relative to the rising edge of DATA_CLK.

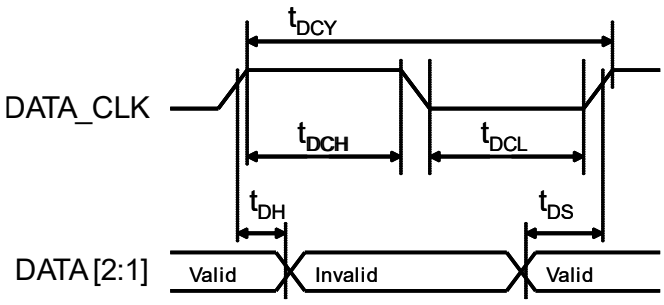


Figure 10 - Audio Interface Timing

Parameter	Symbol	Min	Max	Unit
DATA_CLK pulse width high	t_{DCH}	9.0		ns
DATA_CLK pulse width low	t_{DCL}	9.0		ns
DATA_CLK cycle time	t_{DCY}	20		ns
DATA_CLK duty cycle		45:55	55:45	
DATAx set-up time to DATA_CLK rising edge	t_{DS}	4.1		ns
DATAx hold time to DATA_CLK rising edge	t_{DH}	2.0		ns

Table 11 - Audio Interface Timing Definitions

Pre-Programmed Digital Filters

The ES9033 has 8 pro-programmed digital filters. The latency for each filter reduces (scales) with increasing sample rates. (See Register 52[2:0] FILTER_SHAPE for configuration).

#	Filter	Description
1	Minimum phase (default)	Version 2 of minimum phase fast roll-off (#6) with less ripple and more image rejection.
2	Linear phase apodizing fast roll-off	Full image rejection by fs/2 to avoid any aliasing, with smooth roll-off starting before 20k.
3	Linear phase fast roll-off	Sabre legacy filter, optimized for image rejection @ 0.55 fs
4	Linear phase fast roll-off low-ripple	Sabre legacy filter, optimized for in-band ripple
5	Linear phase slow roll-off	Sabre legacy filter, optimized for lower latency, but symmetric impulse response
6	Minimum phase fast roll-off	Low latency, minimal pre ringing and low passband ripple, image rejection @ 0.55fs
7	Minimum phase slow roll-off	Lowest latency at the cost of image rejection
8	Minimum phase fast roll-off low dispersion	Provides a nice balance of the low latency of minimum phase filters and the low dispersion of linear phase filters. Minimal pre-ringing is added to achieve the low dispersion in the audio band.

Table 12 - Pre-Programmed Digital Filter Properties

Note: Minimum phase filters are asymmetric filters that work to minimize the pre-echo of the filter, while still maintaining an excellent frequency response and they peak earlier than linear phase filters, resulting in a lower group delay. Minimum phase filters usually feature zero cycles of pre-echo, which can result in improved audio quality.

PCM Filter Latency

The following table shows the simulated latency of each filter at 44.1kHz sampling rate. Measurements were taken from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize the data stream. Latency delay will reduce (scale) with sampling rate.

Digital Filter	Delay(us) @ fs=44.1kHz
Minimum Phase (default)	145 us
Linear Phase Apodizing	810 us
Linear Phase Fast Roll-Off	825 us
Linear Phase Fast Roll-Off Low Ripple	817 us
Linear Phase Slow Roll-Off	195 us
Minimum Phase Fast Roll-Off	145 us
Minimum Phase Slow Roll-Off	123 us
Minimum Phase Slow Roll-Off Low Dispersion	280 us

Table 13 - Pre-Programmed Digital Filter Latency

PCM Filter Properties

Minimum Phase					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46FS	Hz
Stop band	-80 dB	0.54FS			Hz
Group Delay		3.53/FS		9.63/FS	s
Flatness (ripple)	0.0034				dB

Linear Phase Apodizing					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.41FS	Hz
Stop band	-74 dB	0.50FS			Hz
Group Delay			33.43/FS		s
Flatness (ripple)	0.0043				dB

Linear Phase Fast Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46FS	Hz
Stop band	-77 dB	0.54FS			Hz
Group Delay			34.06/FS		s
Flatness (ripple)	0.0063				dB

Linear Phase Fast Roll-Off Low Ripple					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46FS	Hz
Stop band	-79 dB	0.55FS			Hz
Group Delay			33.75/FS		s
Flatness (ripple)	0.0041				dB

Linear Phase Slow Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.46FS	Hz
Stop band	-79 dB	0.79FS			Hz
Group Delay			6.30/FS		s
Flatness (ripple)					dB

Minimum Phase Fast Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46FS	Hz
Stop band	-78 dB	0.54FS			Hz
Group Delay		3.53/FS		9.76/FS	s
Flatness (ripple)	0.0043				dB

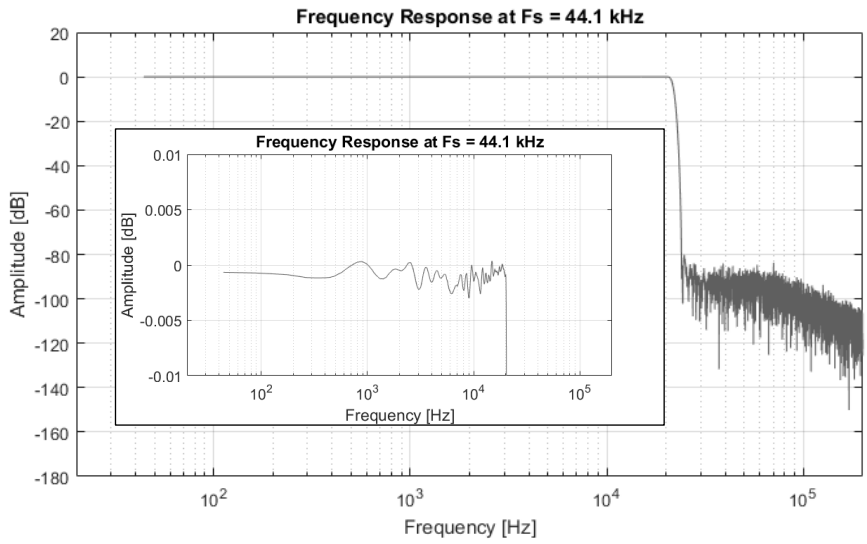
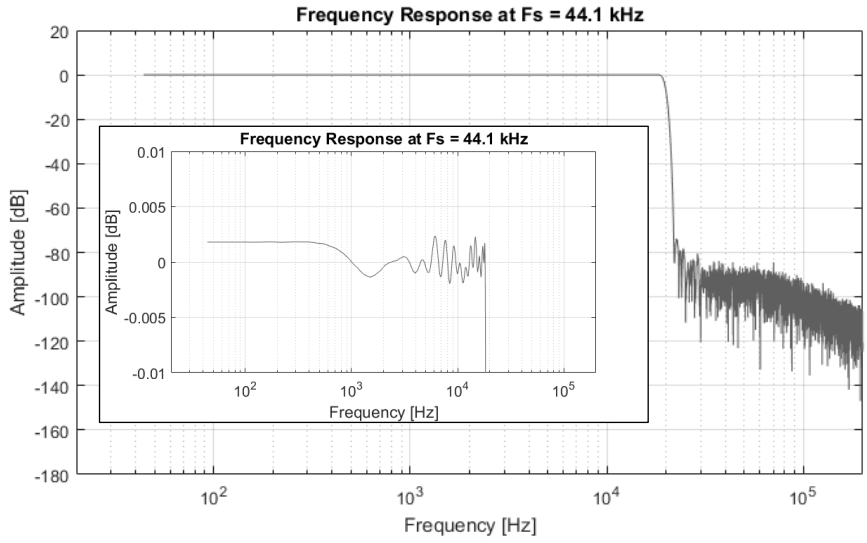
Minimum Phase Slow Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.43FS	Hz
Stop band	-85 dB	0.79FS			Hz
Group Delay		2.71/FS		3.21/FS	s
Flatness (ripple)					dB

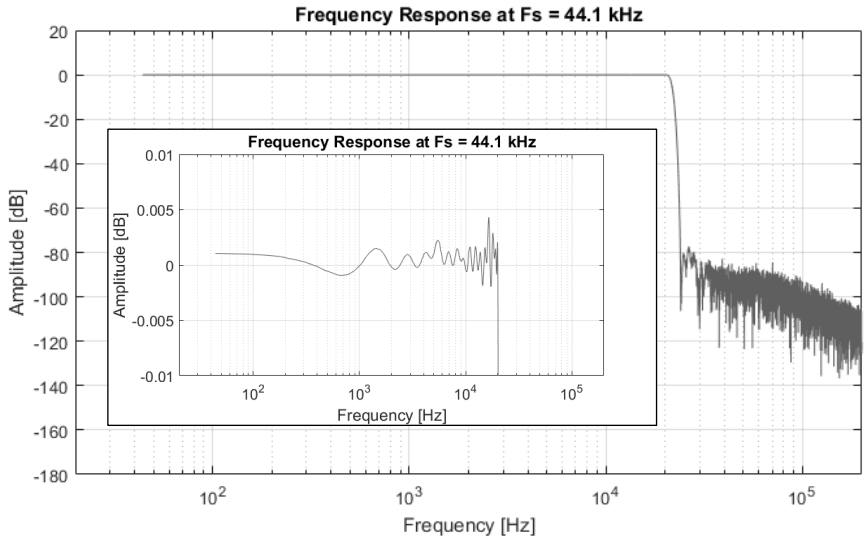
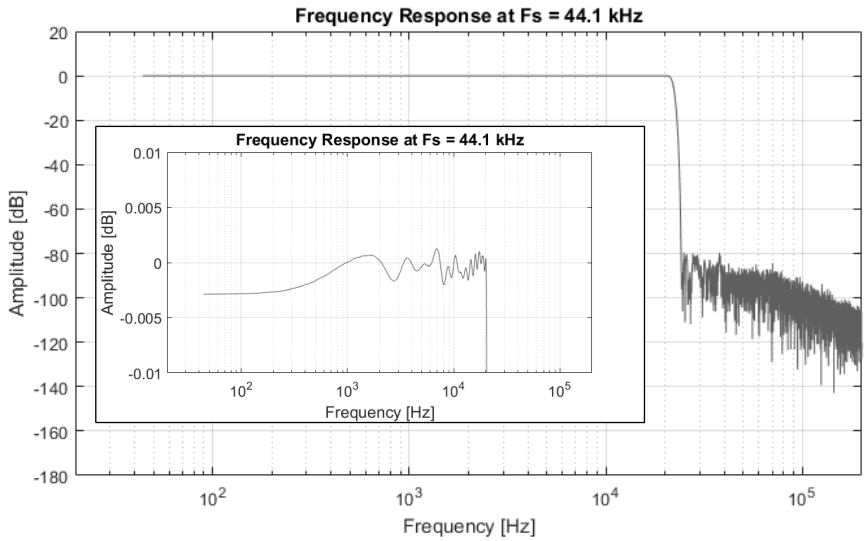
Minimum Phase Slow Roll-off Low Dispersion					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.43FS	Hz
Stop band	-81 dB	0.79FS			Hz
Group Delay		9.85/FS		10.38/FS	s
Flatness (ripple)					dB

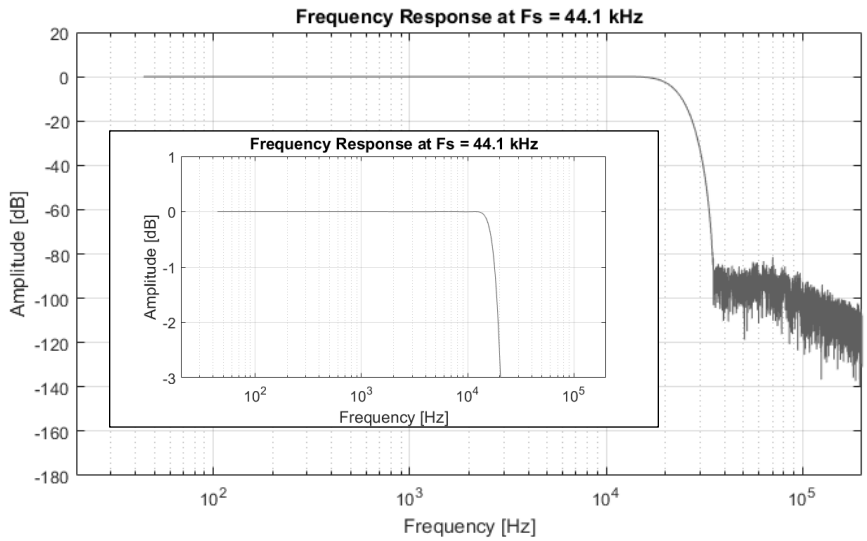
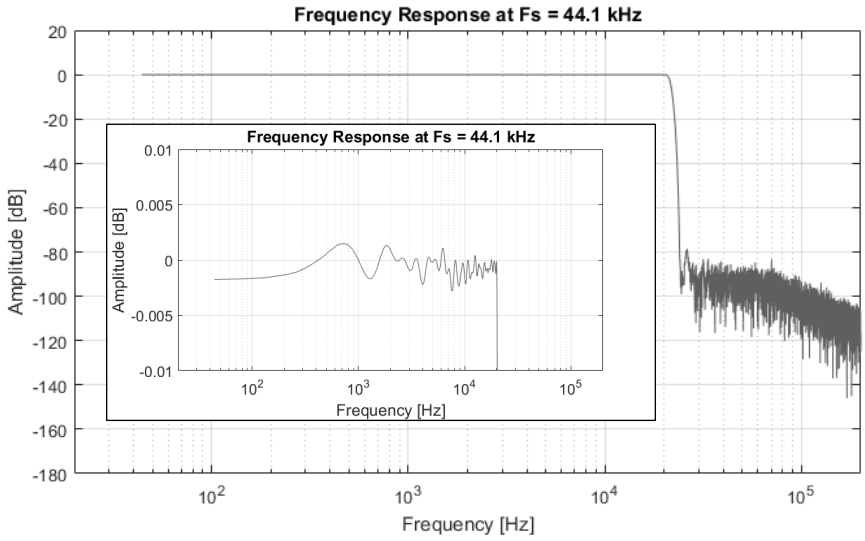
Table 14 - PCM Filter Properties

PCM Filter Frequency Response

The following frequency responses were obtained from software simulations of these filters. Simulation sample rate is 44.1kHz.

Filter	Frequency Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-Off	
Linear Phase Fast Roll-Off Low Ripple	

Linear Phase Slow Roll-Off	
Minimum Phase Fast Roll-Off	

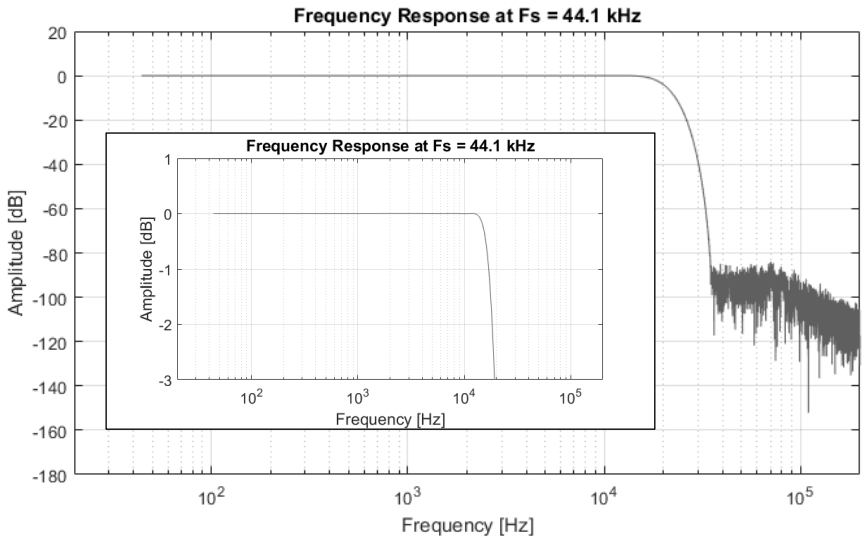
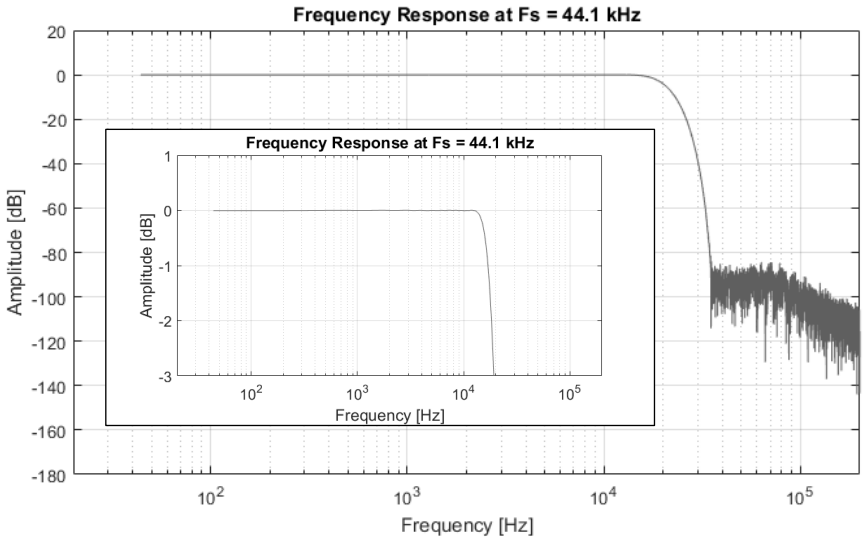
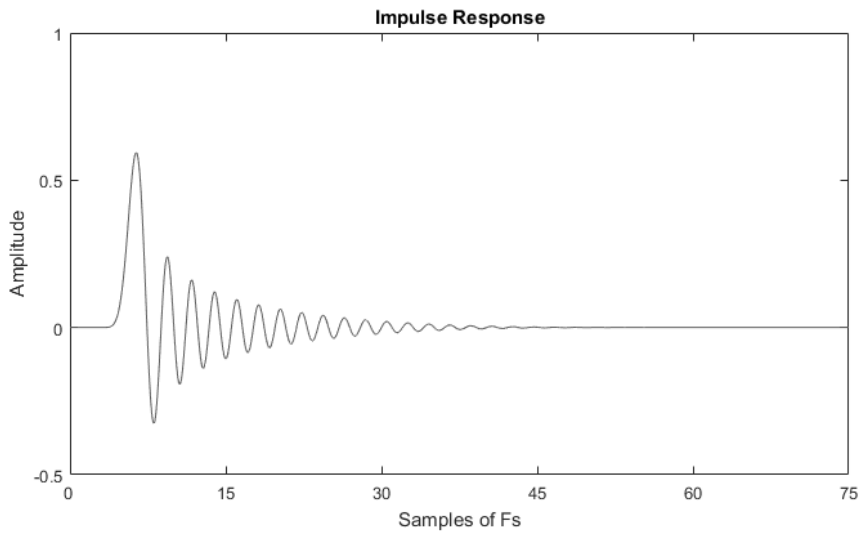
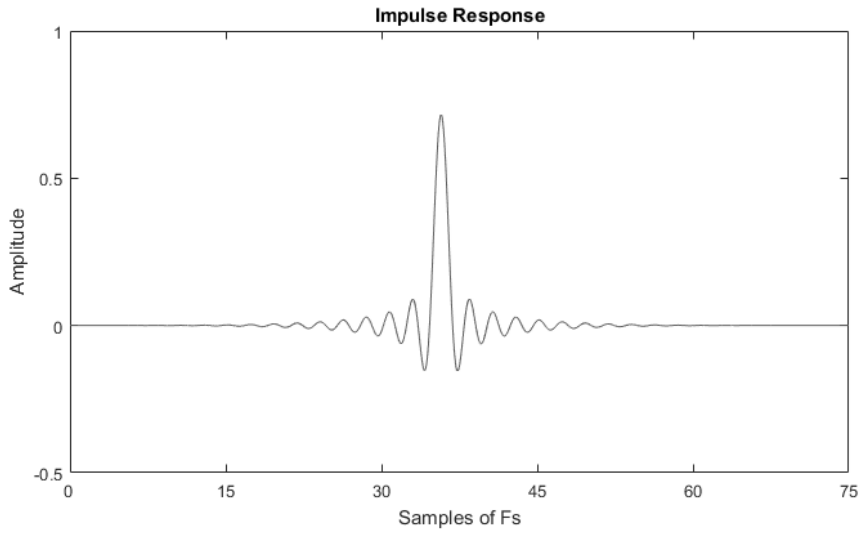
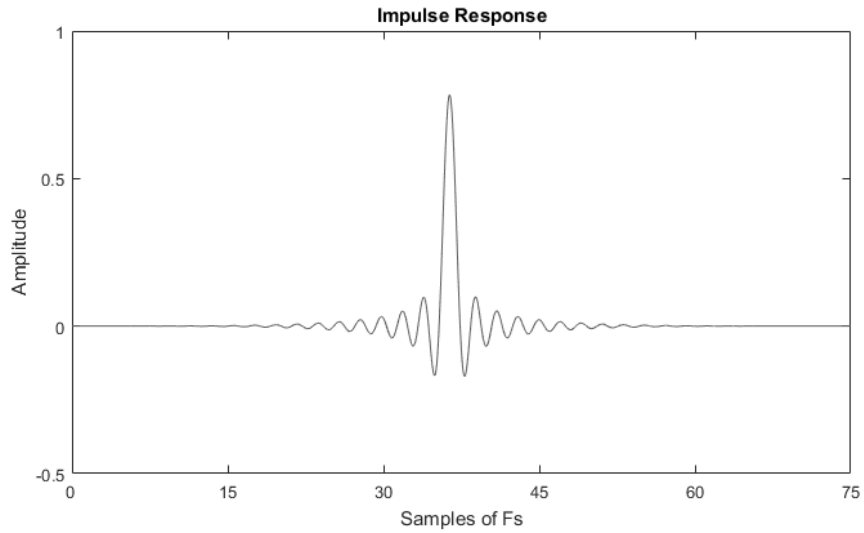
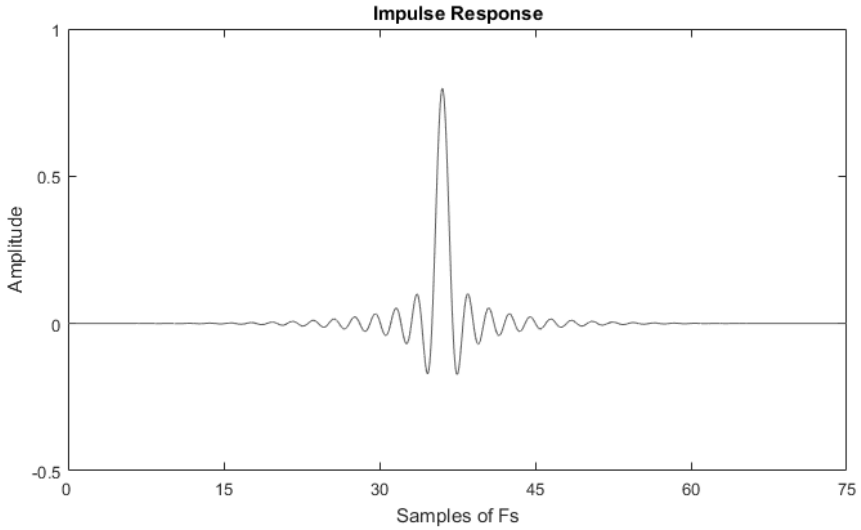
Minimum Phase Slow Roll-Off	
Minimum Phase Slow Roll-Off Low Dispersion	

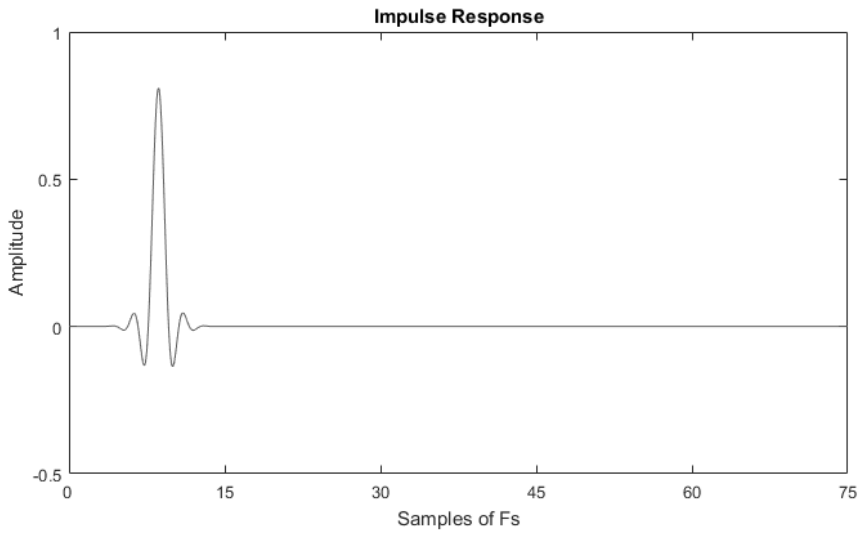
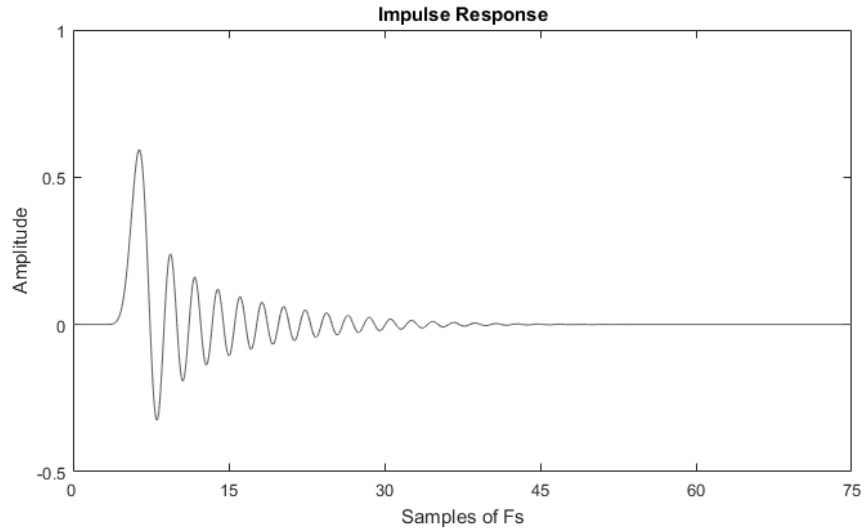
Table 15 - PCM Filter Frequency Response

PCM Filter Impulse Response

The following impulse responses were obtained from software simulations of these filters. They were measured from external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize the data stream.

Filter	Impulse Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-Off	
Linear Phase Fast Roll-Off Low Ripple	

Linear Phase Slow Roll-Off	
Minimum Phase Fast Roll-Off	

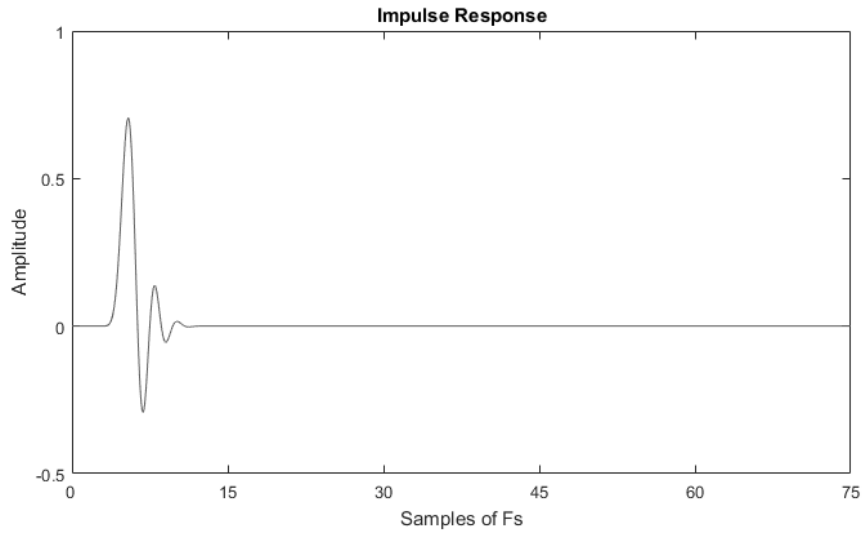
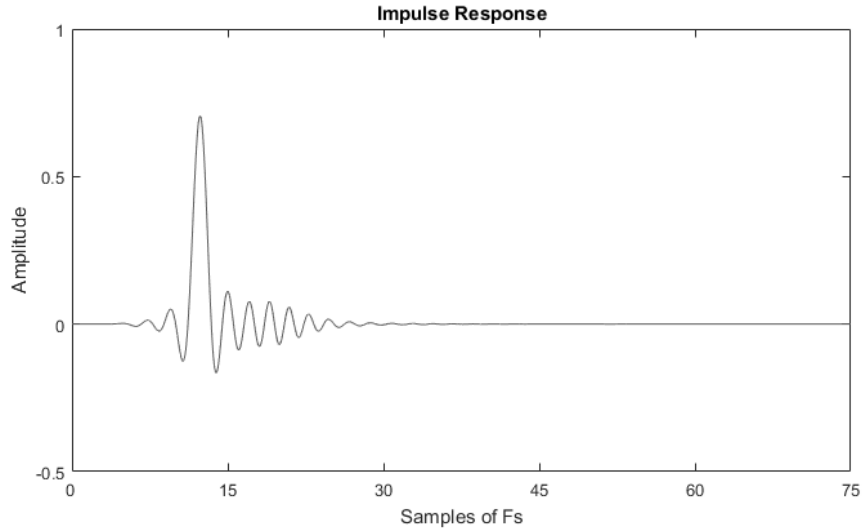
Minimum Phase Slow Roll-Off	
Minimum Phase Slow Roll-Off Low Dispersion	

Table 16 - PCM Filter Impulse Response

64FS Mode

When 64FS (MCLK/FS ratio) is required, it is necessary for the ES9033 to be running in 64FS mode. 64FS Mode can be manually entered by setting Register 0[6] ENABLE_64FS_MODE to 1'b1.

Manual

- Register 0[3] ENABLE_64FS_MODE
  - Use for 64FS ratios, including 705.6/768kHz to 1'b1.

Automatically

- Register 36[7] AUTO_FS_DETECT
  - Auto sets the CLK_IDAC divider according to MCLK/FS ratio
  - Automatically enables 64FS mode when CLK_DAC/CLK_IDAC ratio is 64

Linear Phase 64FS Latency

The following table shows the simulated latency at 705.6kHz sampling rate and would be very similar at 768kHz. Measurements were taken from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize the data stream. Latency delay will reduce (scale) with sampling rate.

Digital Filter	Delay(us) @ fs= 705.6 kHz
Linear Phase 64FS	8.5 us

Table 17 - Linear Phase 64FS Latency

Linear Phase 64FS Properties

Linear Phase Double Rate					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.44FS	Hz
Stop band	-60 dB	0.74FS			Hz
Group Delay			4.08/FS		s
Flatness (ripple)					dB

Table 18 - Linear Phase 64FS Properties

Linear Phase 64FS Frequency Response

This filter gets selected while in 64FS mode.

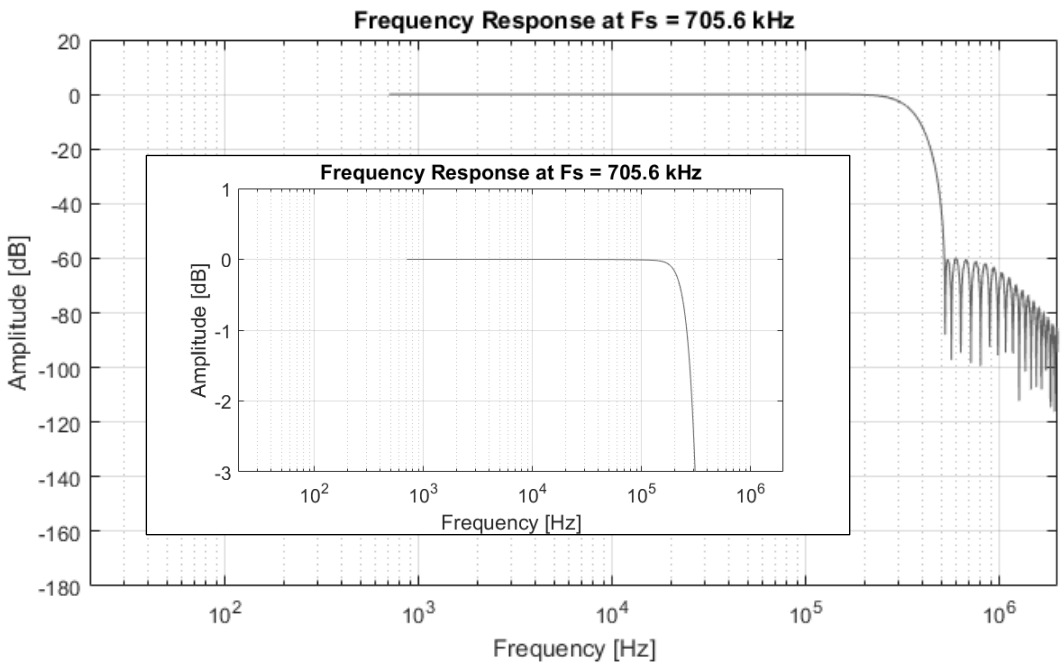


Table 19 - Linear Phase 64FS Frequency Response

Linear Phase 64FS Impulse Response

The following impulse response was obtained from software simulations. It was measured from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize the data stream.

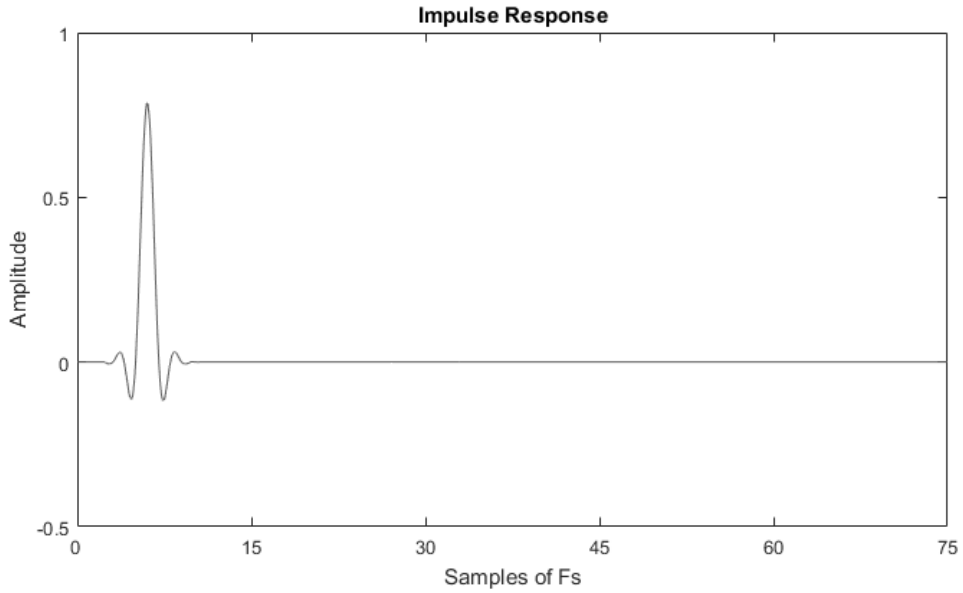


Table 20 - Linear Phase 64FS Impulse Response

Analog Features

APLL

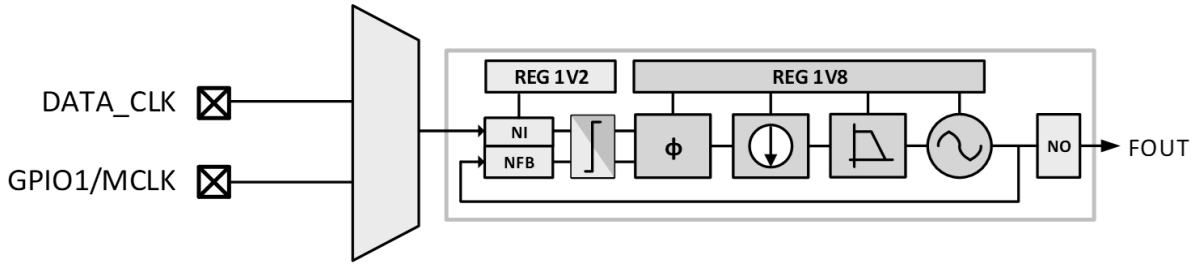


Figure 11 - Functional Block Diagram of ES9033 APLL

The ES9033 has a built in Analog PLL (APLL) for generating frequencies that are unavailable externally.

For calculation of the PLL frequency output, use the following formula:

$$Fout=\left(\frac{FIN}{NI}\right)*\frac{NFB}{NO}$$

$$NFB = \frac{(2^{25})}{FBDIV}$$

Where:

1. FBDIV is a 24-bit number
2. $F_{VCO} = F_{OUT} * NO$, where F_{VCO} must be between 90MHz and 100MHz
3. NI = Input dividing ratio
   - Accessible from Register 202-200[9:1] PLL_CLK_IN_DIV
4. NO = Output dividing ratio
   - Accessible from Register 202-200[13:10] PLL_CLK_OUT_DIV
5. NFB = Feedback dividing ratio
   - Accessible from Register 199-197[23:0] PLL_CLK_FB_DIV

PLL Registers

- NI - Register 202-200[9:1] PLL_CLK_IN_DIV
- NO - Register 202-200[13:10] PLL_CLK_OUT_DIV
- FBDIV - Register 199-197[23:0] PLL_CLK_FB_DIV

Absolute Maximum Ratings

PARAMETER	RATING
Positive Supply Voltage • AVCC_3V3 • AVCC_CP • VCCA • AVDD • DVDD	 • +3.7V with respect to Ground • +3.7V with respect to Ground • +3.7V with respect to Ground • +3.7V with respect to Ground • +1.4V with respect to Ground
Storage temperature	–65°C to + 150°C
Operating Junction Temperature	+125°C
Voltage range for digital input pins	–0.3V to AVDD (nom) + 0.3V
ESD Protection Human Body Model (HBM) Charge Device Model (CDM)	 2kV 500V

Table 21 - Absolute Maximum Ratings

WARNING: Stresses beyond those listed under here may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied.

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

IO Electrical Characteristics

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNIT	COMMENTS
High-level input voltage	VIH	(AVDD / 2) + 0.4		V	
Low-level input voltage	VIL		0.4	V	
High-level output voltage	VOH	AVDD – 0.2		V	IOH = (AVDD / 2) + 1.4 [mA]
Low-level output voltage	VOL		0.2	V	IOL = (AVDD / 2) + 1.7 [mA]

Table 22 - IO Electrical Characteristics

Recommended Operating Conditions

These are the recommended operating conditions for the ES9033.

PARAMETER	SYMBOL	CONDITIONS
Operating temperature	T_A	–20°C to +85°C
DVDD		Internally Generated
AVDD		3.3V
VCCA		3.3V
AVCC		Internally Generated
AVCC_CP		3.3V
AVCC_3V3		3.3V

Table 23 - Recommended Operating Conditions

Power Consumption

Power numbers are given when the device is in slave mode.

Test Conditions 1 (unless otherwise noted)

T_A=25ºC, AVCC_3V3=AVCC_CP=VCAA=AVDD=+3.3V, fs=48kHz, MCLK=49.152MHz, I²S at 2Vrms 1kHz sine full scale

Parameter	Min	Typ.	Max	Unit
Hardware Mode: 3				
AVCC_3V3		11.4		mA
AVCC_CP		7.2		mA
VCCA		0.3		mA
AVDD		11.2		mA
Standby (CHIP_EN = 0V)				
AVCC		<1		µA
AVDD		<1		µA

Table 24 - Power Consumption with Test Conditions 1

Test Conditions 2 (unless otherwise noted)

T_A=25ºC, AVCC_3V3=AVCC_CP=VCAA=AVDD=+3.3V, fs=48kHz, MCLK=49.152MHz, I²S streaming zeros

Parameter	Min	Typ.	Max	Unit
Hardware Mode: 3				
AVCC_3V3		<1		mA
AVCC_CP		0.5		mA
VCCA		0.3		mA
AVDD		9.8		mA
Standby (CHIP_EN = 0V)				
AVCC		<1		µA
AVDD		<1		µA

Table 25 - Power Consumption with Test Conditions 2

Test Conditions 3 (unless otherwise noted)

T_A=25ºC, AVCC_3V3=AVCC_CP=VCAA=AVDD=+3.3V, fs=192kHz, MCLK=24.576MHz, I²S at 2Vrms 1kHz sine full scale

Parameter	Min	Typ.	Max	Unit
Hardware Mode: 3				
AVCC_3V3		10.4		mA
AVCC_CP		7.0		mA
VCCA		0.2		mA
AVDD		10.4		mA
Standby (CHIP_EN = 0V)				
AVCC		<1		µA
AVDD		<1		µA

Table 26 - Power Consumption with Test Conditions 3

Performance

Test Conditions 1 (unless otherwise noted)

T_A=25ºC, AVCC_3V3=AVCC_CP=VCAA=AVDD=+3.3V, fs=48kHz, MCLK=49.152MHz, 1kHz tone

Parameter			Min	Typ.	Max	Unit
Resolution				32		Bit
THD+N Ratio @fs=48kHz, BW=20Hz-20kHz				-108	-105	dB
DNR A-weighted (w/ DRE)	-60dBFS		120	122		dB
DNR A-weighted (w/o DRE)	-60dBFS		112	115		dB
Inter-channel Mismatch				±0.02	±0.02	dB
Output amplitude	0dBFS			2.1		Vrms

Table 27 - Performance Data

Recommended Power-Up Sequence

The recommended power-up sequence is shown in the following diagram.

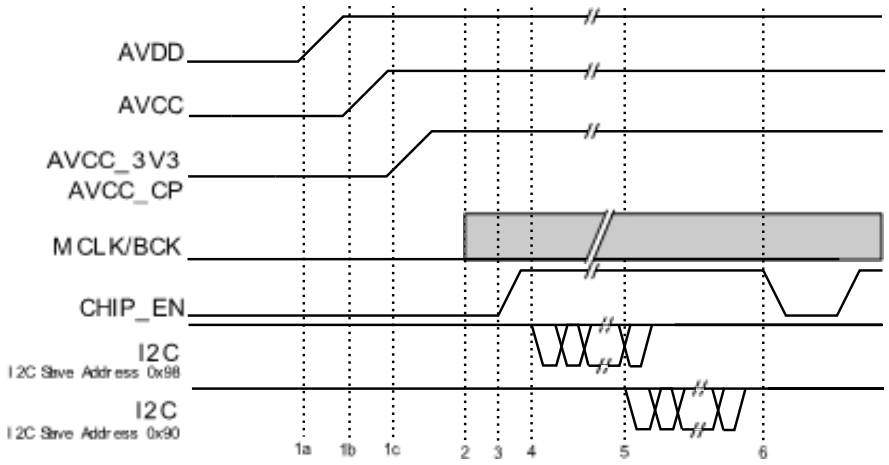


Figure 12 - Recommended Power-Up Sequence

1. Supplies:
    a. AVDD
    b. AVCC
    c. AVCC_3V3, AVCC_CP
2. Enable MCLK
3. Set CHIP_EN high after MCLK is stable
4. Configure the clock setup through I^2C address 0x98
    a. Must wait 100ms after CHIP_EN is set HIGH
5. I^2C address 0x90 can be written/read after clock setup has been established
6. Any reset operation must keep CHIP_EN low for at least 20ns

Recommended Power-Down Sequence

The recommended power-down sequence is shown in the following diagram.

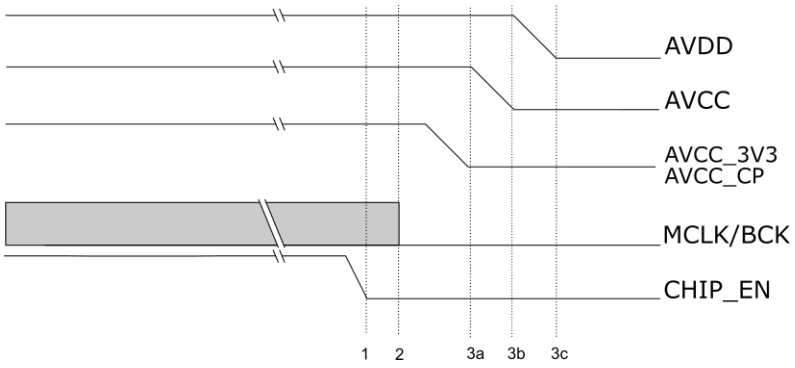


Figure 13 - Recommended Power-Down Sequence

1. Set CHIP_EN to 0V
2. Disable MCLK
3. Supplies
    a. AVCC_3V3, AVCC_CP
    b. AVCC
    c. AVDD

Register Overview

I²C Slave Interface (Device Address 0x90, 0x92, 0x94, 0x96)

This interface contains Read/Write and Read-only registers. A system clock must be present.

Multi-byte registers must be written from LSB to MSB. Data is latched when MSB is written.
Multi-byte registers must be read from LSB to MSB. Data is latched when LSB is read.
MSB is always stored in the highest register address.

Read/Write Register Addresses

Registers 0-88 (0x00 - 0x58) are read/write registers.

Read-Only Register Addresses

Registers 224-241 (0xE0 - 0xF1) are read only registers.

I²C synchronous Slave Interface (Device Address 0x98, 0x9A, 0x9C, 0x9E)

This interface contains Write-only registers. These registers can be written even when there is no system clock present.

When the device is inactive, all peripherals are automatically disabled, and all clocks are stopped. A reset can wake the ES9033.

Write-Only Register Addresses

Registers 192-203 (0xC0 - 0xCB) are write only registers.

Multi-Byte Registers

Multi-byte registers must be written from LSB to MSB. Data is latched when MSB is written.

MSB is always stored in the highest register address.

I²C Slave/Synchronous Slave Interface Timing

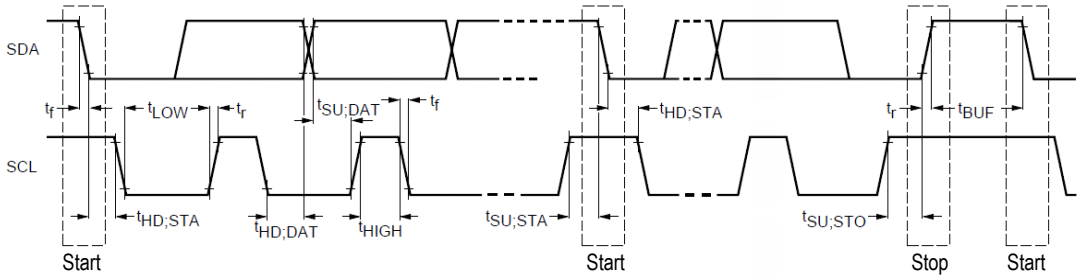


Figure 14 - I²C Slave Control Interface Timing

Parameter	Symbol	CLK Constraint	Standard-Mode		Fast-Mode		Unit
			MIN	MAX	MIN	MAX	
SCL Clock Frequency	f_{SCL}	< CLK/20	0	100	0	400	kHz
START condition hold time	$t_{HD;STA}$		4.0	-	0.6	-	µs
LOW period of SCL	t_{LOW}	>10/CLK	4.7	-	1.3	-	µs
HIGH period of SCL (>10/CLK)	t_{HIGH}	>10/CLK	4.0	-	0.6	-	µs
START condition setup time (repeat)	$t_{SU;STA}$		4.7	-	0.6	-	µs
SDA hold time from SCL falling - All except NACK read - NACK read only	$t_{HD;DAT}$		0 2/CLK	-	0 2/CLK	-	µs s
SDA setup time from SCL rising	$t_{SU;DAT}$		250	-	100	-	ns
Rise time of SDA and SCL	t_r		-	1000		300	ns
Fall time of SDA and SCL	t_f		-	300		300	ns
STOP condition setup time	$t_{SU;STO}$		4	-	0.6	-	µs
Bus free time between transmissions	t_{BUF}		4.7	-	1.3	-	µs
Capacitive load for each bus line	C_b		-	400	-	400	pF

Table 28 - I²C Slave/Synchronous Slave Interface Timing Definitions

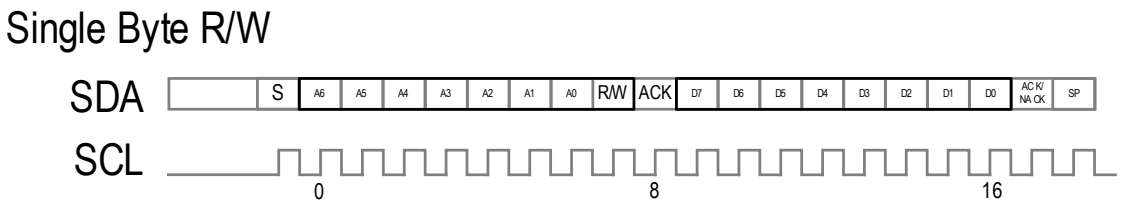


Figure 15 - I²C Single Byte R/W

SPI Slave Interface

The SPI slave interface is used when the MODE pin (Pin 3) is pulled HIGH.

- The SPI Slave interface can be accessed using the Pins 25-28
  - Pin 22 MOSI
  - Pin 21 SCLK
  - Pin 19 SS
  - Pin 20 MISO

The 4-wire SPI data format is: Command (1 byte) + Address (1 byte) + Data

SPI Commands

- 0x01: Read
- 0x03: Write
- 0x07: Write-Only Register Addresses 192-194 (0xC0 - 0xC2)

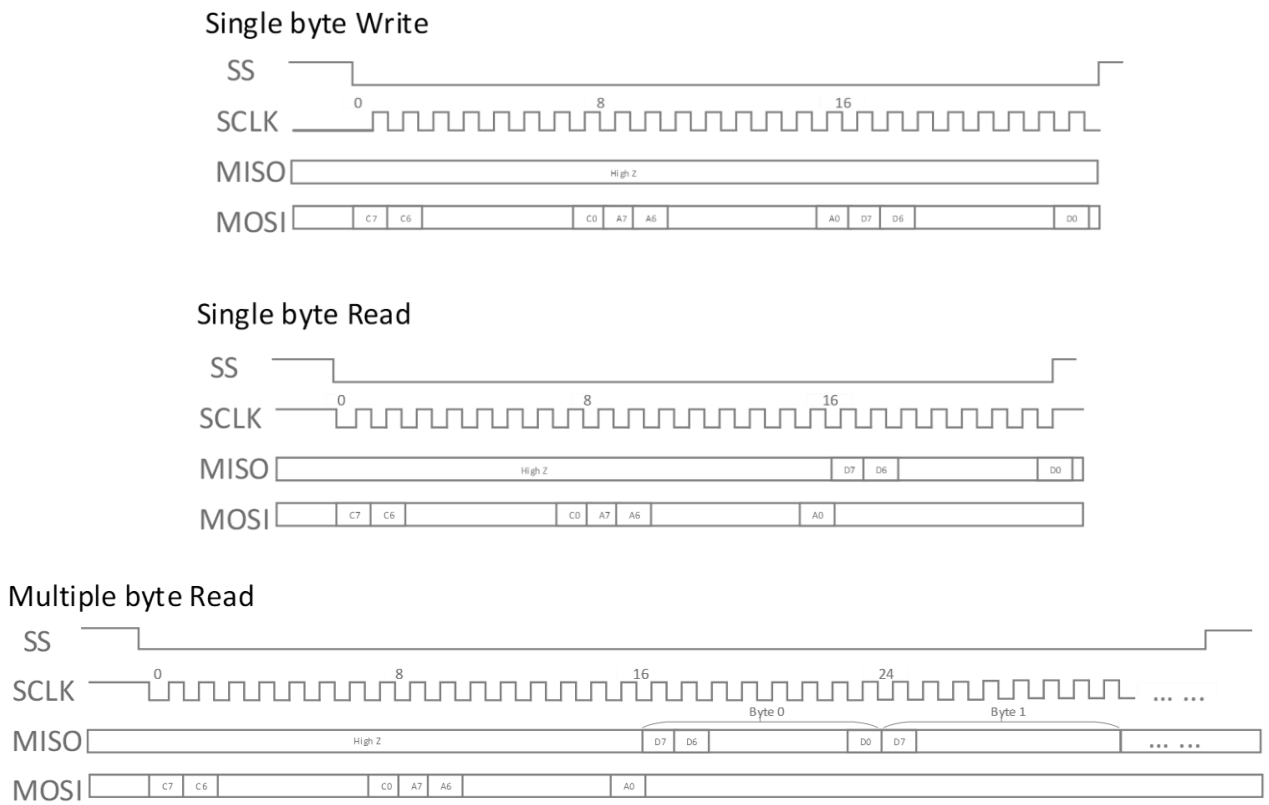


Figure 16 - SPI Timing Diagrams

Register Map

Addr (Hex)	Addr (Dec)	Register	7	6	5	4	3	2	1	0
0x00	0	SYSTEM CONFIG	SOFT_RESET	ENABLE_64FS_ MODE	ENABLE_ ANALOG_DAC_ CH2	ENABLE_ ANALOG_DAC_ CH1	ENABLE_ NSMOD	ENABLE_DAC	AMP_MODE_ REG	RESERVED
0x01	1	SYS MODE CONFIG	RESERVED					ENABLE_DOP_ DECODE	ENABLE_DSD_ DECODE	ENABLE_TDM_ DECODE
0x02	2	DAC CLOCK CONFIG	RESERVED	SELECT_IDAC_ HALF	SELECT_IDAC_NUM					
0x03	3	MASTER CLOCK CONFIG	SELECT_MENC _HALF	SELECT_MENC_NUM						
0x04	4	CP CLOCK DIV	CP_CLK_DIV							
0x05-0x08	5-8	RESERVED	RESERVED							
0x09	9	INTERRUPT MASK P	SOFT_RAMP_ CH2_MASKP	SOFT_RAMP_ CH1_MASKP	DRE_CH2_ MASKP	DRE_CH1_ MASKP	AUTOMUTE_ CH2_MASKP	AUTOMUTE_ CH1_MASKP	VOL_MIN_CH2_ MASKP	VOL_MIN_CH1_ MASKP
0x0A	10		INPUT_DATA_TYPE_MASKP		TDM_DATA_ VALID_MASKP	CLK_AVALID_ MASKP	RESERVED	BCK_WS_ FAILED_MASKP	RESERVED	DOP_VALID_ MASKP
0x0B	11	INTERRUPT MASK N	SOFT_RAMP_ CH2_MASKN	SOFT_RAMP_ CH1_MASKN	DRE_CH2_ MASKN	DRE_CH1_ MASKN	AUTOMUTE_ CH2_MASKN	AUTOMUTE_ CH1_MASKN	VOL_MIN_CH2_ MASKN	VOL_MIN_CH1_ MASKN
0x0C	12		INPUT_DATA_TYPE_MASKN		TDM_DATA_ VALID_MASKN	CLK_AVALID_ MASKN	RESERVED	BCK_WS_ FAILED_MASKN	RESERVED	DOP_VALID_ MASKN
0x0D	13	INTERRUPT CLEAR	SOFT_RAMP_ CH2_CLEAR	SOFT_RAMP_ CH1_CLEAR	DRE_CH2_ CLEAR	DRE_CH1_ CLEAR	AUTOMUTE_ CH2_CLEAR	AUTOMUTE_ CH1_CLEAR	VOL_MIN_CH2_ CLEAR	VOL_MIN_CH1_ CLEAR
0x0E	14		INPUT_DATA_CLEAR		TDM_DATA_ VALID_CLEAR	CLK_AVALID_ CLEAR	RESERVED	BCK_WS_ FAILED_CLEAR	RESERVED	DOP_VALID_ CLEAR
0x0F	15	ANALOG CTRL CONFIG	RESERVED	AMP_PDB_ON_ SS	AMP_PDB_CLK _INVALID	RESERVED			LP_DAC_REG	EN_FCB
0x10	16	LDRV CTRL	ENB_OCP_ LDRV_CH2	ENB_OCP_ LDRV_CH1	RESERVED					
0x11-0x12	17-18	RESERVED	RESERVED							
0x13	19	ANALOG CONTROL OVERRIDE2	TRIB_DAC_CH2	TRIB_DAC_CH1	RESERVED					
0x14-0x17	20-23	RESERVED	RESERVED							
0x18	24	GPIO CONFIG	INVERT_GPIO1	GPIO1_WK_EN	GPIO1_SDB	GPIO1_OE	GPIO1_CFG			
0x19	25	GPIO CONFIG2	GPIO_OR_SS_ RAMP	GPIO_OR_VOL_ MIN	GPIO_OR_ AUTOMUTE	GPIO_AND_SS_ RAMP	GPIO_AND_VOL _MIN	GPIO_AND_ AUTOMUTE	RESERVED	GPIO1_READ
0x1A	26	GPIO INPUT ENABLE	RESERVED						GPIO_AMP_ MODE	GPIO_SEL
0x1B	27	PWM1 COUNT	PWM1_COUNT							
0x1C	28	PWM1 FREQUENCY	PWM1_FREQ							
0x1D	29		PWM1_FREQ							
0x1E	30	PWM2 COUNT	PWM2_COUNT							
0x1F	31	PWM2 FREQUENCY	PWM2_FREQ							
0x20	32		PWM2_FREQ							
0x21	33	PWM3 COUNT	PWM3_COUNT							
0x22	34	PWM3 FREQUENCY	PWM3_FREQ							
0x23	35		PWM3_FREQ							
0x24	36	INPUT CONFIG	AUTO_FS_ DETECT	DSD_NEGEDGE	DSD_MASTER_ MODE	ENABLE_ MASTER_MODE	RESERVED	INPUT_SEL		AUTO_INPUT_ SELECT
0x25	37	MASTER MODE CONFIG	AUTO_FS_ DETECT_ BLOCK_ 64FSMODE	MASTER_BCK_ DIV1	MASTER_WS_ IDLE	MASTER_FRAME_LENGTH		MASTER_WS_ PULSE_MODE	MASTER_WS_ INVERT	MASTER_BCK_ INVERT
0x26	38	TDM CONFIG1	TDM_RESYNC	MASTER_WS_SCALE			TDM_CH_NUM			
0x27	39	TDM CONFIG2	TDM_LJ_MODE	TDM_VALID_ EDGE	TDM_VALID_PULSE_LEN					
0x28	40	TDM CONFIG3	RESERVED	TDM_BIT_WIDTH	TDM_DATA_LATCH_ADJ					
0x29	41	RESERVED	RESERVED							
0x2A	42	TDM SLOT CONFIG	TDM_CH2_SLOT_SEL				TDM_CH1_SLOT_SEL			
0x2B	43	RESERVED	RESERVED							
0x2C	44	RESYNC CONFIG	RESERVED	CP_PDB_ON_ MUTE	RESERVED	SYNC_DAC_ ICG	DOP_CLK_ RESYNC	VOL_THD_ RESYNC	FIR_RESYNC	FS_RESYNC
0x2D	45	FS GENERATOR PHASE	DSD_2DB_ DOWN	RESERVED						
0x2E	46	VOLUME1	VOLUME1							
0x2F	47	VOLUME2	VOLUME2							
0x30	48	DAC VOL UP RATE	DAC_VOL_RATE_UP							
0x31	49	DAC VOL DOWN RATE	DAC_VOL_RATE_DOWN							
0x32	50	DAC VOL DOWN RATE FAST	DAC_VOL_RATE_FAST							
0x33	51	MUTE CTRL	FORCE_ VOLUME	DAC_USE_ MONO_ VOLUME	RUN_VOLUME	RESERVED	DAC_INVERT_ CH2	DAC_INVERT_ CH1	DAC_MUTE_ CH2	DAC_MUTE_ CH1
0x34	52	FILTER CONFIG	AUTO_CH_ DETECT	BYPASS_ DEEMPH	PEAK_FILTER	SEL_DEEMPH		FILTER_SHAPE		
0x35-0x36	53-54	RESERVED	RESERVED							
0x37	55	THD COMP C2 CH1	THD_C2_CH1							
0x38	56		THD_C2_CH1							
0x39	57		THD_C3_CH1							
0x3A	58		THD_C3_CH1							
0x3B	59	THD COMP C2 CH2	THD_C2_CH2							
0x3C	60		THD_C2_CH2							
0x3D	61		THD_C3_CH2							
0x3E	62		THD_C3_CH2							

0x3F	63	AUTOMUTE TIME	AUTOMUTE_TIME							
0x40	64		AUTOMUTE_ RAMP_TO_ GROUND	AUTOMUTE_ WAIT_ON_DRE	RESERVED	AUTOMUTE_EN _CH2	AUTOMUTE_EN _CH1	AUTOMUTE_TIME		
0x41	65	AUTOMUTE LEVEL	AUTOMUTE_LEVEL							
0x42	66		AUTOMUTE_LEVEL							
0x43	67	AUTOMUTE OFF LEVEL	AUTOMUTE_OFF_LEVEL							
0x44	68		AUTOMUTE_OFF_LEVEL							
0x45	69	SOFT RAMP CONFIG	GAIN_18DB_ CH2	GAIN_18DB_ CH1	SOFT_RAMP_ TYPE	SOFT_RAMP_TIME				
0x46-0x48	70-72	RESERVED	RESERVED							
0x49	73	DRE CONFIG	DRE_ZC_ CH2	DRE_ZC_ CH1	RESERVED				DRE_ATR_ EN	DRE_GAIN_EN
0x4A	74	DRE GAIN CH1	DRE_GAIN1							
0x4B	75		DRE_GAIN1							
0x4C	76	DRE GAIN CH2	DRE_GAIN2							
0x4D	77		DRE_GAIN2							
0x4E	78	DRE ON THRESHOLD	DRE_ON_THRESH							
0x4F	79		DRE_ON_THRESH							
0x50	80	DRE OFF THRESHOLD	DRE_OFF_THRESH							
0x51	81		DRE_OFF_THRESH							
0x52	82	DRE DECAY RATE	DRE_ZC_ LEVEL	RESERVED	MIN_PEAK	DRE_DECAY_RATE				
0x53	83	DC OFFSET CH1	DC_OFFSET1							
0x54	84		DC_OFFSET1							
0x55	85	DC OFFSET CH2	DC_OFFSET2							
0x56	86		DC_OFFSET2							
0x57	87	DC RAMP RATE	DC_RAMP_RATE							
0x58	88	MASTER TRIM	MASTER_TRIM							
0xC0	192	RESET & PLL REGISTER1	AO_SOFT_ RESET	PLL_SOFT_ RESET	PLL_VCO_CMP_ISET			RESERVED	GPIO1_SDB_ SYNC	PLL_CLKHV_ PHASE
0xC1	193	PLL REGISTER2	PLL_BYP	DVDD_SHUNTB	SEL_1V_DREG	PLL_HVREG_VREF_SEL			SEL_PLL_IN	EN_PLL_CLKIN
0xC2	194	PLL REGISTER3	RESERVED					AUTO_LOCK_ EN	RESERVED	
0xC3	195	PLL REGISTER4	PLL_CP_BIAS_SEL			PLL_ID_SEL		PLL_VCO_ FMAX	PLL_VCO_PDB	PLL_CP_PDB
0xC4	196	PLL REGISTER5	PLL_VCO_BAND_CTRL			RESERVED			PLL_VCO_IB_AMP_CTRL	
0xC5	197	PLL REGISTER6	PLL_CLK_FB_DIV							
0xC6	198		PLL_CLK_FB_DIV							
0xC7	199		PLL_CLK_FB_DIV							
0xC8	200	PLL REGISTER7	PLL_CLK_IN_DIV							PLL_FB_DIV_ LOAD
0xC9	201		PLL_CLK_OUT_DIV_PHASE		PLL_CLK_OUT_DIV				PLL_CLK_IN_DIV	
0xCA	202		PLL_REG_PDB_ HV	PLL_REG_PDB_ 1V2	RESERVED		PLL_LOW_BW	PLL_CLK_OUT_ DIV_PHASE_EN	PLL_CLK_OUT_DIV_PHASE	
0xCB	203	PLL REGISTER8	RESERVED		PLL_DIG_RSTB	PLL_VCO_ DIODE_EN	RESERVED			
0xE0	224	RESERVED	RESERVED							
0xE1	225	CHIP ID READ	CHIP_ID							
0xE2-0xE4	226-228	RESERVED	RESERVED							
0xE5	229	INTERRUPT STATE	SS_FULL_RAMP_STATE		DRE_SELECT2_ STATE	DRE_SELECT1_ STATE	AUTOMUTE_STATE		VOL_MIN_STATE	
0xE6	230		INPUT_SELECT_OVERRIDE_STATE		TDM_DATA_V ALID_STATE	CLK_AVALID_ STATE	RWS_REF_CNT _FULL_STATE	BCK_WS_FAIL_ STATE	PLL_LOCKED_ STATE	DOP_VALID_ STATE
0xE7	231	INTERRUPT SOURCE	SS_FULL_RAMP_SOURCE		DRE_SELECT2_ SOURCE	DRE_SELECT1_ SOURCE	AUTOMUTE_SOURCE		VOL_MIN_SOURCE	
0xE8	232		INPUT_SELECT_OVERRIDE_ SOURCE		TDM_DATA_ VALID_SOURCE	CLK_AVALID_ SOURCE	RWS_REF_CNT _FULL_ SOURCE	BCK_WS_FAIL_ SOURCE	PLL_LOCKED_ SOURCE	DOP_VALID_ SOURCE
0xE9-0xEE	233-238	RESERVED	RESERVED							
0xEF	239	AUTO TUNING READ	RATIO_VALID	IDAC_DIV_HALF _REG	IDAC_DIV_REG					
0xF0	240	GPIO READ	RESERVED							GPIO1_I_READ
0xF1	241	DAC STATUS READ	SS_RAMP_ DOWN_CH2	SS_RAMP_ DOWN_CH1	SS_RAMP_UP_ CH2	SS_RAMP_UP_ CH1	AUTOMUTE_ CH2	AUTOMUTE_ CH1	VOL_MIN_CH2	VOL_MIN_CH1
0xF2	242		TDM_DATA_ VALID	DOP_VALID	RESERVED		DRE_DETECT_ CH2	DRE_DETECT_ CH1	DRE_SELECT_ CH2	DRE_SELECT_ CH1

Table 29 - Register Map

Register Listing

System Registers

Register 0: SYSTEM CONFIG

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b1	1'b1	1'b1	1'b1	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SOFT_RESET	Performs soft reset to digital core except for the PLL Registers
[6]	ENABLE_64FS_MODE	Enables 64FS mode for 768k sample rate. • 1'b0: 64FS mode disabled (default) • 1'b1: 64FS mode enabled
[5]	ENABLE_ANALOG_DAC_CH2	Enables ch2 analog DAC. • 1'b0: Disabled • 1'b1: Enabled (default)
[4]	ENABLE_ANALOG_DAC_CH1	Enables ch1 analog DAC. • 1'b0: Disabled • 1'b1: Enabled (default)
[3]	ENABLE_NSMOD	Enables nsmod clock. • 1'b0: Clock disabled • 1'b1: Clock enabled (default)
[2]	ENABLE_DAC	Enables DAC interpolation path clock. • 1'b0: Clock disabled • 1'b1: Clock enabled (default)
[1]	AMP_MODE_REG	Sets system mode. • 1'b0: Power Down (default) • 1'b1: HiFi
[0]	RESERVED	NA

Register 1: SYS MODE CONFIG

Bits	[7:3]	[2]	[1]	[0]
Default	5'b00001	1'b0	1'b0	1'b1

Bits	Mnemonic	Description
[7:3]	RESERVED	NA
[2]	ENABLE_DOP_DECODE	Enables DoP decoding. • 1'b0: Disabled (default) • 1'b1: Enabled
[1]	ENABLE_DSD_DECODE	Enables DSD decoding. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	ENABLE_TDM_DECODE	Enables TDM decoding. • 1'b0: Disabled • 1'b1: Enabled (default)

Register 2: DAC CLOCK CONFIG

Bits	[7]	[6]	[5:0]
Default	1'b0	1'b0	6'd7

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6]	SELECT_IDAC_HALF	Specifies whether to half CLK_IDAC divider. • 1'b0: Divide by SELECT_IDAC_NUM + 1 (default) • 1'b1: Divide by half of SELECT_IDAC_NUM + 1 Note: Can only produce half of an odd number divide
[5:0]	SELECT_IDAC_NUM	CLK_IDAC divider. Whole number divide_value + 1 for CLK_IDAC (SYS_CLK/divide_value). • 6'd0: Whole number divide value + 1 = 1 • 6'd1: Whole number divide value + 1 = 2 • 6'd63: Whole number divide value + 1 = 64

Register 3: MASTER CLOCK CONFIG

Bits	[7]	[6:0]
Default	1'b0	7'd7

Bits	Mnemonic	Description
[7]	SELECT_MENC_HALF	Master Encoder (MENC) • 1'b0: Divide by SELECT_MENC_NUM + 1 (default) • 1'b1: Divide by half of SELECT_MENC_NUM + 1 Note: Can only produce half of an odd number divide
[6:0]	SELECT_MENC_NUM	Master mode clock divider. Whole number divide_value + 1 for CLK_Master (SYS_CLK/divide_value). • 7'd0: Whole number divide value + 1 = 1 • 7'd1: Whole number divide value + 1 = 2 • 7'd127: Whole number divide value + 1 = 128

Register 4: CP CLOCK DIV

Bits	[7:0]
Default	8'd31

Bits	Mnemonic	Description
[7:0]	CP_CLK_DIV	Specifies the clk divider for the CP clock source. Valid from 8'd0 to 8'd255. $$CP\_CLK[Hz] = SYS\_CLK/\big((CP\_CLK\_DIV + 1) * 2\big)$$

Register 8-5: RESERVED

Register 10-9: INTERRUPT MASK P

Bits	[15:14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	2'b00	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15:14]	INPUT_DATA_TYPE_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[13]	TDM_DATA_VALID_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[12]	CLK_AVALID_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[11]	RESERVED	NA
[10]	BCK_WS_FAILED_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[9]	RESERVED	NA
[8]	DOP_VALID_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[7]	SOFT_RAMP_CH2_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[6]	SOFT_RAMP_CH1_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[5]	DRE_CH2_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[4]	DRE_CH1_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[3]	AUTOMUTE_CH2_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[2]	AUTOMUTE_CH1_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[1]	VOL_MIN_CH2_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[0]	VOL_MIN_CH1_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive

Register 12-11: INTERRUPT MASK N

Bits	[15:14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	2'b00	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15:14]	INPUT_DATA_TYPE_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[13]	TDM_DATA_VALID_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[12]	CLK_AVALID_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[11]	RESERVED	NA
[10]	BCK_WS_FAILED_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[9]	RESERVED	NA
[8]	DOP_VALID_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[7]	SOFT_RAMP_CH2_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[6]	SOFT_RAMP_CH1_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[5]	DRE_CH2_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[4]	DRE_CH1_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[3]	AUTOMUTE_CH2_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[2]	AUTOMUTE_CH1_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[1]	VOL_MIN_CH2_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[0]	VOL_MIN_CH1_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative

Register 14-13: INTERRUPT CLEAR

Bits	[15:14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	2'b00	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15:14]	INPUT_DATA_CLEAR	Toggle high-low to clear and re-arm interrupt.
[13]	TDM_DATA_VALID_CLEAR	Toggle high-low to clear and re-arm interrupt.
[12]	CLK_AVALID_CLEAR	Toggle high-low to clear and re-arm interrupt.
[11]	RESERVED	NA
[10]	BCK_WS_FAILED_CLEAR	Toggle high-low to clear and re-arm interrupt.
[9]	RESERVED	NA
[8]	DOP_VALID_CLEAR	Toggle high-low to clear and re-arm interrupt.
[7]	SOFT_RAMP_CH2_CLEAR	Toggle high-low to clear and re-arm interrupt.
[6]	SOFT_RAMP_CH1_CLEAR	Toggle high-low to clear and re-arm interrupt.
[5]	DRE_CH2_CLEAR	Toggle high-low to clear and re-arm interrupt.
[4]	DRE_CH1_CLEAR	Toggle high-low to clear and re-arm interrupt.
[3]	AUTOMUTE_CH2_CLEAR	Toggle high-low to clear and re-arm interrupt.
[2]	AUTOMUTE_CH1_CLEAR	Toggle high-low to clear and re-arm interrupt.
[1]	VOL_MIN_CH2_CLEAR	Toggle high-low to clear and re-arm interrupt.
[0]	VOL_MIN_CH1_CLEAR	Toggle high-low to clear and re-arm interrupt.

Register 15: ANALOG CTRL CONFIG

Bits	[7]	[6]	[5]	[4:2]	[1]	[0]
Default	1'd0	1'b1	1'b1	3'b000	1'b0	1'b0

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6]	AMP_PDB_ON_SS	DAC amp power control for soft ramp on normal mute. • 1'b0: When soft ramped to ground during normal mute, keeps DAC AMP on • 1'b1: When soft ramped to ground during normal mute allow DAC AMP to shut down for power saving (default) "normal mute" includes: automute, mute by register, mute by GPIO
[5]	AMP_PDB_CLK_INVALID	DAC amp power control for soft ramp on abnormal mute. • 1'b0: When soft ramped to ground during abnormal mute, keeps DAC AMP on • 1'b1: When soft ramped to ground during abnormal mute allow DAC AMP to shut down for power saving (default) "abnormal mute" includes: PLL unlock, BCK_WS ratio failed
[4:2]	RESERVED	NA
[1]	LP_DAC_REG	Set the low power mode for DAC regulator (Left) • 1'b0: Normal Mode • 1'b1: Low power mode enabled
[0]	EN_FCB	Enable the fast charge for VREF_L AND VREF_R • 1'b0: Enabled (default) • 1'b1: Disable fast charge

Register 16: LDRV CTRL

Bits	[7]	[6]	[5:0]
Default	1'b0	1'b0	6'b000011

Bits	Mnemonic	Description
[7]	ENB_OCP_LDRV_CH2	Line driver over current protection • 1'b0: Enable • 1'b1: Disable
[6]	ENB_OCP_LDRV_CH1	Line driver over current protection • 1'b0: Enable • 1'b1: Disable
[5:0]	RESERVED	NA

Register 17: RESERVED

Register 19-18: ANALOG CONTROL OVERRIDE2

Bits	[15]	[14]	[13:0]
Default	1'b1	1'b1	14'b00000000000000

Bits	Mnemonic	Description
[15]	TRIB_DAC_CH2	Set DAC output tristate. • 1'b0: Tristate • 1'b1: Normal operation
[14]	TRIB_DAC_CH1	Set DAC output tristate. • 1'b0: Tristate • 1'b1: Normal operation
[13:0]	RESERVED	NA

Register 23-20: RESERVED

GPIO Registers

Register 24: GPIO CONFIG

Bits	[7]	[6]	[5]	[4]	[3:0]
Default	1'b0	1'b0	1'b0	1'b0	4'd0

Bits	Mnemonic	Description
[7]	INVERT_GPIO1	Invert GPIO1 • 1'b1: Inverts GPIO1 output.
[6]	GPIO1_WK_EN	Enables GPIO1 weak keeper. • 1'b0: GPIO1 weak keeper disabled (default) • 1'b1: GPIO1 weak keeper enabled
[5]	GPIO1_SDB	Enables GPIO1 input. • 1'b0: Disables GPIO1 input (default) • 1'b1: Enables GPIO1 input
[4]	GPIO1_OE	Enables GPIO1 output. • 1'b0: Tristate GPIO1 (default) • 1'b1: GPIO1 Output Enable
[3:0]	GPIO1_CFG	Configures GPIO1 • 4'd0: output 0 - output • 4'd1: output 0 - output • 4'd2: output 1 - output • 4'd3: CLK_DATA - output • 4'd4: interrupt - output • 4'd5: mute all channel - input • 4'd6: system mode control - input • 4'd7: Reserved • 4'd8: clk_avalid - output • 4'd9: output PWM1 - output • 4'd10: output PWM2 - output • 4'd11: output PWM3 - output • 4'd12: minimum volume - output • 4'd13: automute status - output • 4'd14: soft ramp done - output • 4'd15: output 0 - output

Register 25: GPIO CONFIG2

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b1	1'b0	1'b0

Bits	Mnemonic	Description
[7]	GPIO_OR_SS_RAMP	Sets the GPIO_CFG "Soft Ramp Done" flag output as the bitwise OR of both channel's flags. • 1'b0: Disabled (default) • 1'b1: Enabled, GPIO_CFG output is |(ss_full_ramp[CHx])
[6]	GPIO_OR_VOL_MIN	Sets the GPIO_CFG "Minimum Volume" flag output as the bitwise OR of both channel's flags. • 1'b0: Disabled (default) • 1'b1: Enabled, GPIO_CFG output is |(vol_min[CHx])
[5]	GPIO_OR_AUTOMUTE	Sets the GPIO_CFG "Automute Status" output as the bitwise OR of both channel's statuses. • 1'b0: Disabled (default) • 1'b1: Enabled, GPIO_CFG output is |(automute[CHx])
[4]	GPIO_AND_SS_RAMP	Sets the GPIO_CFG "Soft Ramp Done" flag output as the bitwise AND of both channel's flags. • 1'b0: Disabled • 1'b1: Enabled, GPIO_CFG output is &(ss_full_ramp[CHx]) (default) Note: Overridden by GPIO_OR_SS_RAMP.
[3]	GPIO_AND_VOL_MIN	Sets the GPIO_CFG "Minimum Volume" flag output as the bitwise AND of both channel's flags. • 1'b0: Disabled • 1'b1: Enabled, GPIO_CFG output is &(vol_min[CHx]) (default) Note: Overridden by GPIO_OR_VOL_MIN.
[2]	GPIO_AND_AUTOMUTE	Sets the GPIO_CFG "Automute Status" output as the bitwise AND of both channel's statuses. • 1'b0: Disabled • 1'b1: Enabled, GPIO_CFG output is &(automute[CHx]) (default) Note: Overridden by GPIO_OR_AUTOMUTE.
[1]	RESERVED	NA
[0]	GPIO1_READ	• 1'b0: GPIO1 Readback disabled (default) • 1'b1: Allow readback of GPIO1_I

Register 26: GPIO INPUT ENABLE

Bits	[7:2]	[1]	[0]
Default	5'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:2]	RESERVED	NA
[1]	GPIO_AMP_MODE	When any GPIO_CFG is set to 6 (input system mode control): • 1'b0: Power down when GPIO input is 1 (default) • 1'b1: HiFi when GPIO input is 1 (when GPIO input is 0, system mode is determined by register AMP_MODE (Reg 0[1]))
[0]	GPIO_SEL	Outputs a specific channel's flag if the corresponding GPIO_AND and GPIO_OR are not set. • 1'b0: Outputs status/flag from CH1 • 1'b1: Outputs status/flag from CH2

Register 27: PWM1 COUNT

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	PWM1_COUNT	8-bit value to set the number of SYS_CLK periods the PWM signal is high for. • 8'd0: Disabled (default) • 8'd1: Minimum • 8'd255: Maximum

Register 29-28: PWM1 FREQUENCY

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	PWM1_FREQ	16-bit value to set the frequency of the PWM signal in terms of SYS_CLK divisions. • 16'h0000: Disabled (default) • 16'h0001: Minimum • 16'hFFFF: Maximum $frequency[Hz] = SYS\_CLK/(PWM1\_FREQ + 1)$ $DutyCycle[\%] = \left(PWM1\_COUNT/(PWM1\_FREQ + 1)\right) \times 100$

Register 30: PWM2 COUNT

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	PWM2_COUNT	8-bit value to set the number of SYS_CLK periods the PWM signal is high for. • 8'd0: Disabled (default) • 8'd1: Minimum • 8'd255: Maximum

Register 32-31: PWM2 FREQUENCY

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	PWM2_FREQ	16-bit value to set the frequency of the PWM signal in terms of SYS_CLK divisions. • 16'h0000: Disabled (default) • 16'h0001: Minimum • 16'hFFFF: Maximum $frequency[Hz] = SYS\_CLK/(PWM2\_FREQ + 1)$ $DutyCycle[\%] = \left(PWM2\_COUNT/(PWM2\_FREQ + 1)\right) \times 100$

Register 33: PWM3 COUNT

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	PWM3_COUNT	8-bit value to set the number of SYS_CLK periods the PWM signal is high for. • 8'd0: Disabled (default) • 8'd1: Minimum • 8'd255: Maximum

Register 35-34: PWM3 FREQUENCY

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	PWM3_FREQ	16-bit value to set the frequency of the PWM signal in terms of SYS_CLK divisions. • 16'h0000: Disabled (default) • 16'h0001: Minimum • 16'hFFFF: Maximum $frequency[Hz] = SYS\_CLK/(PWM3\_FREQ + 1)$ $DutyCycle[\%] = \left(PWM3\_COUNT/(PWM3\_FREQ + 1)\right) \times 100$

DAC Registers

Register 36: INPUT CONFIG

Bits	[7]	[6]	[5]	[4]	[3]	[2:1]	[0]
Default	1'b1	1'b0	1'b0	1'b0	1'b0	2'd0	1'b0

Bits	Mnemonic	Description
[7]	AUTO_FS_DETECT	Enables automatic tuning of CLK_DAC/CLK_IDAC ratio according to detected FS. • 1'b0: Auto tune Disabled • 1'b1: Auto tune CLK_DAC/CLK_IDAC ratio according to detected FS (default) Note: Functional for TDM, I²S, and DoP only
[6]	DSD_NEGEDGE	Changes DSD latching edge polarity. • 1'b0: Latch DSD data at positive edge of DSD_CLK (default) • 1'b1: Latch DSD data at negative edge of DSD_CLK
[5]	DSD_MASTER_MODE	DSD master mode config. • 1'b0: DSD slave mode (default) • 1'b1: DSD master mode. DSD_CLK outputs from DATA_CLK
[4]	ENABLE_MASTER_MODE	TDM master mode config. • 1'b0: TDM slave mode (default) • 1'b1: TDM master mode enabled. Master BCK and WS output from DATA_CLK and DATA1
[3]	RESERVED	NA
[2:1]	INPUT_SEL	Selects input data when AUTO_INPUT_SELECT is set to 2'd0. • 2'd0: TDM (default) • 2'd1: DSD • 2'd2: DoP • 2'd3: Reserved
[0]	AUTO_INPUT_SELECT	Auto input data selection config. • 1'b0: Disables auto input select. Input data type is set by INPUT_SEL (default) • 1'b1: Auto select between DSD and TDM inputs.

Register 37: MASTER MODE CONFIG

Bits	[7]	[6]	[5]	[4:3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	2'd0	1'b0	1'b0	1'b1

Bits	Mnemonic	Description
[7]	AUTO_FS_DETECT_BLOCK_64FS MODE	Automatic 64FS mode enable. • 1'b0: Set 64FS mode when the detected CLK_DAC/CLK_IDAC ratio is 64 (default) • 1'b1: Do not set 64FS mode when the detected CLK_DAC/CLK_IDAC ratio is 64
[6]	MASTER_BCK_DIV1	When enabled, master BCK is 128fs clock. Otherwise, BCK is less than or equal to 64fs. • 1'b0: BCK is not 128fs clock (default) • 1'b1: BCK is 128fs clock
[5]	MASTER_WS_IDLE	Sets the value of master WS when WS is idle. • 1'b0: WS is 0 when idle (default) • 1'b1: WS is 1 when idle
[4:3]	MASTER_FRAME_LENGTH	Selects the bit length in each TDM channel in master mode. • 2'd0: 32-bit (default) • 2'd2: 16-bit • others: Reserved
[2]	MASTER_WS_PULSE_MODE	When enabled, master WS is a pulse signal instead of a 50% duty cycle signal. The pulse width is 1 BCK cycle. • 1'b0: 50% duty cycle WS signal (default) • 1'b1: Pulse WS signal
[1]	MASTER_WS_INVERT	Inverts master WS. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[0]	MASTER_BCK_INVERT	Inverts master BCK or DSD_CLK. • 1'b0: Non-inverted • 1'b1: Inverted (default)

Register 38: TDM CONFIG1

Bits	[7]	[6:4]	[3:0]
Default	1'b0	3'd0	4'd1

Bits	Mnemonic	Description
[7]	TDM_RESYNC	Force TDM encoder & decoder to resync. • 1'b0: Enable TDM codec synchronization (default) • 1'b1: Force TDM codec to desynchronize.
[6:4]	MASTER_WS_SCALE	In TDM master mode, tunes master BCK/WS ratio by scaling master WS. It allows more TDM slots in a fixed frame. • 3'd0: No scale (default) • 3'd1: Scale down WS by 2 • 3'd2: Scale down WS by 4 • 3'd3: Scale down WS by 8 • 3'd4: Scale down WS by 16 • others: Reserved
[3:0]	TDM_CH_NUM	Total TDM slot number per frame = TDM_CH_NUM + 1. • 4'd0: Minimum • 4'd1: Default • 4'd15: Maximum

Register 39: TDM CONFIG2

Bits	[7]	[6]	[5:0]
Default	1'b0	1'b0	6'd1

Bits	Mnemonic	Description
[7]	TDM_LJ_MODE	TDM LJ mode. • 1'b0: Standard I²S (default) • 1'b1: LJ mode
[6]	TDM_VALID_EDGE	TDM WS valid edge. • 1'b0: negative edge (default) • 1'b1: positive edge
[5:0]	TDM_VALID_PULSE_LEN	Data valid pulse length adjustment. • 6'd1: Default

Register 40: TDM CONFIG3

Bits	[7]	[6:5]	[4:0]
Default	1'd0	2'd0	5'd0

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6:5]	TDM_BIT_WIDTH	Bit width of each TDM slot. • 2'b00: 32-bit (default) • 2'b01: 24-bit • 2'b10: 16-bit • 2'b11: Reserved
[4:0]	TDM_DATA_LATCH_ADJ	Adjusts the position of the start bit within each TDM slot by TDM_DATA_LATCH_ADJ clock cycles. • 5'd0: Normal position • 5'd1-31: Number of clock cycles to wait Note: Functionality does not work in LJ mode (TDM_LJ = 1'b1).

Register 41: RESERVED

Register 42: TDM SLOT CONFIG

Bits	[7:4]	[3:0]
Default	4'd1	4'd0

Bits	Mnemonic	Description
[7:4]	TDM_CH2_SLOT_SEL	CH2 data slot selection. CH2 receives data from Mth slot. M = TDM_CH2_SLOT_SEL + 1. • 4'd0: Minimum (M=1) • 4'd15: Maximum (M=16)
[3:0]	TDM_CH1_SLOT_SEL	CH1 data slot selection. CH1 receives data from Mth slot. M = TDM_CH1_SLOT_SEL + 1. • 4'd0: Minimum (M=1) • 4'd15: Maximum (M=16)

Register 43: RESERVED

Register 44: RESYNC CONFIG

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b1	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6]	CP_PDB_ON_MUTE	Charge pump state control when mute • 1'b0: Keep charge pump on when mute • 1'b1: Turn off charge pump when mute (default)
[5]	RESERVED	NA
[4]	SYNC_DAC_ICG	Resets the 128*FS clock divider. • 1'b0: Disabled (default) • 1'b1: Reset on every negedge of WS Note: Reset this before any of the other resync bits.
[3]	DOP_CLK_RESYNC	Resets the DoP clock generator. • 1'b0: Disabled (default) • 1'b1: Reset on every negedge of WS
[2]	VOL_THD_RESYNC	Resets Volume/THD block. • 1'b0: Disabled (default) • 1'b1: Reset on every negedge of WS
[1]	FIR_RESYNC	Reset the FIR filters. • 1'b0: Disabled (default) • 1'b1: Reset on every negedge of WS
[0]	FS_RESYNC	Resets the FS clock generator. • 1'b0: Disabled (default) • 1'b1: Reset on every negedge of WS

Register 45: FS GENERATOR PHASE

Bits	[7]	[6:0]
Default	1'b1	7'd64

Bits	Mnemonic	Description
[7]	DSD_2DB_DOWN	Scale down DSD data by 2dB to match PCM data. • 1'b0: No scaling • 1'b1: Scaled down (default)
[6:0]	RESERVED	NA

Register 46: VOLUME1

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME1	DAC CH1 volume. -0dB to -127.5dB 0.5dB steps. • 8'd0: 0dB • 8'd255: -127.5dB

Register 47: VOLUME2

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME2	DAC CH2 volume. -0dB to -127.5dB 0.5dB steps. • 8'd0: 0dB • 8'd255: -127.5dB

Register 48: DAC VOL UP RATE

Bits	[7:0]
Default	8'h96

Bits	Mnemonic	Description
[7:0]	DAC_VOL_RATE_UP	Value by which the old VOLUME value is incremented to reach the new VOLUME value. • 8'h00: Instant change • 8'h00: Slowest change • 8'h96: Default • 8'hFF: Fastest change $rate[s] = 2^14/(DAC\_VOL\_RATE\_UP * FS)$

Register 49: DAC VOL DOWN RATE

Bits	[7:0]
Default	8'h96

Bits	Mnemonic	Description
[7:0]	DAC_VOL_RATE_DOWN	Value by which the old VOLUME value is incremented to reach the new VOLUME value. • 8'h00: Instant change • 8'h00: Slowest change • 8'h96: Default • 8'hFF: Fastest change $rate[s] = 2^14/(DAC\_VOL\_RATE\_DOWN * FS)$

Register 50: DAC VOL DOWN RATE FAST

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	DAC_VOL_RATE_FAST	Value by which the old VOLUME value is incremented to reach the new VOLUME value. Only used during abnormal mute (PLL unlock or BCK_WS ratio failed) • 8'h00: Instant change (default) • 8'h01: Slowest change • 8'hFF: Fastest change $rate[s] = 2^14/(DAC\_VOL\_RATE\_FAST * FS)$

Register 51: MUTE CTRL

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	FORCE_VOLUME	Volume update control. • 1'b0: Volume updates after toggling RUN_VOLUME (default) • 1'b1: Volume updates after register is changed
[6]	DAC_USE_MONO_VOLUME	Defines how volume is controlled between channels. • 1'b0: Separated volume control (default) • 1'b1: Ch2 volume shares Ch1 volume setting
[5]	RUN_VOLUME	Toggle RUN_VOLUME to update volumes set by VOLUME1 & VOLUME2 • 1'b0: Disabled (default) • 1'b1: Enabled
[4]	RESERVED	NA
[3]	DAC_INVERT_CH2	Invert the output on Ch2 at the input to the NSMOD. • 1'b0: Disabled (default) • 1'b1: Enabled
[2]	DAC_INVERT_CH1	Invert the output on Ch1 at the input to the NSMOD. • 1'b0: Disabled (default) • 1'b1: Enabled
[1]	DAC_MUTE_CH2	DAC channel 2 mute control. • 1'b0: Normal operation (default) • 1'b1: Mute ch2
[0]	DAC_MUTE_CH1	DAC channel 1 mute control. • 1'b0: Normal operation (default) • 1'b1: Mute ch1

Register 52: FILTER CONFIG

Bits	[7]	[6]	[5]	[4:3]	[2:0]
Default	1'b0	1'b1	1'b0	2'b01	3'd0

Bits	Mnemonic	Description
[7]	AUTO_CH_DETECT	Auto detect BCK/FRAME ratio to determine the number of TDM channels. • 1'b0: Disabled (default) • 1'b1: Enabled
[6]	BYPASS_DEEMPH	De-emphasis filter control for ch1/2 only. • 1'b0: Enabled • 1'b1: Disables de-emphasis filters (default)
[5]	PEAK_FILTER	DRE peak filter control. • 1'b0: Disabled (default) • 1'b1: Enabled
[4:3]	SEL_DEEMPH	Configures the de-emphasis filters for various sample rate. • 2'b00: FS=32kHz • 2'b01: FS=44.1kHz (default) • 2'b10: FS=48kHz • 2'b11: Reserved
[2:0]	FILTER_SHAPE	Selects the 8x interpolation FIR filter shape. • 3'd0: Minimum phase (default) • 3'd1: Linear phase apodizing • 3'd2: Linear phase fast roll-off • 3'd3: Linear phase fast roll-off low ripple • 3'd4: Linear phase slow roll-off • 3'd5: Minimum phase fast roll-off • 3'd6: Minimum phase slow roll-off • 3'd7: Minimum phase slow roll-off low dispersion

Register 54-53: RESERVED

Register 56-55: THD COMP C2 CH1

Bits	[15:0]
Default	16'd360

Bits	Mnemonic	Description
[15:0]	THD_C2_CH1	A 16-bit signed coefficient for correcting for the CH1 second harmonic distortion. $output = x + c2 * x^2 + c3 * x^3$

Register 58-57: THD COMP C3 CH1

Bits	[15:0]
Default	16'd141

Bits	Mnemonic	Description
[15:0]	THD_C3_CH1	A 16-bit signed coefficient for correcting for the CH1 third harmonic distortion. $output = x + c2 * x^2 + c3 * x^3$

Register 60-59: THD COMP C2 CH2

Bits	[15:0]
Default	16'd360

Bits	Mnemonic	Description
[15:0]	THD_C2_CH2	A 16-bit signed coefficient for correcting for the CH2 second harmonic distortion. $output = x + c2 * x^2 + c3 * x^3$

Register 62-61: THD COMP C3 CH2

Bits	[15:0]
Default	16'd141

Bits	Mnemonic	Description
[15:0]	THD_C3_CH2	A 16-bit signed coefficient for correcting for the CH2 third harmonic distortion. $output = x + c2 * x^2 + c3 * x^3$

Register 64-63: AUTOMUTE TIME

Bits	[15]	[14]	[13]	[12]	[11]	[10:0]
Default	1'b1	1'b1	1'b0	1'b1	1'b1	11'd15

Bits	Mnemonic	Description
[15]	AUTOMUTE_RAMP_TO_GROUND	When ramped to minimum volume during normal mute, allow soft ramp to ground for power saving. • 1'b0: Disabled • 1'b1: Enabled (default) Note: Normal mute includes automute, mute by register and mute by GPIO.
[14]	AUTOMUTE_WAIT_ON_DRE	Automute flag control. • 1'b0: Automute is flagged when automute condition is met • 1'b1: Automute is flagged when automute condition is met and DRE is engaged (default)
[13]	RESERVED	NA
[12]	AUTOMUTE_EN_CH2	Channel 2 automute. • 1'b0: Disables ch2 automute • 1'b1: Enables ch2 automute (default) Note: Automute is available for PCM only
[11]	AUTOMUTE_EN_CH1	Channel 1 automute. • 1'b0: Disables ch1 automute • 1'b1: Enables ch1 automute (default) Note: Automute is available for PCM only
[10:0]	AUTOMUTE_TIME	Configures the amount of time in seconds the audio must remain below AUTOMUTE_LEVEL before an automute condition is flagged. • 11'h000: Disabled • 11'h001: Slowest • 11'h00F: Default • 11'h7FF: Fastest $Time[s] = 2^18/(AUTOMUTE\_TIME * FS)$

Register 66-65: AUTOMUTE LEVEL

Bits	[15:0]
Default	16'd8

Bits	Mnemonic	Description
[15:0]	AUTOMUTE_LEVEL	Configures the threshold which the audio must be below before an automute condition is flagged. • 16'h0001: Minimum (-132dB) • 16'hFFFF: Maximum (-42dB) Note: this register works in tandem with AUTOMUTE_TIME to create the automute condition

Register 68-67: AUTOMUTE OFF LEVEL

Bits	[15:0]
Default	16'd10

Bits	Mnemonic	Description
[15:0]	AUTOMUTE_OFF_LEVEL	The threshold which the audio must be above before the automute condition is immediately cleared. Shift right 1 bit corresponds to -6dB. • 16'h0001: Minimum (-132dB) • 16'hFFFF: Maximum (-42dB)

Register 69: SOFT RAMP CONFIG

Bits	[7]	[6]	[5]	[4:0]
Default	1'b0	1'b0	1'b0	5'd2

Bits	Mnemonic	Description
[7]	GAIN_18DB_CH2	Applies +18dB digital gain on channel 2. • 1'b0: Disabled (default) • 1'b1: Enabled
[6]	GAIN_18DB_CH1	Applies +18dB digital gain on channel 1. • 1'b0: Disabled (default) • 1'b1: Enabled
[5]	SOFT_RAMP_TYPE	Sets whether the soft start ramp is linear or quadratic. • 1'b0: Uses a quadratic function for the soft start ramp (default) • 1'b1: Uses the standard soft start ramp
[4:0]	SOFT_RAMP_TIME	Sets the amount of time that it takes to perform a soft start ramp. This time affects both ramp to ground and ramp to AVCC/2. • 5'd00: Minimum • 5'd02: Default • 5'd20: Maximum

Register 72-70: RESERVED

Register 73: DRE CONFIG

Bits	[7]	[6]	[5:2]	[1]	[0]
Default	1'b1	1'b1	4'b0000	1'b1	1'b1

Bits	Mnemonic	Description
[7]	DRE_ZC_CH2	Removes the signal zero cross requirement for DRE transitions. Thresholds are still required. • 1'b0: Requires signal zero cross for DRE transition • 1'b1: Bypass signal zero cross requirement (default)
[6]	DRE_ZC_CH1	Removes the signal zero cross requirement for DRE transitions. Thresholds are still required. • 1'b0: Requires signal zero cross for DRE transition • 1'b1: Bypass signal zero cross requirement (default)
[5:2]	RESERVED	NA
[1]	DRE_ATR_EN	Control the Analog THD Removal when DRE enabled • 1'b0: DRE does not control ATR • 1'b1: DRE does control ATR (default)
[0]	DRE_GAIN_EN	DRE gain enable • 1'b0: DRE does not control analog gain • 1'b1: DRE controls analog gain (default)

Register 75-74: DRE GAIN CH1

Bits	[15:0]
Default	16'h1A34

Bits	Mnemonic	Description
[15:0]	DRE_GAIN1	Sets the DRE gain for CH1. Shift right 1 bit corresponds to -6dB. • 16'h07FF (0dB): Minimum • 16'h1A34 (16.33dB): Default • 16'h7FFF (30dB): Maximum

Register 77-76: DRE GAIN CH2

Bits	[15:0]
Default	16'h1A34

Bits	Mnemonic	Description
[15:0]	DRE_GAIN2	Sets the DRE gain for CH2. Shift right 1 bit corresponds to -6dB. • 16'h07FF (0dB): Minimum • 16'h1A34 (16.33dB): Default • 16'h7FFF (30dB): Maximum

Register 79-78: DRE ON THRESHOLD

Bits	[15:0]
Default	16'h0CF1

Bits	Mnemonic	Description
[15:0]	DRE_ON_THRESH	DRE on threshold. Shift right 1 bit corresponds to -6dB. • 16'h0CF1 (-28dB): Default • 16'hFFFF (-24dB): Maximum

Register 81-80: DRE OFF THRESHOLD

Bits	[15:0]
Default	16'h8184

Bits	Mnemonic	Description
[15:0]	DRE_OFF_THRESH	DRE off threshold. Shift right 1 bit corresponds to -6dB. • 16'h818F (-48dB): Default • 16'hFFFF (-24dB): Maximum

Register 82: DRE DECAY RATE

Bits	[7]	[6]	[5]	[4:0]
Default	1'b1	1'b0	1'b1	5'd15

Bits	Mnemonic	Description
[7]	DRE_ZC_LEVEL	Determines the functionality of DRE_ZC_CHx • 1'b0: Posedge of DRE_ZC_CHx acts as a single use zc_detect bypass, signal level must be past the threshold • 1'b1: DRE_ZC_CHx acts as a zc_detect bypass (default)
[6]	RESERVED	NA
[5]	MIN_PEAK	DRE peak detector starting point control. • 1'b0: DRE peak detector starts from max • 1'b1: DRE peak detector starts from min (default)
[4:0]	DRE_DECAY_RATE	Sets the speed at which the stored value of the DRE peak detector will decay when the input signal is below the stored value. • 5'd31: slowest decay • 5'd0: instant decay

Register 84-83: DC OFFSET CH1

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	DC_OFFSET1	DC offset for CH1. $V\_offset = (DC\_OFFSET1)/(2^{24} - 1) * Vref$

Register 86-85: DC OFFSET CH2

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	DC_OFFSET2	DC offset for CH2. $V\_offset = (DC\_OFFSET2)/(2^{24} - 1) * Vref$

Register 87: DC RAMP RATE

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	DC_RAMP_RATE	Value by which the old DC value is incremented/decremented per sample to reach the new DC value. • 8'd0: Instant (default) • 8'd1: Slowest • 8d'255: Fastest

Register 88: MASTER TRIM

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	MASTER_TRIM	Master trim volume. unsigned, range 0dB(8'hFF) to -42dB(8'h01), 0 is bypass. • 8'h00: Bypass (default) • 8'h01 (-42dB): Minimum • 8'hFF (0dB): Maximum

PLL Registers

Register 192: RESET & PLL REGISTER1

Bits	[7]	[6]	[5:3]	[2]	[1]	[0]
Default	1'b0	1'b0	3'b000	1'b0	1'b0	1'b1

Bits	Mnemonic	Description
[7]	AO_SOFT_RESET	Performs soft reset to Slave Registers. • 1'b0: Disabled (default) • 1'b1: Enabled
[6]	PLL_SOFT_RESET	Performs soft reset to Synchronous Slave Registers. • 1'b0: Disabled (default) • 1'b1: Enabled
[5:3]	PLL_VCO_CMP_ISET	Selects current of the VCO comparator. • Must set to 3'b110, for normal operation
[2]	RESERVED	NA
[1]	GPIO1_SDB_SYNC	Configures GPIO1_SDB (Shutdown_b). When SYS_CLK is provided through GPIO1, set this bit to '1' to allow SYS_CLK input. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	PLL_CLKHV_PHASE	Digital/analog DAC clock phase control. • 1'b0: Digital/analog DAC clocks have inverted phase • 1'b1: Digital/analog DAC clocks have the same phase (default)

Register 193: PLL REGISTER2

Bits	[7]	[6]	[5]	[4:2]	[1]	[0]
Default	1'b0	1'b0	1'b0	2'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	PLL_BYP	PLL bypass mode. • 1'b0: Disabled (default) • 1'b1: Enabled
[6]	DVDD_SHUNTB	Enables digital regulator output shunt to ground (10k). Active low. • 1'b0: Enabled (default) • 1'b1: Disabled
[5]	SEL_1V_DREG	Sets digital regulator output voltage to 1V. • 1'b0: Disabled (default) • 1'b1: Enabled
[4:2]	PLL_HVREG_VREF_SEL	PLL HVREG reference voltage selection • 3'b001: 1.6V (optimum setting, normal operation) • Others: Reserved
[1]	SEL_PLL_IN	Selects PLL input clock sources. • 1'b0: MCLK (default) • 1'b1: BCK
[0]	EN_PLL_CLKIN	Controls PLL input clocks. • 1'b0: Disables PLL input clocks (default) • 1'b1: Enables PLL input clocks

Register 194: PLL REGISTER3

Bits	[7:3]	[2]	[1:0]
Default	5'd0	1'b0	2'b00

Bits	Mnemonic	Description
[7:3]	RESERVED	NA
[2]	AUTO_LOCK_EN	Allows PLL to relock when PLL lock is lost and there are 256 valid PLL input clock cycles. • 1'b0: Disabled (default) • 1'b1: Enabled
[1:0]	RESERVED	NA

Register 195: PLL REGISTER4

Bits	[7:5]	[4:3]	[2]	[1]	[0]
Default	3'd0	2'b00	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:5]	PLL_CP_BIAS_SEL	Sets the Charge Pump Bias current: • 3'b011: 4uA (optimum setting, for normal operation)
[4:3]	PLL_ID_SEL	Sets the PLL Internal Delay: • 2'b11: 1.5nS (optimum setting, for normal operation) Note: Fixed to 1.5nS, no other possible cases
[2]	PLL_VCO_FMAX	Disables the VCO's FMAX-limiting • 1'b0: Limit is set (default) • 1'b1: No limit (for normal operation)
[1]	PLL_VCO_PDB	Enables/disables the PLL voltage-controlled oscillator (VCO). • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	PLL_CP_PDB	Enables/disables the PLL charge pump. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 196: PLL REGISTER5

Bits	[7:5]	[4:2]	[1:0]
Default	3'd0	3'd0	2'd0

Bits	Mnemonic	Description
[7:5]	PLL_VCO_BAND_CTRL	Selects the frequency band of the VCO. • 3'b011 (for optimum operation)
[4:2]	RESERVED	NA
[1:0]	PLL_VCO_IB_AMP_CTRL	Selects the V to I Amplifier's bias current: • 2'b10 (for optimum operation)

Register 199-197: PLL REGISTER6

Bits	[23:0]
Default	24'd0

Bits	Mnemonic	Description
[23:0]	PLL_CLK_FB_DIV	Sets the PLL clock feedback divider. • 24'd0: Reserved • 24'dn: Divide by (2^25)/n

Register 202-200: PLL REGISTER7

Bits	[23]	[22]	[21:20]	[19]	[18]	[17:14]	[13:10]	[9:1]	[0]
Default	1'b0	1'b0	2'b00	1'b0	1'b0	4'd0	4'd0	9'd0	1'b0

Bits	Mnemonic	Description
[23]	PLL_REG_PDB_HV	Power Down the regulators. • 1'b0: Disable the PLL HV-regulator (default) • 1'b1: Enable the PLL HV-regulator
[22]	PLL_REG_PDB_1V2	Power Down the regulators. • 1'b0: Disable the PLL 1V2-regulator (default) • 1'b1: Enable the PLL 1V2-regulator
[21:20]	RESERVED	NA
[19]	PLL_LOW_BW	PLL low bandwidth mode. • 1'b0: Disabled (default) • 1'b1: Enabled (for normal operation, optimum setting)
[18]	PLL_CLK_OUT_DIV_PHASE_EN	• 1'b0: Disabled (default) • 1'b1: Tune the PLL clock output divider phase according to PLL_CLK_OUT_DIV_PHASE
[17:14]	PLL_CLK_OUT_DIV_PHASE	Sets the PLL clock output divider phase
[13:10]	PLL_CLK_OUT_DIV	Sets the Output Division (No) of the PLL. • 4'd0: Reserved • 4'dn: Divide by n+1
[9:1]	PLL_CLK_IN_DIV	Sets the Input Division (Ni) of the PLL. • 9'd0: Reserved • 9'dn: Divide by n+1
[0]	PLL_FB_DIV_LOAD	Writes 1 then write 0 to load CLK_FB_DIV.

Register 203: PLL REGISTER8

Bits	[7:6]	[5]	[4]	[3:0]
Default	2'b00	1'b0	1'b0	4'b0000

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5]	PLL_DIG_RSTB	Resets the Digital core of the PLL. • 1'b0: PLL digital core is off (default) • 1'b1: PLL digital core is on
[4]	PLL_VCO_DIODE_EN	Enables/disables the diode for upper-limiting for VCO frequency. The diode is disconnected by default, to allow proper functioning of the FMAX-Limiter. • 1'b0: Diode is disconnected (default) • 1'b1: Diode is connected
[3:0]	RESERVED	NA

Read Only Registers

Register 224: RESERVED

Register 225: CHIP ID READ

Bits	[7:0]
Default	8'h69

Bits	Mnemonic	Description
[7:0]	CHIP_ID	CHIP ID. • ES9033: 0x69

Register 228-226: RESERVED

Register 230-229: INTERRUPT STATE

Bits	[15:14]	[13]	[12]	[11]	[10]	[9]	[8]	[7:6]	[5]	[4]	[3:2]	[1:0]
Default	-	-	-	-	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[15:14]	INPUT_SELECT_OVERRIDE_STATE	
[13]	TDM_DATA_VALID_STATE	
[12]	CLK_AVALID_STATE	
[11]	RWS_REF_CNT_FULL_STATE	
[10]	BCK_WS_FAIL_STATE	
[9]	PLL_LOCKED_STATE	
[8]	DOP_VALID_STATE	
[7:6]	SS_FULL_RAMP_STATE	
[5]	DRE_SELECT2_STATE	
[4]	DRE_SELECT1_STATE	
[3:2]	AUTOMUTE_STATE	
[1:0]	VOL_MIN_STATE	

Register 232-231: INTERRUPT SOURCE

Bits	[15:14]	[13]	[12]	[11]	[10]	[9]	[8]	[7:6]	[5]	[4]	[3:2]	[1:0]
Default	-	-	-	-	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[15:14]	INPUT_SELECT_OVERRIDE_SOURCE	
[13]	TDM_DATA_VALID_SOURCE	
[12]	CLK_AVALID_SOURCE	
[11]	RWS_REF_CNT_FULL_SOURCE	
[10]	BCK_WS_FAIL_SOURCE	
[9]	PLL_LOCKED_SOURCE	
[8]	DOP_VALID_SOURCE	
[7:6]	SS_FULL_RAMP_SOURCE	
[5]	DRE_SELECT2_SOURCE	
[4]	DRE_SELECT1_SOURCE	
[3:2]	AUTOMUTE_SOURCE	
[1:0]	VOL_MIN_SOURCE	

Register 238-233: RESERVED

Register 239: AUTO TUNING READ

Bits	[7]	[6]	[5:0]
Default	-	-	-

Bits	Mnemonic	Description
[7]	RATIO_VALID	Indicates the CLK_DAC/CLK_IDAC ratio is valid (N or N.5) • 1'b0: Invalid • 1'b1: Valid
[6]	IDAC_DIV_HALF_REG	Result of auto FS tuning divider for IDAC_HALF flag
[5:0]	IDAC_DIV_REG	Result of auto FS tuning divider for CLK_DAC/CLK_IDAC ratio

Register 240: GPIO READ

Bits	[7:1]	[0]
Default	-	-

Bits	Mnemonic	Description
[7:1]	RESERVED	NA
[0]	GPIO1_I_READ	GPIO1 input readback. • 1’b0: Low • 1’b1: High

Register 241: DAC STATUS READ

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	SS_RAMP_DOWN_CH2	Channel 2 soft ramped down flag readback. • 1'b0: Soft ramp down not detected on channel 2 • 1'b1: Soft ramp down detected on channel 2
[6]	SS_RAMP_DOWN_CH1	Channel 1 soft ramped down flag readback. • 1'b0: Soft ramp down not detected on channel 1 • 1'b1: Soft ramp down detected on channel 1
[5]	SS_RAMP_UP_CH2	Channel 2 soft ramped up flag readback. • 1'b0: Soft ramp up not detected on channel 2 • 1'b1: Soft ramp up detected on channel 2
[4]	SS_RAMP_UP_CH1	Channel 1 soft ramped up flag readback. • 1'b0: Soft ramp up not detected on channel 1 • 1'b1: Soft ramp up detected on channel 1
[3]	AUTOMUTE_CH2	Channel 2 automute status readback. • 1'b0: Automute not detected on channel 2 • 1'b1: Automute detected on channel 2
[2]	AUTOMUTE_CH1	Channel 1 automute status readback. • 1'b0: Automute not detected on channel 1 • 1'b1: Automute detected on channel 1
[1]	VOL_MIN_CH2	Channel 2 minimum volume flag readback. • 1'b0: Minimum volume not detected on channel 2 • 1'b1: Minimum volume detected on channel 2
[0]	VOL_MIN_CH1	Channel 1 minimum volume flag readback. • 1'b0: Minimum volume not detected on channel 1 • 1'b1: Maximum volume detected on channel 1

Register 242: DRE STATUS READ

Bits	[7]	[6]	[5:4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	TDM_DATA_VALID	TDM data valid flag • 1'b0: TDM data Not valid • 1'b1: TDM data Valid
[6]	DOP_VALID	DoP valid flag • 1'b0: Not Invalid • 1'b1: Valid
[5:4]	RESERVED	NA
[3]	DRE_DETECT_CH2	Channel 2 DRE detection status. • 1'b0: DRE not detected on channel 2 • 1'b1: DRE detected on channel 2
[2]	DRE_DETECT_CH1	Channel 1 DRE detection status. • 1'b0: DRE not detected on channel 1 • 1'b1: DRE detected on channel 1
[1]	DRE_SELECT_CH2	Channel 2 DRE engage status. • 1'b0: DRE not engaged on channel 2 • 1'b1: DRE engaged on channel 2
[0]	DRE_SELECT_CH1	Channel 1 DRE engage status. • 1'b0: DRE not engaged on channel 1 • 1'b1: DRE engaged on channel 1

Reference Schematic

Hardware Mode

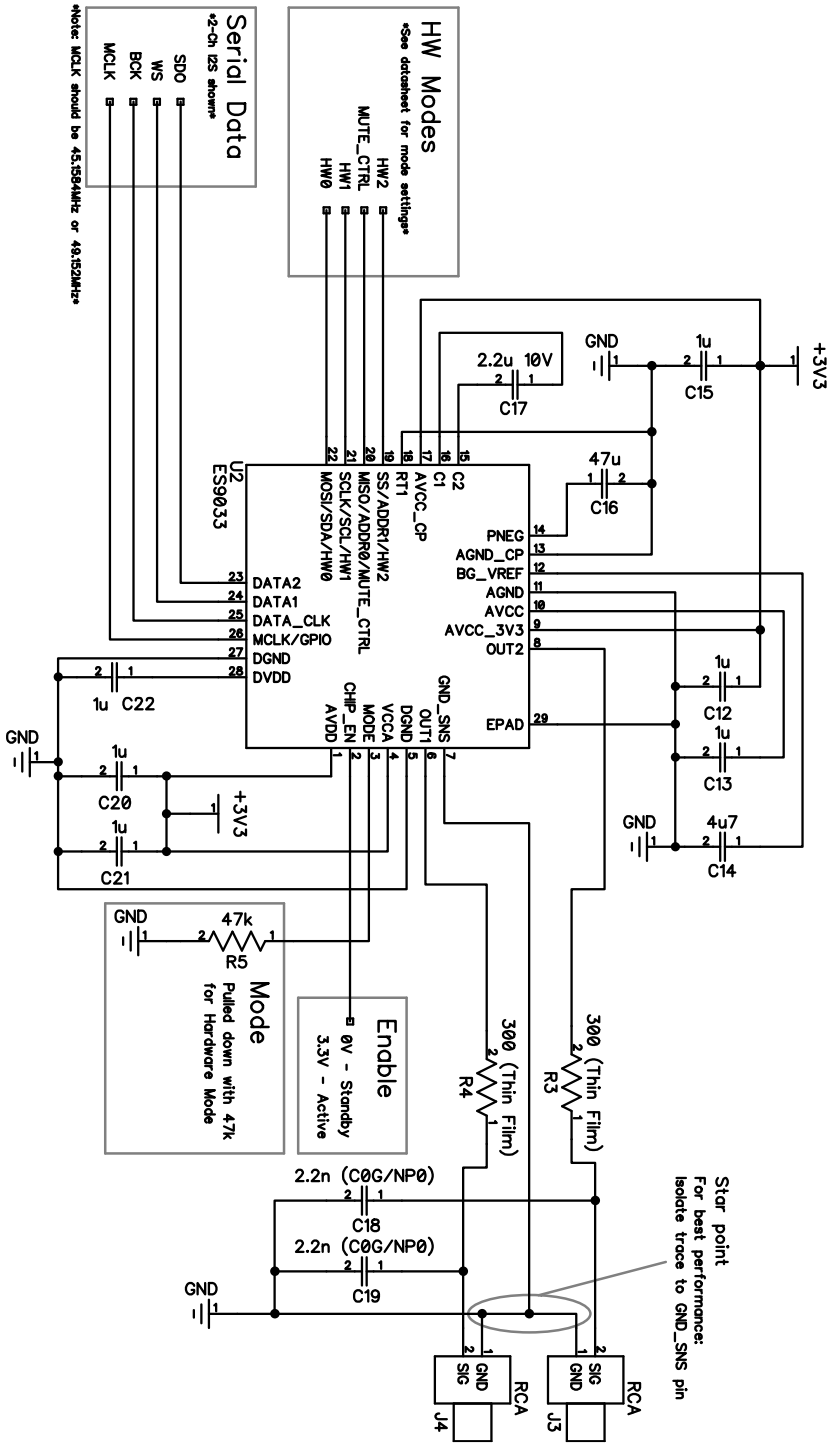


Figure 17 - Hardware Mode Reference Schematic

Software Mode

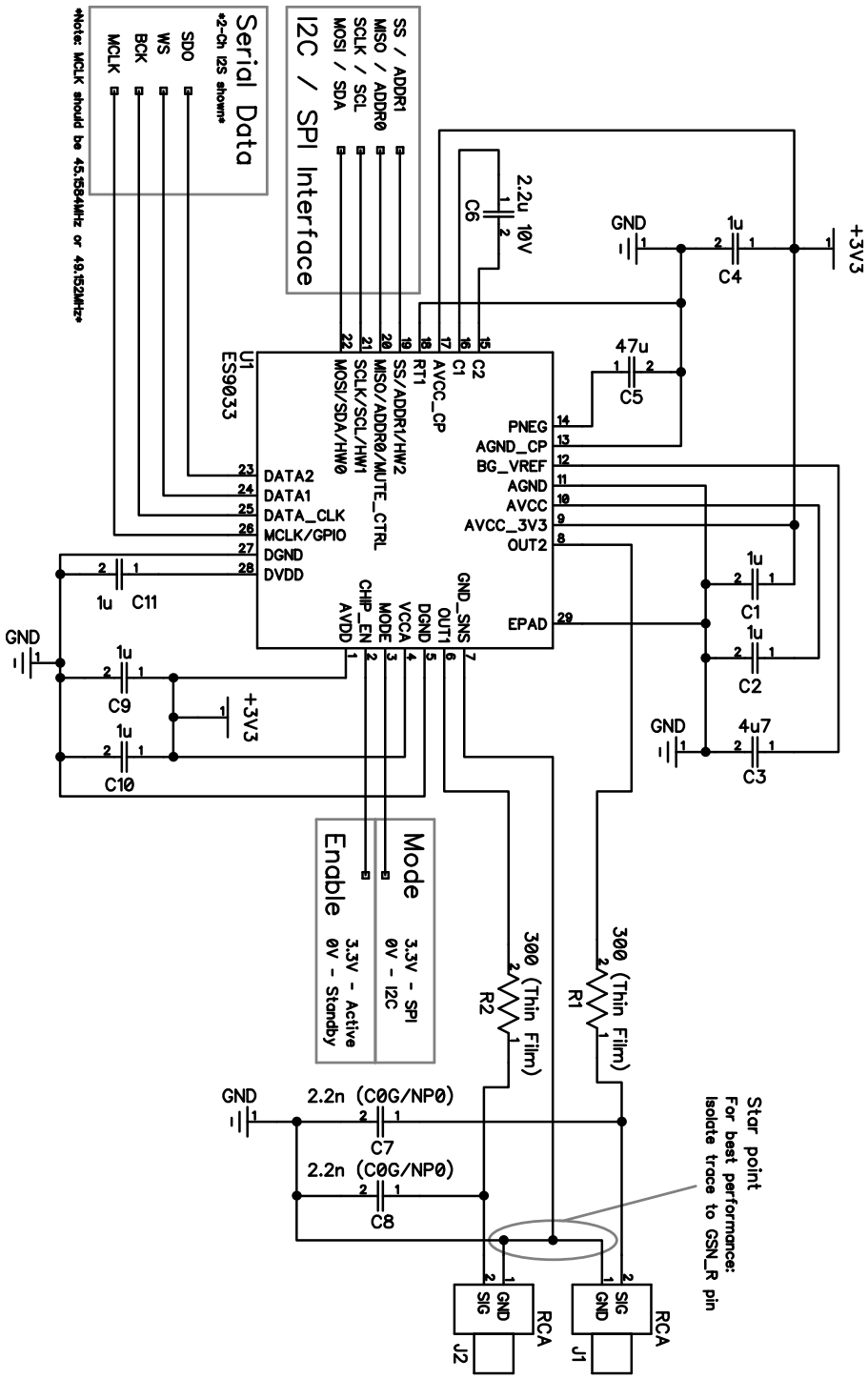
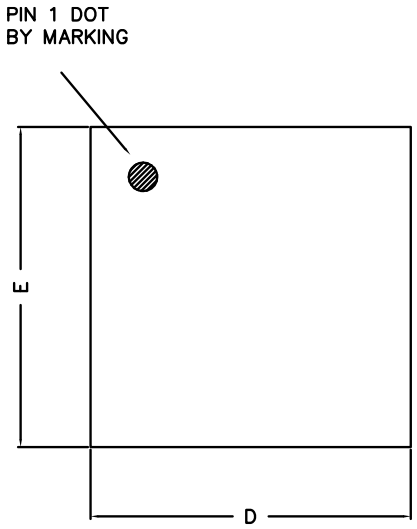
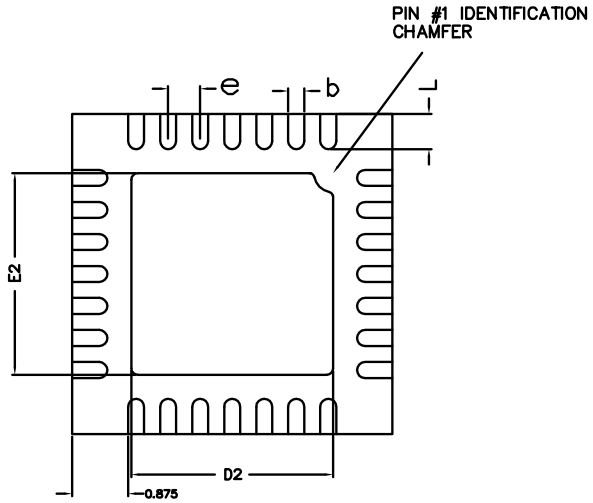


Figure 18 - Software Mode Reference Schematic

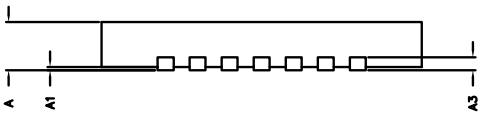
28 QFN Package Dimensions



TOP VIEW



BOTTOM VIEW



SIDE VIEW

COMMON DIMENSIONS(MM)			
PKG.	W: VERY VERY THIN		
REF.	MIN.	NOM.	MAX
A	0.70	0.75	0.80
A1	0.00	–	0.05
A3	0.2 REF.		
D	4.95	5.00	5.05
E	4.95	5.00	5.05
b	0.18	0.23	0.30
L	0.45	0.55	0.65
D2	3.00	3.15	3.25
E2	3.00	3.15	3.25
e	0.5 BSC		

Figure 19 - QFN Package Dimensions

28 QFN Top View Marking

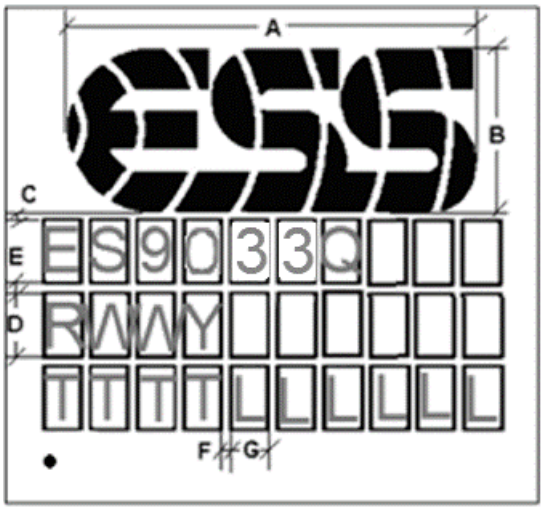


Figure 20 - QFN Top View Markings

	Dimension in mm						
Package Type	A	B	C	D	E	F	G
28 QFN 5mm x 5mm	4.0	1.6	0.2	0.4	0.2	0.1	0.3

Table 30 - 28 QFN Top View Markings

T	Tracking Number
W	Work Week
Y	Last Digit of Year
L	Lot Number
R	Silicon Revision

Table 31 - 28 QFN Top View Marking Definitions

Reflow Process Considerations

Temperature Controlled

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor to consider.

The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size (RPC-2 Pb-Free Process – Classification Temperatures (Tc)). This narrows the process window for lead-free soldering to 10°C to 20°C.

The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used.

Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits (Table RPC-2).

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

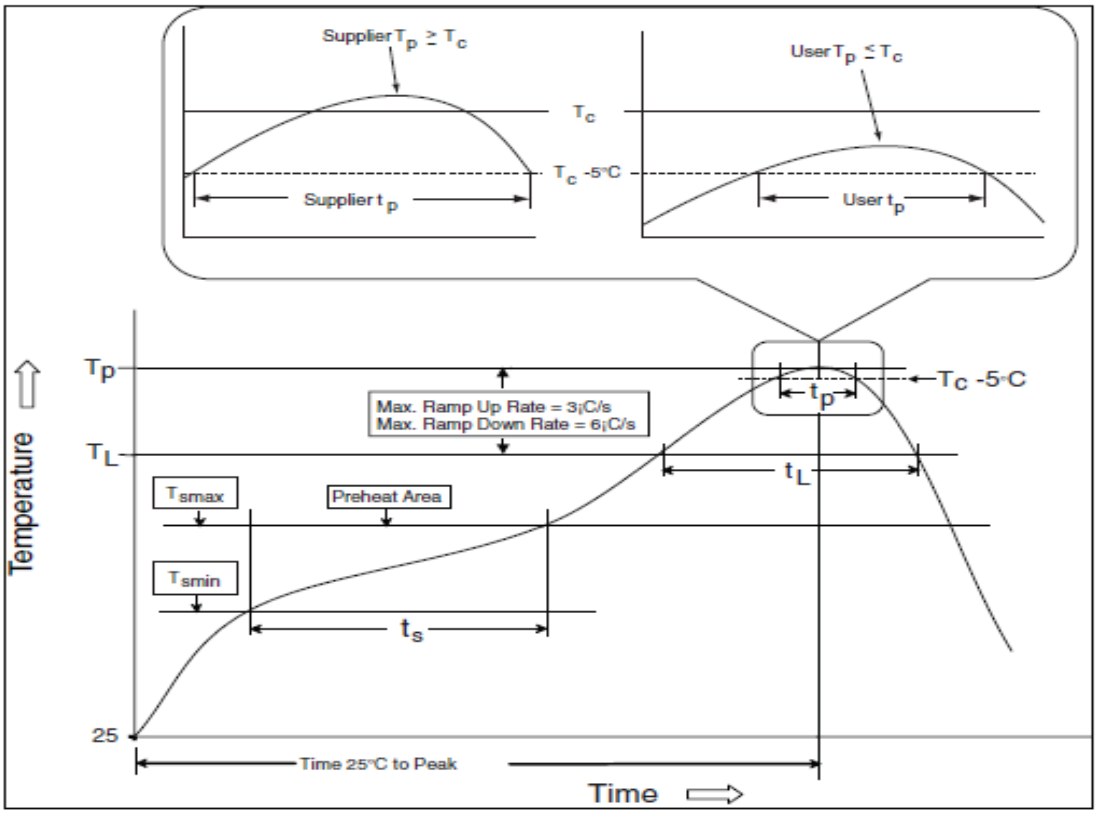


Figure 21 - IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)

Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time bake the board according to the moisture sensitivity label instructions.

Manual

Allowed up to 2 times with maximum temperature of 350°C no longer than 3 seconds.

RPC-1 Classification Reflow Profile

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150°C 200°C 60-120 seconds
Ramp-up rate (TL to Tp)	3°C / second maximum
Liquidous temperature (TL) Time (tL) maintained above TL	217°C 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the classification temp in Table RPC-2. For suppliers Tp must equal or exceed the Classification temp in Table RPC-2.
Time (tp)* within 5°C of the specified classification temperature (Tc), see Figure 22	30* seconds
Ramp-down rate (Tp to TL)	6°C / second maximum
Time 25°C to peak temperature	8 minutes maximum
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.	

Table 32 - RPC-1 Classification reflow profile

All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp shall be within ±2°C of the live-bug Tp and still meet the Tc requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures, refer to JEP140 for recommended thermocouple use.

Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.

For example, if Tc is 260°C and time tp is 30 seconds, this means the following for the supplier and the user.
For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.
For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

All components in the test load shall meet the classification profile requirements.

RPC-2 Pb-Free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm3, <350	Volume mm3, 350 to 2000	Volume mm3, >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Table 33 - RPC-2 Pb-Free Process

At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).

Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.

The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

Ordering Information

Part Number	Description	Package
ES9033Q	SABRE 32-bit 2 Channel DAC with built in line driver & digital filters	5mm x 5mm 28 QFN
ES9033QT • **Inquire for availability**	SABRE 32-bit 2 Channel DAC with built in line driver & digital filters Extended temperature range of -40ºC to 125ºC	

Table 34 - Ordering Information

Revision History

Current Version 0.4.0

Rev.	Date	Notes
0.1.0	April 5, 2021	Initial release
0.4.0	August, 2024	• Updated formatting • Added DRE section • Added Pre-programmed Digital Filters Section • Renamed 2x mode to 64FS mode • Updated automute section • Added auto fs detect note under DSD input format • Updated internal supply and reference pin types and reset states • Reserved Reg 10-9[11], 12-11[11], 14-13[11], 230-229[11], 232-231[11] • Reserved 224[4:1], 236-233[26:0] • Unreserved 73[1:0] • Updated Reg 36[7], 40[4:0], 73[0, 1, 6, 7], 82[7], 202-200[13:10, 9:1] desc and/or names

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

ESS Technology:

ES9033Q