

# 30V P-Channel Enhancement Mode MOSFET

Voltage

-30 V

Current

-38 A

#### **Features**

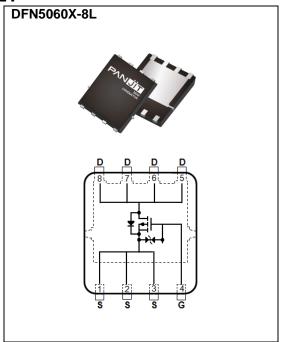
- RDS(ON), VGS@-10V, ID@-20A<15m $\Omega$
- RDS(ON), VGS@-4.5V, ID@-10A<26m $\Omega$
- 100% UIS tested
- Reliable and Rugged
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

#### **Mechanical Data**

• Case: DFN5060X-8L Package

• Terminals : Solderable per MIL-STD-750, Method 2026

• Approx. Weight: 0.087 grams



#### **Maximum Ratings and Thermal Characteristics** (T<sub>A</sub>=25°C unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS	
Drain-Source Voltage		V <sub>DS</sub>	-30	V	
Gate-Source Voltage		$V_{GS}$	±25	V	
Continuous Drain Current(Note 3)	T <sub>C</sub> =25°C	l <sub>D</sub>	-38		
	T <sub>C</sub> =100°C		-24	Α	
Pulsed Drain Current <sup>(Note 1)</sup>	T <sub>C</sub> =25°C	I <sub>DM</sub>	-128		
Power Dissipation	T <sub>C</sub> =25°C	Po	35	W	
	T <sub>C</sub> =100°C		14		
Continuous Drain Current(Note 4)	T <sub>A</sub> =25°C	I <sub>D</sub>	-11		
	T <sub>A</sub> =70°C		-8.6	Α	
Power Dissipation	T <sub>A</sub> =25°C	Po	2.8	W	
	T <sub>A</sub> =70°C	PD	1.8		
Single Pulse Avalanche Energy <sup>(Note 5)</sup>		Eas	56	mJ	
Operating Junction and Storage Temperature Range		T <sub>J</sub> ,T <sub>STG</sub>	-55~150	°C	
Thermal Resistance <sup>(Note 4)</sup>	Junction to Case	$R_{ heta JC}$	3.6	°C/W	
	Junction to Ambient	$R_{\theta JA}$	45		



#### Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise noted)

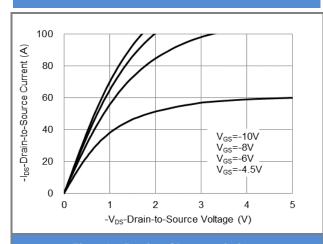
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-250uA	-30	-	-	V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250uA	-1	-1.8	-2.5	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-20A	-	12	15	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-10A	-	20	26	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V	-	-	-1	uA
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±25V, V <sub>DS</sub> =0V	-	-	±10	uA
		V <sub>GS</sub> =±10V, V <sub>DS</sub> =0V	-	-	±1	
Dynamic <sup>(Note 6)</sup>						
Total Gate Charge	$Q_g$	V <sub>DS</sub> =-24V, I <sub>D</sub> =-20A, V <sub>GS</sub> =-10V	-	32	-	nC
Gate-Source Charge	Qgs		-	5	-	
Gate-Drain Charge	$Q_{gd}$		-	10	-	
Input Capacitance	Ciss	V <sub>DS</sub> =-25V, V <sub>GS</sub> =0V, f=1MHz	-	1270	-	
Output Capacitance	Coss		-	190	-	pF
Reverse Transfer Capacitance	Crss		-	170	-	
Gate resistance	Rg	f=1MHz	-	7	-	Ω
Turn-On Delay Time	td <sub>(on)</sub>	$V_{DS}$ =-24V, $I_{D}$ =-20A, $V_{GS}$ =-10V, $R_{G}$ =3 $\Omega$ (Note 2)	-	7	-	
Turn-On Rise Time	tr		-	9	-	ns
Turn-Off Delay Time	td <sub>(off)</sub>		-	32	-	
Turn-Off Fall Time	tf	(14016-2)	-	39	-	
Drain-Source Diode	•					
Diode Forward Current	Is	Tc=25°C	-	-	-38	Α
Pulsed Diode Forward Current	I <sub>SM</sub>	1C=25 C	-	-	-128	
Diode Forward Voltage	V <sub>SD</sub>	Is=-20A, V <sub>G</sub> S=0V	-	-0.9	-1.3	V
Reverse Recovery Time	Trr	V <sub>GS</sub> =0V, I <sub>S</sub> =-20A	-	18	-	ns
Reverse Recovery Charge	Qrr	dls/dt=100A/us	-	8	-	nC

#### NOTES:

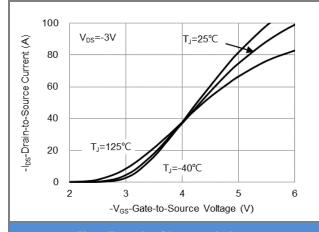
- 1. Pulse width<300us, Duty cycle<2%.
- 2. Essentially independent of operating temperature typical characteristics.
- 3. The maximum current rating is package limited.
- 4. R<sub>BJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch<sup>2</sup> with 2oz.square pad of copper.
- 5. The test condition is L=0.5mH, I<sub>AS</sub>=-15A, V<sub>DD</sub>=-30V, V<sub>GS</sub>=-10V, Starting T<sub>J</sub>=25°C.
- 6. Guaranteed by design, not subject to production testing.



#### **TYPICAL CHARACTERISTIC CURVES**



**Fig.1 On-Region Characteristics** 



**Fig.2 Transfer Characteristics** 

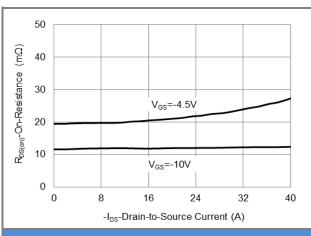


Fig.3 On-Resistance vs. Drain Current

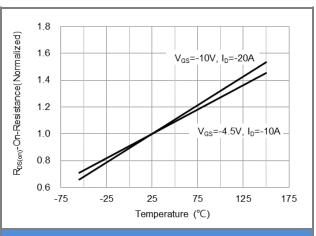
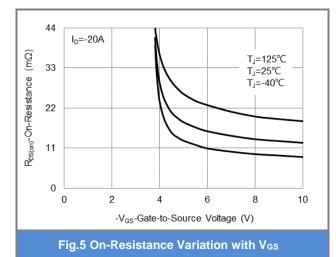
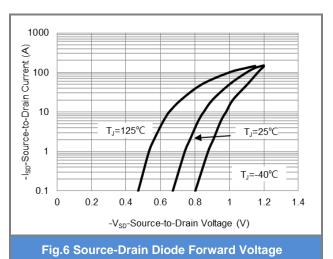


Fig.4 On-Resistance vs. Junction temperature







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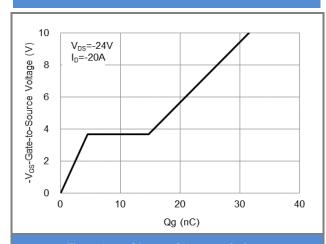


Fig.7 Gate-Charge Characteristics

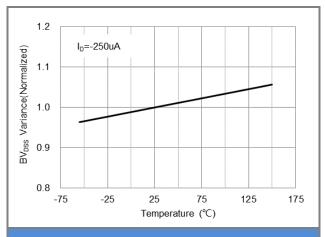


Fig.8 Breakdown Voltage Variation vs. Temperature

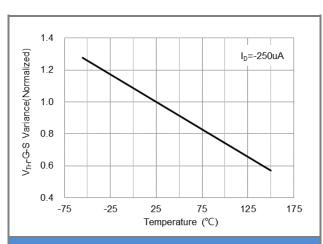


Fig.9 Threshold Voltage Variation with Temperature

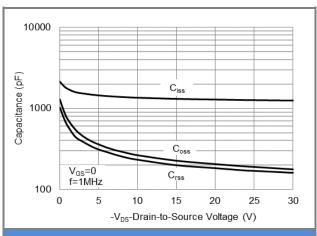
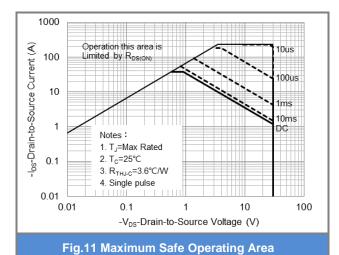


Fig.10 Capacitance vs. Drain-Source Voltage



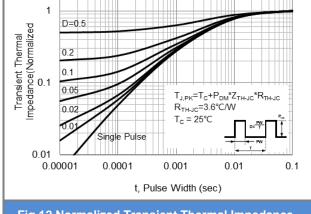


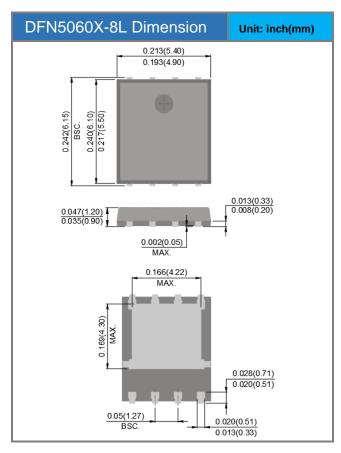
Fig.12 Normalized Transient Thermal Impedance

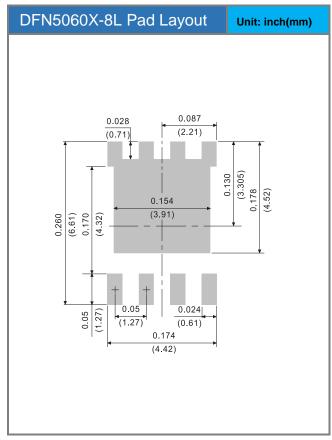


#### **Product and Packing Information**

Part No.	Package Type	Packing Type	Marking
PJQ5437E	DFN5060X-8L	3K pcs / 13" reel	Q5437E

#### **Packaging Information & Mounting Pad Layout**







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