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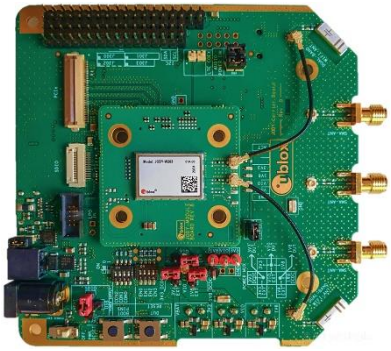
EVK-JODY-W2 User Guide

Evaluation kit for JODY-W2 host-based modules

User guide



Abstract

This document describes how to set up the EVK-JODY-W2 evaluation kit used to evaluate JODY-W2 series multiradio modules with Wi-Fi and Bluetooth.

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C1 - Public

Document information

Title	**EVK-JODY-W2 User Guide**	
Subtitle	Evaluation kit for JODY-W2 host-based modules	
Document type	User guide	
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This document applies to the following products:

Product name	Type number	Hardware version
EVK-JODY-W263	EVK-JODY-W263-01A-00	Module board rev. B, Carrier board rev. D

Contents

1 Kit description

The JODY-W2 series comprises compact modules based on the NXP 88W8987 chipset family. The chipsets used in the automotive grade JODY-W2 modules are AEC-Q100 compliant. They enable Wi-Fi, Bluetooth, and Bluetooth Low Energy (LE) communication, and are ideal for automotive and industrial applications.

EVK-JODY-W2 allows an external host processor to access several practical features for testing and evaluating the Wi-Fi and Bluetooth connectivity supported in JODY-W2 series modules, including:

- An external connector to all host interfaces (SDIO and UART)
- PCM interface through an on-board accessible connector
- GPIO pins that are accessible through an on-board connector
- Internal dual-band 2.4/5 GHz antennas for Wi-Fi and Bluetooth
- SMA connectors for external antennas.
- Module interfaces that are all externally available via the pin headers

For more information about JODY-W2 modules, see the JODY-W2 series data sheet [1] and system integration manual [2].

1.1 Overview

Table 1 lists the different evaluation kit versions:

Evaluation kit	Ordering code	Description	Suitable for evaluating
EVK-JODY-W263	EVK-JODY-W263-01A	Evaluation kit for JODY-W263 Antennas:1 Wi-Fi dual-band,1 Bluetooth. Host-based NXP 88W8987 chipset family.	JODY-W263-00A JODY-W263-01A JODY-W263-00B JODY-W263-10B

Table 1: Available EVK-JODY-W2 User Guide evaluation kits

Figure 1 shows the attached peripherals and connectors of the EVK-JODY-W2.

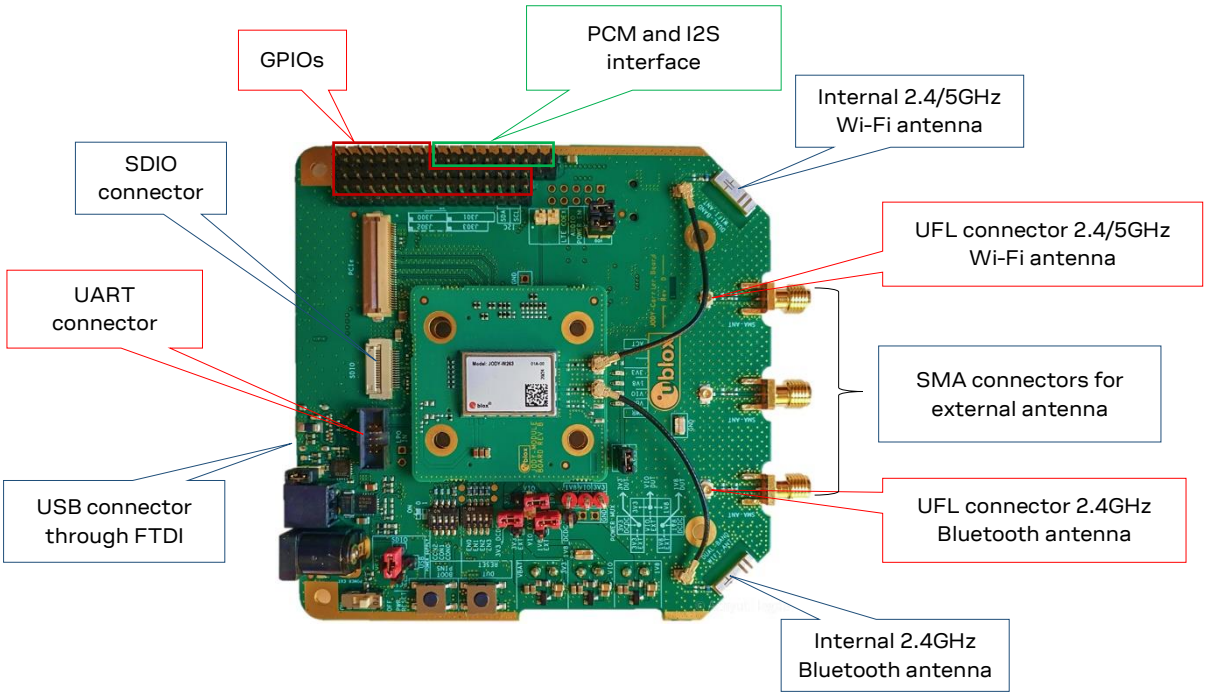


Figure 1: EVK-JODY-W2 outline showing peripherals and connectors

1.2 Kit includes

Connectors for the use of different interfaces of the module are included in the evaluation kit. Table 2 shows the various components included in the EVK-JODY-W2 User Guide.

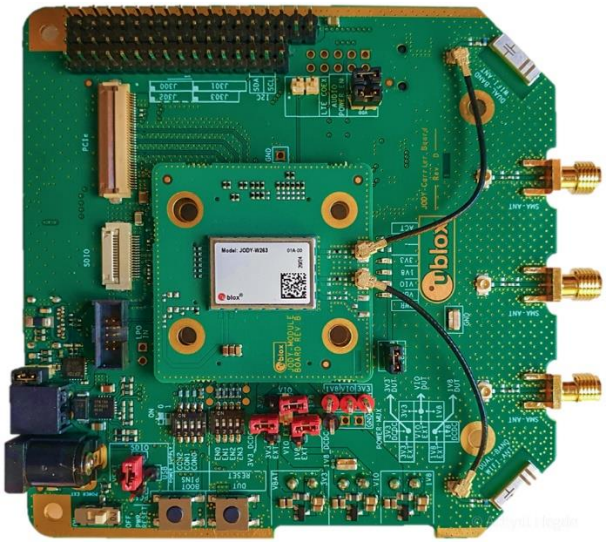
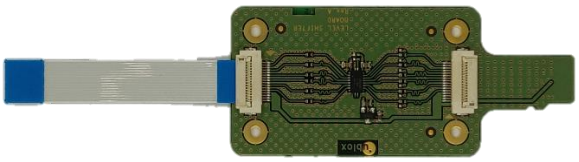
Part	Description	Outline
Evaluation board (EVB)	Evaluation board for JODY-W263 series modules. The board includes SMA antenna connectors that connect to external antennas for Wi-Fi and Bluetooth. It has two internal dual-band Wi-Fi/Bluetooth antennas.	
Level shifter with micro SDIO ZIF adapter and flat cable	SDIO level shifter to be used if the host only supports a 3.3 V interface voltage (High Speed Mode).	
Micro SDIO ZIF adapter and flat cable.	Micro SDIO adapter for Wi-Fi and/or Bluetooth host communication. The adapter is compatible with host sockets designed for micro-SD memory cards.	
Full-size SDIO adapter	SDIO adapter for Wi-Fi (optionally Bluetooth) host communication. The adapter is compatible with host sockets designed for full-size SD memory cards.	
Type-C USB cable	Type-C USB cable for Bluetooth host communication over UART connected through FTDI.	
External Antennas (2)	Dual band Wi-Fi/Bluetooth antenna, Linx Technologies ANT-DB1-RAF-SMA	

Table 2: EVK-JODY-W2 component list

1.3 Software

JODY-W2 series modules are based on the NXP 88W8987 chipset family. The drivers and firmware required to operate JODY-W2 series modules are developed by NXP and are already integrated into the Linux BSP for the NXP i.MX application processors [6] and the MCUXpresso SDK for NXP MCU devices [8].

The documentation for NXP software releases contains Wi-Fi and Bluetooth release notes and a list of supported software features. The driver source code is provided free of charge as open-source software under NXP licensing terms. As open-source software, the drivers can be integrated or ported to other non-NXP based host platforms. Yocto recipes for the driver (`nxp-wlan-sdk`, `kernel-module-nxp89xx`) and firmware (`linux-firmware`), that can be used to develop custom Linux-based systems, are part of the NXP i.MX Linux BSP.

1.3.1 Driver source code

The latest version of the driver source code and Wi-Fi/Bluetooth firmware are available from the following open-source repositories:

- Wi-Fi driver: https://github.com/nxp-imx/mwifiex
- Firmware: https://github.com/NXP/imx-firmware/
- i.MX meta-layer: https://github.com/nxp-imx/meta-imx

☞ Use the repository branches matching the latest Linux BSP release version. At the time of document publication, this is version 5.15.52_2.1.0.

The Wi-Fi driver uses the TCP/IP stack from the Linux kernel for data transmission and the `cfg80211` subsystem in the kernel for configuration and control. The `hci_uart` driver from the Linux kernel and BlueZ host stack are used for the Bluetooth part. For further information about initialization and configuration of the Wi-Fi and Bluetooth features, see also the NXP User Manual UM11490 [7].

Contact your local u-blox support team for information about additional software options for the JODY-W2 series modules.

1.4 System requirements

The evaluation kit has the following system requirements:

- Host (PC or embedded system) with Micro SDIO slot and USB 2.0 interface for access to the Bluetooth UART interface through USB-to-UART bridge
- Operating System: Linux (3.x/4.x/5.x), Android Pie (9.0.0_2.3.4), Q (10.0.0_2.3.0), and 11.0.0_1.0.0

1.5 Operating conditions

Table 3 describes the absolute range for key EVK operating parameters.

Symbol	Parameter	Min.	Typ.	Max.	Units
VBAT	Power supply voltage	2.8	3.3	5.5	V
VIO	I/O supply voltage 1.8 V	1.67	1.8	1.92	V
	I/O supply voltage 3.3 V	3.07	3.3	3.53	V
1V8	Analog power supply voltage 1.8 V	1.71	1.8	1.89	V
T_A	Ambient operating temperature	-40	-	+85*	°C
Ripple Noise	Peak-to-peak voltage ripple on all supply lines.	-	-	10	mV

Table 3: EVK-JODY-W2 operating conditions

☞ The signal voltage for the SDIO interface of the JODY-W2 series module is powered from the **1V8** supply. A level shifter is required to operate the module in default Speed and High-Speed modes at 3.3 V signal voltage.

2 Getting started

Figure 2 shows an outline of the evaluation board and the placement of the connectors, jumpers, and switches. The EVB makes all interfaces of the JODY-W2 module accessible through connectors or pin headers. See also Jumpers and connectors.

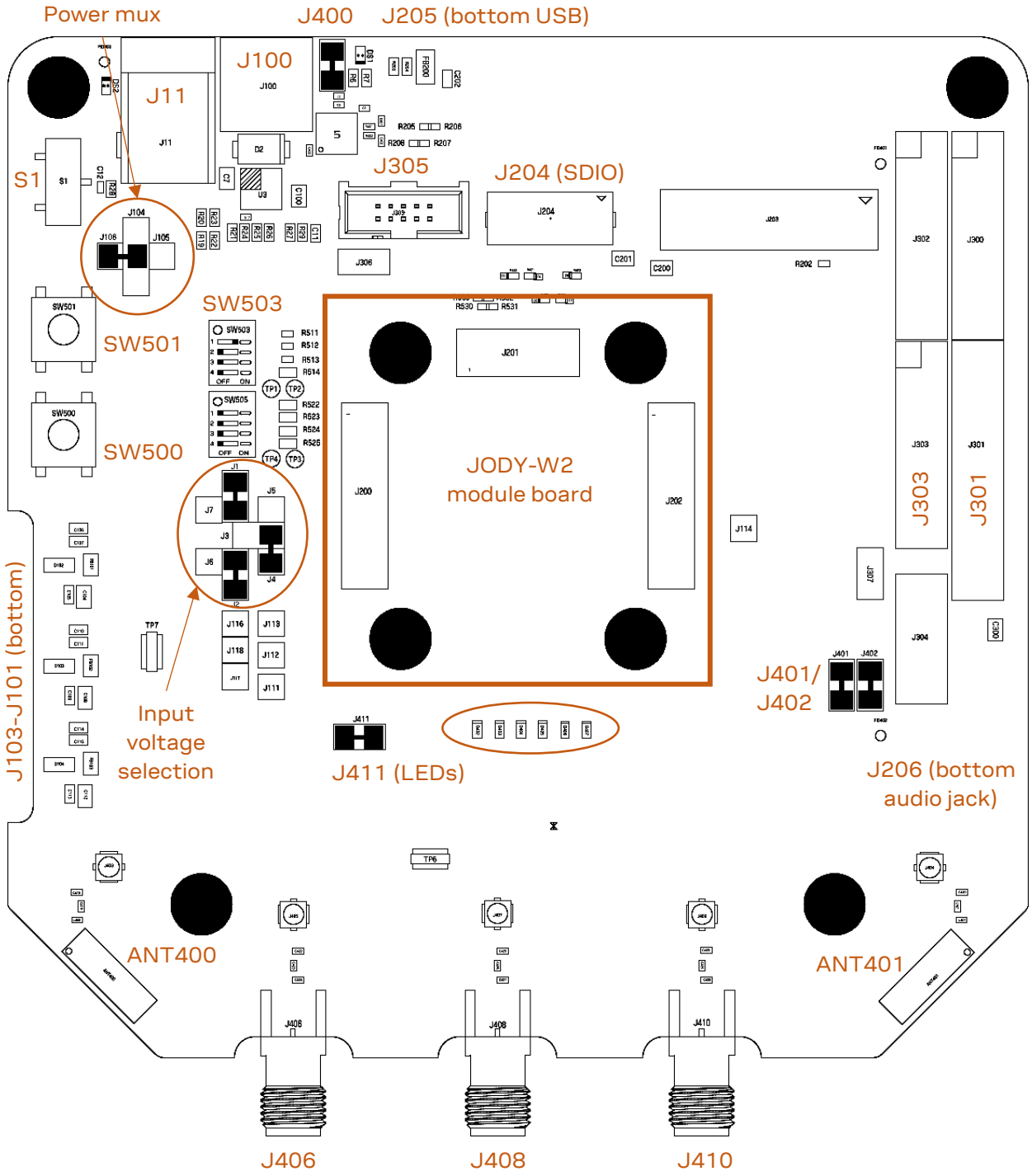


Figure 2: EVK-JODY-W2 connectors

2.1 Jumpers and connectors

Table 4 provides a summary of the connectors and jumpers used to configure EVK-JODY-W2.

Designator	Connector	Description
J104-J106	Power supply selection (power mux)	Jumper settings for external power supply configuration (3.3.1)
J1 - J7	Input voltage configuration	Jumper settings for selecting the input voltage for the module (3.3.2)
J204	SDIO Connector	ZIF connector for SDIO host interface on EVB (3.5)
J305	Bluetooth UART	UART connector for Bluetooth host interface (3.6)
J205	Type-C USB	USB connector for Bluetooth through USB-to-UART bridge (3.6)
J401, J402	Audio codec enable	Jumpers to enable the audio codec on the EVB (3.7)
J206	Audio jack	Audio jack for the audio codec (3.7)
J301	Bluetooth audio	Connector for the PCM audio interface (3.7)
J303	Control lines	Connector for host wake for Bluetooth and WLAN (3.8)
SW503	Bootstrapping	Switch for host interface selection (3.4)
J400	USB-UART Enable	Jumper to enable/disable the Bluetooth host interface via USB-to-UART bridge (3.6)
J406, J408, J410	SMA Connectors	SMA coaxial RF connectors for external antennas (3.9)
ANT400, ANT401	Internal antennas	Internal dual-band chip antennas (3.9)
SW500, SW501	Reset buttons	Reset buttons for module and power supply
S1	Power enable switch	External EVB power supply switch
J11, J100	Power jack	External power jack to connect the wall adapter. S1 needs to be switched ON.
J101-J103	External supply	Connectors for individual external supplies
J411	LEDs	Jumper to enable power supply LEDs (3.10)

Table 4: JODY-W2 evaluation board connectors

2.2 EVK setup procedure

Use the following procedure to evaluate JODY-W2 series modules:

1. By default, internal antennas are selected for any transmission and reception using pig-tail coaxial cables, as shown in Figure 18. To use external antennas, connect the cables to another pair of U.FL adapters and then connect the external dual-band antennas to the SMA connectors.
2. Connect the SDIO adapter to the connector on the board.
3. Connect the evaluation board to the host system through the supplied micro or full-size SDIO adapter card. The evaluation board uses zero insertion force (ZIF) connectors and flat cables to connect the adapters. To connect the cable, gently flip up the small locking flap of the connector, align and insert the cable with the blue marking pointing upwards, and then close the locking flap.
4. Check the LEDs. They correspond to different input voltage levels and turn green when the appropriate levels are reached. At this point, the module should be detected by the host system.
5. For evaluation of the Bluetooth features, use either an SDIO interface (with flat cable shared with Wi-Fi) or UART (with Type-C USB cable). See also Bluetooth UART interface and Bootstrapping.
6. Install the necessary driver software for JODY-W2 series modules, as described in the system integration manual [2].

2.3 Host interface for Wi-Fi (1.8 V UHS)

The SDIO interface is the only available option for Wi-Fi communication. Follow the procedure outlined below to connect the SDIO interface for Wi-Fi:

1. Connect the micro SDIO adapter card with the micro SDIO connector **J204** to the board using the flat ribbon cable. Make sure that the blue strip at the end of the connector faces upwards when connecting each end of the cable.

2. Connect the evaluation board to the host system by inserting the adapter card into an SDIO connector on the host system.

⚠ Be careful when inserting the SDIO adapter into the SDIO slot of a laptop. Built-in readers can be poorly designed and damage more easily than those on more compact development platforms.

2.4 Host interface for Wi-Fi (3.3 V HS)

By default, EVK-JODY-W2 operates with host interface voltage of 1.8 V. For the designs with host interface voltage 3.3 V, a level shifter is needed to convert the voltage level of the SDIO signals. Only SDIO High Speed (HS) mode is supported when using a 3.3 V interface voltage.

Figure 3 shows how the level shifter and EVK are connected. See also the level shifter integration application note [3].

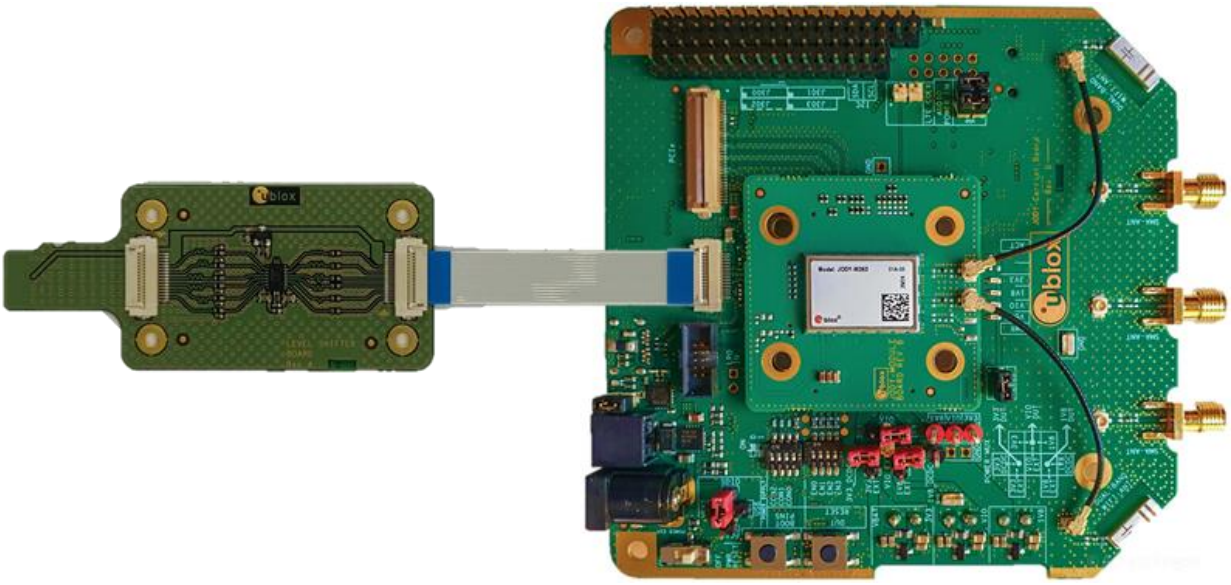


Figure 3: EVK connection to level shifter

⚠ Level shifters are voltage sensitive. To avoid damaging the level shifter IC, connect the level shifter so that host is in the same direction of the micro-SD adapter, as shown in Figure 4.

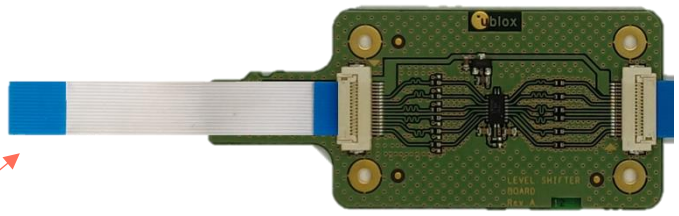


Figure 4: Level shifter direction

⚠ The level shifter is designed to connect with a host platform through the ZIF cable connector only. It cannot work if connected directly to an SD card slot or adapter through the micro-SD extension of the level shifter board. For the level shifter to work, position the resistors on the SDIO lines from a horizontal to vertical orientation, as shown in the Figure 5.

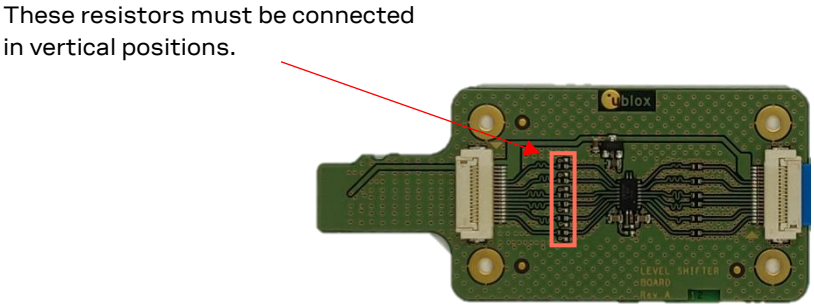


Figure 5: Resistor modification to enable host connection through an adapter

2.5 Host interface for Bluetooth

JODY-W2 series modules support a high-speed UART interface for Bluetooth communication.

A USB-to-UART bridge (FTDI FT231X) is included on the evaluation board. Follow the procedure outlined below to connect the board to a host system through USB.

1. Connect one end of the USB cable to the Bluetooth USB connector on the board.
2. Connect the other end of the USB cable to the host system.
3. Check that jumper **J400** is bridged to enable Bluetooth communication over UART through FTDI.

☞ The 4-pin UART interface of the JODY-W2 series modules can be directly accessed through the pins on the Bluetooth UART connector **J305** of the EVK. For information on how to use the Bluetooth UART on the evaluation board, see also Bluetooth host interface.

3 Board description

This chapter describes the logical components, connectors, jumpers, and switches used to configure EVK-JODY-W2.

3.1 Block diagram

EVK-JODY-W2 design is organized between the module board and carrier board. The carrier board includes all the necessary peripherals and connectors. It also includes a slot for mounting the module board. The module board holds the JODY-W2 module. Figure 6 shows the placement of carrier boards in relation to the module boards of the EVK-JODY-W2.

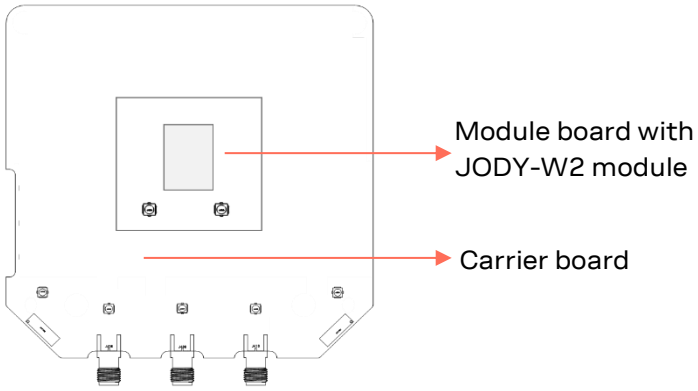


Figure 6: Carrier and module board

Figure 7 shows the EVK with the various peripherals and connectors that surround it.

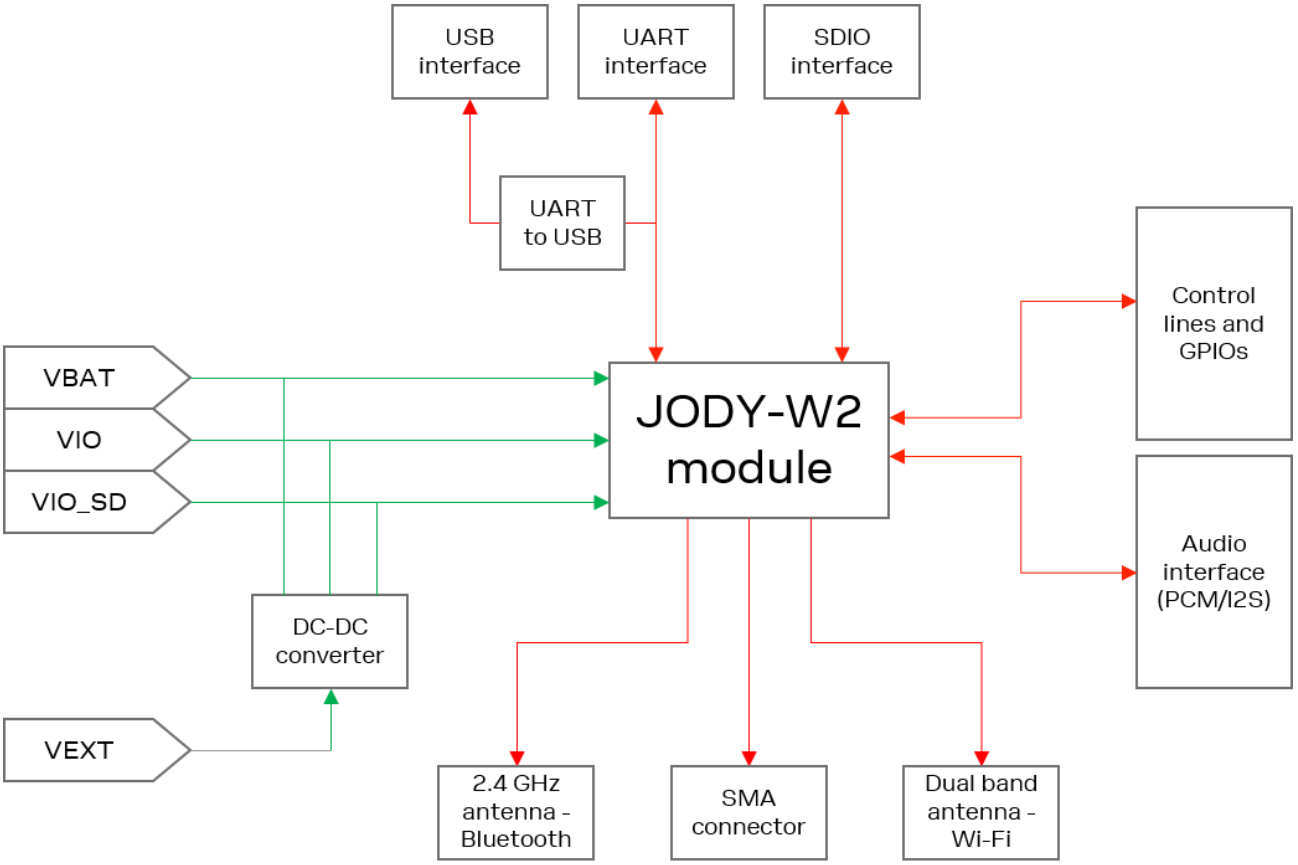


Figure 7: EVK-JODY-W2 block diagram

3.2 Jumper conventions

Figure 8 shows the graphical conventions used for jumper settings. Pin 1 is shown in grey color. All jumpers are shown with red lines terminated with round edges.

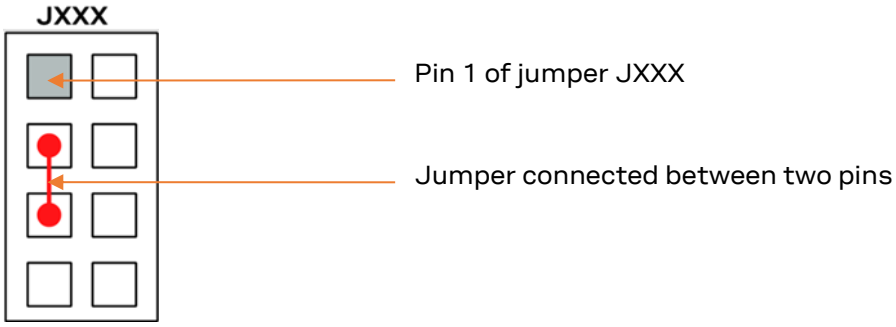


Figure 8: Jumper convention

3.3 Power supply configuration

JODY-W2 series modules are supplied with **VBAT** (3.3 V), **1V8** (1.8 V), and **VIO** voltage (either 3.3 V or 1.8 V). Different interfaces and external sources can also provide input voltages to the module.

Power to EVK-JODY-W2 can be supplied through different interfaces:

- SDIO interface: The host connector for all Wi-Fi and Bluetooth (optional) communication can be used to generate the power needed for operation.
- USB: If Bluetooth is connected through USB, the bus can also be used as a power supply.
- External power supply: EVK-JODY-W2 can be powered by an external 5 V to 24 V supply using a terminal connector or power jack. In this case, a DC-DC converter is used for generating all the required internal voltages. **S1** is used to switch on the board when supplied through J100 (terminal connector) or **J11** (power jack). Only one supply should be used at a time. The power jack should be 2.1 mm in diameter with positive polarity at the center.
- Individual supply: All necessary voltage levels, **VBAT**, **VIO**, and **1V8** have pinouts that can be connected individually using an external power source.

Figure 9 shows the external connectors and jumpers used for configuring the different power supply options.

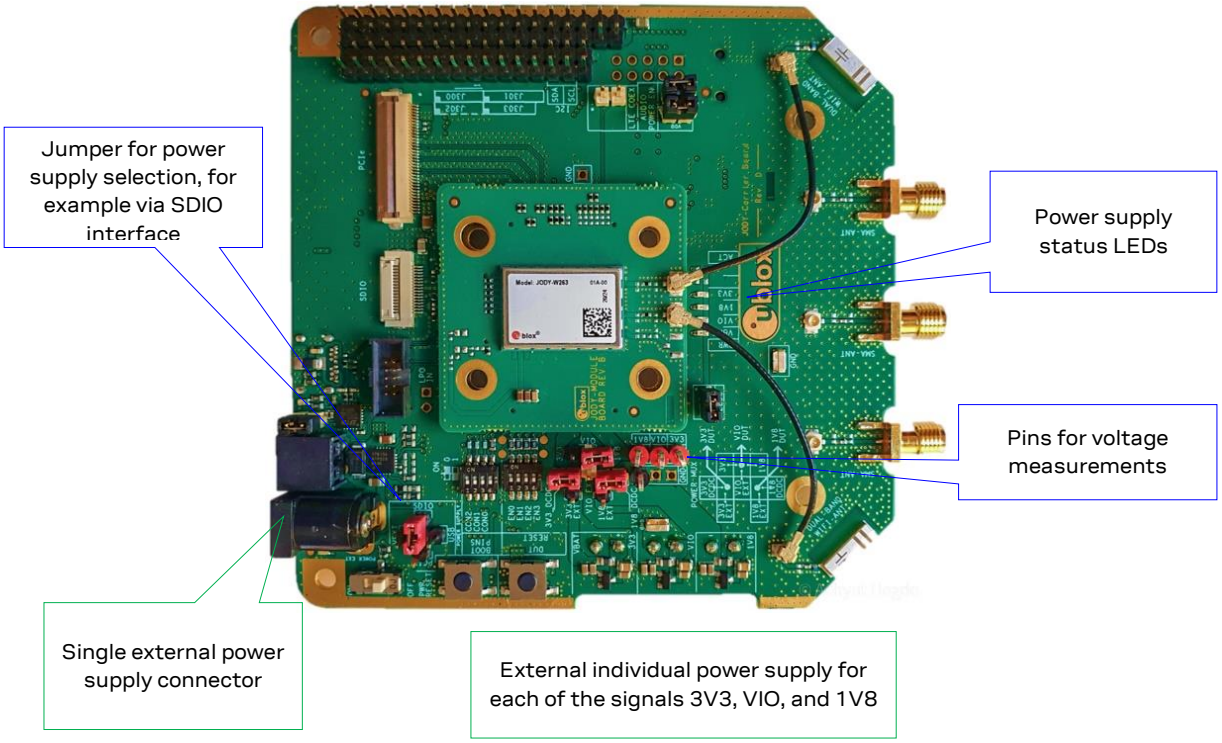


Figure 9: Overview of EVB power supply configuration

To operate the JODY-W2 EVB, the external power supply source (power mux) and input voltage levels to the module must be configured using jumpers on the EVB. The power supply tree, including the jumpers on the EVB, is shown in Figure 10. See also Jumpers and connectors.

- J104–J106 configure the EVB power supply source (SDIO, USB or external) to the **VIN_3V3** domain, which generates the internal power rails for the module.
- J1-J7 configure the input voltages for the JODY-W2 series module, which can be selected between the internally generated voltages and the external supplies from J101-J103.

DC-DC converters are used to step-down the external and USB supplies to the power mux and generate the required input voltages for the module.

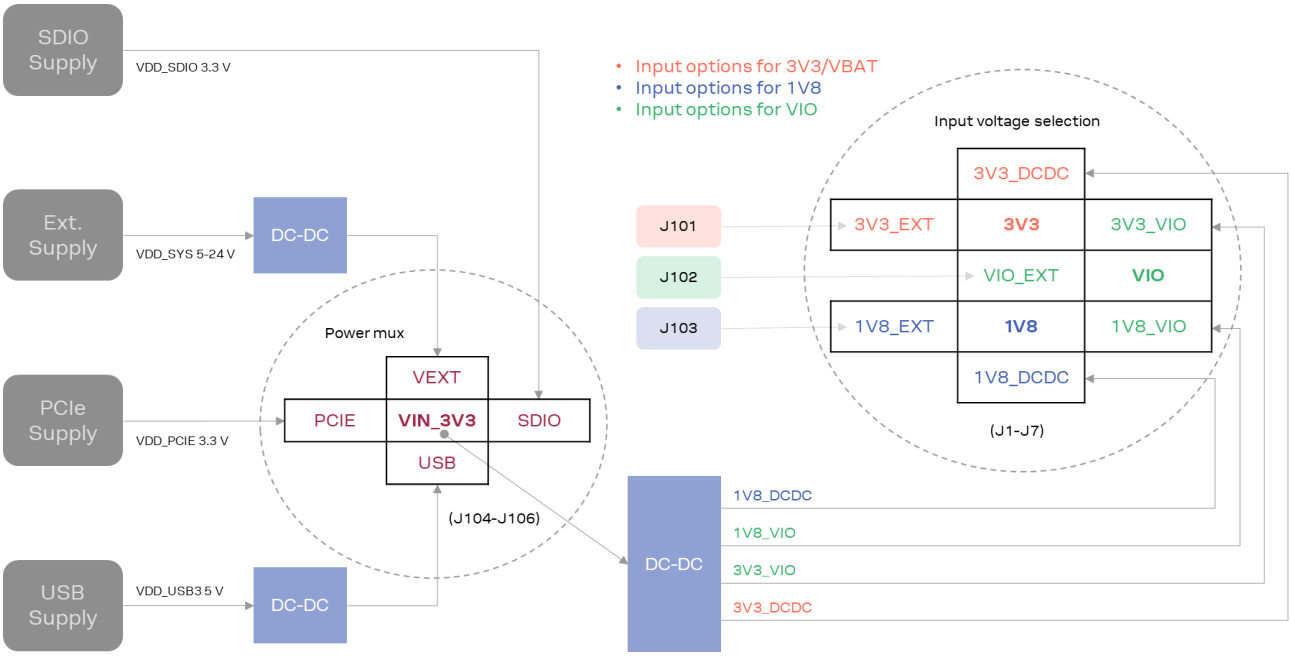


Figure 10: EVB power supply tree

☞ The PCIe interface is not supported on JODY-W2 modules.

3.3.1 Selecting the EVB power supply

Use jumpers J104–J106 to select the EVB power supply (power mux) for the EVB. Figure 11 shows the arrangement of external power supply sources for each jumper position.

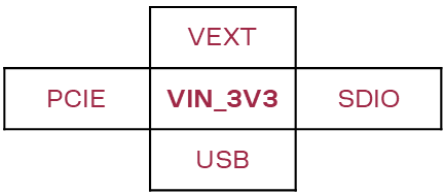


Figure 11: External power supply selection, J104-J106

☞ The option for using the PCIe interface is not available in JODY-W2.

VIN_3V3 is the input to the DC-DC converter on the EVB that generates the required voltage rails (**3V3_DCDC**, **1V8_DCDC**, **3V3_VIO**, and **1V8_VIO**) for the module, as shown in Figure 10. A single jumper is connected between **VIN_3V3** and the chosen voltage supply to the EVB.

Table 5 shows the (J104–J106) jumper positions for selecting the power supply source for the EVB.

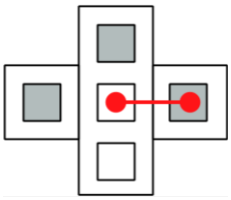
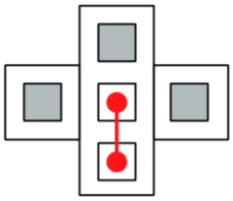
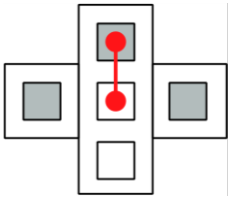
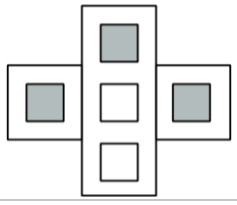
Input voltage	Jumper configuration
3.3 V from SDIO interface. Use SDIO adapter with the flat cable to connect to the host.	
5 V from USB interface. Use Type-C USB cable to connect with the host. The USB host port must be able to deliver a current of up to 1000 mA for Wi-Fi operation. The current provided by a standard USB 2.0 interface is sufficient for Bluetooth only operation.	
5 – 24 V external power supply. External supply must be connected to the power jack J11 or J100 and switch S1 must be ON. The external supply voltage is converted to 3.3 V using a DC-DC on the EVB. J11: 2.1 x 6.3 mm DC power jack J100: Phoenix Contact 1721986 See the links in [5] for further details about terminal connector and power jack.	
All input voltages are supplied from individual sources. External supplies must be connected to the power jacks located on the bottom side of the EVB for 3V3 (J101), 1V8 (J103) and VIO (J102). J101-J103: Phoenix contact 1721986.	

Table 5: Selecting power supply to the EVK

For more information about the EVK design, see the Schematics.

3.3.2 Selecting the module input voltages

Use jumpers J1-J7 to select the external power source to the module, as shown in Figure 12. The input voltage to the module can be sourced from either the on-board DC-DC generated voltages or the direct input voltages from the separate external supplies J101-J103.

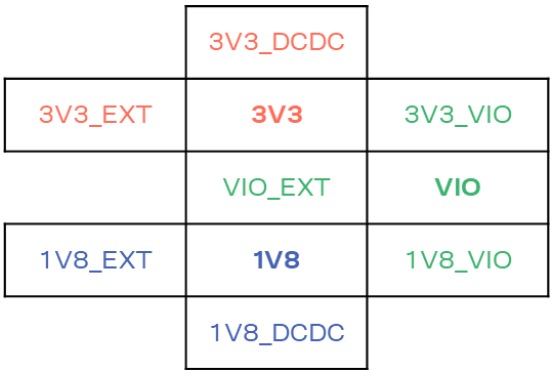


Figure 12: Input voltage selection (J1-J7)

The input voltage options for selecting the JODY-W2 module supply are described in Table 6.

Designator	Module supply	Source
3V3	VBAT	Can be connected to 3V3_DCDC or 3V3_EXT
VIO	VIO	Can be connected to 1V8_VIO or VIO_EXT
1V8	1V8	Can be connected to 1V8_DCDC or 1V8_EXT

Table 6: Input voltage options

Table 7 describes the different options to select the module input voltages using jumper J1-J7.

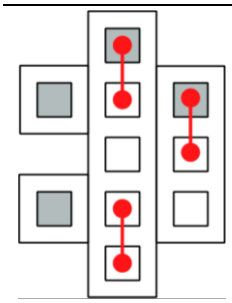
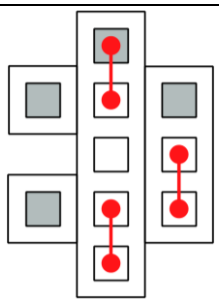
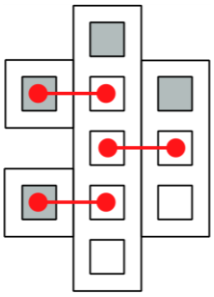
Jumper settings	Remarks/Voltage levels
 VIO (3.3 V)  VIO (1.8 V)	Selects the power supply from the host interface (SDIO or USB) or common external supply (VEXT) and on-board DC-DC generated voltages. VIO is derived from either 1V8 or 3V3. • VBAT – 3.3 V • 1V8 – 1.8 V • VIO – 1.8 V or 3.3 V
	Selects the power supply using separate external input sources for each of the voltage rails VBAT, 1V8 and VIO. External supplies are connected to J101-J103 at the bottom of the EVB carrier board.

Table 7: Input voltage jumper selection

3.4 Bootstrapping

JODY-W2 supports the following host interface combinations:

- **SDIO-UART** mode: Commands and data for the Wi-Fi traffic are transferred through the SDIO bus to the module. The Bluetooth traffic uses the high-speed UART interface.
- **SDIO-SDIO** mode: Commands and data for the Wi-Fi and Bluetooth traffic are transferred through the SDIO bus to the module.

DIP switch SW503 is used on the EVB to define the boot mode and the physical interfaces used for Wi-Fi and Bluetooth communication. Set each switch ON to pull the configuration signal low (GND, logic level “0”), and OFF to pull it high (logic level “1”).

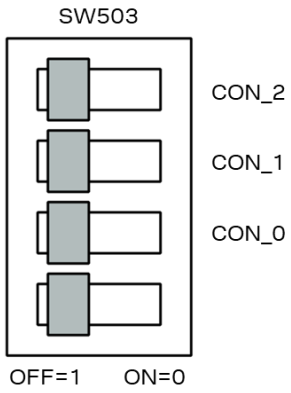


Figure 13: Boot and host interface configuration

Table 8 describes the DIP switch positions for configuring the boot mode and host interface options.

Boot mode	CON_2	CON_1	CON_0	Description
SDIO-UART	-	OFF	ON	Wi-Fi through SDIO (J203), Bluetooth through USB-to-UART (J205) or UART (J305)
SDIO-SDIO	-	OFF	OFF	Wi-Fi and Bluetooth through SDIO (J204)

Table 8: Boot mode selection options

☞ The UART interface for Bluetooth can be accessed either directly through J305, or through the USB type-C connector J205 and USB-to-UART bridge. For further information about the Bluetooth UART interface, see also Bluetooth host interface.

3.5 SDIO Interface

The boards can be connected through a micro or full-size SDIO connector for Wi-Fi communication with the host system. The SDIO connector can optionally be used for Bluetooth. The SDIO host interface connector **J204** is shown in Figure 14.

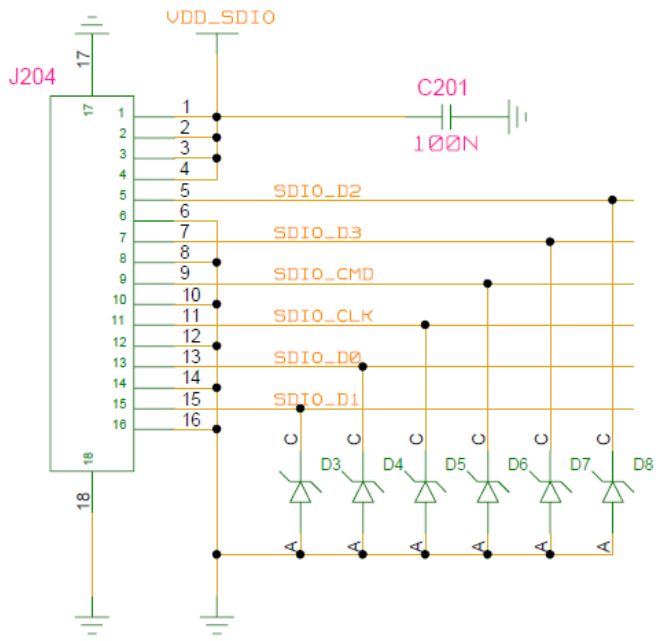


Figure 14: SDIO interface connector

All signals except **VDD_SDIO** are directly connected to the JODY-W2 module through 22 Ω series resistors connected on module board.

VDD_SDIO is connected to the power supply connector (J105) and is used for supplying 3.3 V for **VBAT** from the SDIO interface. The SDIO interface has 50 Ω impedance. The SDIO signals are powered by the **1V8** voltage domain.

☞ Pull-up resistors for the SDIO lines are not installed on the EVB because they are typically included in the host CPU. The EVB carrier board has the provision to install them in case if needed by the design.

3.6 Bluetooth host interface

The Bluetooth UART host interface of the JODY-W2 series module can be accessed either directly through the UART pins on J305, or through the USB type-C connector J205 through a USB-to-UART bridge (default).

A USB-to-UART bridge (FTDI FT231X) is included on the evaluation board to connect to the high speed UART interface of the JODY-W2 series modules. **VDD_USB3** from the USB connector is converted by a DC-DC to 3.3 V and can be used for supplying **VBAT** from the USB interface. Place the jumper on J400 to use Bluetooth through the USB type-C connector.

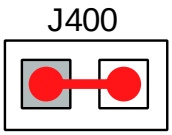


Figure 15: Jumper setting to use Bluetooth over USB

The 4-pin UART interface of the JODY-W2 series modules can be directly accessed through the Bluetooth UART connector J305, as shown in Figure 16. To use the UART interface directly, remove the jumper on **J400** and connect the UART host interface to the respective module side pins and GND on **J305**, as shown in Figure 16 and Table 9. The UART signals are powered by the **VIO** voltage domain.

Name	I/O	Description	Remarks
UART_TXD	O	UART TX signal	Connect to Host RX
UART_RXD	I	UART RX signal	Connect to Host TX
UART_RTS	O	UART RTS signal	Connect to Host CTS
UART_CTS	I	UART CTS signal	Connect to Host RTS

Table 9: UART signal description

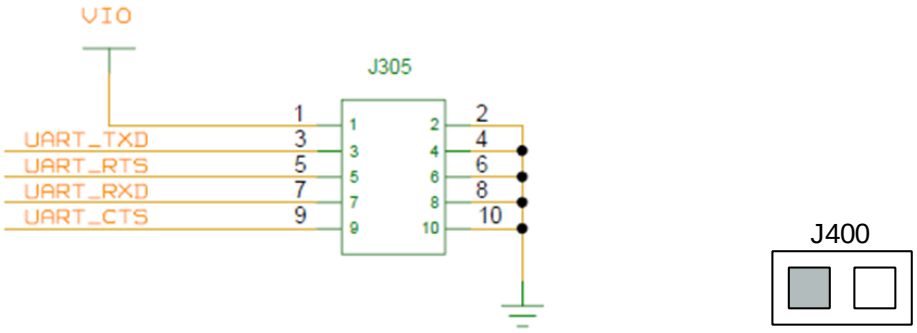


Figure 16: Bluetooth over UART interface

3.7 Bluetooth audio interface

A MAX9860 16-bit audio codec for Bluetooth voice applications is provided on the JODY-W2 EVK and connected to the PCM interface of the module. A 3.5 mm audio jack (J206) to connect a headset is available on the bottom side of the EVK. The codec is operated with a master clock (MCLK) of 19.2 MHz. The MAX9860 audio codec is completely controlled through software using an I2C interface. The codec responds to the I2C slave address 0x20 for all write commands and 0x21 for all read operations.

Place jumpers J401 and J402 to enable the audio codec, as shown in Figure 17.

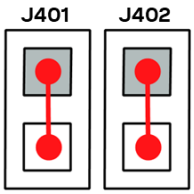


Figure 17: Enable audio codec option

The I2C interface of the audio codec is provided on connector **J303** of the EVK as shown in Figure 2 and Table 10.

The PCM interface of the JODY-W2 module is directly connected to the serial audio interface of the MAX9860 audio codec. The PCM pins are additionally provided on connector **J301,** as shown in Table 10.

Name	I/O	Connector / pin no.	Description
I2C_SDA	I/O	J303 / 11	I2C Serial-Data Input/Output
I2C_SCL	I	J303 / 13	I2C Serial-Data clock
PCM_CLK	I/O	J301 / 16	PCM clock
PCM_SYNC	I/O	J301 / 15	PCM frame sync
PCM_IN	I	J301 / 18	PCM data in
PCM_OUT	O	J301 / 17	PCM data out

Table 10: Audio interfaces

3.8 Control lines

Connectors J301 and J303 provide several other interfaces from the JODY-W2 series module, such as host wake-up signals, GPIOs, and audio interfaces. See Schematics for more information.

Pin no	Module pin no	Signal	Pin no	Module pin no	Signal
1	-	NC	2	-	NC
3	41	GPIO_19	4	42	GPIO_0[1]
5	35	GPIO_3	6	32	GPIO_14
7	10	HOST_WAKE/GPIO_1	8	11	GPIO_12
9	-	GND	10	-	GND
11	-	I2C_SDA	12	-	GND
13	-	I2C_SCL	14	-	GND
15	-	GND	16	-	GND

Table 11: Connector J303

Pin no	Module pin no	Signal	Pin no	Module pin no	Signal
1	-	NC	2	-	NC
3	-	NC	4	-	NC
5	33	GPIO_15	6	40	GPIO_18
7	12	GPIO_20	8	34	GPIO_2
9	-	RESET	10	9	GPIO_13
11	-	NC	12	-	NC
13	-	NC	14	-	NC
15	15	PCM_SYNC	16	16	PCM_CLK
17	17	PCM_OUT	18	18	PCM_IN
19	-	NC	20	-	GND

Table 12: Connector J301

3.9 Antenna interfaces

The evaluation board includes two dual-band 2.4/5 GHz chip antennas (Pulse Electronics W3006) for Wi-Fi and Bluetooth connections. Two 50 Ω female SMA antenna connectors are used to connect external antennas or measurement instruments to the antenna pins of JODY-W2 series modules. The antenna interfaces are selected by connecting U.FL connectors on the EVB module board with designated U.FL connectors on the EVB carrier board using coaxial RF cables.

The module board has two U.FL connectors which connect to the antenna pins of the JODY-W2 series module. To use any of the chip antennas or SMA connectors on the EVB carrier board, connect the coaxial RF cables between the U.FL connector on the module board and U.FL connectors on the carrier board. See also Figure 18.

[1] Indicates the sleep state of the module

Table 13 describes the available radio interfaces of the JODY-W2 module.

Module antenna pin	Function
ANT0	2.4 GHz Bluetooth
ANT1	2.4 and 5 GHz Wi-Fi

Table 13: JODY-W2 antenna interfaces

Figure 18 shows the connections for using internal (left) and external (right) antennas.

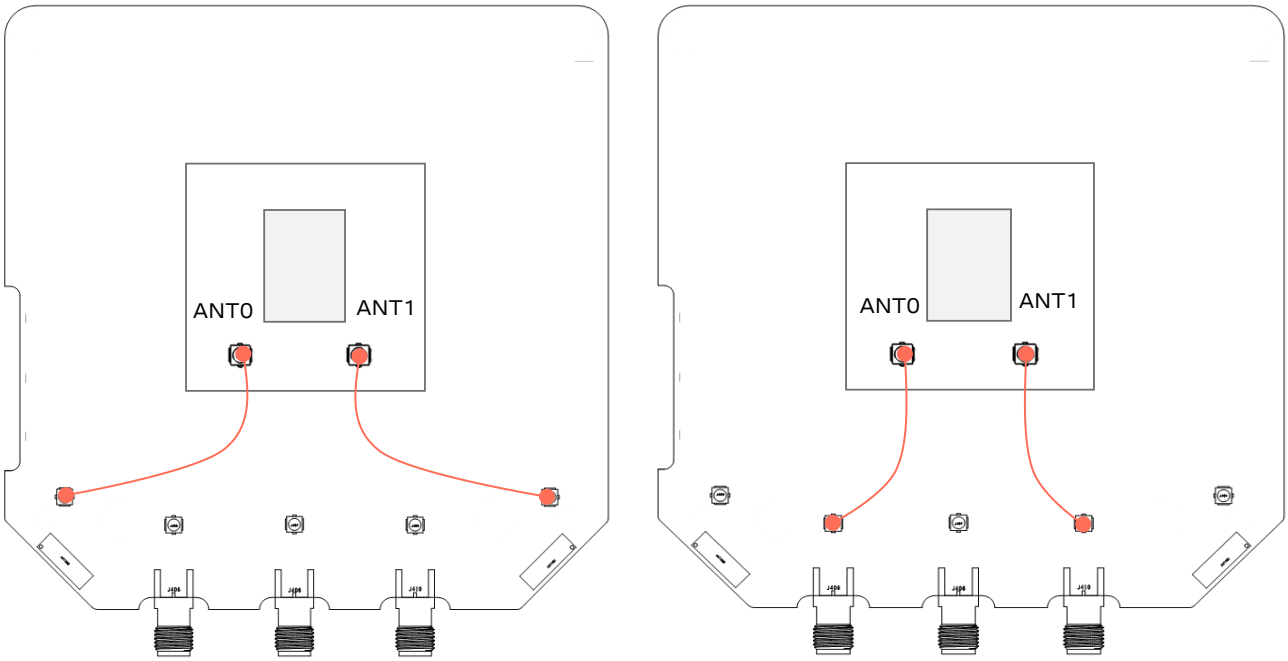


Figure 18: Connection of pig-tail coaxial cables with the U.FL connectors for internal antennas (left) or SMA connectors (right).

3.10 LEDs

Table 14 describes the function and description of the available LEDs on the EVK-JODY-W2 evaluation board.

Function	Description	Designator	Color
3V3	Main power supply (VBAT) status indication	D402	Green
VIO	VIO Supply (1.8 V or 3.3 V)	D403	Green
1V8	Aanalog power supply and SDIO (1V8)	D404	Green
VDD_3V3	Board voltage to supply for audio codecs, LEDs	D405	Green

Table 14: LED Description

Remove jumper **J411** for accurate power measurement of the average power in low power sleep modes. With the jumper removed all LEDs will be off.

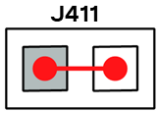


Figure 19: LED selection option

3.11 Schematics

The schematics for the JODY-W2 evaluation board (carrier board, module board and level shifter) can be shared with the customers upon request. Contact your local support team for further information.

Appendix

A Glossary

Abbreviation	Definition
EVB	Evaluation board
EVK	Evaluation kit
HCI	Host controller interface
I/O	Input / output
I2S	Inter-Integrated circuit sound
LED	Light-Emitting Diode
LDO	Low-dropout regulator
LPO	Low-power oscillator
LTE	Long-Term Evolution
MAC	Medium access control
MIMO	Multiple input multiple output
MMC	Multimedia card
PC	Personal computer
PCI	Peripheral component interconnect
PCIe	Peripheral component interconnect express
PCM	Pulse-code modulation
SD	Secure digital
SDIO	Secure digital input output
UART	Universal asynchronous receiver/transmitter
USB	Universal serial bus
Wi-Fi	Wireless local area network
ZIF	Zero Insertion Force
HS	High Speed (SDIO mode)
UHS	Ultra-High Speed (SDIO mode)

Table 15: Explanation of the abbreviations and terms used

Related documents

[1] JODY-W2 series data sheet, UBX-18017567
[2] JODY-W2 system integration manual, UBX-18068879
[3] JODY-W2 level shifter integration application note, UBX-19034257
[4] EVK-JODY-W2 schematics.
[5] Connector for the power jack, terminal connector and power jack
[6] Embedded Linux for i.MX Applications Processors
[7] NXP UM11490 - Feature Configuration Guide for NXP-based Wireless Modules on i.MX 8M Quad EVK
[8] MCUXpresso Software Development Kit (SDK)

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Revision history

Revision	Date	Name	Comments
R01	16-Jul-2019	aheg	Initial release.
R02	18-Oct-2019	aheg	Updated some diagrams and schematics based on the new EVK. Updated information about configuring the bootstrapping options, voltage level jumpers etc. Also updated the design files as per the latest design. Removed references to SDIO pull-up resistors.
R03	8-Jul-2020	aheg	Revised to reflect the latest module board used in the EVK for validating the engineering sample of the JODY-W2 module. Updated to include the revised schematics for the C.R2 version of the carrier board.
R04	4-Dec-2020	aheg	Added full-sized SDIO adapter in Table 2: EVK-JODY-W2 component list; revised Wi-Fi host interface in sections 2.3 and 2.4; revised Figure 6 and Figure 18 to show carrier and module and pig-tail coaxial cable connections with U.FL adapters; removed obsolete WLAN/BT LED notifications in Table 14; removed resolved issues in known issues list.
R05	19-Feb-2021	aheg	Included changes in the section 1 as per the Rev. D design of the EVK. Additional power jack to connect with a power jack is included on the carrier board. Details are explained in section 3.3.
R06	9-Nov-2022	sebs	Extended document scope to included JODY-W263-10B reflected in Table 1. Updated Software, Power supply configuration, and Control lines. Table 1. Reorganized Kit description chapter to include Operating conditions. Updated Software and added Driver source code information. Revised and added additional designator descriptions in Jumpers and connectors. Updated Host interface for Wi-Fi (3.3 V HS). Revised EVB power supply tree with other changes in Power supply configuration section. Added Selecting the EVB power supply and Bootstrapping sections. Revised Bluetooth host interface. Added connector information in Control lines section. Included changes in Antenna interfaces. Added references to the list of related documents and updated contact information.

Contact

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