THIS SPEC IS OBSOLETE

Spec No: 002-14948

Spec Title: CYW4334W - SINGLE-CHIP IEEE 802.11 B/G/N MAC/BASEBAND/ RADIO WITH INTEGRATED BLUETOOTH 4.0 (ADVANCE)

Replaced by: 002-15432

ADVANCE

CYW4334W

Single-Chip IEEE 802.11 b/g/n MAC/Baseband/ Radio with Integrated Bluetooth 4.0

The Cypress CYW4334W single-chip device provides the highest level of integration for a mobile or handheld wireless system, with integrated IEEE 802.11 b/g and single-stream IEEE 802.11n MAC/baseband/radio, and Bluetooth 4.0. It is designed to be used with external 2.4 GHz front-end modules that include power amplifiers, low-noise amplifiers, and T/R switches.

Using advanced design techniques and process technology to reduce active and idle power, the CYW4334W is designed to address the needs of highly mobile devices that require minimal power consumption and compact size. It includes a power management unit which simplifies the system power topology and allows for operation directly from a mobile platform battery while maximizing battery life.

The CYW4334W implements the highly sophisticated Enhanced Collaborative Coexistence algorithms and hardware mechanisms, allowing for an extremely collaborative Bluetooth coexistence scheme along with coexistence support for external radios (such as cellular, GPS, WiMAX, and Ultra-Wideband) and a single shared 2.4 GHz antenna for Bluetooth and WLAN. As a result, enhanced overall quality for simultaneous voice, video, and data transmission on a handheld system is achieved.

An SDIO v2.0 (including gSPI) host interface is provided for the WLAN section. An independent, high-speed UART is provided for the Bluetooth host interface.

Cypress part numbering

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

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Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM4334W	CYW4334W
BCM4334WKWBG	CYW4334WKWBG
BCM4334WKUBG	CYW4334WKUBG

Features

- IEEE 802.11x Key Features
  - Single-band 2.4 GHz IEEE 802.11 b/g/n
  - Single-stream IEEE 802.11n support for 20 MHz and 40 MHz channels provides PHY layer rates up to 150 Mbps for typical upper-layer throughput in excess of 90 Mbps.
  - Supports the IEEE 802.11n STBC (space-time block coding) and LDPC (low-density parity check) options for improved range and power efficiency.
  - Up to 11 RF control signals are available to support external PAs and LNAs.
  - Supports a single 2.4 GHz antenna shared between WLAN and Bluetooth.
  - Shared Bluetooth and WLAN receive signal path eliminates the need for an external power splitter while maintaining excellent sensitivity for both Bluetooth and WLAN.
  - Internal fractional nPLL allows support for a wide range of reference clock frequencies
  - Supports IEEE 802.15.2 external coexistence interface to optimize bandwidth utilization with other co-located wireless technologies such as GPS, WiMAX, or UWB
  - Improved Tx Out of Band emissions and Rx blocking performance for LTE coexistence.
  - Supports standard SDIO v2.0 and gSPI (48 MHz) host interfaces.
  - Integrated ARM® Cortex-M3™ processor and on-chip memory for complete WLAN subsystem functionality, minimizing the need to wake up the applications processor for standard WLAN functions. This allows for further minimization of power consumption, while maintaining the ability to field upgrade with future features. On-chip memory includes 512 KB SRAM and 640 KB ROM.
  - OneDriver™ software architecture for easy migration from existing embedded WLAN and Bluetooth devices as well as future devices.

Bluetooth Key Features

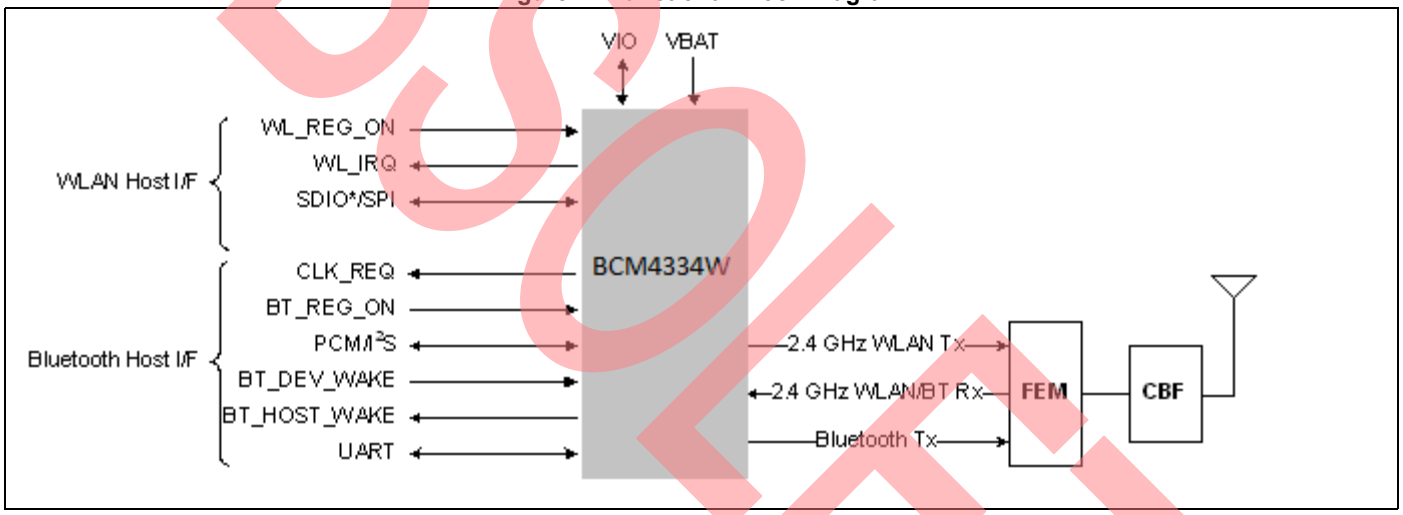
- Complies with Bluetooth Core Specification Version 4.0 + HS with provisions for supporting future specifications.
- Bluetooth Class 1 or Class 2 transmitter operation
- Supports extended Synchronous Connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
- Adaptive Frequency Hopping (AFH) for reducing radio frequency interference
- Interface support—Host Controller Interface (HCI) using a high-speed UART interface and PCM for audio data
- Low power consumption improves battery life of handheld devices.

- Supports multiple simultaneous Advanced Audio Distribution Profiles (A2DP) for stereo sound.
- Automatic frequency detection for standard crystal and TCXO values

General Features

- Supports battery voltage range from 2.3V to 4.8V supplies with internal switching regulator.
- Programmable dynamic power management
- 3072-bit One-Time Programmable (OTP) memory for storing board parameters
- 8 GPIOs on the WLBGA package, 16 GPIOs on the WLCSP package
- Package options:
- 109 ball WLBGA (4.08 mm × 4.48 mm, 0.4 mm pitch)
- 208 bump WLCSP low-profile (4.08 mm × 4.48 mm, 0.2 mm pitch)
- Security:
- WPA™ and WPA2™ (Personal) support for powerful encryption and authentication
- AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility
- Reference WLAN subsystem provides Cisco® Compatible Extensions (CCX, CCX 2.0, CCX 3.0, CCX 4.0, CCX 5.0)
- Reference WLAN subsystem provides Wi-Fi Protected Setup (WPS)
- Worldwide regulatory support: Global products supported with worldwide homologated design

Figure 1. Functional Block Diagram



IOT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (http://community.cypress.com/).

Contents

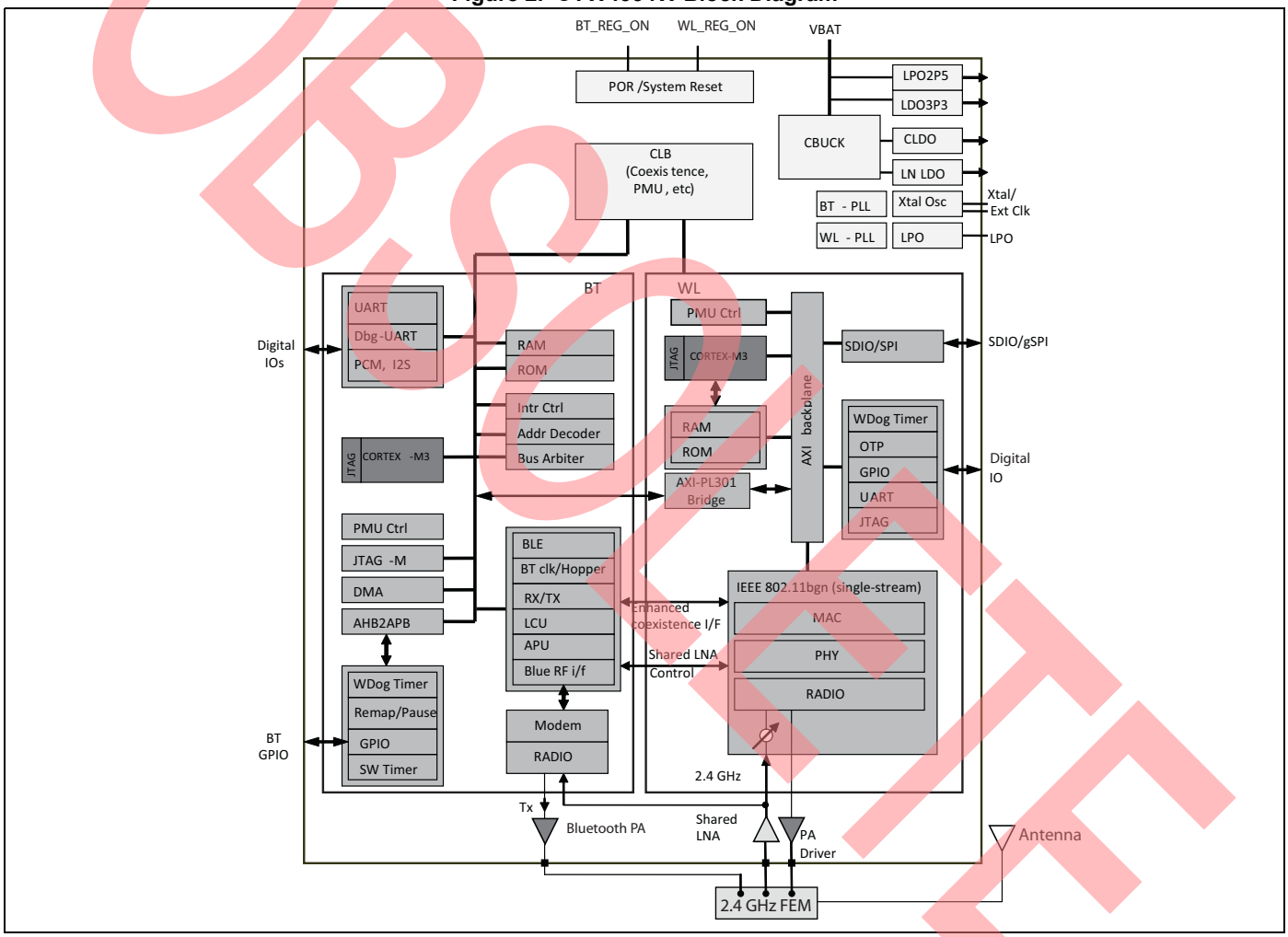
1. CYW4334W Overview

1.1 Introduction

The Cypress CYW4334W single-chip device provides the highest level of integration for a mobile and handheld wireless systems, with integrated IEEE 802.1 b/g/n MAC/baseband/radio, Bluetooth 4.0 + EDR (enhanced data rate). It provides a small form-factor solution with minimal external components to drive down cost for mass volumes and allows for handheld device flexibility in size, form, and function. Comprehensive power management circuitry and software ensure the system can meet the needs of highly mobile devices that require minimal power consumption and reliable operation.

Figure 2 shows the interconnect of all the major physical blocks in the CYW4334W and their associated external interfaces, which are described in greater detail in the following sections.

Figure 2. CYW4334W Block Diagram



1.2 Features

The CYW4334W supports the following features:

- IEEE 802.11b/g/n SINGLE-band radio
- Bluetooth v4.0 + EDR with integrated Class 1 PA
- Concurrent Bluetooth and WLAN operation
- On-chip WLAN driver execution capable of supporting IEEE 802.11 functionality
- Single- and dual-antenna support

- Single antenna with shared LNA
- Simultaneous Bluetooth/WLAN receive with single antenna

- WLAN host interface options:
  - SDIO v2.0
  - gSPI (up to 48 MHz clock rate)
- Bluetooth host digital interface (can be used concurrently with WLAN host interfaces; see above):
  - UART (up to 4 Mbps)
- ECI-enhanced coexistence support, ability to coordinate Bluetooth SCO transmissions around WLAN receives
- I^2S/PCM for Bluetooth audio
- HCI high-speed UART (H4, H4+, H5) transport support
- Wideband speech support (16 bits linear data, MSB first, left justified at 4K samples/s for transparent air coding, both through I^2S and PCM interface)
- Bluetooth SmartAudio® technology improves voice and music quality to headsets
- Bluetooth low power inquiry and page scan
- Bluetooth Low Energy (BLE) support
- Bluetooth Packet Loss Concealment (PLC)
- Bluetooth Wide Band Speech (WBS)
- Audio rate-matching algorithms
- Multiple simultaneous A2DP audio stream
- MP3, AAC on-chip decoder for low power music playback

1.3 Standards Compliance

The CYW4334W supports the following standards:

- Bluetooth 2.1 + EDR
- Bluetooth 3.0 + HS
- Bluetooth 4.0 (Bluetooth Low Energy)
- IEEE 802.11n (Handheld Device Class; Section 11)
- IEEE 802.11b
- IEEE 802.11g
- IEEE 802.11d
- IEEE 802.11h
- IEEE 802.11i

The CYW4334W will support the following future drafts/standards:

- IEEE 802.11r—Fast roaming (between APs)
- IEEE 802.11k—Resource management
- IEEE 802.11w—Secure management frames
- IEEE 802.11 extensions:
  - IEEE 802.11e QoS enhancements (as per the WMM® specification is already supported)
  - IEEE 802.11i MAC enhancements
  - IEEE 802.11r fast roaming support
  - IEEE 802.11k radio resource measurement

The CYW4334W supports the following security features and proprietary protocols:

- Security:
  - WEP
  - WPA™ Personal
  - WPA2™ Personal
  - WMM

- WMM-PS (U-APSD)
- WMM-SA
- WAPI
- AES (Hardware Accelerator)
- TKIP (HW Accelerator)
- CKIP (SW Support)

■ Proprietary Protocols:

- CCXv2
- CCXv3
- CCXv4
- CCXv5

■ IEEE 802.15.2 Coexistence Compliance—on silicon solution compliant with IEEE 3 wire requirements

1.4 Mobile Phone Usage Model

The CYW4334W incorporates a number of unique features to simplify integration into mobile phone platforms. Its flexible PCM and UART interfaces enable it to transparently connect with the existing circuits. In addition, the TCXO and LPO inputs allow the use of existing handset features to further minimize the size, power, and cost of the complete system.

■ The PCM interface provides multiple modes of operation to support both master and slave as well as hybrid interfacing to single or multiple external codec devices.

■ The UART interface supports hardware flow control with tight integration to power control sideband signaling to support the lowest power operation.

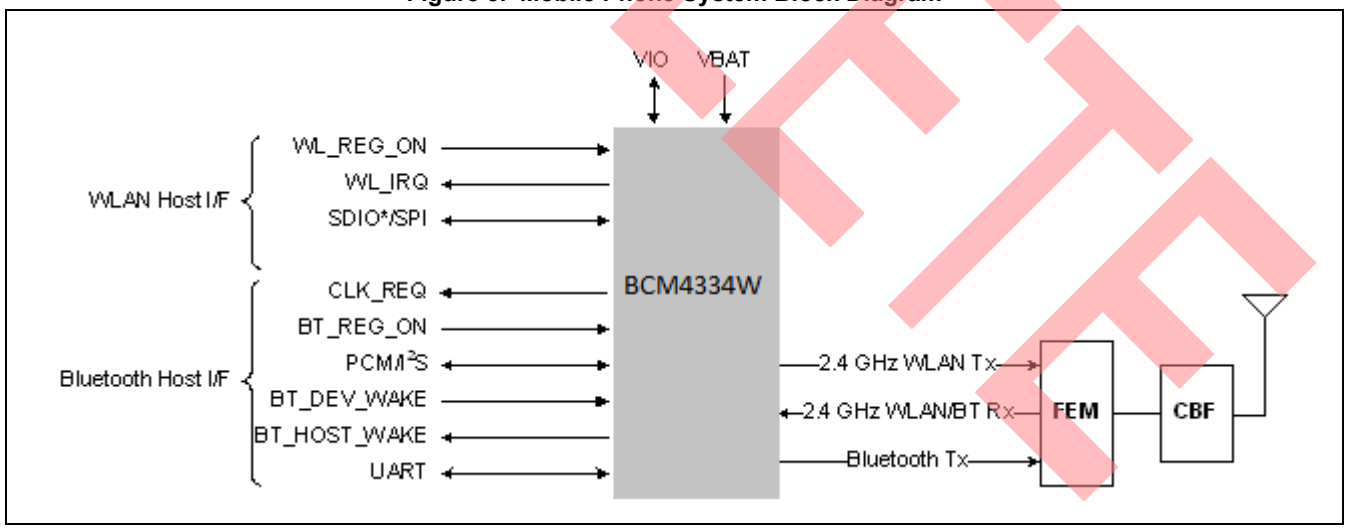
■ The TCXO interface accommodates any of the typical reference frequencies used by cell phones.

■ The highly linear design of the radio transceiver ensures that the device has the lowest spurious emissions output regardless of the state of operation. It has been fully characterized in the global cellular bands.

■ The transceiver design has excellent blocking (eliminating desensitization of the Bluetooth receiver) and intermodulation performance (distortion of the transmitted signal caused by the mixing of the cellular and Bluetooth transmissions) in the presence of a any cellular transmission (GSM®, GPRS, CDMA, WCDMA, or iDEN). Minimal external filtering is required for integration inside the handset.

The CYW4334W is designed to provide direct interface with new and existing handset designs as shown in Figure 3.

Figure 3. Mobile Phone System Block Diagram



2. Power Supplies and Power Management

2.1 Power Supply Topology

One Buck regulator, multiple LDO regulators, and a Power Management Unit (PMU) are integrated into the CYW4334W. All regulators are programmable via the PMU. These blocks simplify power supply design for Bluetooth and WLAN functions in embedded designs.

A single VBAT (2.3V to 4.8V) and VIO supply (1.8V to 3.3V) can be used, with all additional voltages being provided by the regulators in the CYW4334W.

Two control signals, BT_REG_ON and WL_REG_ON, are used to power-up the regulators and take the respective section out of reset. The CBUCK CLDO and LNLDO power up when any of the reset signals are deasserted. All regulators are powered down only when both BT_REG_ON and WL_REG_ON are deasserted. The CLDO and LNLDO may be turned off/on based on the dynamic demands of the digital baseband.

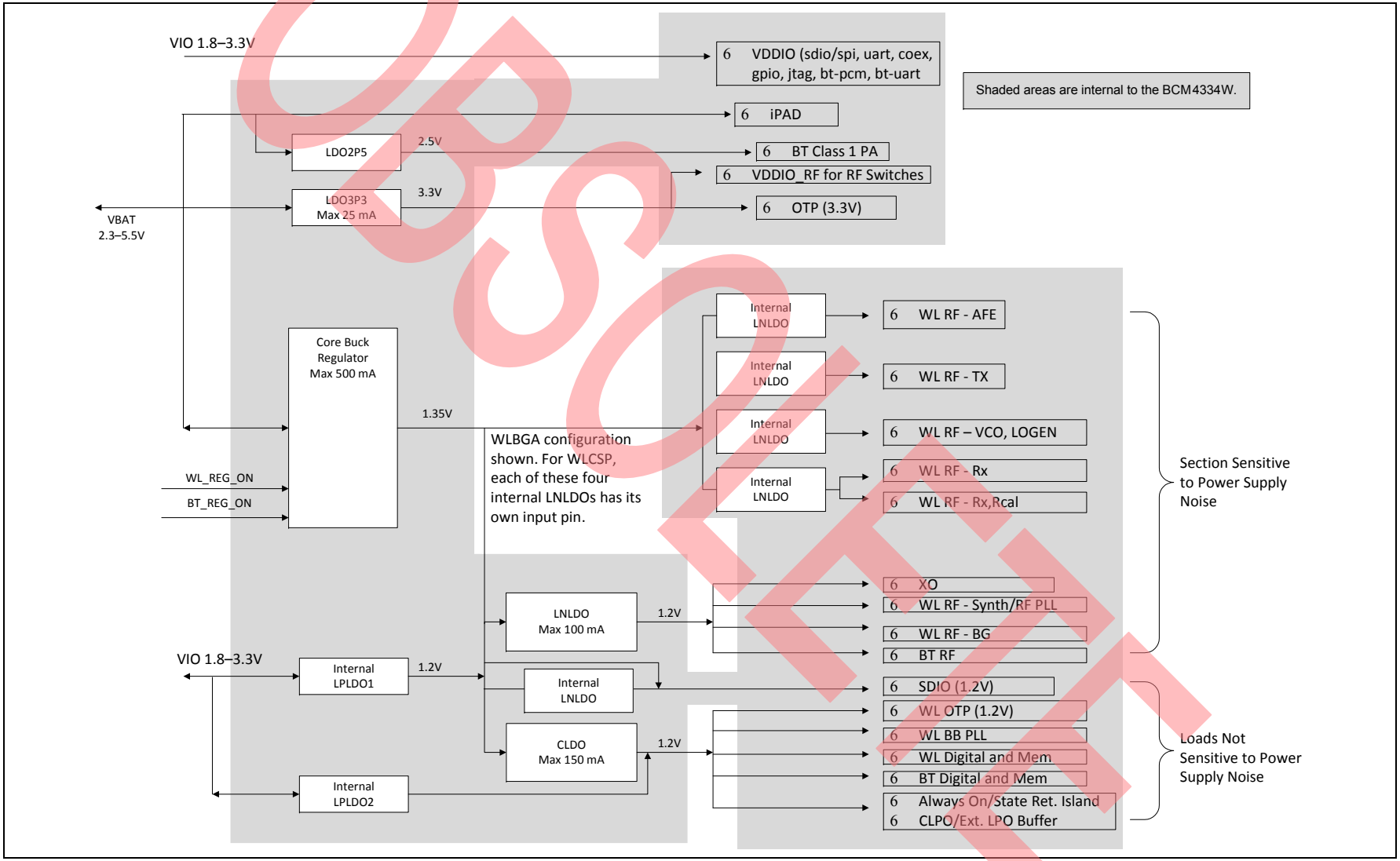
The CYW4334W allows for an extremely low power-consumption mode by completely shutting down the CBUCK, CLDO, and LNDLO regulators. When in this state, LPLDO1 and LPLDO2 (which are low-power linear regulators that are supplied by the system VIO supply) provide the CYW4334W with all the voltages it requires, further reducing leakage currents.

2.1.1 CYW4334W PMU Features

- VBAT to 1.35Vout (372 mA maximum) Core-Buck (CBUCK) switching regulator
- VBAT to 3.3Vout (50 mA maximum) LDO3P3 (external-capacitor)
- VBAT to 2.5Vout (70 mA maximum) LDO2P5 (external-capacitor)
- 1.35V to 1.2Vout (100 mA maximum) LNLDO (external-capacitor)
- 1.35V to 1.2Vout (150 mA maximum) CLDO (external-capacitor)
- Additional internal LDOs (not externally accessible)

Figure 4 shows the regulators and a typical power topology.

Figure 4. Typical Power Topology



2.2 WLAN Power Management

The CYW4334W has been designed with the stringent power consumption requirements of mobile devices in mind. All areas of the chip design are optimized to minimize power consumption. Silicon processes and cell libraries were chosen to reduce leakage current and supply voltages. Additionally, the CYW4334W integrated RAM is a high Vt memory with dynamic clock control. The dominant supply current consumed by the RAM is leakage current only. Additionally, the CYW4334W includes an advanced WLAN power management unit (PMU) sequencer. The PMU sequencer provides significant power savings by putting the CYW4334W into various power management states appropriate to the current environment and activities that are being performed. The power management unit enables and disables internal regulators, switches, and other blocks based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them. Power up sequences are fully programmable. Configurable, free-running counters (running at 32.768 kHz LPO clock) in the PMU sequencer are used to turn on/turn off individual regulators and power switches. Clock speeds are dynamically changed (or gated altogether) for the current mode. Slower clock speeds are used wherever possible.

The CYW4334W WLAN power states are described as follows:

- Active mode—All WLAN blocks in the CYW4334W are powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.
- Doze mode—The radio, analog domains, and most of the linear regulators are powered down. The rest of the CYW4334W remains powered up in an IDLE state. All main clocks (PLL, crystal oscillator or TCXO) are shut down to reduce active power to the minimum. The 32.768 kHz LPO clock is available only for the PMU sequencer. This condition is necessary to allow the PMU sequencer to wake up the chip and transition to Active mode. In Doze mode, the primary power consumed is due to leakage current.
- Deep-sleep mode—Most of the chip including both analog and digital domains and most of the regulators are powered off. Logic states in the digital core are saved and preserved into a retention memory in the always-ON domain before the digital core is powered off. Upon a wake-up event triggered by the PMU timers, an external interrupt or a host resume through the SDIO bus, logic states in the digital core are restored to their pre-deep-sleep settings to avoid lengthy hardware reinitialization.
- Power-down mode—The CYW4334W is effectively powered off by shutting down all internal regulators. The chip is brought out of this mode by external logic re-enabling the internal regulators.

2.3 PMU Sequencing

The PMU sequencer is responsible for minimizing system power consumption. It enables and disables various system resources based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them.

Resource requests may come from several sources: clock requests from cores, the minimum resources defined in the ResourceMin register, and the resources requested by any active resource request timers. The PMU sequencer maps clock requests into a set of resources required to produce the requested clocks.

Each resource is in one of four states: enabled, disabled, transition_on, and transition_off and has a timer that contains 0 when the resource is enabled or disabled and a non-zero value in the transition states. The timer is loaded with the time_on or time_off value of the resource when the PMU determines that the resource must be enabled or disabled. That timer decrements on each 32.768 kHz PMU clock. When it reaches 0, the state changes from transition_off to disabled or transition_on to enabled. If the time_on value is 0, the resource can go immediately from disabled to enabled. Similarly, a time_off value of 0 indicates that the resource can go immediately from enabled to disabled. The terms enable sequence and disable sequence refer to either the immediate transition or the timer load-decrement sequence.

During each clock cycle, the PMU sequencer performs the following actions:

1. Computes the required resource set based on requests and the resource dependency table.
2. Decrements all timers whose values are non zero. If a timer reaches 0, the PMU clears the ResourcePending bit for the resource and inverts the ResourceState bit.
3. Compares the request with the current resource status and determines which resources must be enabled or disabled.
4. Initiates a disable sequence for each resource that is enabled, no longer being requested, and has no powered up dependents.
5. Initiates an enable sequence for each resource that is disabled, is being requested, and has all of its dependencies enabled.

2.4 Power-Off Shutdown

The CYW4334W provides a low-power shutdown feature that allows the device to be turned off while the host, and any other devices in the system, remain operational. When the CYW4334W is not needed in the system, VDDIO_RF and VDDC are shut down while VDDIO remains powered. This allows the CYW4334W to be effectively off while keeping the I/O pins powered so that they do not draw extra current from any other devices connected to the I/O.

During a low-power shut-down state, provided VDDIO remains applied to the CYW4334W, all outputs are tristated, and most inputs signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths

or create loading on any digital signals in the system, and enables the CYW4334W to be fully integrated in an embedded device and take full advantage of the lowest power-savings modes.

Two signals on the CYW4334W, the frequency reference input (WRF_XTAL_CAB_OP) and the LPO_IN input, are designed to be high-impedance inputs that do not load down the driving signal even if the chip does not have VDDIO power applied to it.

When the CYW4334W is powered on from this state, it is the same as a normal power-up and the device does not retain any information about its state from before it was powered down.

2.5 Power-Up/Power-Down/Reset Circuits

The CYW4334W has two signals (see Table 2) that enable or disable the Bluetooth and WLAN circuits and the internal regulator blocks, allowing the host to control power consumption. For timing diagrams of these signals and the required power-up sequences, see Section 20. “Power-Up Sequence and Timing,” on page 99.

Table 2. Power-Up/Power-Down/Reset Control Signals

Signal	Description
WL_REG_ON	This signal is used by the PMU (with BT_REG_ON) to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal CYW4334W regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low, the WLAN section is in reset. If BT_REG_ON and WL_REG_ON are both low, the regulators are disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
BT_REG_ON	This signal is used by the PMU (with WL_REG_ON) to decide whether or not to power down the internal CYW4334W regulators. If BT_REG_ON and WL_REG_ON are low, the regulators will be disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.

3. Frequency References

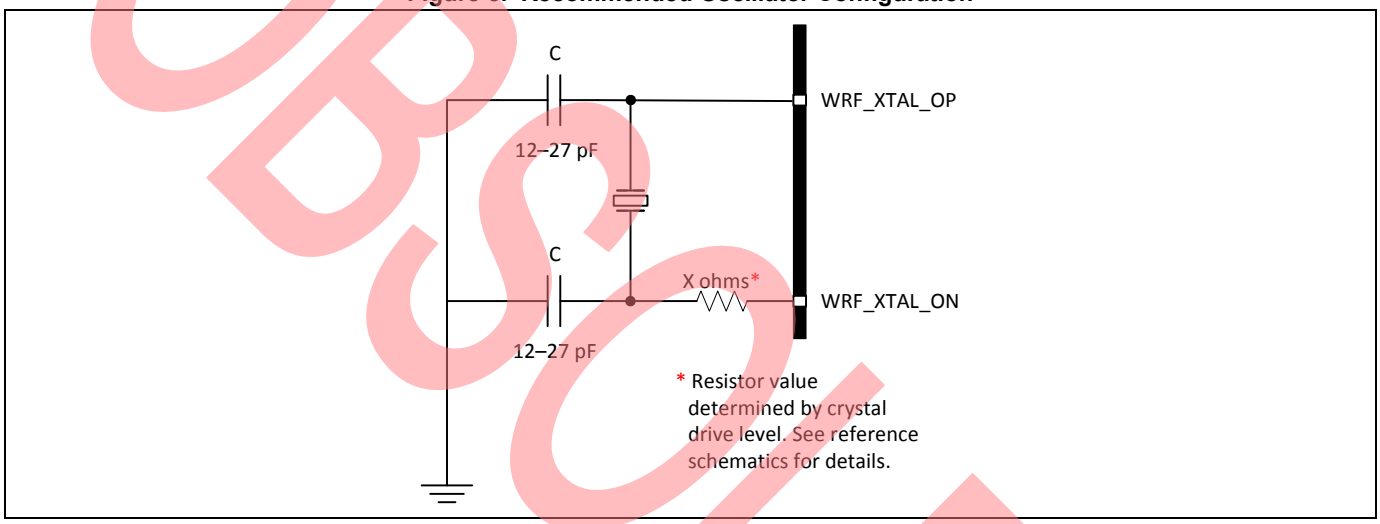
An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference driven by a temperature-compensated crystal oscillator (TCXO) signal may be used. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

Note: The crystal and TCXO implementations have different power supplies (WRF_XTAL_VDD1P2 for crystal, WRF_TCXO_VDD for TCXO).

3.1 Crystal Interface and Clock Generation

The CYW4334W can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator including all external components is shown in Figure 5. Consult the reference schematics for the latest configuration.

Figure 5. Recommended Oscillator Configuration



A fractional-N synthesizer in the CYW4334W generates the radio frequencies, clocks, and data/packet timing, enabling it to operate using a wide selection of frequency references.

For SDIO applications, the default frequency reference is a 37.4 MHz crystal or TCXO. The signal characteristics for the crystal interface are listed in Table 3 on page 13.

Note: Although the fractional-N synthesizer can support alternative reference frequencies, frequencies other than the default require support to be added in the driver, plus additional extensive system testing. Contact Cypress for further details.

3.2 TCXO

As an alternative to a crystal, an external precision TCXO can be used as the frequency reference, provided that it meets the Phase Noise requirements listed in Table 3 on page 13. When the clock is provided by an external TCXO, there are two possible connection methods, as shown in Figure 6 and Figure 7:

1. If the TCXO is dedicated to driving the CYW4334W, it should be connected to the WRF_XTAL_OP pin through an external 1000 pF coupling capacitor, as shown in Figure 6. The internal clock buffer connected to this pin will be turned OFF when the CYW4334W goes into sleep mode. When the clock buffer turns ON and OFF there will be a small impedance variation. Power must be supplied to the WRF_XTAL_VDD1P2 pin.
2. For 2.4 GHz operation only, an alternative is to DC-couple the TCXO to the WRF_TCXO_CK pin, as shown in Figure 7. Use this method when the same TCXO is shared with other devices and a change in the input impedance is not acceptable because it may cause a frequency shift that cannot be tolerated by the other device sharing the TCXO. This pin is connected to a clock buffer powered from WRF_TCXO_VDD. If the power supply to this buffer is always on (even in sleep mode), the clock buffer is always on, thereby ensuring a constant input impedance in all states of the device. The maximum current drawn from WRF_TCXO_VDD is approximately 500 µA.

Figure 6. Recommended Circuit to Use with an External Dedicated TCXO

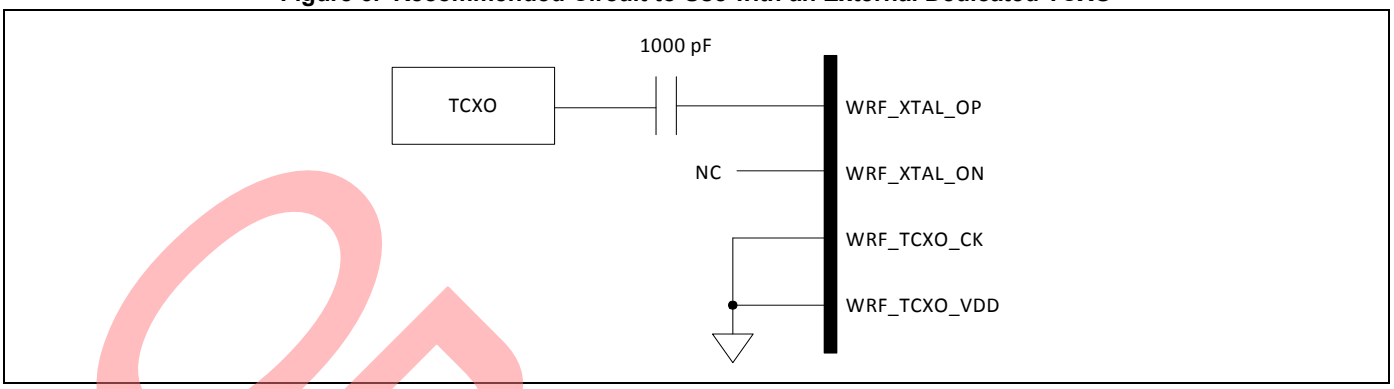
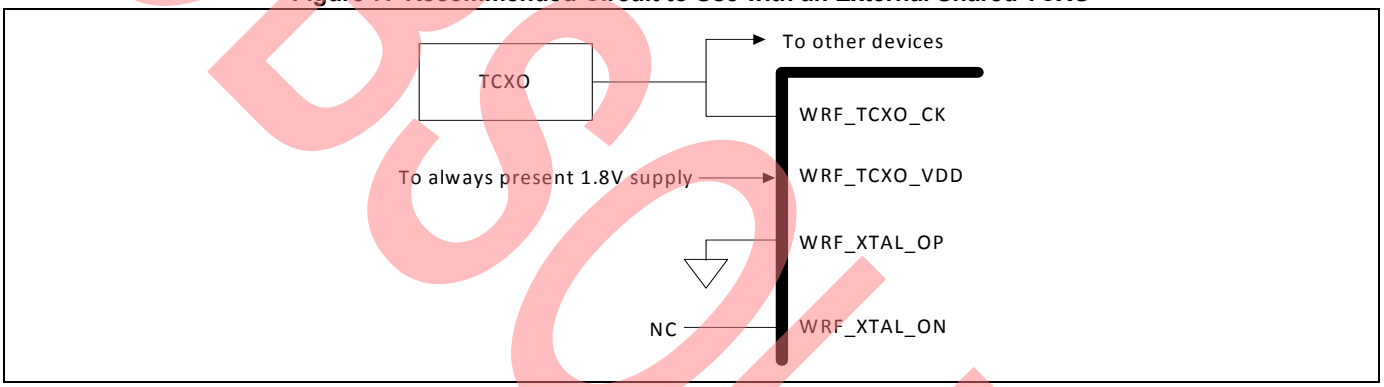


Figure 7. Recommended Circuit to Use with an External Shared TCXO



3.3 Frequency Selection

Table 3. Crystal Oscillator and External Clock – Requirements and Performance

Parameter	Conditions/Notes	*Crystal*[a]			*External Frequency Reference*[b c]			
		Min	Typ	Max	Min	Typ	Max	Units
Frequency	–	Between 12 MHz and 52 MHz[d,e]						
Crystal load capacitance	–	–	12	–	–	–	–	pF
ESR	–	–	–	60	–	–	–	Ω
Drive level	External crystal requirement	200[f]	–	–	–	–	–	µW
Input impedance (WRF_XTAL_OP)	Resistive	30	100	–	30	100	–	kΩ
	Capacitive	–	–	7.5	–	–	7.5	pF
Input impedance (WRF_TCXO_IN)	Resistive	–	–	–	30k	100	–	Ω
	Capacitive	–	–	–	–	–	4	pF
WRF_XTAL_OP Input low level	DC-coupled digital signal	–	–	–	0	–	0.2	V
WRF_XTAL_OP Input high level	DC-coupled digital signal	–	–	–	1.0	–	1.26	V
WRF_XTAL_OP input voltage	AC-coupled analog signal (see Figure 6 on page 12)	–	–	–	400	–	1200	mV_{p-p}
WRF_TCXO_IN Input voltage	DC-coupled analog signal (see Figure 7 on page 12)	–	–	–	400	–	1980	mV_{p-p}
Frequency tolerance over the lifetime of the equipment, including temperature	Without trimming	–20	–	20	–20	–	20	ppm
Duty cycle	37.4 MHz clock	–	–	–	40	50	60	%
Phase noise (802.11b/g)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–131	dBc/Hz
	37.4 MHz clock at 100 kHz or greater offset	–	–	–	–	–	–138	dBc/Hz
Phase noise (802.11n, 2.4 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–136	dBc/Hz
	37.4 MHz clock at 100 kHz or greater offset	–	–	–	–	–	–143	dBc/Hz

a. (Crystal) Use WRF_XTAL_OP and WRF_XTAL_ON, internal power to pin WRF_XTAL_VDD1P2.
b. (TCXO) See "TCXO" on page 11 for alternative connection methods.
c. For a clock reference other than 37.4 MHz, 20 × log10(f/ 37.4) dB should be added to the limits, where f = the reference clock frequency in MHz.
d. BT_TM6 should be tied low for a 52 MHz clock reference. For other frequencies, BT_TM6 should be tied high. Note that 52 MHz is not an auto-detected frequency using the LPO clock.
e. The frequency step size is approximately 80 Hz resolution.
f. The crystal should be capable of handling a 200uW drive level from the CYW4334W.

Any frequency within the ranges specified for the crystal and TCXO reference may be used. These include not only the standard handset reference frequencies of 12, 13, 14.4, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8, 20, 26, 37.4, and 52 MHz, but also other frequencies in this range, with approximately 80 Hz resolution. The CYW4334W must have the reference frequency set correctly in order for any of the UART or PCM interfaces to function correctly, since all bit timing is derived from the reference frequency.

Note: The fractional-N synthesizer can support many reference frequencies. However, frequencies other than the default require support to be added in the driver plus additional, extensive system testing. Contact Cypress for further details.

The reference frequency for the CYW4334W may be set in the following ways:

■ Set the *xtalfreq=xxxxx* parameter in the nvram.txt file (used to load the driver) to correctly match the crystal frequency.

■ Auto-detect any of the standard handset reference frequencies using an external LPO clock.

For applications such as handsets and portable smart communication devices, where the reference frequency is one of the standard frequencies commonly used, the CYW4334W automatically detects the reference frequency and programs itself to the correct reference frequency. In order for auto frequency detection to work correctly, the CYW4334W must have a valid and stable 32.768 kHz LPO clock that meets the requirements listed in Table 4 on page 14 and is present during power-on reset.

3.4 External 32.768 kHz Low-Power Oscillator

The CYW4334W uses a secondary low frequency clock for low-power-mode timing. Either the internal low-precision LPO or an external 32.768 kHz precision oscillator is required. The internal LPO frequency range is approximately 33 kHz ± 30% over process, voltage, and temperature, which is adequate for some applications. However, a trade-off caused by this wide LPO tolerance is a small current consumption increase during WLAN power save mode that is incurred by the need to wake up earlier to avoid missing beacons. Whenever possible, the preferred approach for WLAN is to connect a precision external 32.768 kHz clock to the LPO_IN pin that meets the requirements listed in Table 4 .

Note: Bluetooth operations require the use of an external LPO that meets the requirements listed in Table 4 .

Table 4. External 32.768 kHz Sleep Clock Specifications

Parameter	LPO Clock	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	±200	ppm
Duty cycle	30 – 70	%
Input signal amplitude	200 – 3300	mV, p-p
Input impedance[a, b]	> 100	kΩ
	< 5	pF
Signal type	Square-wave or sine-wave	–
Clock jitter (during initial start-up)	< 10,000	ppm

a. This pin is internally ac coupled.
b. When power is applied or switched off.

4. Bluetooth Subsystem Overview

The Cypress CYW4334W is a Bluetooth 4.0 + EDR-compliant, baseband processor/2.4 GHz transceiver. It features the highest level of integration and eliminates all critical external components, thus minimizing the footprint, power consumption, and system cost of a Bluetooth solution.

The CYW4334W is the optimal solution for any Bluetooth voice and/or data application. The Bluetooth subsystem presents a standard Host Controller Interface (HCI) via a high speed UART and PCM for audio. The CYW4334W incorporates all Bluetooth 4.0 features including Secure Simple Pairing, Sniff Subrating, and Encryption Pause and Resume.

The CYW4334W Bluetooth radio transceiver provides enhanced radio performance to meet the most stringent mobile phone temperature applications and the tightest integration into mobile handsets and portable devices. It is fully compatible with any of the standard TCXO frequencies and provides full radio compatibility to operate simultaneously with GPS, WLAN, and cellular radios.

The Bluetooth transmitter also features a Class 1 power amplifier with Class 2 capability.

4.1 Features

Major Bluetooth features of the CYW4334W include:

- Supports key features of upcoming Bluetooth standards
- Fully supports Bluetooth Core Specification version 4.0 + (Enhanced Data Rate) EDR features:
  - Adaptive Frequency Hopping (AFH)
  - Quality of Service (QoS)
  - Extended Synchronous Connections (eSCO)—Voice Connections
  - Fast Connect (interlaced page and inquiry scans)
  - Secure Simple Pairing (SSP)
  - Sniff Subrating (SSR)
  - Encryption Pause Resume (EPR)
  - Extended Inquiry Response (EIR)
  - Link Supervision Timeout (LST)
- UART baud rates up to 4 Mbps
- Supports all Bluetooth 4.0 + HS packet types
- Supports maximum Bluetooth data rates over HCI UART
- Multipoint operation with up to seven active slaves
  - Maximum of seven simultaneous active ACL links
  - Maximum of three simultaneous active SCO and eSCO connections with scatternet support
- Trigger Cypress fast connect (TBFC)
- Narrowband and wideband packet loss concealment
- Scatternet operation with up to four active piconets with background scan and support for scatter mode
- High-speed HCI UART transport support with low-power out-of-band BT_DEV_WAKE and BT_HOST_WAKE signaling (see "Host Controller Power Management" on page 18)
- Channel quality driven data rate and packet type selection
- Standard Bluetooth test modes
- Extended radio and production test mode features
- Full support for power savings modes
  - Bluetooth clock request
  - Bluetooth standard sniff
  - Deep-sleep modes and software regulator shutdown
  - TCXO input and auto-detection of all standard handset clock frequencies. Also supports a low-power crystal, which can be used during power save mode for better timing accuracy.

4.2 Bluetooth Radio

The CYW4334W has an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with the Bluetooth Radio Specification and EDR specification and meets or exceeds the requirements to provide the highest communication link quality of service.

4.2.1 Transmit

The CYW4334W features a fully integrated zero-IF transmitter. The baseband transmit data is GFSK-modulated in the modem block and upconverted to the 2.4 GHz ISM band in the transmitter path. The transmitter path consists of signal filtering, I/Q upconversion, output power amplifier, and RF filtering. The transmitter path also incorporates π/4−DQPSK for 2 Mbps and 8−DPSK for 3 Mbps to support EDR. The transmitter section is compatible to the Bluetooth Low Energy specification. The transmitter PA bias can also be adjusted to provide Bluetooth class 1 or class 2 operation.

4.2.2 Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK, π/4−DQPSK, and 8−DPSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

4.2.3 Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit-synchronization algorithm.

4.2.4 Power Amplifier

The fully integrated PA supports Class 1 or Class 2 output using a highly linearized, temperature-compensated design. This provides greater flexibility in front-end matching and filtering. Due to the linear nature of the PA combined with some integrated filtering, external filtering is required to meet the Bluetooth and regulatory harmonic and spurious requirements. For integrated mobile handset applications in which Bluetooth is integrated next to the cellular radio, external filtering can be applied to achieve near thermal noise levels for spurious and radiated noise emissions. The transmitter features a sophisticated on-chip transmit signal strength indicator (TSSI) block to keep the absolute output power variation within a tight range across process, voltage, and temperature.

4.2.5 Receiver

The receiver path uses a low-IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology with built-in out-of-band attenuation enables the CYW4334W to be used in most applications with minimal off-chip filtering. For integrated handset operation, in which the Bluetooth function is integrated close to the cellular transmitter, external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

4.2.6 Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

4.2.7 Receiver Signal Strength Indicator

The radio portion of the CYW4334W provides a Receiver Signal Strength Indicator (RSSI) signal to the baseband, so that the controller can take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

4.2.8 Local Oscillator Generation

Local Oscillator (LO) generation provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The LO generation subblock employs an architecture for high immunity to LO pulling during PA operation. The CYW4334W uses an internal RF and IF loop filter.

4.2.9 Calibration

The CYW4334W radio transceiver features an automated calibration scheme that is fully self contained in the radio. No user interaction is required during normal operation or during manufacturing to provide the optimal performance. Calibration optimizes the performance of all the major blocks within the radio to within 2% of optimal conditions, including gain and phase characteristics of filters, matching between key components, and key gain blocks. This takes into account process variation and temperature variation. Calibration occurs transparently during normal operation during the settling time of the hops and calibrates for temperature variations as the device cools and heats during normal operation in its environment.

5. Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements all of the time critical functions required for high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types, and HCI command types.

The following transmit and receive functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data before sending over the air:

- Symbol timing recovery, data deframing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data dewhitening in the receiver.
- Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening in the transmitter.

5.1 Bluetooth 4.0 Features

The BBC supports all Bluetooth 4.0 features, with the following benefits:

- Dual-mode bluetooth Low Energy (BT and BLE operation)
- Extended Inquiry Response (EIR): Shortens the time to retrieve the device name, specific profile, and operating mode.
- Encryption Pause Resume (EPR): Enables the use of Bluetooth technology in a much more secure environment.
- Sniff Subrating (SSR): Optimizes power consumption for low duty cycle asymmetric data flow, which subsequently extends battery life.
- Secure Simple Pairing (SSP): Reduces the number of steps for connecting two devices, with minimal or no user interaction required.
- Link Supervision Time Out (LSTO): Additional commands added to HCI and Link Management Protocol (LMP) for improved link time-out supervision.
- QoS enhancements: Changes to data traffic control, which results in better link performance. Audio, human interface device (HID), bulk traffic, SCO, and enhanced SCO (eSCO) are improved with the erroneous data (ED) and packet boundary flag (PBF) enhancements.

5.2 Bluetooth Low Energy

The CYW4334W is forward compatible with the impending Bluetooth Low Energy operating mode, which provides a dramatic reduction in the power consumption of the Bluetooth radio and baseband. The primary application for this mode is to provide support for low data rate devices, such as sensors and remote controls.

5.3 Link Control Layer

The link control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the link control unit (LCU). This layer consists of the command controller that takes commands from the software, and other controllers that are activated or configured by the command controller, to perform the link control tasks. Each task performs a different state in the Bluetooth Link Controller.

- Major states:
  - Standby
  - Connection
- Substates:
  - Page
  - Page Scan
  - Inquiry
  - Inquiry Scan
  - Sniff

5.4 Test Mode Support

The CYW4334W fully supports Bluetooth Test mode as described in Part I:1 of the *Specification of the Bluetooth System Version 3.0*. This includes the transmitter tests, normal and delayed loopback tests, and reduced hopping sequence.

In addition to the standard Bluetooth Test Mode, the CYW4334W also supports enhanced testing features to simplify RF debugging and qualification and type-approval testing. These features include:

- Fixed frequency carrier wave (unmodulated) transmission

- ❒ Simplifies some type-approval measurements (Japan)
- ❒ Aids in transmitter performance analysis

■ Fixed frequency constant receiver mode
- ❒ Receiver output directed to I/O pin
- ❒ Allows for direct BER measurements using standard RF test equipment
- ❒ Facilitates spurious emissions testing for receive mode

■ Fixed frequency constant transmission
- ❒ Eight-bit fixed pattern or PRBS-9
- ❒ Enables modulated signal measurements with standard RF test equipment

5.5 Bluetooth Power Management Unit

The Bluetooth Power Management Unit (PMU) provides power management features that can be invoked by either software through power management registers or packet handling in the baseband core. The power management functions provided by the CYW4334W are:

■ RF Power Management

■ Host Controller Power Management

■ BBC Power Management

5.5.1 RF Power Management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4 GHz transceiver. The transceiver then processes the power-down functions accordingly.

5.5.2 Host Controller Power Management

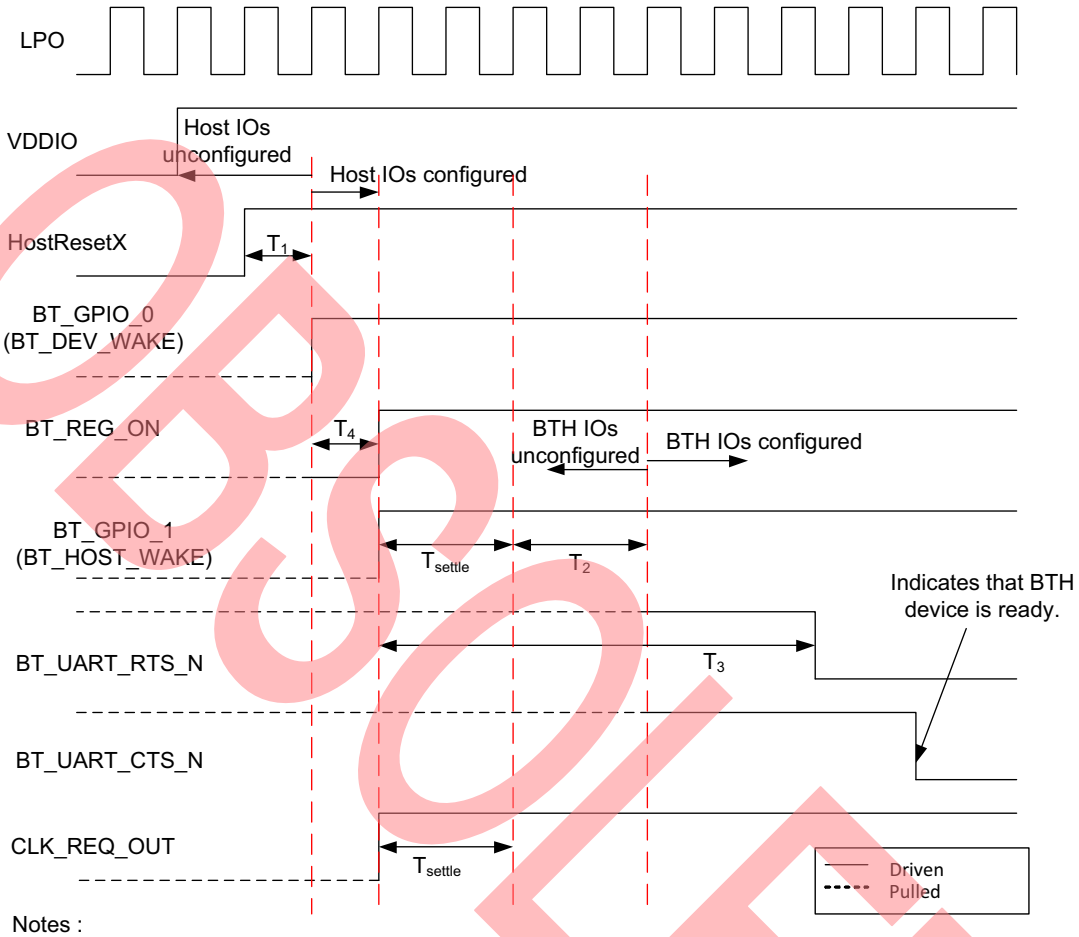
When running in UART mode, the CYW4334W can be configured so that dedicated signals are used for power management handshaking between the CYW4334W and the host. The basic power saving functions supported by those hand-shaking signals include the standard Bluetooth defined power savings modes and standby modes of operation.

Note: Table 5 describes the power-control hand-shake signals used with the UART interface. The pad function control register is set to 0 for these pins (see "Multiplexed Bluetooth GPIO Signals" on page 66 for details).

Table 5. Power Control Pin Description

Signal	Mapped to Pin	Type	Description
BT_DEV_WAKE	BT_GPIO_0	I	Bluetooth device wake-up: Signal from the host to the CYW4334W indicating that the host requires attention. Asserted: The Bluetooth device must wake-up or remain awake. Deasserted: The Bluetooth device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
BT_HOST_WAKE	BT_GPIO_1	O	Host wake up. Signal from the CYW4334W to the host indicating that the CYW4334W requires attention. Asserted: Host device must wake-up or remain awake. Deasserted Host device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
CLK_REQ	BT_CLK_REQ_OUT WL_CLK_REQ_OUT	O	The CYW4334W asserts CLK_REQ when Bluetooth or WLAN wants the host to turn on the reference clock. The CLK_REQ polarity is active-high. Add an external 100 kΩ pull-down resistor to ensure the signal is deasserted when the CYW4334W powers up or resets when VDDIO is present.

Figure 8. Startup Signaling Sequence



Notes :

- T_1 is the time for host to settle its IOs after a reset.
- T_2 is the time for the BTH device to settle its IOs after a reset and ref clk settling time elapsed.
- T_3 is the time for the BT device to complete initialization and drive BT_UART_RTS_N low.
- T_4 is the setup time for BT_WAKE prior to driving BT_REG_ON high; BT_DEV_WAKE must be high prior to BT_REG_ON being released. BT_DEV_WAKE should not be driven low until after the host has completed configuration.
- T_{settle} is the time for the ref clk signal from the host to be guaranteed to have settled.

5.5.3 BBC Power Management

The following are low-power operations for the BBC:

- Physical layer packet-handling turns the RF on and off dynamically within transmit/receive packets.
- Bluetooth-specified low-power connection modes: sniff, hold, and park. While in these modes, the CYW4334W runs on the low-power oscillator and wakes up after a predefined time period.
- A low-power shutdown feature allows the device to be turned off while the host and any other devices in the system remain operational. When the CYW4334W is not needed in the system, the RF and core supplies are shut down while the I/O remains powered. This allows the CYW4334W to effectively be off while keeping the I/O pins powered so they do not draw extra current from any other devices connected to the I/O.

During the low-power shut-down state, provided VDDIO remains applied to the CYW4334W, all outputs are tri-stated, and most input signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths

or create loading on any digital signals in the system and enables the CYW4334W to be fully integrated in an embedded device to take full advantage of the lowest power-saving modes.

Two CYW4334W input signals are designed to be high-impedance inputs that do not load the driving signal even if the chip does not have VDDIO power supplied to it: the frequency reference input (WRF_TCXO_IN) and the 32.768 kHz input (LPO). When the CYW4334W is powered on from this state, it is the same as a normal power-up, and the device does not contain any information about its state from the time before it was powered down.

5.5.4 Wideband Speech

The CYW4334W provides support for wideband speech (WBS) using on-chip Smart Audio technology. The CYW4334W can perform subband-codec (SBC), as well as mSBC, encoding and decoding of linear 16 bits at 16 kHz (256 Kbps rate) transferred over the PCM bus.

5.5.5 Packet Loss Concealment

Packet Loss Concealment (PLC) improves apparent audio quality for systems with marginal link performance. Bluetooth messages are sent in packets. When a packet is lost, it creates a gap in the received audio bit-stream. Packet loss can be mitigated in several ways:

- Fill in zeros.
- Ramp down the output audio signal toward zero (this is the method used in current Bluetooth headsets).
- Repeat the last frame (or packet) of the received bit-stream and decode it as usual (frame repeat).

These techniques cause distortion and popping in the audio stream. The CYW4334W uses a proprietary waveform extension algorithm to provide dramatic improvement in the audio quality. Figure 10 and Figure 10 show audio waveforms with and without Packet Loss Concealment. Cypress PLC/BEC algorithms also support wide band speech.

Figure 9. CVSD Decoder Output Waveform Without PLC

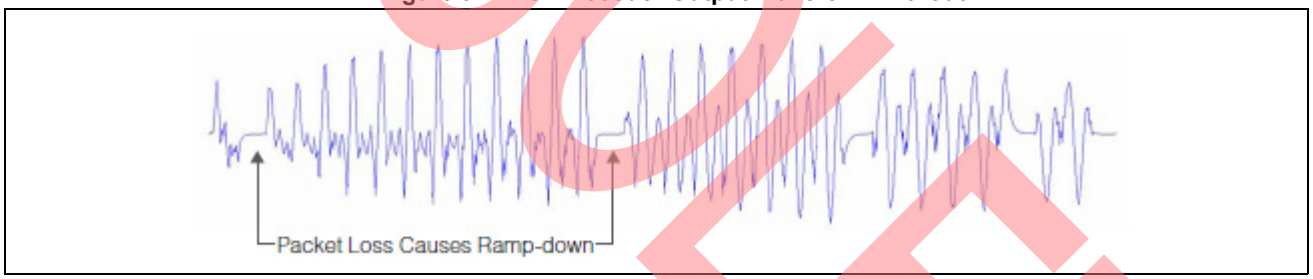
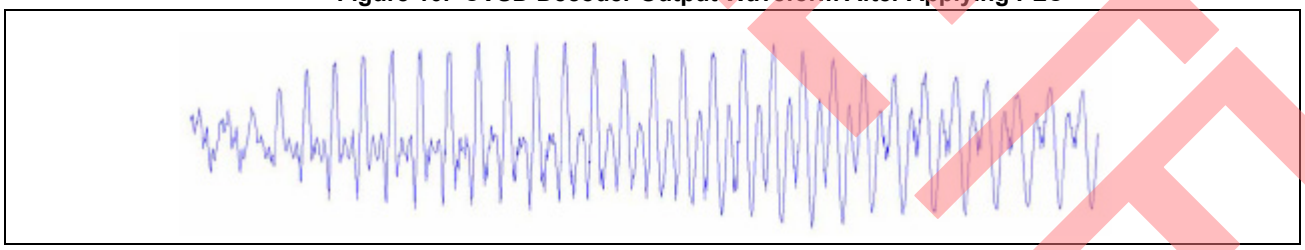


Figure 10. CVSD Decoder Output Waveform After Applying PLC



5.5.6 Audio Rate-Matching Algorithms

The CYW4334W has an enhanced rate-matching algorithm that uses interpolation algorithms to reduce audio stream jitter that may be present when the rate of audio data coming from the host is not the same as the Bluetooth audio data rates.

5.5.7 Codec Encoding

The CYW4334W can support SBC and mSBC encoding and decoding for wideband speech.

5.5.8 Multiple Simultaneous A2DP Audio Stream

The CYW4334W has the ability to take a single audio stream and output it to multiple Bluetooth devices simultaneously. This allows a user to share his or her music (or any audio stream) with a friend.

5.5.9 Burst Buffer Operation

The CYW4334W has a data buffer that can buffer data being sent over the HCI and audio transports, then send the data at an increased rate. This mode of operation allows the host to sleep for the maximum amount of time, dramatically reducing system current consumption.

5.6 Adaptive Frequency Hopping

The CYW4334W gathers link quality statistics on a channel by channel basis to facilitate channel assessment and channel map selection. The link quality is determined using both RF and baseband signal processing to provide a more accurate frequency-hop map.

5.7 Advanced Bluetooth/WLAN Coexistence

The CYW4334W includes advanced coexistence technologies that are only possible with a Bluetooth/WLAN integrated die solution. These coexistence technologies are targeted at small form-factor platforms, such as cell phones and media players, including applications such as VoWLAN + SCO and Video-over-WLAN + High Fidelity BT Stereo.

Support is provided for platforms that share a single antenna between Bluetooth and WLAN. Dual-antenna applications are also supported. The CYW4334W radio architecture allows for lossless simultaneous Bluetooth and WLAN reception for shared antenna applications. This is possible only via an integrated solution (shared LNA and joint AGC algorithm). It has superior performance versus implementations that need to arbitrate between Bluetooth and WLAN reception.

The CYW4334W integrated solution enables MAC-layer signaling (firmware) and a greater degree of sharing via an enhanced coexistence interface. Information is exchanged between the Bluetooth and WLAN cores without host processor involvement.

The CYW4334W also supports Transmit Power Control on the STA together with standard Bluetooth TPC to limit mutual interference and receiver desensitization. Preemption mechanisms are utilized to prevent AP transmissions from colliding with Bluetooth frames. Improved channel classification techniques have been implemented in Bluetooth for faster and more accurate detection and elimination of interferers (including non-WLAN 2.4 GHz interference).

The Bluetooth AFH classification is also enhanced by the WLAN core's channel information.

5.8 Fast Connection (Interlaced Page and Inquiry Scans)

The CYW4334W supports page scan and inquiry scan modes that significantly reduce the average inquiry response and connection times. These scanning modes are compatible with the Bluetooth version 2.1 page and inquiry procedures.

6. Music and Audio

The CYW4334W provides superior total system current during music or audio playback and recording. To enable these functions, several features of the device are combined to provide superior system power consumption.

6.1 MP3 Encoder

- ISO/IEC 11172-3 compliant
- Supports 32 kHz sampling frequencies only
- Encodes mono and stereo signals

6.2 MP3 Decoder

The MP3 decoder supports mono and stereo audio recording with the following specifications:

- Supports MPEG-1 Layer 3 decoding
- Output is fully bit compliant with MPEG-1 standard specification
- Supports sampling frequencies from 32 kHz to 48 kHz
- Minimum bit-rate supported 32 kbps and maximum bit-rate supported 320 kbps for Layer 3

6.3 AAC Decoder

Compliant to ISO/IEC 14496-3: 2004 specifications:

- MPEG-2, MPEG-4 AAC LC decoding up to level 2
- SBR tool, up to level 3
- Low power SBR tool
- Full support up to level 3 for the HE AAC profile
- Implicit and explicit SBR signaling mechanisms
- Mono and stereo channel streams decoding sampling frequencies from 8 kHz to 96 kHz only
- ADTS frame decoding

7. Microprocessor and Memory Unit for Bluetooth

The Bluetooth microprocessor core is based on the ARM® Cortex-M3™ 32-bit RISC processor with embedded ICE-RT debug and JTAG interface units. It runs software from the link control (LC) layer, up to the host controller interface (HCI).

The ARM core is paired with a memory unit that contains 680 KB of ROM memory for program storage and boot ROM, 173 KB of RAM for data scratchpad and patch RAM code. The internal ROM allows for flexibility during power-on reset to enable the same device to be used in various configurations. At power-up, the lower-layer protocol stack is executed from the internal ROM memory.

External patches may be applied to the ROM-based firmware to provide flexibility for bug fixes or features additions. These patches may be downloaded from the host to the CYW4334W through the UART transports. The mechanism for downloading via UART is identical to the proven interface of the CYW4329 and CYW4330 devices.

7.1 RAM, ROM, and Patch Memory

The CYW4334W Bluetooth core has 173 KB of internal RAM which is mapped between general purpose scratch pad memory and patch memory and 680 KB of ROM used for the lower-layer protocol stack, test mode software, and boot ROM. The patch memory capability enables the addition of code changes for purposes of feature additions and bug fixes to the ROM memory.

7.2 Reset

The CYW4334W has an integrated power-on reset circuit that resets all circuits to a known power-on state. The BT power-on reset (POR) circuit is out of reset after BT_REG_ON goes High. If BT_REG_ON is low, then the POR circuit is held in reset.

8. Bluetooth Peripheral Transport Unit

8.1 SPI Interface and Transport Selection

The CYW4334W supports a slave SPI HCI transport with an input clock of up to 16 MHz, although higher clock rates may be possible. The physical interface between the SPI master and the CYW4334W contains four SPI signals (SPI_CSB, SPI_CLK, SPI_MOSI, and SPI_MISO) and one interrupt signal (SPI_INT). The CYW4334W can be configured to accept active-low or active-high polarity on the SPI_CSB chip select signal. It can also be configured to drive an active-low or active-high SPI_INT interrupt signal.

The following additional details apply to the SPI interface:

- Bit ordering on the SPI_MOSI and SPI_MISO data lines can be configured as either little endian or big endian.
- Proprietary sleep mode, half-duplex handshaking is implemented between the SPI master and the CYW4334W.
- SPI_INT is required to negotiate the start of a transaction.
- The SPI interface does not require flow control in the middle of a payload.
- The FIFO is large enough to handle the largest packet size.
- Only the SPI master can stop the flow of bytes on the data lines because it controls SPI_CSB and SPI_CLK.
- Flow control should be implemented in higher layer protocols.

The SPI signals are multiplexed onto the UART signals as shown in Table 6 . See “UART Interface” on page 31 for more information on the UART interface.

Table 6. SPI and UART Signal Multiplexing

SPI Signal	UART Signal
SPI_CLK	UART_CTS_N
SPI_CSB	UART_RTS_N
SPI_MISO	UART_RXD
SPI_MOSI	UART_TXD
SPI_INT	BT_HOST_WAKE

The Bluetooth HCI transport interface (which will be either SPI or UART) is selected during power-up per the state of the BT_HOST_WAKE (BT_GPIO_1) signal (listed in Table 6 as a UART signal). Transport interface selection is as follows:

- If the BT_HOST_WAKE signal is low during power-up, then the SPI transport interface will be selected.
- If the BT_HOST_WAKE signal is not low during power-up, then the UART transport interface will be selected.

Note: BT_HOST_WAKE is pulled up in the device. Attach it to an external pull-down to select the SPI as the transport interface.

8.2 PCM Interface

The CYW4334W supports two independent PCM interfaces that share the pins with the I^2S interfaces. The PCM Interface on the CYW4334W can connect to linear PCM Codec devices in master or slave mode. In master mode, the CYW4334W generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the CYW4334W.

The PCM interface configuration can be adjusted by the host via the use of vendor-specific HCI commands.

8.2.1 Slot Mapping

The CYW4334W supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate of 128 kHz, 512 kHz, or 1024 kHz. The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tri-states its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tri-states its output after the falling edge of the PCM clock during the last bit of the slot.

8.2.2 Frame Synchronization

The CYW4334W supports both short- and long-frame synchronization in both master and slave modes. In short-frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

8.2.3 Data Formatting

The CYW4334W may be configured to generate and accept several different data formats. For conventional narrowband speech mode, the CYW4334W uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2's complement data, left justified, and clocked MSB first.

8.2.4 Wideband Speech Support

When the host encodes Wideband Speech (WBS) packets in transparent mode, the encoded packets are transferred over the PCM bus for an eSCO voice connection. In this mode, the PCM bus is typically configured in master mode for a 4 kHz sync rate with 16-bit samples, resulting in a 64 kbps bit rate. The CYW4334W also supports slave transparent mode using a proprietary rate-matching scheme. In SBC-code mode, linear 16-bit data at 16 kHz (256 kbps rate) is transferred over the PCM bus.

8.2.5 Burst PCM Mode

In this mode of operation, the PCM bus runs at a significantly higher rate of operation to allow the host to duty cycle its operation and save current. In this mode of operation, the PCM bus can operate at a rate of up to 24 MHz. This mode of operation is initiated with an HCI command from the host.

8.2.6 PCM Interface Timing

Short Frame Sync, Master Mode

Figure 11. PCM Timing Diagram (Short Frame Sync, Master Mode)

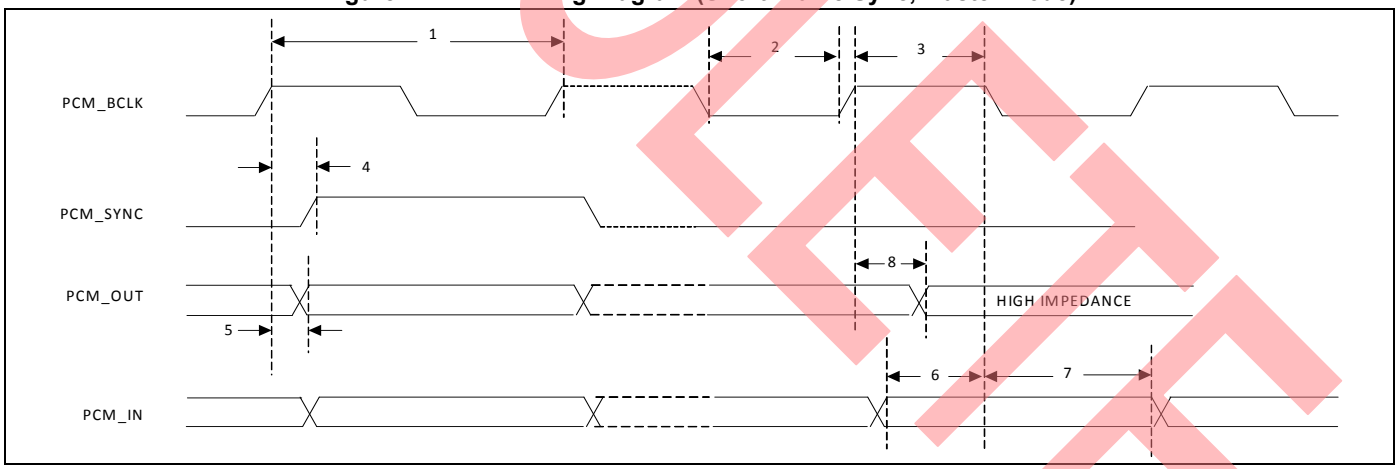


Table 7. PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Short Frame Sync, Slave Mode

Figure 12. PCM Timing Diagram (Short Frame Sync, Slave Mode)

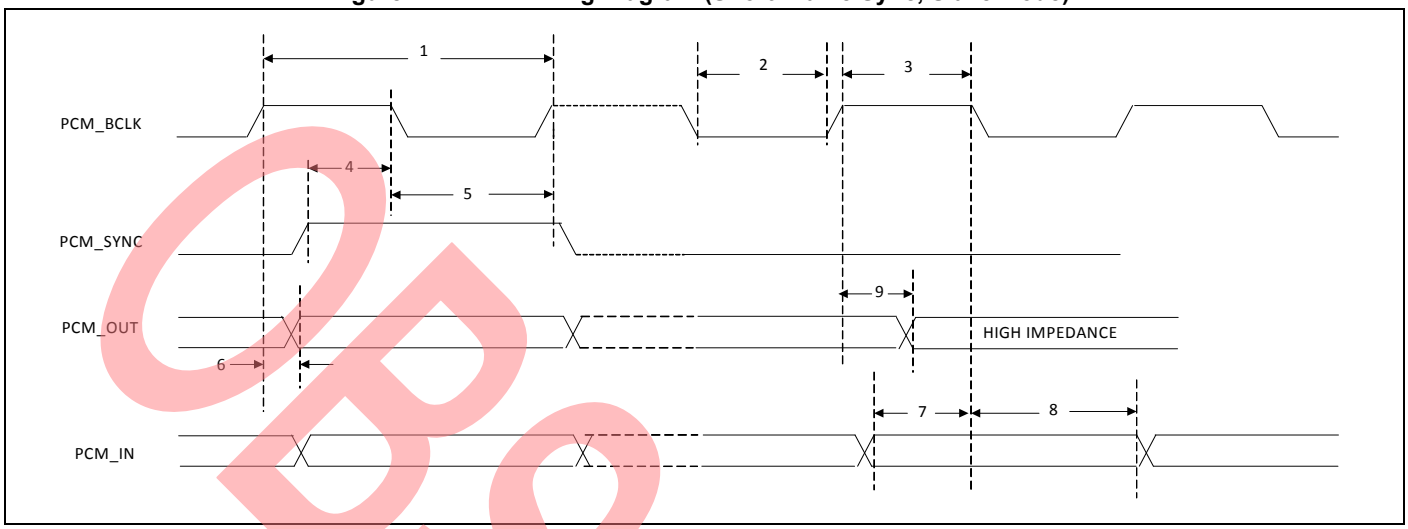


Table 8. PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Long Frame Sync, Master Mode

Figure 13. PCM Timing Diagram (Long Frame Sync, Master Mode)

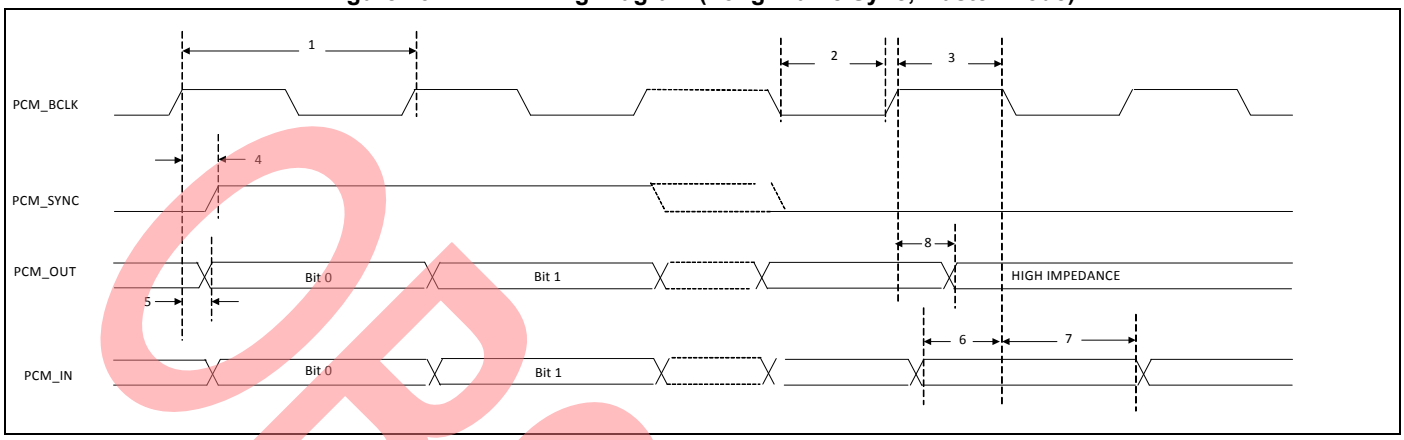


Table 9. PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Long Frame Sync, Slave Mode

Figure 14. PCM Timing Diagram (Long Frame Sync, Slave Mode)

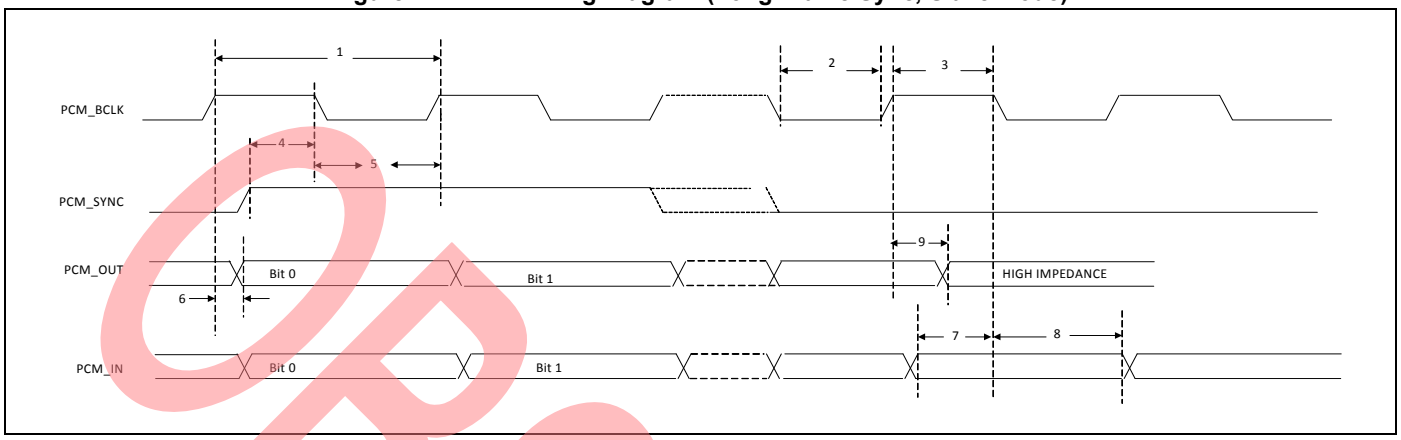


Table 10. PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Short Frame Sync, Burst Mode

Figure 15. PCM Burst Mode Timing (Receive Only, Short Frame Sync)

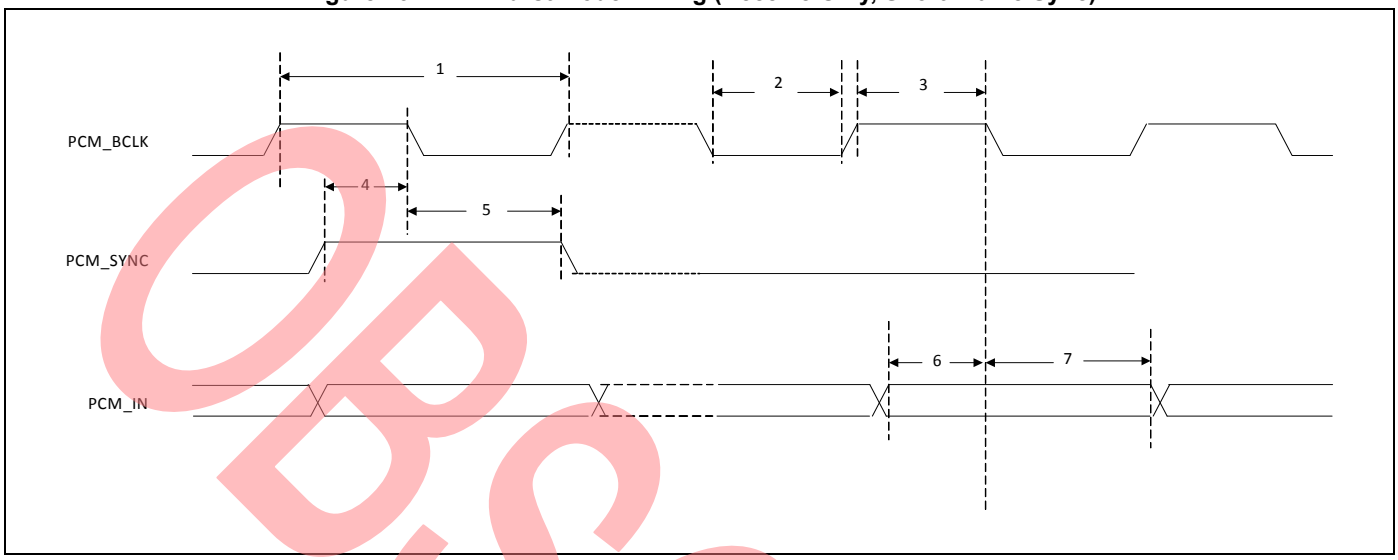


Table 11. PCM Burst Mode (Receive Only, Short Frame Sync)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock low	20.8	–	–	ns
3	PCM bit clock high	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

Long Frame Sync, Burst Mode

Figure 16. PCM Burst Mode Timing (Receive Only, Long Frame Sync)

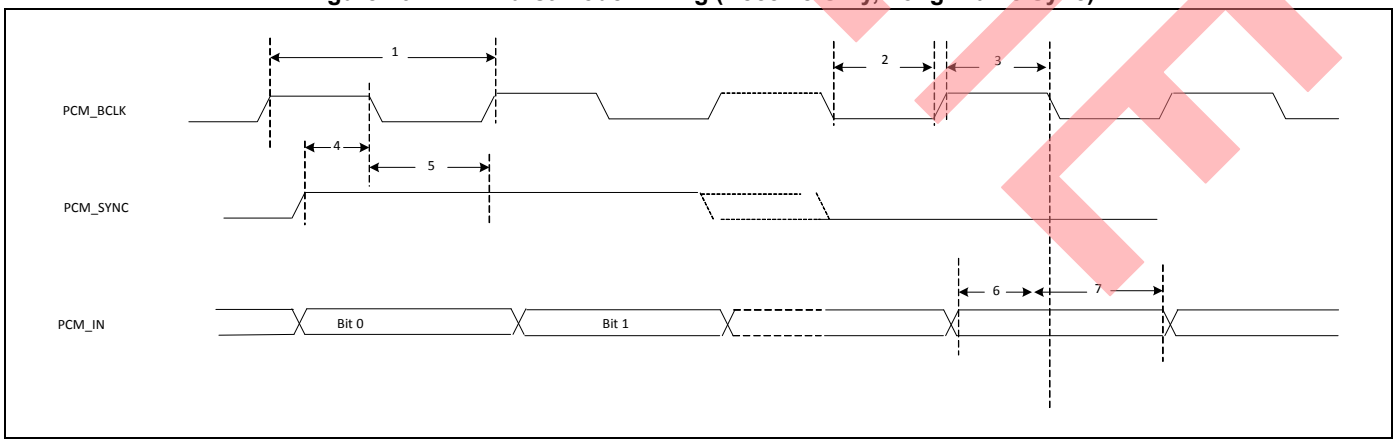


Table 12. PCM Burst Mode (Receive Only, Long Frame Sync)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock low	20.8	–	–	ns
3	PCM bit clock high	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

8.3 UART Interface

The CYW4334W includes a single UART for Bluetooth. The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 4.0 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (“Three-wire UART Transport Layer”). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

The CYW4334W UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The CYW4334W UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

Table 13. Example of Common Baud Rates

Desired Rate	Actual Rate	Error (%)
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

Figure 17. UART Timing

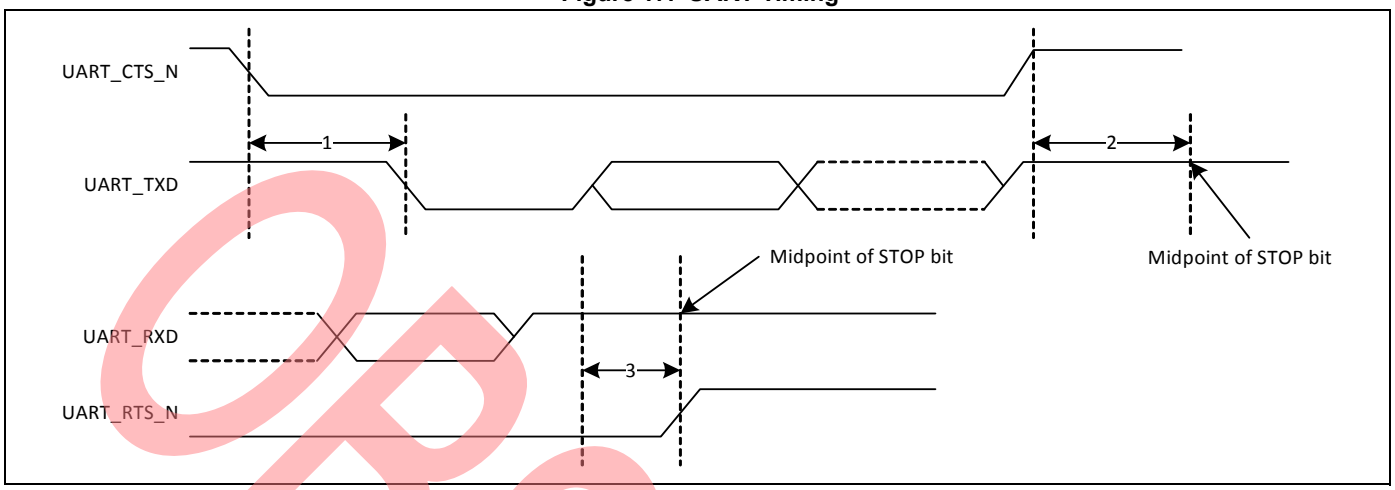


Table 14. UART Timing Specifications

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	–	0.5	Bit periods

8.4 I²S Interface

The CYW4334W has an I²S digital audio port for Bluetooth.

The I²S signals are:

- I²S clock: I²S SCK
- I²S Word Select: ²S WS
- I²S Data Out: I²S SDO
- I²S Data In: I²S SDI

I²S SCK and I²S WS become outputs in master mode and inputs in slave mode, while I²S SDO always stays as an output. The channel word length is 16 bits and the data is justified so that the MSB of the left-channel data is aligned with the MSB of the I²S bus, per the I²S specification. The MSB of each data word is transmitted one bit clock cycle after the I²S WS transition, synchronous with the falling edge of bit clock. Left-channel data is transmitted when I²S WS is low, and right-channel data is transmitted when I²S WS is high. Data bits sent by the CYW4334W are synchronized with the falling edge of I2S_SCK and should be sampled by the receiver on the rising edge of I2S_SSCK.

The clock rate in master mode is either of the following:

48 kHz x 32 bits per frame = 1.536 MHz

48 kHz x 50 bits per frame = 2.400 MHz

The master clock is generated from the input reference clock using a N/M clock divider.

In the slave mode, any clock rate is supported to a maximum of 3.072 MHz.

8.4.1 I²S Timing

Note: Timing values specified in Table 15 are relative to high and low threshold levels.

Table 15. Timing for I²S Transmitters and Receivers

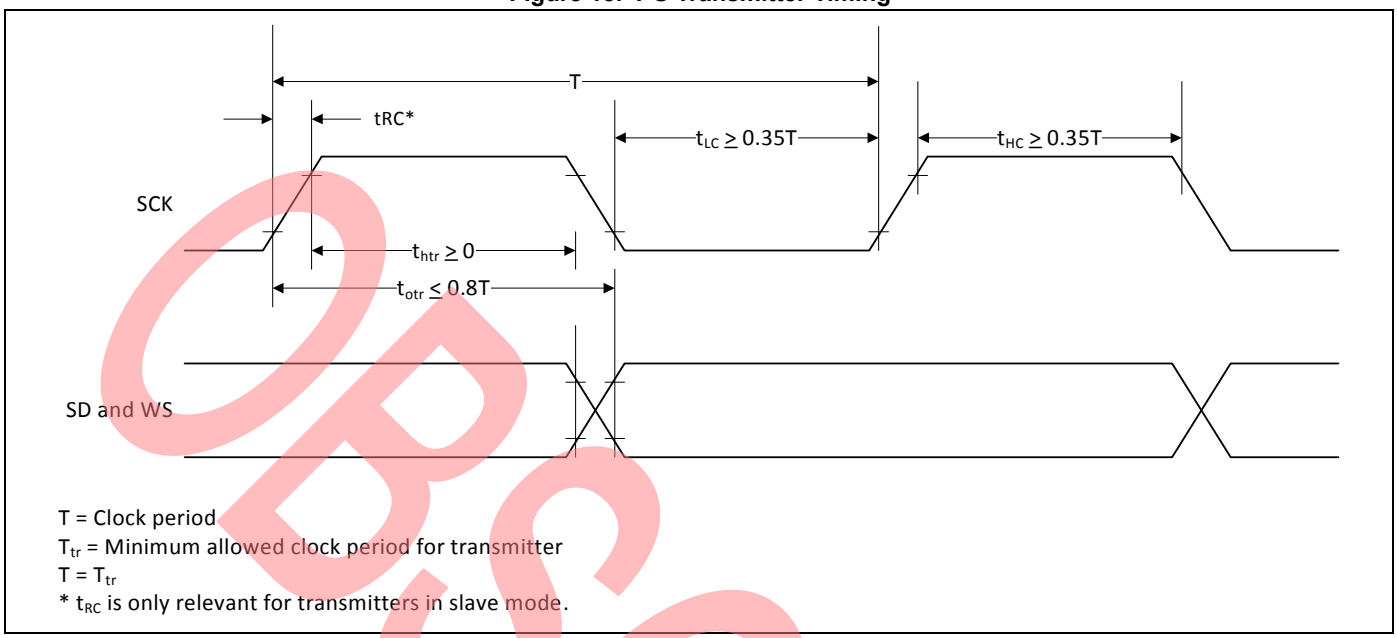
Parameter	Transmitter				Receiver				Notes
	Lower LImit		Upper Limit		Lower Limit		Upper Limit		
	Min	Max	Min	Max	Min	Max	Min	Max	
Clock Period T	T_{tr}	–	–	–	T_r	–	–	–	1
Master Mode: Clock generated by transmitter or receiver									
High t_{HC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	2
Low t_{LC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	2
Slave Mode: Clock accepted by transmitter or receiver									
High t_{HC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	3
Low t_{LC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	3
Rise time t_{RC}	–	–	$0.15T_{tr}$	–	–	–		–	4
Transmitter									
Delay t_{dtr}	–	–	–	0.8T	–	–	–	–	5
Hold time t_{htr}	0	–	–	–	–	–	–	–	4
Receiver									
Setup time t_{sr}	–	–	–	–	–	$0.2T_r$	–	–	6
Hold time t_{hr}	–	–	–	–	–	0	–	–	6

Note:

- The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.
- At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t_{HC} and t_{LC} are specified with respect to T.
- In slave mode, the transmitter and receiver need a clock signal with minimum high and low periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_r$, any clock that meets the requirements can be used.
- Because the delay (t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC} which means t_{htr} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{htr} is greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than t_{RCmax}, where t_{RCmax} is not less than $0.15T_{tr}$.
- To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
- The data setup and hold time must not be less than the specified receiver setup and hold time.

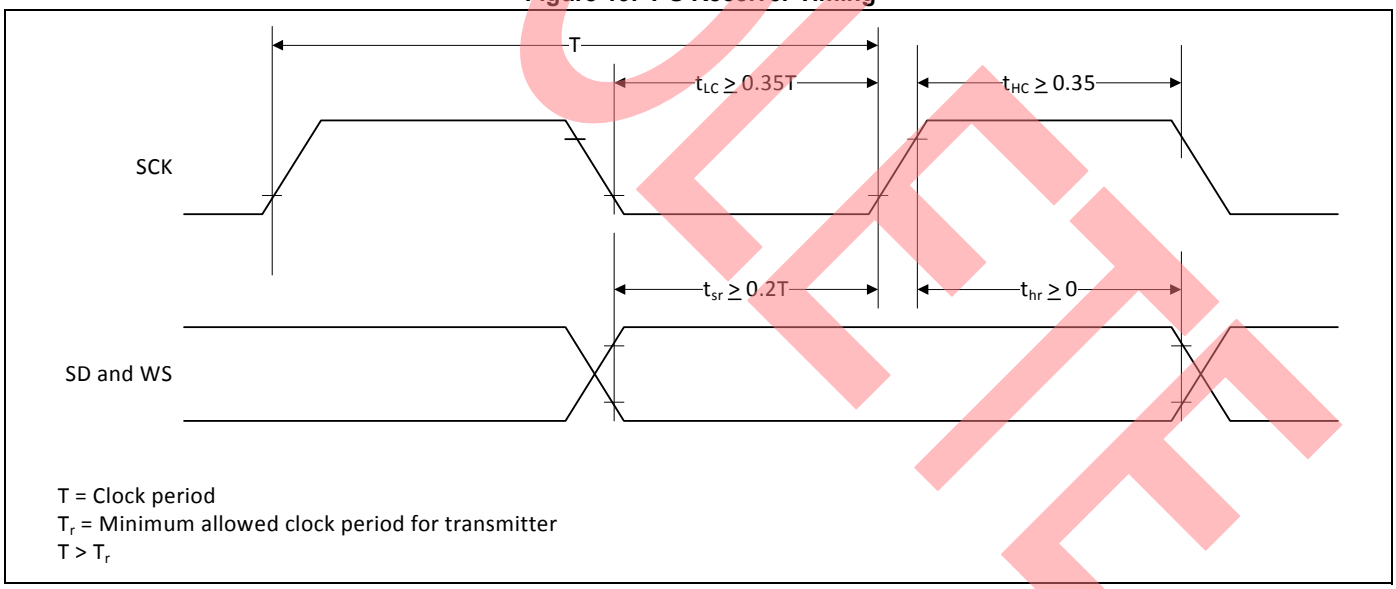
Note: The time periods specified in Figure 18 and Figure 19 on page 34 are defined by the transmitter speed. The receiver specifications must match transmitter performance.

Figure 18. I²S Transmitter Timing



T = Clock period
T_{tr} = Minimum allowed clock period for transmitter
$T = T_{tr}$
* t_{RC} is only relevant for transmitters in slave mode.

Figure 19. I²S Receiver Timing



T = Clock period
T_r = Minimum allowed clock period for transmitter
$T > T_r$

9. WLAN Global Functions

9.1 WLAN CPU and Memory Subsystem

The CYW4334W includes an integrated ARM Cortex-M3™ processor with internal RAM and ROM. The ARM Cortex-M3 processor is a low-power processor that features low gate count, low interrupt latency, and low-cost debug. It is intended for deeply embedded applications that require fast interrupt response features. The processor implements the ARM architecture v7-M with support for Thumb®-2 instruction set. ARM Cortex-M3 delivers 30% more performance gain over ARM7TDMI.

At 0.19 µW/MHz, the Cortex-M3 is the most power efficient general purpose microprocessor available, outperforming 8- and 16-bit devices on MIPS/µW. It supports integrated sleep modes.

ARM Cortex-M3 uses multiple technologies to reduce cost through improved memory utilization, reduced pin overhead, and reduced silicon area. ARM Cortex-M3 supports independent buses for code and data access (ICode/DCode and system buses). ARM Cortex-M3 supports extensive debug features including real time trace of program execution.

On-chip memory for the CPU includes 512 KB SRAM and 640 KB ROM.

9.2 One-Time Programmable Memory

Various hardware configuration parameters may be stored in an internal 3072-bit One-Time Programmable (OTP) memory, which is read by the system software after device reset. In addition, customer-specific parameters, including the system vendor ID and the MAC address can be stored, depending on the specific board design.

The initial state of all bits in an unprogrammed OTP device is 0. After any bit is programmed to a 1, it cannot be reprogrammed to 0. The entire OTP array can be programmed in a single write cycle using a utility provided with the Cypress WLAN manufacturing test tools. Alternatively, multiple write cycles can be used to selectively program specific bytes, but only bits which are still in the 0 state can be altered during each programming cycle.

Prior to OTP programming, all values should be verified using the appropriate editable nvram.txt file, which is provided with the reference board design package.

9.3 GPIO Interface

In the WLAN section of the CYW4334W, there are 16 general purpose I/O (GPIO) pins on the WLCSP package and 8 GPIO pins on the WLBGA package that can be used to connect to various external devices.

9.4 UART Interface

One UART interface can be enabled by software as an alternate function on pins WL_GPIO_4 and WL_GPIO_5. Provided primarily for debugging during development, this UART enables the CYW4334W to operate as RS-232 data termination equipment (DTE) for exchanging and managing data with other serial devices. It is compatible with the industry standard 16550 UART and provides a FIFO size of 64 × 8 in each direction.

9.5 JTAG Interface

The CYW4334W supports the IEEE 1149.1 JTAG boundary scan standard for performing device package and PCB assembly testing during manufacturing. In addition, the JTAG interface allows Cypress to assist customers by using proprietary debug and characterization test tools during board bring-up. Therefore, it is highly recommended to provide access to the JTAG pins by means of test points or a header on all PCB designs.

10. WLAN Host Interfaces

10.1 SDIO v2.0

The CYW4334W WLAN section supports SDIO v2.0, including the following modes:

DS: Default speed up to 25 MHz, including 1- and 4-bit modes

HS: High speed up to 50 MHz

It also has the ability to map the interrupt signal onto a GPIO pin for applications requiring an interrupt different than what is provided by the SDIO interface. The ability to force control of the gated clocks from within the device is also provided. SDIO mode is enabled using the strapping option pins strap_host_ifc_[3:1] (Table 21: "WLAN GPIO Functions and Strapping Options (Advance Information)," on page 65).

Three functions are supported:

- Function 0 standard SDIO function (Max BlockSize/ByteCount = 32B)
- Function 1 backplane function to access the internal system-on-chip (SoC) address space (Max BlockSize/ByteCount = 64B)
- Function 2 WLAN function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount = 512B)

10.1.1 SDIO Pin Descriptions

Table 16. SDIO Pin Description

SD 4-Bit Mode		*SD 1-Bit Mode*		*gSPI Mode*	
DATA0	Data line 0	DATA	Data line	DO	Data output
DATA1	Data line 1 or Interrupt	IRQ	Interrupt	IRQ	Interrupt
DATA2	Data line 2 or Read Wait	RW	Read Wait	NC	Not used
DATA3	Data line 3	N/C	Not used	CS	Card select
CLK	Clock	CLK	Clock	SCLK	Clock
CMD	Command line	CMD	Command line	DI	Data input

Figure 20. Signal Connections to SDIO Host (SD 4-Bit Mode)

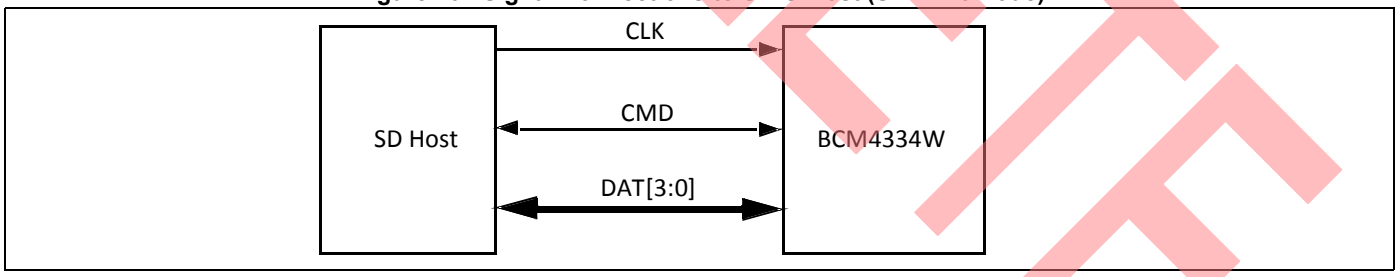
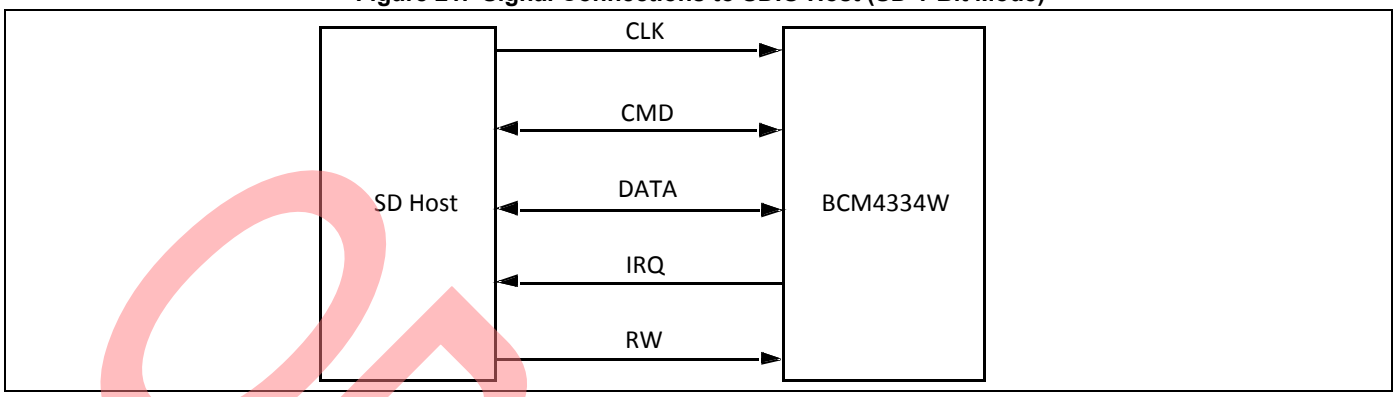


Figure 21. Signal Connections to SDIO Host (SD 1-Bit Mode)



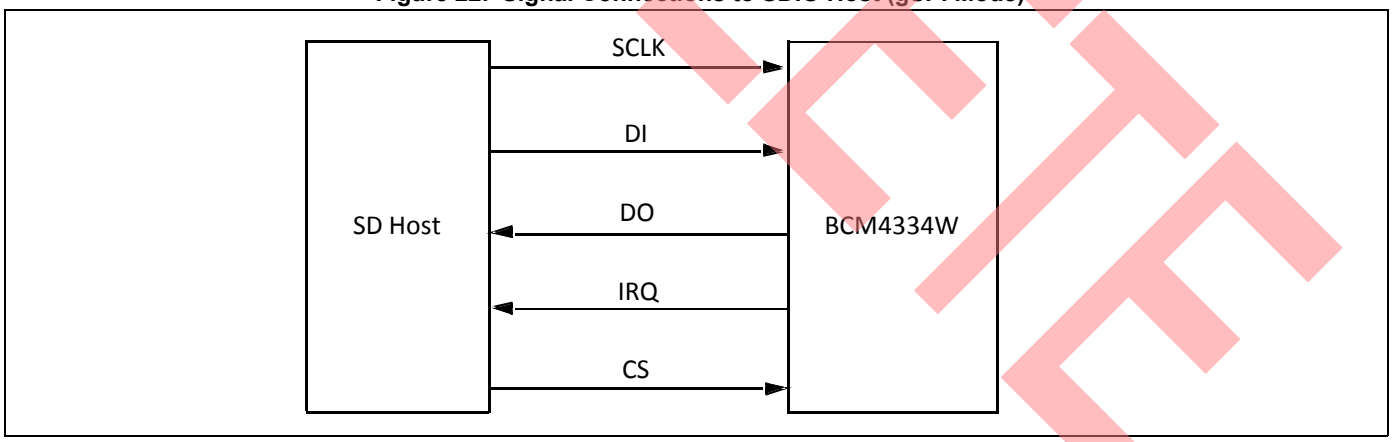
10.2 Generic SPI Mode

In addition to the full SDIO mode, the CYW4334W includes the option of using the simplified generic SPI (gSPI) interface/protocol. Characteristics of the gSPI mode include:

- Supports up to 48 MHz operation
- Supports fixed delays for responses and data from device
- Supports alignment to host gSPI frames (16 or 32 bits)
- Supports up to 2 KB frame size per transfer
- Supports little endian (default) and big endian configurations
- Supports configurable active edge for shifting
- Supports packet transfer through DMA for WLAN

gSPI mode is enabled using the strapping option pins strap_host_ifc_[3:1], Table 21: “WLAN GPIO Functions and Strapping Options (Advance Information),” on page 65.

Figure 22. Signal Connections to SDIO Host (gSPI Mode)



10.2.1 SPI Protocol

The SPI protocol supports both 16-bit and 32-bit word operation. Byte endianness is supported in both modes. Figure 23 and Figure 24 show the basic write and write/read commands.

Figure 23. gSPI Write Protocol

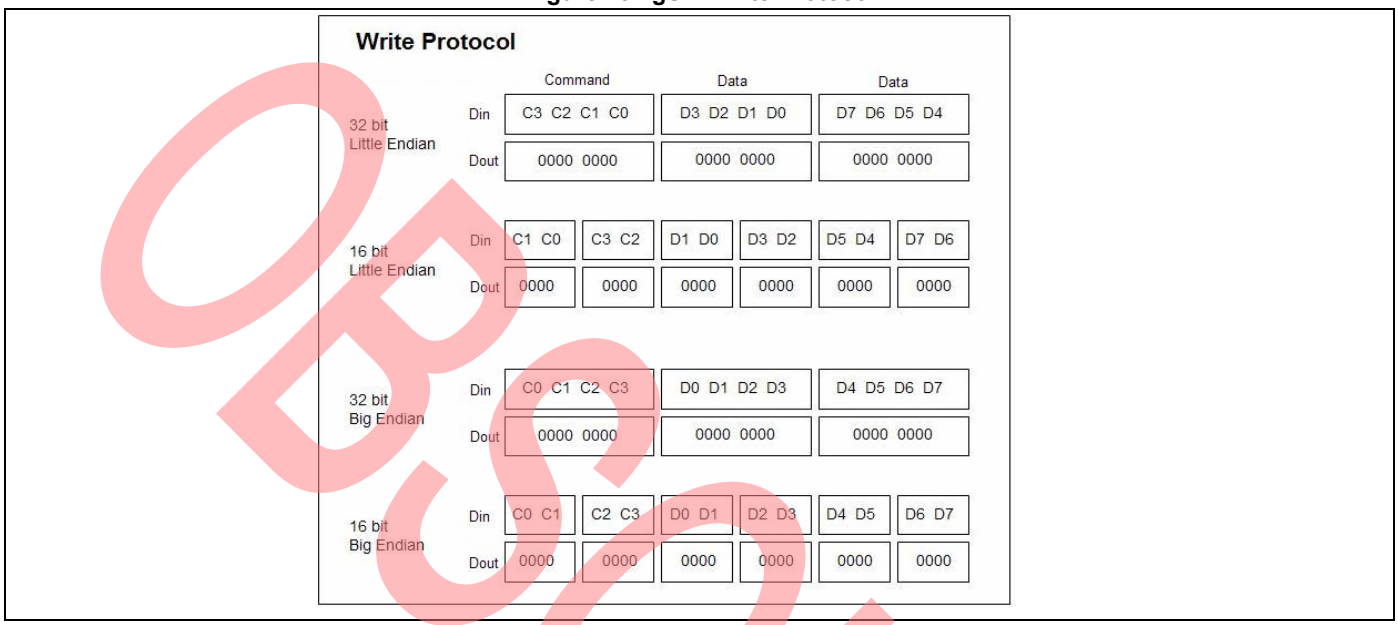
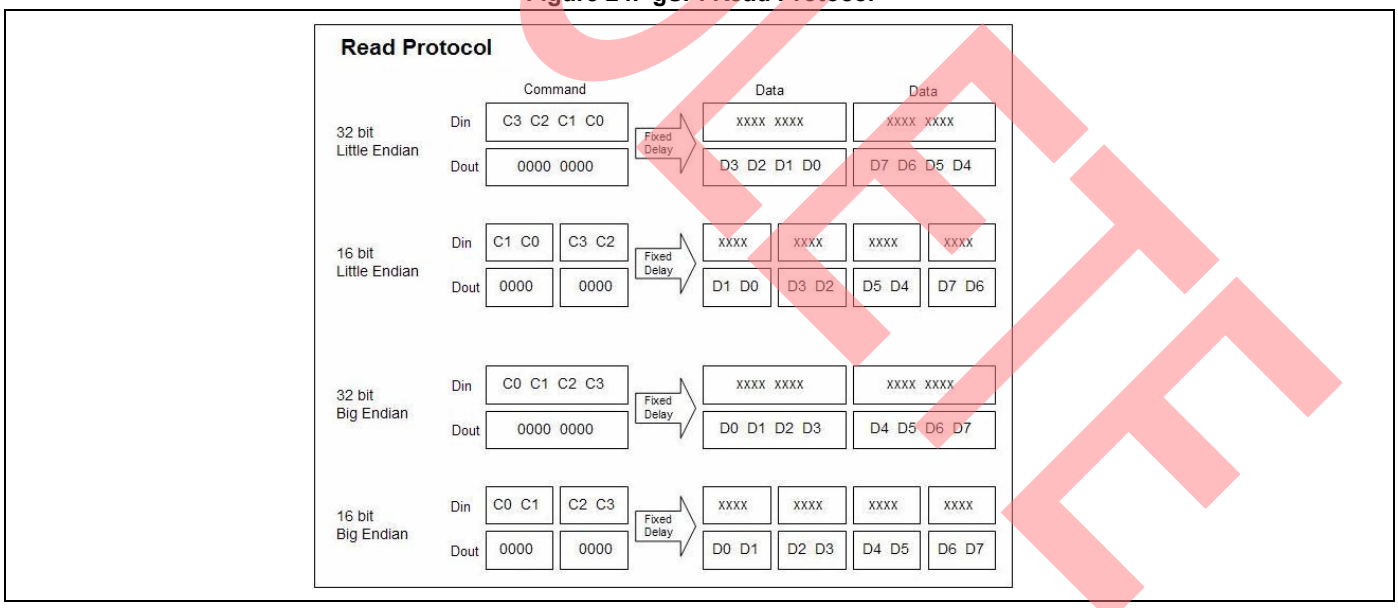


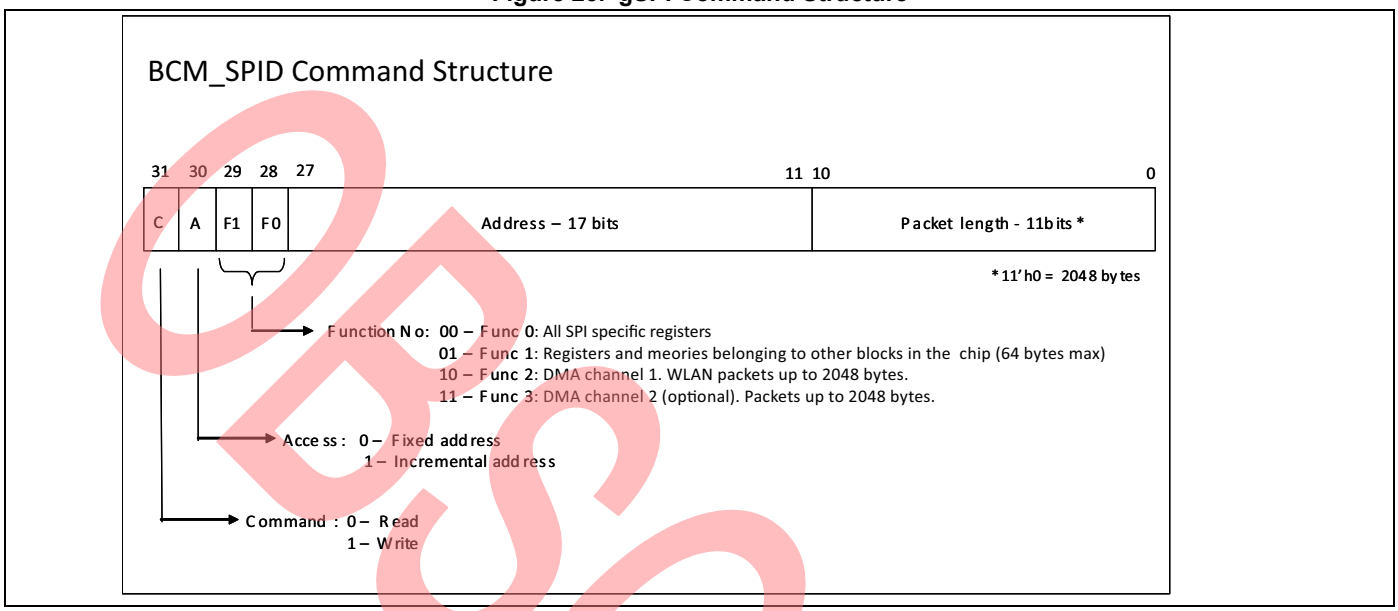
Figure 24. gSPI Read Protocol



Command Structure

The gSPI command structure is 32 bits. The bit positions and definitions are as shown in Figure 25.

Figure 25. gSPI Command Structure



Write

The host puts the first bit of the data onto the bus half a clock-cycle before the first active edge following the CS going low. The following bits are clocked out on the falling edge of the gSPI clock. The device samples the data on the active edge.

Write/Read

The host reads on the rising edge of the clock requiring data from the device to be made available before the first rising clock edge of the clock burst for the data. The last clock edge of the fixed delay word can be used to represent the first bit of the following data word. This allows data to be ready for the first clock edge without relying on asynchronous delays.

Read

The read command always follows a separate write to set up the WLAN device for a read. This command differs from the write/read command in the following respects: a) chip selects go high between the command/address and the data and b) the time interval between the command/address is not fixed.

Status

The gSPI interface supports status notification to the host after a read/write transaction. This status notification provides information about any packet errors, protocol errors, information about available packet in the RX queue, etc. The status information helps in reducing the number of interrupts to the host. The status-reporting feature can be switched off using a register bit, without any timing overhead. The gSPI bus timing for read/write transactions with and without status notification are as shown in Figure 26 and Figure 27 on page 41. See Table 17 on page 41 for information on status field details.

Figure 26. gSPI Signal Timing Without Status (32-bit big endian shown)

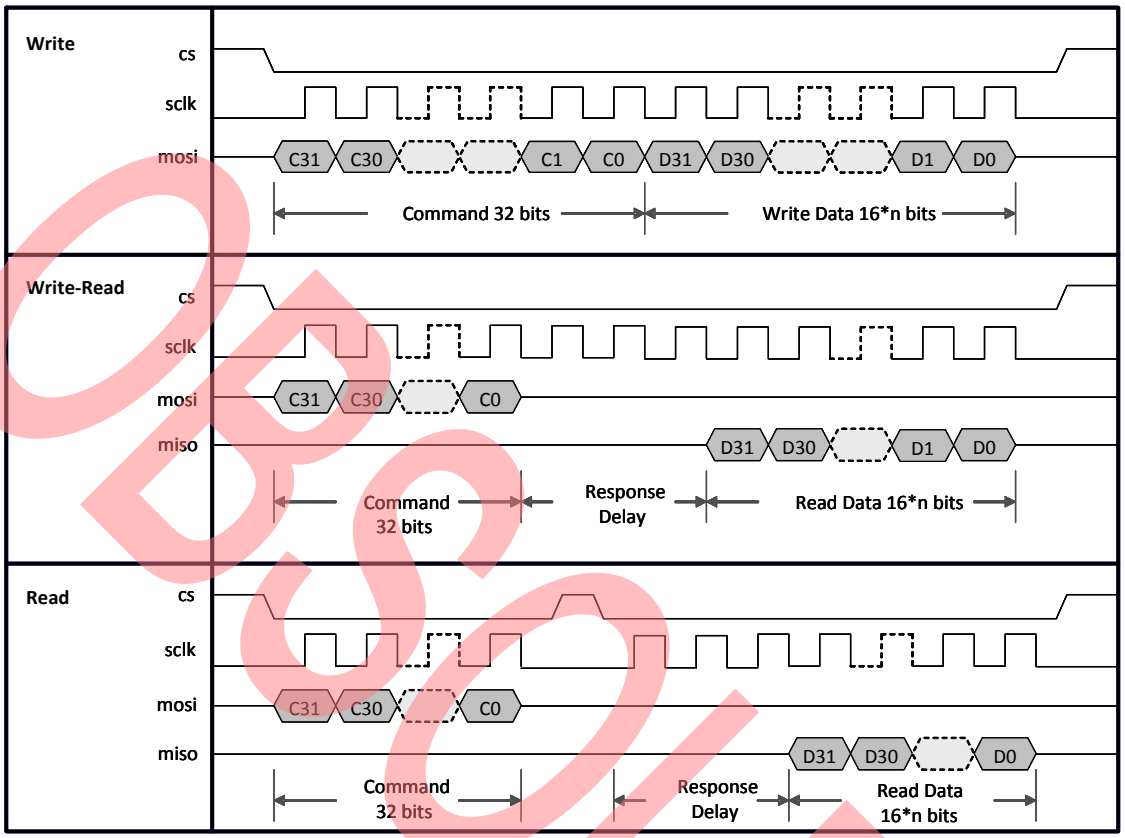


Figure 27. gSPI Signal Timing with Status (Response Delay = 0) (32-bit big endian shown)

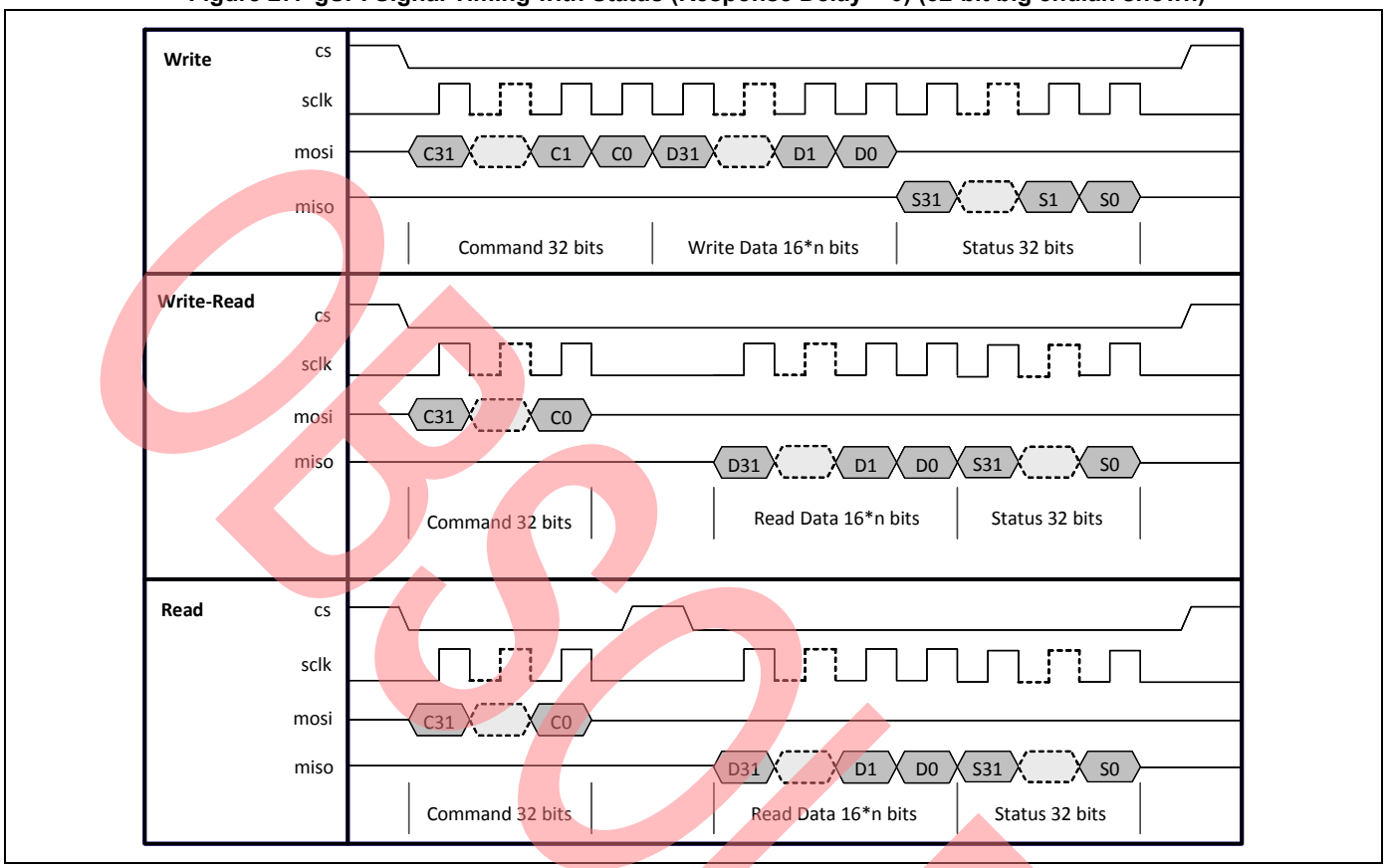


Table 17. gSPI Status Field Details

Bit	Name	Description
0	Data not available	The requested read data is not available
1	Underflow	FIFO underflow occurred due to current (F2, F3) read command
2	Overflow	FIFO overflow occurred due to current (F1, F2, F3) write command
3	F2 interrupt	F2 channel interrupt
4	F3 interrupt	F3 channel interrupt
5	F2 RX Ready	F2 FIFO is ready to receive data (FIFO empty)
6	F3 RX Ready	F3 FIFO is ready to receive data (FIFO empty)
7	Reserved	–
8	F2 Packet Available	Packet is available/ready in F2 TX FIFO
9:19	F2 Packet Length	Length of packet available in F2 FIFO
20	F3 Packet Available	Packet is available/ready in F3 TX FIFO
21:31	F3 Packet Length	Length of packet available in F3 FIFO

10.2.2 gSPI Host-Device Handshake

To initiate communication through the gSPI after power-up, the host needs to bring up the WLAN/Chip by writing to the wake-up WLAN register bit. Writing a 1 to this bit will start up the necessary crystals and PLLs so that the CYW4334W is ready for data transfer. The device can signal an interrupt to the host indicating that the device is awake and ready. This procedure also needs to be followed for waking up the device in sleep mode. The device can interrupt the host using the WLAN IRQ line whenever it has any information to pass to the host. On getting an interrupt, the host needs to read the interrupt and/or status register to determine the cause of interrupt and then take necessary actions.

10.2.3 Boot-Up Sequence

After power-up, the gSPI host needs to wait 150 ms for the device to be out of reset. For this, the host needs to poll with a read command to F0 addr 0x14. Address 0x14 contains a predefined bit pattern. As soon as the host gets a response back with the correct register content, it implies that the device has powered up and is out of reset. After that, the host needs to set the wakeup-WLAN bit (F0 reg 0x00 bit 7). The wakeup-WLAN issues a clock request to the PMU.

For the first time after power-up, the host must wait for the availability of low power clock inside the device. Once that is available, the host must write to a PMU register to set the crystal frequency, which turns on the PLL. After the PLL is locked, the chipActive interrupt is issued to the host. This interrupt indicates the device awake/ready status. See Table 18 for information on gSPI registers.

In Table 18 , the following notation is used for register access:

- R: Readable from host and CPU
- W: Writable from host
- U: Writable from CPU

Table 18. gSPI Registers

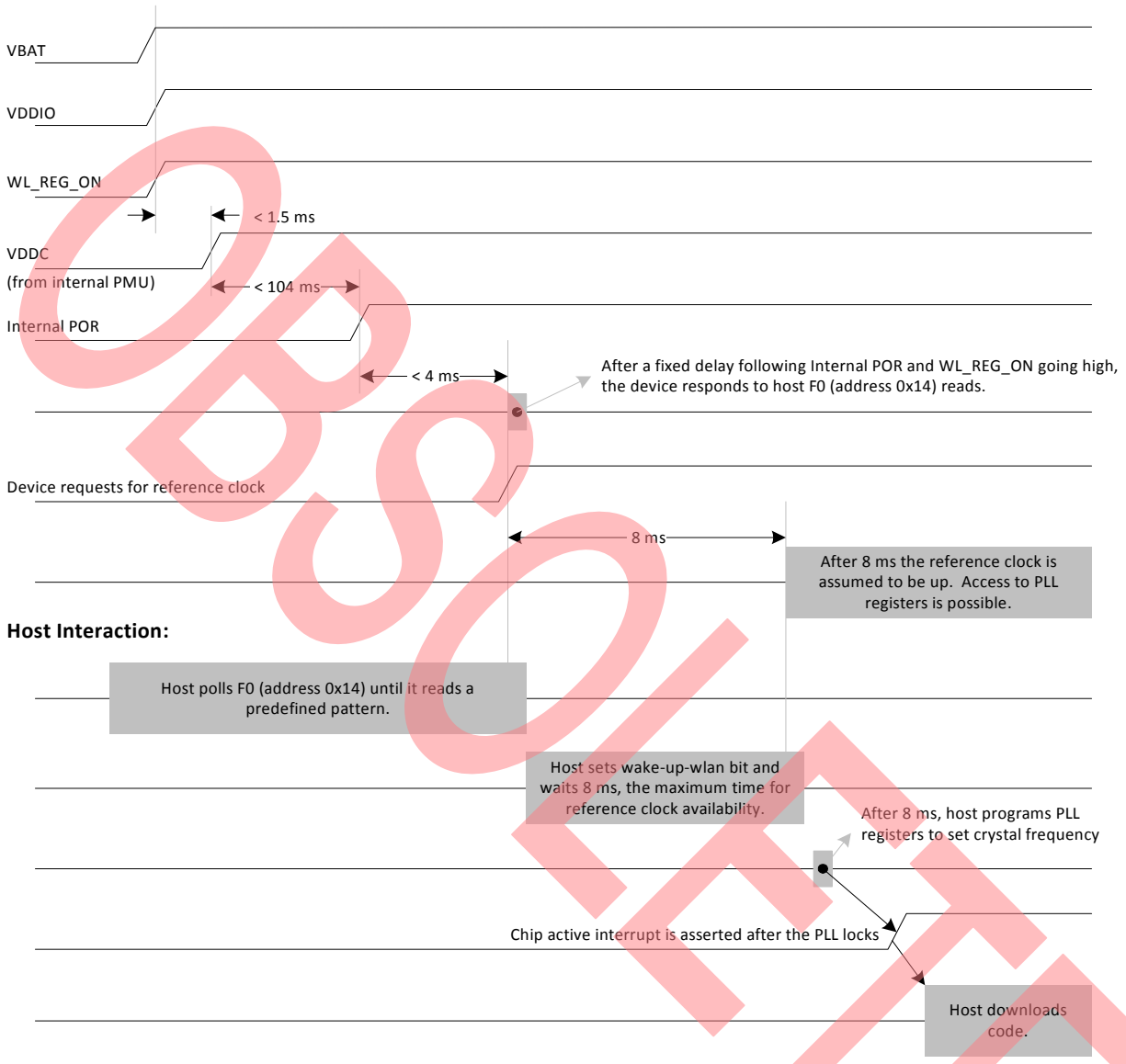
Address	Register	Bit	Access	Default	Description
x0000	Word length	0	R/W/U	0	0: 16 bit word length 1: 32 bit word length
	Endianness	1	R/W/U	0	0: Little Endian 1: Big Endian
	High-speed mode	4	R/W/U	1	0: Normal mode. RX and TX at different edges. 1: High speed mode. RX and TX on same edge (default).
	Interrupt polarity	5	R/W/U	1	0: Interrupt active polarity is low 1: Interrupt active polarity is high (default)
	Wake-up	7	R/W	0	A write of 1 will denote a wake-up command from the host to the device. This will be followed by an F2 Interrupt from the gSPI device to the host, indicating device awake status.
x0001	Response delay	7:0	R/W/U	8'h04	Configurable read response delay in multiples of 8 bits
x0002	Status enable	0	R/W	1	0: no status sent to host after read/write 1: status sent to host after read/write
	Interrupt with status	1	R/W	0	0: do not interrupt if status is sent 1: interrupt host even if status is sent
	Response delay for all	2	R/W	0	0: response delay applicable to F1 read only 1: response delay applicable to all function read
x0003	Reserved	–	–	–	–
x0004	Interrupt register	0	R/W	0	Requested data not available; Cleared by writing a 1 to this location
		1	R	0	F2/F3 FIFO underflow due to last read
		2	R	0	F2/F3 FIFO overflow due to last write
		5	R	0	F2 packet available
		6	R	0	F3 packet available
		7	R	0	F1 overflow due to last write

Table 18. gSPI Registers (Cont.)

Address	Register	Bit	Access	Default	Description
x0005	Interrupt register	5	R	0	F1 Interrupt
		6	R	0	F2 Interrupt
		7	R	0	F3 Interrupt
x0006–x0007	Interrupt enable register	15:0	R/W/U	16'hE0E7	Particular Interrupt is enabled if a corresponding bit is set
x0008–x000B	Status register	31:0	R	32'h0000	Same as status bit definitions
x000C–x000D	F1 info register	0	R	1	F1 enabled
		1	R	0	F1 ready for data transfer
		13:2	R/U	12'h40	F1 max packet size
x000E–x000F	F2 info register	0	R/U	1	F2 enabled
		1	R	0	F2 ready for data transfer
		15:2	R/U	14'h800	F2 max packet size
x0010–x0011	F3 info register	0	R/U	1	F3 enabled
		1	R	0	F3 ready for data transfer
		15:2	R/U	14'h800	F3 max packet size
x0014–x0017	Test–Read only register	31:0	R	32'hFEEDBEAD	This register contains a predefined pattern, which the host can read and determine if the gSPI interface is working properly.
x0018–x001B	Test–R/W register	31:0	R/W/U	32'h00000000	This is a dummy register where the host can write some pattern and read it back to determine if the gSPI interface is working properly.

Figure 28. Figure 29 **shows the WLAN boot-up sequence from power-up to firmware download.**

Figure 29. WLAN Boot-Up Sequence



Notes:
1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

11. Wireless LAN MAC and PHY

11.1 MAC Features

The CYW4334W WLAN media access controller (MAC) supports features specified in the IEEE 802.11 base standard, and amended by IEEE 802.11n. The salient features are listed below:

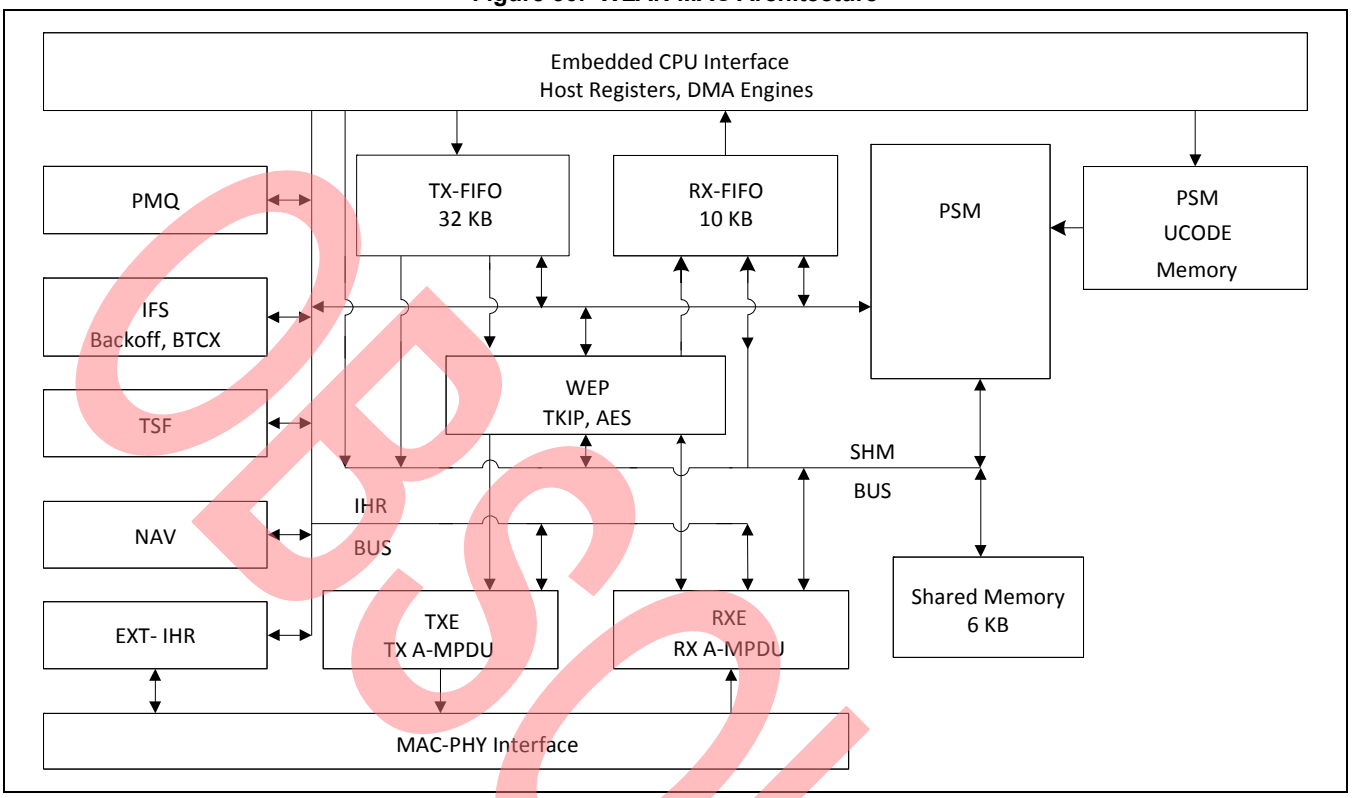
- Transmission and reception of aggregated MPDUs (A-MPDU)
- Support for power management schemes, including WMM power-save, power-save multi-poll (PSMP) and multiphase PSMP operation
- Support for immediate ACK and Block-ACK policies
- Interframe space timing support, including RIFS
- Support for RTS/CTS and CTS-to-self frame sequences for protecting frame exchanges
- Back-off counters in hardware for supporting multiple priorities as specified in the WMM specification
- Timing synchronization function (TSF), network allocation vector (NAV) maintenance, and target beacon transmission time (TBTT) generation in hardware
- Hardware offload for AES-CCMP, legacy WPA TKIP, legacy WEP ciphers, and support for key management
- Support for coexistence with Bluetooth and other external radios
- Programmable independent basic service set (IBSS) or infrastructure basic service set functionality
- Statistics counters for MIB support

11.1.1 MAC Description

The CYW4334W WLAN MAC is designed to support high-throughput operation with low-power consumption. It does so without compromising the Bluetooth coexistence policies, thereby enabling optimal performance over both networks. In addition, several power saving modes have been implemented that allow the MAC to consume very little power while maintaining network-wide timing synchronization. The architecture diagram of the MAC is shown in Figure 30 on page 46.

The following sections provide an overview of the important modules in the MAC.

Figure 30. WLAN MAC Architecture



PSM

The programmable state machine (PSM) is a micro-coded engine, which provides most of the low-level control to the hardware, to implement the IEEE 802.11 specification. It is a microcontroller that is highly optimized for flow control operations, which are predominant in implementations of communication protocols. The instruction set and fundamental operations are simple and general, which allows algorithms to be optimized until very late in the design process. It also allows for changes to the algorithms to track evolving IEEE 802.11 specifications.

The PSM fetches instructions from the microcode memory. It uses the shared memory to obtain operands for instructions, as a data store, and to exchange data between both the host and the MAC data pipeline (via the SHM bus). The PSM also uses a scratchpad memory (similar to a register bank) to store frequently accessed and temporary variables.

The PSM exercises fine-grained control over the hardware engines, by programming internal hardware registers (IHR). These IHRs are co-located with the hardware functions they control, and are accessed by the PSM via the IHR bus.

The PSM fetches instructions from the microcode memory using an address determined by the program counter, instruction literal, or a program stack. For ALU operations the operands are obtained from shared memory, scratchpad, IHRs, or instruction literals, and the results are written into the shared memory, scratchpad, or IHRs.

There are two basic branch instructions: conditional branches and ALU based branches. To better support the many decision points in the IEEE 802.11 algorithms, branches can depend on either a readily available signals from the hardware modules (branch condition signals are available to the PSM without polling the IHRs), or on the results of ALU operations.

WEP

The wired equivalent privacy (WEP) engine encapsulates all the hardware accelerators to perform the encryption and decryption, and MIC computation and verification. The accelerators implement the following cipher algorithms: legacy WEP, WPA TKIP, WPA2 AES-CCMP.

The PSM determines, based on the frame type and association information, the appropriate cipher algorithm to be used. It supplies the keys to the hardware engines from an on-chip key table. The WEP interfaces with the TXE to encrypt and compute the MIC on transmit frames, and the RXE to decrypt and verify the MIC on receive frames.

TXE

The transmit engine (TXE) constitutes the transmit data path of the MAC. It coordinates the DMA engines to store the transmit frames in the TXFIFO. It interfaces with WEP module to encrypt frames, and transfers the frames across the MAC-PHY interface at the appropriate time determined by the channel access mechanisms.

The data received from the DMA engines are stored in transmit FIFOs. The MAC supports multiple logical queues to support traffic streams that have different QoS priority requirements. The PSM uses the channel access information from the IFS module to schedule a queue from which the next frame is transmitted. Once the frame is scheduled, the TXE hardware transmits the frame based on a precise timing trigger received from the IFS module.

The TXE module also contains the hardware that allows the rapid assembly of MPDUs into an A-MPDU for transmission. The hardware module aggregates the encrypted MPDUs by adding appropriate headers and pad delimiters as needed.

RXE

The receive engine (RXE) constitutes the receive data path of the MAC. It interfaces with the DMA engine to drain the received frames from the RXFIFO. It transfers bytes across the MAC-PHY interface and interfaces with the WEP module to decrypt frames. The decrypted data is stored in the RXFIFO.

The RXE module contains programmable filters that are programmed by the PSM to accept or filter frames based on several criteria such as receiver address, BSSID, and certain frame types.

The RXE module also contains the hardware required to detect A-MPDUs, parse the headers of the containers, and disaggregate them into component MPDUS.

IFS

The IFS module contains the timers required to determine interframe space timing including RIFS timing. It also contains multiple backoff engines required to support prioritized access to the medium as specified by WMM.

The interframe spacing timers are triggered by the cessation of channel activity on the medium, as indicated by the PHY. These timers provide precise timing to the TXE to begin frame transmission. The TXE uses this information to send response frames or perform transmit frame-bursting (RIFS or SIFS separated, as within a TXOP).

The backoff engines (for each access category) monitor channel activity, in each slot duration, to determine whether to continue or pause the backoff counters. When the backoff counters reach 0, the TXE gets notified, so that it may commence frame transmission. In the event of multiple backoff counters decrementing to 0 at the same time, the hardware resolves the conflict based on policies provided by the PSM.

The IFS module also incorporates hardware that allows the MAC to enter a low-power state when operating under the IEEE power save mode. In this mode, the MAC is in a suspended state with its clock turned off. A sleep timer, whose count value is initialized by the PSM, runs on a slow clock and determines the duration over which the MAC remains in this suspended state. Once the timer expires the MAC is restored to its functional state. The PSM updates the TSF timer based on the sleep duration ensuring that the TSF is synchronized to the network.

The IFS module also contains the PTA hardware that assists the PSM in Bluetooth coexistence functions.

TSF

The timing synchronization function (TSF) module maintains the TSF timer of the MAC. It also maintains the target beacon transmission time (TBTT). The TSF timer hardware, under the control of the PSM, is capable of adopting timestamps received from beacon and probe response frames in order to maintain synchronization with the network.

The TSF module also generates trigger signals for events that are specified as offsets from the TSF timer, such as uplink and downlink transmission times used in PSMP.

NAV

The network allocation vector (NAV) timer module is responsible for maintaining the NAV information conveyed through the duration field of MAC frames. This ensures that the MAC complies with the protection mechanisms specified in the standard.

The hardware, under the control of the PSM, maintains the NAV timer and updates the timer appropriately based on received frames. This timing information is provided to the IFS module, which uses it as a virtual carrier-sense indication.

MAC-PHY Interface

The MAC-PHY interface consists of a data path interface to exchange RX/TX data from/to the PHY. In addition, there is an programming interface, which can be controlled either by the host or the PSM to configure and control the PHY.

11.2 WLAN PHY Description

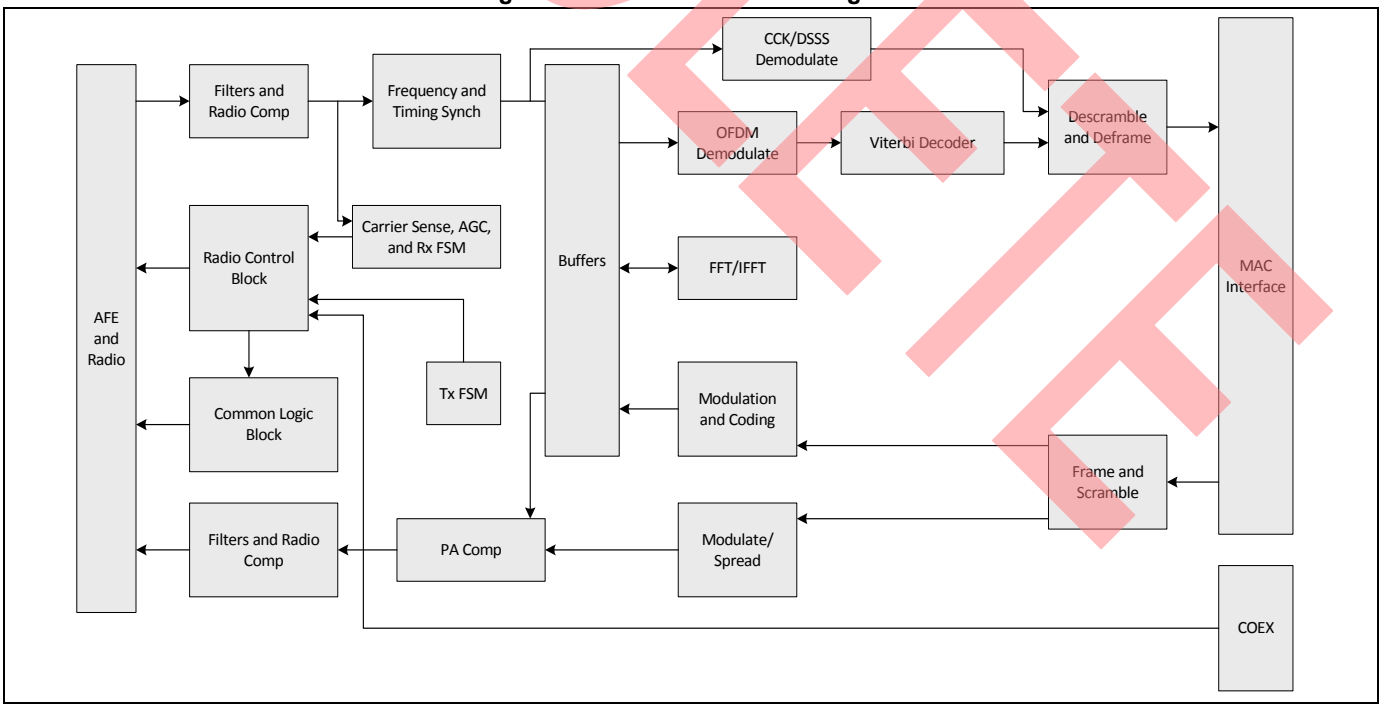
The CYW4334W WLAN Digital PHY is designed to comply with IEEE 802.11b/g/n single-stream to provide wireless LAN connectivity supporting data rates from 1 Mbps to 150 Mbps for low-power, high-performance handheld applications.

The PHY has been designed to work with interference, radio nonlinearity, and impairments. It incorporates efficient implementations of the filters, FFT and Viterbi decoder algorithms. Efficient algorithms have been designed to achieve maximum throughput and reliability, including algorithms for carrier sense/rejection, frequency/phase/timing acquisition and tracking, channel estimation and tracking. The PHY receiver also contains a robust IEEE 802.11b demodulator. The PHY carrier sense has been tuned to provide high throughput for IEEE 802.11g/11b hybrid networks with Bluetooth coexistence. It has also been designed for shared single antenna systems between WL and BT to support simultaneous Rx-Rx.

11.2.1 PHY Features

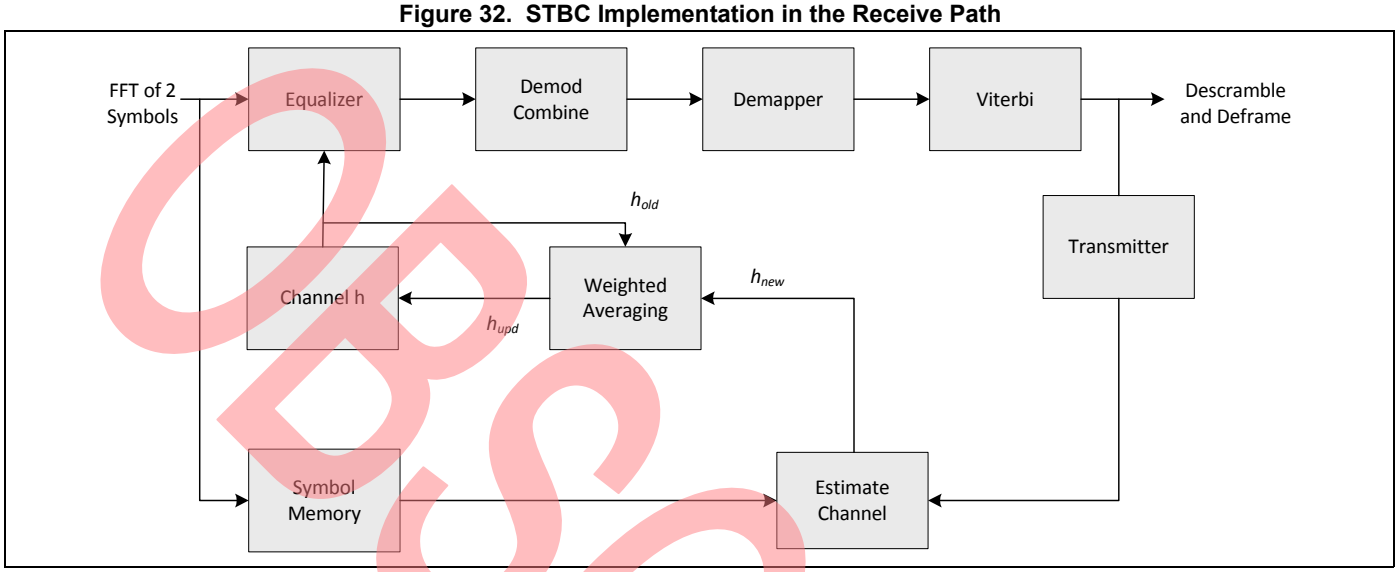
- Supports IEEE 802.11b, 11g, and 11n single-stream PHY standards.
- IEEE 802.11n single-stream operation in 20 MHz and 40 MHz channels
- Supports Optional Short GI and Green Field modes in Tx and Rx.
- Supports optional space-time block code (STBC) receive of two space-time streams.
- Tx LDPC for improved range and power efficiency
- Supports IEEE 802.11h/k for worldwide operation.
- Advanced algorithms for low power, enhanced sensitivity, range, and reliability
- Algorithms to improve performance in presence of Bluetooth
- Simultaneous Rx-Rx (WL-BT) architecture
- Automatic gain control scheme for blocking and non blocking application scenario for cellular applications
- Closed loop transmit power control
- Digital RF chip calibration algorithms to handle CMOS RF chip non-idealities
- On-the-fly channel frequency and transmit power selection
- Supports per packet Rx antenna diversity.
- Designed to meet FCC and other worldwide regulatory requirements.

Figure 31. WLAN PHY Block Diagram



One of the key features of the PHY is its space-time block coding (STBC) capability. The STBC scheme can obtain diversity gains in a fading channel environment. On a connection with an access point that uses multiple transmit antennas and supports STBC, the CYW4334W can process two space-time streams to improve receiver performance. Figure 32 is a block diagram showing the STBC implementation in the receive path.

Figure 32. STBC Implementation in the Receive Path



In STBC mode, symbols are processed in pairs. Equalized output symbols are linearly combined and decoded. The channel estimate is refined on every pair of symbols using the received symbols and reconstructed symbols.

12. WLAN Radio Subsystem

The CYW4334W includes an integrated single-band WLAN RF transceiver that has been optimized for use in 2.4 GHz wireless LAN systems. It has been designed to provide low-power, low-cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. The transmit and receive sections include all on-chip filtering, mixing, and gain control functions.

Up to 11 (WLCSP = 11, WLBGA = 8) RF control signals are available to drive the external RF switches and support external power amplifiers and low noise amplifiers for each band. See the reference board schematics for further details.

12.1 Receiver Path

The CYW4334W has a wide dynamic range, direct conversion receiver. It employs high order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. Control signals are available that can support the use of optional external low noise amplifiers (LNA), which can increase the receive sensitivity by several dB.

12.2 Transmit Path

Baseband data is modulated and up converted to the 2.4 GHz ISM band. A linear on-chip PA driver that is designed to drive an external power amplifier is included. This PA driver can be powered directly from VBAT. Hence, if the external PA is also capable of being powered directly from VBAT, the need for a PALDO is eliminated. Closed-loop output power control is provided by a g-band TSSI input from an external power detector. Several spare RF control signals are available to support the external power amplifiers and RF switches for either or both bands.

12.3 Calibration

The CYW4334W features dynamic and automatic on-chip calibration to continually compensate for temperature and process variations across components. This enables the CYW4334W to be used in high-volume applications, because calibration routines are not required during manufacturing testing. These calibration routines are performed periodically in the course of normal radio operation. Examples of some of the automatic calibration algorithms are baseband filter calibration for optimum transmit and receive performance and LOFT calibration for carrier leakage reduction. In addition, I/Q Calibration, R Calibration, and VCO Calibration are performed on-chip. No per-board calibration is required in manufacturing test, which helps to minimize test time and cost during large volume production.

13. Pinout and Signal Descriptions

13.1 Signal Assignments

Figure 33 shows the WLBGA ball map. Figure 34 shows the WLCSP bump map.

Table 19 on page 53 contains the WLCSP bump coordinates.

Table 20 on page 59 contains the signal description for all packages.

Figure 33. 109-WLBGA Ball Map (Bottom View)

	10	9	8	7	6	5	4	3	2	1	
A	SR_PVSS	SR_VDDBATP5V	LDO_VDD1P5	VOUT_LNLDO	CLK_REQ	BT_REG_ON	WL_REG_ON	NC_7	GND_10	FM_LNAVCOVDD	A
B	SR_VLX	SR_VDDBATA5V	VOUT_CLDO	VOUT_3P3	LPO_IN	BT_UART_RXD	BT_DEV_WAKE/GPIO0	GND_9	GND_3	NC_1	B
C	PMU_AVSS	VSSC	VDDIO	BT_PCM_CLK	VDDC	VSSC	BT_PCM_SYNC	BT_PLLVSS	BT_VCOVSS	BT_VCOVDD	C
D	NC_90	AGND12PLL	HSIC_DVDD1p2_OUT	BT_PCM_IN	VDDC	VSSC	BT_UART_CTS_N	BT_IFVDD	BT_PLLVDD	BT_LNAVDD	D
E	NC_89	NC_91	SDIO_DATA_3	BT_PCM_OUT	BT_I2S_DI	BT_UART_TXD	BT_UART_RTS_N	BT_IFVSS	BT_PAVSS	BT_RF	E
F	SDIO_CLK	SDIO_DATA_1	VSSC	VDDC	BT_I2S_CLK	BT_I2S_DO	BT_HOST_WAKE/GPIO1	BT_LDOVSS	BT_VDDBAT	BT_LDOPAVDD2P5	F
G	SDIO_CMD	SDIO_DATA_0	SDIO_DATA_2	VDDIO	GPIO_3/TMS	BT_I2S_WS	WRF_AFE_GND1P2	WRF_RX_GND1P2	WRF_LNA_2G_GND1P2	WRF_RFIN	G
H	RF_SW_CTRL_4	RF_SW_CTRL_3	RF_SW_CTRL_5	GPIO_4/TDI/UART_RX	GPIO_2/TCK	No Connect	WRF_BUCK_VDD1P5	WRF_TX_GND1P2	WRF_GPIO_OUT	WRF_RFOUT	H
J	RF_SW_CTRL_0	RF_SW_CTRL_2	RF_SW_CTRL_6	GPIO_12/JTAG_TRST_L	GPIO_6/SPI_MODE_SEL	GPIO_1/WL_DEV_WAKE	GPIO_0/WL_HOST_WAKE	PA_Lin_Ctrl	WRF_PADRV_VBAT_GND5P0	WRF_PADRV_VBAT_VDD5P0	J
K	VDDIO_RF	RF_SW_CTRL_1	VSSC	WRF_TCXO_VDD1P8	WRF_XTAL_CAB_VDD1P2	WRF_SYNTH_VDD1P2	WRF_SYNTH_GND1P2		WRF_G_TSSI_IN	NC_43	K
L	VDDC	GPIO_5/TDO/UART_TX	JTAG_SEL	WRF_TCXO_CKIN2V	WRF_XTAL_CAB_ON	WRF_XTAL_CAB_OP	WRF_XTAL_CAB_GND1P2	WRF_VCO_GND1P2	WRF_LNA_5G_GND1P2	NC_41	L
	10	9	8	7	6	5	4	3	2	1	

Figure 34. 208-WLCSP Bump Map (Bottom View)

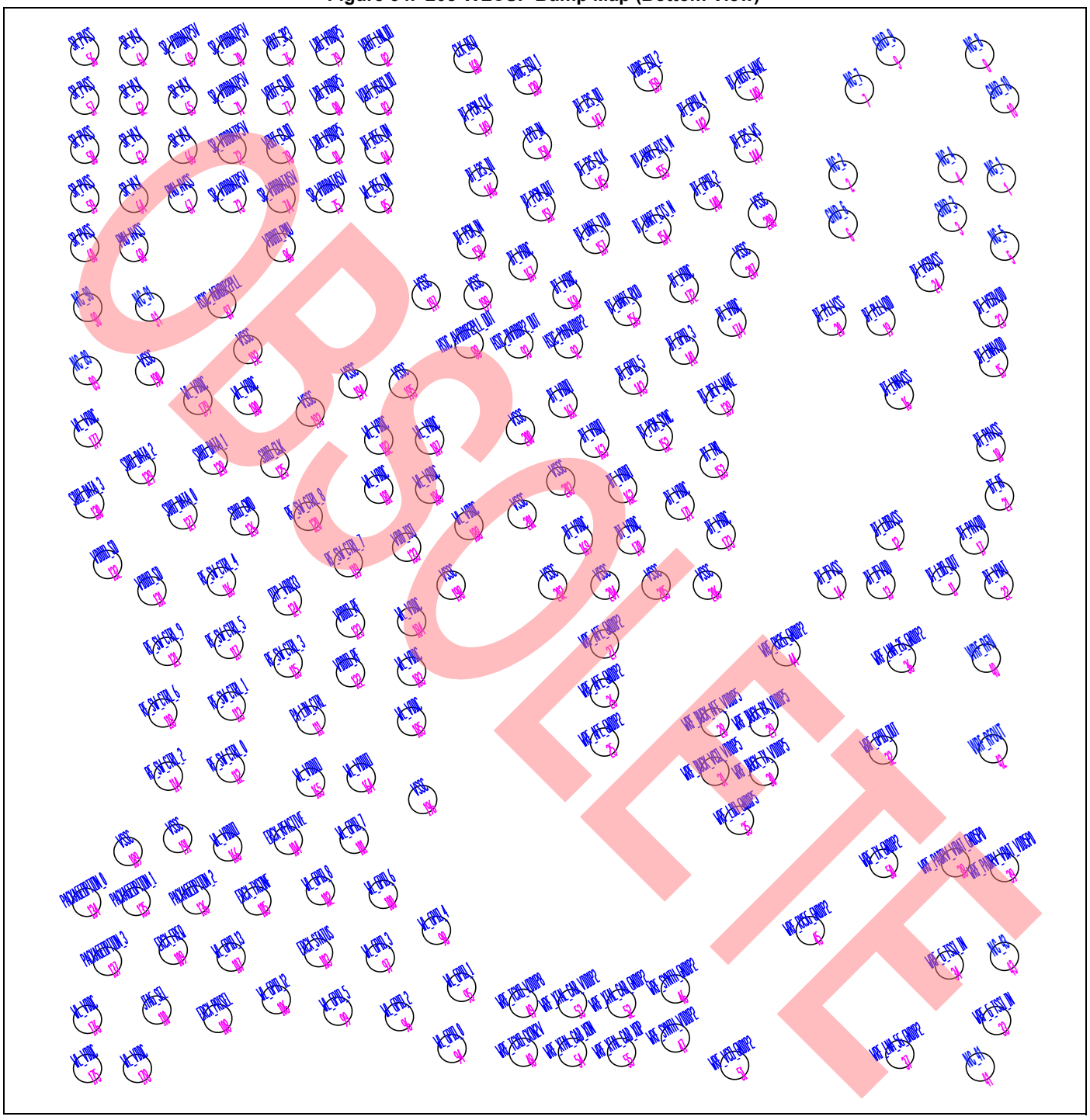


Table 19. WLCSP 208−Bump Coordinates

Bump#	Signal Name	Bump Side View (0,0 center of die)		Package Top Side View (0,0 center of die)	
		X	Y	X	Y
1	NC_1	1861.513	1556.690	−1861.513	1556.690
2	NC_2	1216.447	1569.799	−1216.447	1569.799
3	GND_3	1661.515	1397.597	−1661.515	1397.597
4	NC_4	1661.515	1597.595	−1661.515	1597.595
5	NC_5	1874.896	1279.868	−1874.896	1279.868
6	GND_6	1216.447	1369.801	−1216.447	1369.801
7	NC_7	1283.146	1918.864	−1283.146	1918.864
8	NC_8	1773.021	2061.473	−1773.021	2061.473
9	GND_9	1409.718	2074.856	−1409.718	2074.856
10	GND_10	1874.896	1880.785	−1874.896	1880.785
11	BT_LDO_OUT	1634.866	−84.600	−1634.866	−84.600
12	BT_PALDO_VSS	1406.896	99.977	−1406.896	99.977
13	BT_IFVDD	1370.410	−100.021	−1370.410	−100.021
14	BT_IFVSS	1170.412	−100.021	−1170.412	−100.021
15	BT_LNAVDD	1829.676	805.285	−1829.676	805.285
16	BT_LNAVSS	1445.092	673.187	−1445.092	673.187
17	BT_PAVDD	1750.971	81.864	−1750.971	81.864
18	BT_PAVSS	1819.443	461.507	−1819.443	461.507
19	BT_PLLVDD	1370.410	974.458	−1370.410	974.458
20	BT_PLLVSS	1170.412	974.458	−1170.412	974.458
21	BT_RF	1853.890	261.509	−1853.890	261.509
22	BT_VBAT	1851.654	−100.021	−1851.654	−100.021
23	BT_VCOVDD	1828.501	1008.356	−1828.501	1008.356
24	BT_VCOVSS	1569.112	1152.599	−1569.112	1152.599
25	WRF_AFE_GND1P2	243.196	−742.036	−243.196	−742.036
26	WRF_AFE_GND1P2	243.196	−542.038	−243.196	−542.038
27	WRF_AFE_GND1P2	243.196	−342.040	−243.196	−342.040
28	WRF_BUCK_AFE_VDD1P5	693.565	−660.924	−693.565	−660.924
29	WRF_BUCK_RX_VDD1P5	893.563	−660.924	−893.563	−660.924
30	WRF_BUCK_TX_VDD1P5	893.563	−860.922	−893.563	−860.922
31	WRF_BUCK_VCO_VDD1P5	693.565	−860.922	−693.565	−860.922
32	WRF_GPIO_OUT	1378.222	−774.355	−1378.222	−774.355
33	WRF_G_TSSI_IN	1842.033	−1877.481	−1842.033	−1877.481
34	WRF_G_TSSI_IN	1648.830	−1650.915	−1648.830	−1650.915

Table 19. WLCSP 208−Bump Coordinates (Cont.)

Bump#	Signal Name	Bump Side View (0,0 center of die)		Package Top Side View (0,0 center of die)	
		X	Y	X	Y
35	WRF_LDO_GND1P5	793.564	−1060.920	−793.564	−1060.920
36	WRF_LNA_2G_GND1P2	1454.916	−400.018	−1454.916	−400.018
37	WRF_LNA_5G_GND1P2	1447.441	−2014.947	−1447.441	−2014.947
38	WRF_PADRV_VBAT_GND5P0	1673.998	−1234.102	−1673.998	−1234.102
39	WRF_PADRV_VBAT_VDD5P0	1873.996	−1253.731	−1873.996	−1253.731
40	WRF_RFIN	1799.998	−400.018	−1799.998	−400.018
41	NC_41	1775.266	−2066.746	−1775.266	−2066.746
42	WRF_RFOUT	1827.547	−769.585	−1827.547	−769.585
43	NC_43	1873.996	−1616.116	−1873.996	−1616.116
44	WRF_RX2G_GND1P2	983.604	−373.869	−983.604	−373.869
45	WRF_RX5G_GND1P2	1082.388	−1510.618	−1082.388	−1510.618
46	WRF_SYNTH_GND1P2	532.600	−1748.596	−532.600	−1748.596
47	WRF_SYNTH_VDD1P2	532.600	−1948.594	−532.600	−1948.594
48	WRF_TCXO_CKIN2V	−86.744	−2006.775	86.744	−2006.775
49	WRF_TCXO_VDD1P8	−86.744	−1806.777	86.744	−1806.777
50	WRF_TX_GND1P2	1381.939	−1236.406	−1381.939	−1236.406
51	WRF_VCO_GND1P2	774.273	−2060.194	−774.273	−2060.194
52	WRF_XTAL_CAB_GND1P2	313.252	−1806.777	−313.252	−1806.777
53	WRF_XTAL_CAB_VDD1P2	113.254	−1806.777	−113.254	−1806.777
54	WRF_XTAL_CAB_XON	113.254	−2006.775	−113.254	−2006.775
55	WRF_XTAL_CAB_XOP	313.252	−2006.775	−313.252	−2006.775
56	SR_PVSS	−1875.008	2074.964	1875.008	2074.964
57	SR_PVSS	−1875.008	1874.966	1875.008	1874.966
58	SR_PVSS	−1875.008	1674.968	1875.008	1674.968
59	SR_PVSS	−1875.008	1474.970	1875.008	1474.970
60	SR_PVSS	−1875.008	1274.972	1875.008	1274.972
61	SR_VLX	−1675.010	2074.964	1675.010	2074.964
62	SR_VLX	−1675.010	1874.966	1675.010	1874.966
63	SR_VLX	−1675.010	1674.968	1675.010	1674.968
64	SR_VLX	−1675.010	1474.970	1675.010	1474.970
65	SR_VLX	−1475.012	1874.966	1475.012	1874.966
66	SR_VLX	−1475.012	1674.968	1475.012	1674.968
67	PMU_AVSS	−1475.012	1474.970	1475.012	1474.970
68	PMU_AVSS	−1675.010	1274.972	1675.010	1274.972
69	SR_VDDBATP5V	−1475.012	2074.964	1475.012	2074.964

Table 19. WLCSP 208−Bump Coordinates (Cont.)

Bump#	Signal Name	Bump Side View (0,0 center of die)		Package Top Side View (0,0 center of die)	
		X	Y	X	Y
70	SR_VDDBATP5V	−1275.014	2074.964	1275.014	2074.964
71	SR_VDDBATP5V	−1275.014	1874.966	1275.014	1874.966
72	SR_VDDBATP5V	−1275.014	1674.968	1275.014	1674.968
73	SR_VDDBATP5V	−1275.014	1474.970	1275.014	1474.970
74	SR_VDDBATA5V	−1075.016	1474.970	1075.016	1474.970
75	SR_VDDBATA5V	−875.018	1474.970	875.018	1474.970
76	VOUT_3P3	−1075.016	2074.964	1075.016	2074.964
77	VOUT_CLDO	−1075.016	1874.966	1075.016	1874.966
78	VOUT_CLDO	−1075.016	1674.968	1075.016	1674.968
79	LDO_VDD1P5	−875.018	2074.964	875.018	2074.964
80	LDO_VDD1P5	−875.018	1874.966	875.018	1874.966
81	LDO_VDD1P5	−875.018	1674.968	875.018	1674.968
82	VOUT_LNLDO	−675.020	2074.964	675.020	2074.964
83	VOUT_HSICLDO	−675.020	1874.966	675.020	1874.966
84	BT_REG_ON	−675.020	1674.968	675.020	1674.968
85	WL_REG_ON	−675.020	1474.970	675.020	1474.970
86	VDDIO_PMU	−1075.016	1274.972	1075.016	1274.972
87	HSIC_AGND1p2PLL	−1316.882	1044.986	1316.882	1044.986
88	HSIC_AVDD1p2PLL_OUT	−308.288	881.600	308.288	881.600
89	NC_89	−1863.839	772.520	1863.839	772.520
90	NC_90	−1862.633	1030.190	1862.633	1030.190
91	NC_91	−1610.156	1031.486	1610.156	1031.486
92	HSIC_PADVDD1p2	97.000	881.600	−97.000	881.600
93	HSIC_DVDD1p2_OUT	−105.725	881.600	105.725	881.600
94	WL_GPIO_0	−377.957	−1991.074	377.957	−1991.074
95	WL_GPIO_1	−338.672	−1742.170	338.672	−1742.170
96	WL_GPIO_2	−592.121	−1861.474	592.121	−1861.474
97	WL_GPIO_3	−670.385	−1621.309	670.385	−1621.309
98	WL_GPIO_4	−441.200	−1509.376	441.200	−1509.376
99	WL_GPIO_5	−842.636	−1839.190	842.636	−1839.190
100	WL_GPIO_6	−658.334	−1363.018	658.334	−1363.018
101	WL_GPIO_7	−776.783	−1138.450	776.783	−1138.450
102	WL_GPIO_8	−914.546	−1347.826	914.546	−1347.826
103	WL_GPIO_9	−921.809	−1600.906	921.809	−1600.906
104	WL_GPIO_10	−1045.496	−1141.960	1045.496	−1141.960

Table 19. WLCSP 208−Bump Coordinates (Cont.)

Bump#	Signal Name	Bump Side View (0,0 center of die)		Package Top Side View (0,0 center of die)	
		X	Y	X	Y
105	WL_GPIO_11	−1173.548	−1389.424	1173.548	−1389.424
106	WL_GPIO_12	−1094.258	−1792.165	1094.258	−1792.165
107	WL_GPIO_13	−1278.317	−1618.699	1278.317	−1618.699
108	WL_GPIO_14	−1332.434	−1868.710	1332.434	−1868.710
109	WL_GPIO_15	−1514.225	−1590.493	1514.225	−1590.493
110	JTAG_SEL	−1581.032	−1834.312	1581.032	−1834.312
111	PA_LIN_CTRL	−952.895	−652.936	952.895	−652.936
112	RF_SW_CTRL_0	−1281.395	−848.002	1281.395	−848.002
113	RF_SW_CTRL_1	−1278.011	−595.192	1278.011	−595.192
114	RF_SW_CTRL_2	−1534.160	−881.041	1534.160	−881.041
115	RF_SW_CTRL_3	−1045.982	−419.512	1045.982	−419.512
116	RF_SW_CTRL_4	−1317.755	−87.493	1317.755	−87.493
117	RF_SW_CTRL_5	−1287.470	−343.642	1287.470	−343.642
118	RF_SW_CTRL_6	−1556.822	−623.596	1556.822	−623.596
119	RF_SW_CTRL_7	−800.687	−10.327	800.687	−10.327
120	RF_SW_CTRL_8	−964.010	178.520	964.010	178.520
121	RF_SW_CTRL_9	−1539.218	−372.262	1539.218	−372.262
122	VDDIO_RF	−791.804	−459.184	791.804	−459.184
123	VDDIO_RF	−791.804	−256.891	791.804	−256.891
124	OTP_VDD33	−1049.186	−166.324	1049.186	−166.324
125	SDIO_CLK	−1100.288	394.079	1100.288	394.079
126	SDIO_CMD	−1223.291	159.818	1223.291	159.818
127	SDIO_DATA_0	−1474.841	184.226	1474.841	184.226
128	SDIO_DATA_1	−1351.442	407.444	1351.442	407.444
129	SDIO_DATA_2	−1643.717	368.906	1643.717	368.906
130	SDIO_DATA_3	−1854.857	228.992	1854.857	228.992
131	VDDIO_SD	−1601.183	−125.806	1601.183	−125.806
132	VDDIO_SD	−1781.903	−18.103	1781.903	−18.103
133	VDD_ISO	−562.799	52.322	562.799	52.322
134	PACKAGEOPTION_0	−1867.196	−1395.688	1867.196	−1395.688
135	PACKAGEOPTION_1	−1665.758	−1391.620	1665.758	−1391.620
136	PACKAGEOPTION_2	−1421.669	−1385.581	1421.669	−1385.581
137	PACKAGEOPTION_3	−1782.461	−1635.583	1782.461	−1635.583
138	VDDC_ISO_1	−69.626	1956.956	69.626	1956.956
139	BT_DEV_WAKE	715.183	651.326	−715.183	651.326

Table 19. WLCSP 208−Bump Coordinates (Cont.)

Bump#	Signal Name	Bump Side View (0,0 center of die)		Package Top Side View (0,0 center of die)	
		X	Y	X	Y
140	BT_GPIO_2	667.627	1486.517	−667.627	1486.517
141	BT_GPIO_3	567.844	855.824	−567.844	855.824
142	BT_GPIO_4	613.663	1808.663	−613.663	1808.663
143	BT_GPIO_5	361.771	733.820	−361.771	733.820
144	BT_I2S_WS	831.301	1679.396	−831.301	1679.396
145	BT_I2S_CLK	201.877	1571.432	−201.877	1571.432
146	BT_I2S_DI	−250.544	1541.453	250.544	1541.453
147	BT_I2S_DO	190.033	1823.603	−190.033	1823.603
148	BT_HOST_WAKE	833.011	1933.061	−833.011	1933.061
149	BT_PCM_CLK	−269.444	1793.471	269.444	1793.471
150	LPO_IN	−29.936	1693.643	29.936	1693.643
151	BT_PCM_OUT	−15.473	1440.320	15.473	1440.320
152	BT_PCM_SYNC	463.066	504.365	−463.066	504.365
153	BT_TM1	690.802	393.845	−690.802	393.845
154	BT_UART_CTS_N	457.252	1349.708	−457.252	1349.708
155	BT_UART_RTS_N	451.735	1616.144	−451.735	1616.144
156	BT_UART_RXD	333.871	1013.531	−333.871	1013.531
157	BT_UART_TXD	205.819	1307.444	−205.819	1307.444
158	BT_PCM_IN	−298.154	1286.816	298.154	1286.816
159	VDDC_ISO_2	422.089	1969.871	−422.089	1969.871
160	CLK_REQ	−312.509	2045.219	312.509	2045.219
161	BT_VDDO	74.500	639.500	−74.500	639.500
162	BT_VDDO	317.680	291.452	−317.680	291.452
163	BT_VDDO	203.560	476.600	−203.560	476.600
164	WL_VDDIO	−748.091	−887.233	748.091	−887.233
165	WL_VDDIO	−954.407	−906.439	954.407	−906.439
166	WL_VDDIO	−1292.078	−1169.455	1292.078	−1169.455
167	BT_VDDC	−87.635	1200.083	87.635	1200.083
168	BT_VDDC	90.997	1083.056	−90.997	1083.056
169	BT_VDDC	137.473	82.526	−137.473	82.526
170	BT_VDDC	351.295	82.526	−351.295	82.526
171	BT_VDDC	551.356	223.304	−551.356	223.304
172	BT_VDDC	568.312	1108.571	−568.312	1108.571
173	BT_VDDC	719.233	103.703	−719.233	103.703
174	BT_VDDC	762.991	970.286	−762.991	970.286

Table 19. WLCSP 208−Bump Coordinates (Cont.)

Bump#	Signal Name	Bump Side View (0,0 center of die)		Package Top Side View (0,0 center of die)	
		X	Y	X	Y
175	WL_VDDC	−1863.614	−2072.695	1863.614	−2072.695
176	WL_VDDC	−1863.614	−1872.652	1863.614	−1872.652
177	WL_VDDC	−1860.833	518.837	1860.833	518.837
178	WL_VDDC	−1660.403	−2072.695	1660.403	−2072.695
179	WL_VDDC	−1413.830	651.497	1413.830	651.497
180	WL_VDDC	−1209.557	651.497	1209.557	651.497
181	WL_VDDC	−676.541	289.013	676.541	289.013
182	WL_VDDC	−676.541	489.578	676.541	489.578
183	WL_VDDC	−542.135	−453.685	542.135	−453.685
184	WL_VDDC	−542.135	−250.618	542.135	−250.618
185	WL_VDDC	−542.135	−657.796	542.135	−657.796
186	WL_VDDC	−469.037	289.013	469.037	289.013
187	WL_VDDC	−469.037	489.578	469.037	489.578
188	WL_VDDC	−309.035	140.576	309.035	140.576
189	VSSC	−1698.581	−1188.112	1698.581	−1188.112
190	VSSC	−1610.579	770.702	1610.579	770.702
191	VSSC	−1496.486	−1135.102	1496.486	−1135.102
192	VSSC	−1210.106	858.245	1210.106	858.245
193	VSSC	−955.703	603.374	955.703	603.374
194	VSSC	−781.427	718.529	781.427	718.529
195	VSSC	−576.137	718.529	576.137	718.529
196	VSSC	−497.342	−976.405	497.342	−976.405
197	VSSC	−483.086	1079.807	483.086	1079.807
198	VSSC	−381.647	−102.262	381.647	−102.262
199	VSSC	−271.244	1079.807	271.244	1079.807
200	VSSC	−98.903	530.618	98.903	530.618
201	VSSC	−92.378	187.115	92.378	187.115
202	VSSC	32.146	−102.262	−32.146	−102.262
203	VSSC	65.266	321.719	−65.266	321.719
204	VSSC	245.671	−102.262	−245.671	−102.262
205	VSSC	453.949	−102.262	−453.949	−102.262
206	VSSC	663.469	−102.262	−663.469	−102.262
207	VSSC	815.848	1210.613	−815.848	1210.613
208	VSSC	887.785	1413.095	−887.785	1413.095

13.2 Signal Descriptions

The signal name, type, and description of each pin in the CYW4334W is listed in Table 20 . The symbols shown under Type indicate pin directions (I/O = bidirectional, I = input, O = output) and the internal pull-up/pull-down characteristics (PU = weak internal pull-up resistor and PD = weak internal pull-down resistor), if any. See also Table 21 on page 65 for resistor strapping options.

Table 20. WLBGA and WLCSP Signal Descriptions

WLCSP Bump	WLBGA Ball	Signal Name	Type	Description
WLAN RF Signal Interface				
40	G1	WRF_RFIN	I	RF input
42	H1	WRF_RFOUT	O	RF output
33, 34	K2	WRF_G_TSSI_IN	I	TSSI input
RF Control Signals				
112	J10	RF_SW_CTRL_0	O	RF switch enable
113	K9	RF_SW_CTRL_1	O	RF switch enable
114	J9	RF_SW_CTRL_2	O	RF switch enable
115	H9	RF_SW_CTRL_3	O	RF switch enable
116	H10	RF_SW_CTRL_4	O	RF switch enable
117	H8	RF_SW_CTRL_5	O	RF switch enable
118	J8	RF_SW_CTRL_6	O	RF switch enable
119	–	RF_SW_CTRL_7	O	RF switch enable
120	–	RF_SW_CTRL_8	O	RF switch enable
121	–	RF_SW_CTRL_9	O	RF switch enable
111	J3	PA_LIN_CTRL	O	External PA linearity control
SDIO Bus Interface				
125	F10	SDIO_CLK	I	SDIO clock input
126	G10	SDIO_CMD	I/O	SDIO command line
127	G9	SDIO_DATA_0	I/O	SDIO data line 0
128	F9	SDIO_DATA_1	I/O	SDIO data line 1. Also used as a strapping option (see Table 21 on page 65).
129	G8	SDIO_DATA_2	I/O	SDIO data line 2. Also used as a strapping option (see Table 21 on page 65).
130	E8	SDIO_DATA_3	I/O	SDIO data line 3. Also used for the JTAG TDI signal when JTAG mode is selected with the JTAG_SEL pin.
Note: The CYW4334W SDIO DATA and CMD lines have internal pull-ups when the chip is in SDIO mode. These pull-ups are enabled by default after the strapping options have been read, and can be disabled by software.				
JTAG Interface				
110	L8	JTAG_SEL	I/O	JTAG select: Connect this pin high (VDDIO) in order to use WL_GPIO_2 through WL_GPIO_5 and GPIO_12 as JTAG signals. See “WLAN GPIO Interface”for the JTAG signal pins. This pin has an internal pull-down resistor. If JTAG is not needed, then this pin can be a No_Connect.
WLAN GPIO Interface				

Table 20. WLBGA and WLCSP Signal Descriptions (Cont.)

WLCSP Bump	WLBGA Ball	Signal Name	Type	Description
94	J4	WL_GPIO_0/WL_HOST_WAKE	I/O	This pin can be programmed by software to be a GPIO or a WLAN_HOST_WAKE output indicating that host wake-up should be performed.
95	J5	WL_GPIO_1/WL_DEV_WAKE	I/O	This pin can be programmed by software to be a GPIO or AP_READY. This pin is also used as an out-of- band wake-up when the host wants to wake WLAN from the deep sleep mode.
96	H6	WL_GPIO_2/TCK	I/O	This pin can be programmed by software to be a GPIO, the JTAG TCK signal.
97	G6	WL_GPIO_3/TMS	I/O	This pin can be programmed by software to be a GPIO or the JTAG TMS signal.
98	H7	WL_GPIO_4/TDI/UART_RX	I/O	This pin can be programmed by software to be a GPIO, the JTAG TDI signal or the UART Rx signal.
99	L9	WL_GPIO_5/TDO/UART_TX	I/O	This pin can be programmed by software to be a GPIO, the JTAG TDO signal or the UART Tx signal.
100	J6	WL_GPIO_6/SPI_MODE_SEL	I/O	WL_GPIO_6. Also used as SPI_MODE_SEL strapping option (see Table 21 on page 65).
106	J7	WL_GPIO_12/JTAG_TRST_L	I/O	This pin can be programmed by software to be a GPIO or the JTAG TRST_L signal. This pin has an internal pull-down resistor that is enabled whenever VDDIO is present (even when the chip is in reset). Once the chip is out of reset and booted, the software can disable this pull down if desired. When JTAG_SEL is high, WL_GPIO 12 is used as JTAG_TRST_L and is pulled up.
101	–	WL_GPIO_7	I/O	GPIO/Debug pins. These are also used as strapping options (see Table 21 on page 65.
102	–	WL_GPIO_8	I/O	–
107	–	WL_GPIO_13	I/O	–
103	–	WL_GPIO_9	I/O	By default, this is an input pin. It can be programmed as a GPIO pin in the software.
104	–	WL_GPIO_10	I/O	By default, this is an input pin. It can be programmed as a GPIO pin in the software.
105	–	WL_GPIO_11	I/O	This pin has an internal pull-down resistor that is enabled whenever VDDIO is present (even when the chip is in reset). Once the chip is out of reset and booted, the software can disable this pull down if desired. By default, this is an output pin. It can be programmed as a GPIO pin in the software
108	–	WL_GPIO_14	I/O	By default, this is an output pin. It can be programmed as a GPIO pin in the software.
109	–	WL_GPIO_15	I/O	By default, this is an input pin. It can be programmed as a GPIO pin in the software.

Table 20. WLBGA and WLCSP Signal Descriptions (Cont.)

WLCSP Bump	WLBGA Ball	Signal Name	Type	Description
Clocks				
55	L5	WRF_XTAL_CAB_OP	I	XTAL oscillator input
54	L6	WRF_XTAL_CAB_ON	O	XTAL oscillator output
48	L7	WRF_TCXO_CKIN2V	I	TCXO buffered input. When not using a TCXO this pin should be connected to ground.
160	A6	CLK_REQ	O	XTAL clock request—shared by BT and WLAN
150	B6	LPO_IN	I	External sleep clock input (32.768 kHz)
Bluetooth				
21	E1	BT_RF	I/O	Bluetooth transceiver RF antenna port
Bluetooth PCM				
149	C7	BT_PCM_CLK	I/O	PCM clock; can be master (output) or slave (input)
158	D7	BT_PCM_IN	I	PCM data input sensing
151	E7	BT_PCM_OUT	O	PCM data output
152	C4	BT_PCM_SYNC	I/O	PCM sync; can be master (output) or slave (input)
Bluetooth UART				
154	D4	BT_UART_CTS_N	I	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.
155	E4	BT_UART_RTS_N	O	UART request-to-send. Active-low request-to-send signal for the HCI UART interface.
156	B5	BT_UART_RXD	I	UART serial input. Serial data input for the HCI UART interface.
157	E5	BT_UART_TXD	O	UART serial output. Serial data output for the HCI UART interface.
Bluetooth/I^2S				
145	F6	BT_I2S_CLK	I/O	I^2S clock; can be master (output) or slave (input)
147	F5	BT_I2S_DO	I/O	I^2S data output
144	G5	BT_I2S_WS	I/O	I^2S WS; can be master (output) or slave (input)
146	E6	BT_I2S_DI	I/O	I^2S data input
Bluetooth Test Mode				
153	–	BT_TM1	I/O	ARMJTAGMode
Bluetooth GPIO				
140		BT_GPIO_2	I/O	BT GPIO: multiplexed functions (see Table 23 on page 67).
141		BT_GPIO_3	I/O	BT GPIO: multiplexed functions (see Table 23 on page 67).
142		BT_GPIO_4	I/O	BT GPIO: multiplexed functions (see Table 23 on page 67).
143		BT_GPIO_5	I/O	BT GPIO: multiplexed functions (see Table 23 on page 67).
Miscellaneous				
1	B1	NC_1	I	No connect
2	–	NC_2	I	Connect to VOUT_LNLDO
4	–	NC_4	I	Connect to VOUT_LNLDO

Table 20. WLBGA and WLCSP Signal Descriptions (Cont.)

WLCSP Bump	WLBGA Ball	Signal Name	Type	Description
–	A1	FM_LNAVCOVDD	I	Connect to VOUT_LNLDO
5	–	NC_5	I	No connect
7	A3	NC_7	I	Connect to VOUT_LNLDO
8	–	NC_8	I	Connect to VOUT_LNLDO
41	L1	NC_41	I	Connect to ground
43	K1	NC_43	O	No connect
32	H2	WRF_GPIO_OUT	I/O	No connect
83	–	VOUT_HSICLDO	I	No connect
84	A5	BT_REG_ON	I	Used by PMU to power up or power down the internal CYW4334W regulators used by the Bluetooth section. Also, when deasserted, this pin holds the Bluetooth section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
85	A4	WL_REG_ON	I	Used by PMU to power up or power down the internal CYW4334W regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
88	–	HSIC_AVDD1p2PLL_OUT	O	No connect
89	E10	NC_89	I/O	No connect
90	D10	NC_90	I	No connect
91	E9	NC_91	I	No connect
92	–	HSIC_PADVDD1p2	I	No connect
93	D8	HSIC_DVDD1p2_OUT	O	No connect
139	B4	BT_DEV_WAKE/BT_GPIO_0	I/O	DEV_WAKE or general-purpose I/O signal
148	F4	BT_HOST_WAKE/BT_GPIO_1	I/O	HOST_WAKE or general-purpose I/O signal

Table 20. WLBGA and WLCSP Signal Descriptions (Cont.)

WLCSP Bump	WLBGA Ball	Signal Name	Type	Description
Integrated Voltage Regulators				
74, 75	B9	SR_VDDBATA5V	I	Quiet VBAT
69–73	A9	SR_VDDBATP5V	I	Power VBAT
61–66	B10	SR_VLX	O	Cbuck switching regulator output. See Table 39 on page 87 for details of the inductor and capacitor required on this output.
79–81	A8	LDO_VDD1P5	I	LNLDO input
82	A7	VOUT_LNLDO	O	Output of low-noise LNLDO
77, 78	B8	VOUT_CLDO	O	Output of core LDO
76	B7	VOUT_3P3	O	LDO3p3 output
Bluetooth Power Supplies				
17	–	BT_PAVDD	I	Bluetooth PA power supply
15	D1	BT_LNAVDD	I	Bluetooth LNA power supply
13	D3	BT_IFVDD	I	Bluetooth IF block power supply
19	D2	BT_PLLVDD	I	Bluetooth RF PLL power supply
23	C1	BT_VCOVDD	I	Bluetooth RF power supply
138	–	VDDC_ISO_1	I	Core supply for power-on/off island VDDC_G
159	–	VDDC_ISO_2	I	Core supply for power-on/off island VDDB
11	–	BT_LDO_OUT	O	2.5V Bluetooth LDO output
–	F1	BT_LDOPAVDD2P5	I/O	2.5V BT LDO output and Bluetooth PA power supply
22	F2	BT_VDDBAT	I	VBAT for Bluetooth
WLAN Power Supplies				
–	H4	WRF_BUCK_VDD1P5	I	Internal capacitor-less LDO input supply
47	K5	WRF_SYNTH_VDD1P2	I	Synth VDD 1.2V input
39	J1	WRF_PADRV_VBAT_VDD5P0	I	PA Driver VBAT supply
53	K6	WRF_XTAL_CAB_VDD1P2	I	XTAL oscillator supply
49	K7	WRF_TCXO_VDD1P8	I	Supply to the WRF_TCXO_CKIN input buffer. When not using a TCXO, this pin should be connected to ground.
31	–	WRF_BUCK_VCO_VDD1P5	I	Internal LDO input supply (from CBUCK)
28	–	WRF_BUCK_AFE_VDD1P5	I	Internal AFE LDO input supply (from CBUCK)
29	–	WRF_BUCK_RX_VDD1P5	I	Internal LDO input supply (from CBUCK)
30	–	WRF_BUCK_TX_VDD1P5	I	Internal LDO input supply (from CBUCK)

Table 20. WLBGA and WLCSP Signal Descriptions (Cont.)

WLCSP Bump	WLBGA Ball	Signal Name	Type	Description
Miscellaneous Power Supplies				
124	–	OTP_VDD33	I	OTP 3.3V supply
167–174, 175–188	C6, D6, F7, L10	VDDC	I	Core supply for WLAN and BT.
133	–	VDD_ISO	I	Core supply for the Power On/Off island
86, 164–166	C8, G7	VDDIO	I	IO supply (1.8–3.3V) for PMU controls and WLAN. Must be directly connected to BT_VDDO on the PCB. Labeled VDDIO_PMU on WLCSP documentation.
161–163	–	BT_VDDO	I	IO supply (1.8–3.3V) for BT. Must be directly connected to VDDIO_PMU and WL_VDDIO on the PCB.
131, 132	–	VDDIO_SD	I	IO supply for SDIO pads (1.8-3.3V)
122, 123	K10	VDDIO_RF	I/O	IO supply for RF switch control pads (3.3V)
Ground				
46	K4	WRF_SYNTH_GND1P2	I	Synth ground
51	L3	WRF_VCO_GND1P2	I	VCO/logen ground
25–27	G4	WRF_AFE_GND1P2	I	AFE ground
35	–	WRF_LDO_GND1P5	I	LDO Ground
36	G2	WRF_LNA_2G_GND1P2	I	2 GHz internal LNA ground
37	L2	WRF_LNA_5G_GND1P2	I	Ground
–	G3	WRF_RX_GND1P2	I	RX ground
50	H3	WRF_TX_GND1P2	I	TX ground
38	J2	WRF_PADRV_VBAT_GND5P0	I	PAD ground
52	L4	WRF_XTAL_CAB_GND1P2	I	XTAL ground
44	–	WRF_RX2G_GND1P2	I	RX2G ground
45	–	WRF_RX5G_GND1P2	I	Ground
12	F3	BT_LDOVSS	I	Bluetooth PA and LDO ground. Labeled BT_PALDO_VSS on WLCSP documentation.
189–208	C5, C9, D5, F8, K8	VSSC	I	Core ground for WLAN and BT
56–60	A10	SR_PVSS	I	Power Gnd
67 and 68	C10	PMU_AVSS	I	Quiet Gnd
87	D9	AGND12PLL/HSIC_AGND1p2PLL	I	Ground
18	E2	BT_PAVSS	I	Bluetooth PA ground
16	–	BT_LNAVSS	I	Bluetooth LNA ground
14	E3	BT_IFVSS	I	1.2V Bluetooth IF block ground
20	C3	BT_PLLVSS	I	Bluetooth RF PLL ground
24	C2	BT_VCOVSS	I	1.2V Bluetooth RF ground
10	A2	GND_10	I	Ground
3	B2	GND_3	I	Ground
9	B3	GND_9	I	Ground
6	–	GND_6	I	Ground
134	–	PACKAGEOPTION_0	O	PAD ground
135	–	PACKAGEOPTION_1	O	PAD ground
136	–	PACKAGEOPTION_2	O	PAD ground

Table 20. WLBGA and WLCSP Signal Descriptions (Cont.)

WLCSP Bump	WLBGA Ball	Signal Name	Type	Description
137	–	PACKAGEOPTION_3	O	PAD ground
No Connect				
–	–	–	–	–

13.2.1 WLAN GPIO Signals and Strapping Options

The pins listed in Table 21 are sampled at power-on reset (POR) to determine the various operating modes. Sampling occurs a few milliseconds after an internal POR or deassertion of the external POR. After the POR, each pin assumes the GPIO or alternative function specified in the signal descriptions table. Each strapping option pin has an internal pull-up (PU) or pull-down (PD) resistor that determines the default mode. To change the mode, connect an external PU resistor to VDDIO or a PD resistor to GND, using a 10 kΩ resistor or less.

Note: Refer to the reference board schematics for more information.

Table 21. WLAN GPIO Functions and Strapping Options (Advance Information)

Pin Name	WLCSP Pin #	WLBGA Pin #	Default	Function	Description
SDIO_DATA_1	128	F9	N/A[a]	strap_host_ifc_1	The three strap pins strap_host_ifc_[3:1] select the host interface to enable: 0XX: SDIO 10X: gSPI 110: Not supported 111: Not supported
SDIO_DATA_2	129	G8	N/A[a]	strap_host_ifc_2	0: Select gSPI mode
WL_GPIO_6/ SPI_MODE_SEL	100	J6	1	strap_host_ifc_3	0: Select SDIO mode 1: Select when using gSPI mode
WL_GPIO_7	101	–	1	OTPEnabled	This strapping option selects the use of OTP or the default CIS in the SDIO core as described in Table 22 on page 66.
WL_GPIO_8	102	–	1	LPOAutoDetEn	This strapping option selects the enable of LPO auto-detection circuit. 0: The LPOSelect strapping option determines the source of the ILP clock. 1: The LPOSelect strapping option is ignored and the external LPO is selected if it is detected; otherwise, the internal LPO is used.
WL_GPIO_13	107	–	0	LPOSelect	0: Select external sleep clock as ILP clock. 1: Select internal LPO clock. This value is ignored if the LPOAutoDetEn option is set to 1.
JTAG_SELECT	110	L8	N/A	JTAG select	Connect this pin high (VDDIO) in order to use WL_GPIO_2 through WL_GPIO_5 and WL_GPIO_12 as JTAG signals. ***Note:*** See "WLAN GPIO Interface" on page 59for the JTAG signal pins. This pin has an internal pull-down resistor. If JTAG is not needed then this pin can be a No_Connect.

a. The SDIO_DATA_1 and SDIO_DATA_2 pins have unknown default states because they are not attached to internal pulls during the strapping period (the internal pull-up resistors for the SDIO DATA and CMD lines in SDIO mode are turned on after the strapping process is completed). Pull these pins high or low to select the appropriate mode.

Table 22. OTP Select

Use SPROM	OTPEnabled	CIS Source	OTP State	ChipID Source
0	0	Default	OFF	Default
0	1	OTP if programmed, else default	ON	OTP if programmed, else default
1	0	SPROM	OFF	Default
1	1	SPROM	ON	OTP if programmed, else default

13.2.2 Multiplexed Bluetooth GPIO Signals

The Bluetooth GPIO pins (BT_GPIO_0 to BT_GPIO_7) are multiplexed pins and can be programmed to be used as GPIOs or for other Bluetooth interface signals such as I^2S. The specific function for a given BT_GPIO_X pin is chosen by programming the Pad Function Control Register for that specific pin. Table 23 shows the possible options for each BT_GPIO_X pin. Note that each BT_GPIO_X pin's Pad Function Control Register Setting is independent (BT_GPIO_1 can be set to Pad Function 7 at the same time that BT_GPIO_3 is set to PAD Function 0). When the Pad Function Control Register is set to 0, the BT_GPIOs do not have specific functions assigned to them and behave as generic GPIOs. The A_GPIO_X pins described below are multiplexed behind the CYW4334W's PCM and I^2S interface pins.

Table 23. GPIO Multiplexing Matrix

Name	Pad Function Control Register Setting							
	0	1	2	3	4	5	6	7
BT_UART_CTS_N	UART_CTS_N	–	–	–	–	–	–	A_GPIO[1]
BT_UART_RTS_N	UART_RTS_N	–	–	–	–	–	–	A_GPIO[0]
BT_UART_RXD	UART_RXD	–	–	–	–	–	–	GPIO[5]
BT_UART_TXD	UART_TXD	–	–	–	–	–	–	GPIO[4]
BT_PCM_IN	A_GPIO[3]	PCM_IN	PCM_IN	HCLK	–	–	–	I2S_SSDI/MSDI
BT_PCM_OUT	A_GPIO[2]	PCM_OUT	PCM_OUT	LINK_IND	–	I2S_MSDO	–	I2S_SSDO
BT_PCM_SYNC	A_GPIO[1]	PCM_SYNC	PCM_SYNC	HCLK	INT_LPO	I2S_MWS	–	I2S_SWS
BT_PCM_CLK	A_GPIO[0]	PCM_CLK	PCM_CLK	–	–	I2S_MSCK	–	I2S_SSCK
BT_I2S_DO	A_GPIO[5]	PCM_OUT	–	–	I2S_SSDO	I2S_MSDO	–	STATUS
BT_I2S_DI	A_GPIO[6]	PCM_IN	–	HCLK	I2S_SSDI/MSDI	–	–	TX_CON_FX
BT_I2S_WS	GPIO[7]	PCM_SYNC	–	LINK_IND	–	I2S_MWS	–	I2S_SWS
BT_I2S_CLK	GPIO[6]	PCM_CLK	–	–	INT_LPO	I2S_MSCK	–	I2S_SSCK
BT_GPIO_5[a]	GPIO[5]	HCLK	–	I2S_MSCK	I2S_SSCK	–	–	CLK_REQ
BT_GPIO_4[a]	GPIO[4]	LINK_IND	–	I2S_MSDO	I2S_SSDO	–	–	–
BT_GPIO_3[a]	GPIO[3]	–	–	I2S_MWS	I2S_SWS	–	–	–
BT_GPIO_2[a]	GPIO[2]	–	–	–	I2S_SSDI/MSDI	–	–	–
BT_GPIO_1	GPIO[1]	–	–	–	–	–	–	CLASS1[2]
BT_GPIO_0	GPIO[0]	–	–	–	clk_12p288	–	–	–
CLK_REQ	WL/BT_CLK_REQ	–	–	–	–	–	–	A_GPIO[7]

a. Available only in the WLCSP package.

The multiplexed GPIO signals are described in Table 24 .

Table 24. Multiplexed GPIO Signals

Pin Name	Type	Description
UART_CTS_N	I	Host UART clear to send
UART_RTS_N	O	Device UART request to send
UART_RXD	I	Device UART receive data
UART_TXD	O	Host UART transmit data
PCM_IN	I	PCM data input
PCM_OUT	O	PCM data output
PCM_SYNC	I/O	PCM sync signal, can be master (output) or slave (input)
PCM_CLK	I/O	PCM clock, can be master (output) or slave (input)
GPIO[7:0]	I/O	General purpose I/O
A_GPIO[7:0]	I/O	A group general purpose I/O
I2S_MSDO	O	I^2S master data output
I2S_MWS	O	I^2S master word select
I2S_MSCK	O	I^2S master clock
I2S_SSCK	I	I^2S slave clock
I2S_SSDO	O	I^2S slave data output
I2S_SWS	I	I^2S slave word select
I2S_SSDI/MSDI	I	I^2S slave/master data input
STATUS	O	Signals Bluetooth priority status
TX_CON_FX	I	WLAN-BT coexist. Transmission confirmation; permission for BT to transmit
RF_ACTIVE	O	WLAN-BT coexist. Asserted (logic high) during local BT RX and TX slots
LINK_IND	O	BT receiver/transmitter link indicator
CLK_REQ	O	WLAN/BT clock request output

13.3 I/O States

The following notations are used in Table 25 on page 69:

- I: Input signal
- O: Output signal
- I/O: Input/Output signal
- PU: Pulled up
- PD: Pulled down
- NoPull: Neither pulled up or pulled down

Table 25. I/O States

Name	*I/O*	*Keeper*	*Active Mode*	*Low Power State/ Sleep (All Power Present)*	*Power-down (BT_REG_ON and WL_REG_ON Held Low)*	*Out-of-Reset; Before SW Download (BT_REG_ON=1; WL_REG_ON=1)*	*(WL_REG_ON=1 and BT_REG_ON=0) and VDDIOs Are Present*	*(WL_REG_ON=0 and BT_REG_ON=1) and VDDIOs Are Present*	*Power Rail*
WL_REG_ON	I	N	Input; PD (pull-down can be disabled)	Input; PD (pull-down can be disabled)	Input; PD (of 200K)	Input; PD (of 200 kΩ)	Input; PD (of 200 kΩ)	Input; PD (pull-down can be disabled)	–
BT_REG_ON	I	N	Input; PD (pull down can be disabled)	Input; PD (pull down can be disabled)	Input; PD (of 200K)	Input; PD (of 200 kΩ)	Input; PD (of 200 kΩ)	Input; PD (pull down can be disabled)	–
CLK_REQ	I/O	Y	Open drain or push-pull (programmable). Active high.	Open drain or push-pull (programmable). Active high	PD	Open drain. Active high.	Open drain. Active high.	–	BT_VDDO
BT_HOST_ WAKE	I/O	Y	I/O; PU, PD, NoPull (programmable)	I/O; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PD	Input, PD	I/O; PU, PD, NoPull (programmable)	BT_VDDO
BT_DEV_WAKE	I/O	Y	I/O; PU, PD, NoPull (programmable)	Input; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PD	Input, PD	I/O; PU, PD, NoPull (programmable)	BT_VDDO
BT_GPIO2– BT_GPIO5	I/O	Y	I/O; PU, PD, NoPull (programmable)	I/O; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PD	Input, PD	I/O; PU, PD, NoPull (programmable)	BT_VDDO
BT_UART_CTS	I	Y	Input; NoPull	Input; NoPull	High-Z, NoPull	Input; PU	Input; PU	Input; NoPull	BT_VDDO
BT_UART_RTS	O	Y	Output; NoPull	Output; NoPull	High-Z, NoPull	Input; PU	Input; PU	Output; NoPull	BT_VDDO
BT_UART_RXD	I	Y	Input; PU	Input; NoPull	High-Z, NoPull	Input; PU	Input; PU	Input; PU	BT_VDDO
BT_UART_TXD	O	Y	Output; NoPull	Output; NoPull	High-Z, NoPull	Input; PU	Input; PU	Output; NoPull	BT_VDDO
SDIO_DATA_0	I/O	N	SDIO MODE = PU	SDIO MODE = PU	SDIO MODE = NoPull	SDIO MODE = PU	SDIO MODE = PU	SDIO MODE = NoPull	WL_VDDIO
SDIO_DATA_1	I/O	N	SDIO MODE = PU	SDIO MODE = PU	SDIO MODE = NoPull	SDIO MODE = PU	SDIO MODE = PU	SDIO MODE = NoPull	WL_VDDIO
SDIO_DATA_2	I/O	N	SDIO MODE = PU	SDIO MODE = PU	SDIO MODE = NoPull	SDIO MODE = PU	SDIO MODE = PU	SDIO MODE = NoPull	WL_VDDIO
SDIO_DATA_3	I/O	N	SDIO MODE = PU	SDIO MODE = PU	SDIO MODE = NoPull	SDIO MODE = PU	SDIO MODE = PU	SDIO MODE = NoPull	WL_VDDIO
SDIO_CMD	I/O	N	SDIO MODE = PU	SDIO MODE = PU	SDIO MODE = NoPull	SDIO MODE = PU	SDIO MODE = PU	SDIO MODE = NoPull	WL_VDDIO
SDIO_CLK	I	N	SDIO MODE = NoPull	SDIO MODE = NoPull	SDIO MODE = NoPull	SDIO MODE = NoPull	SDIO MODE = NoPull	SDIO MODE = NoPull	WL_VDDIO
BT_PCM_CLK	I/O	Y	Input; NoPull (Note 4)	Input; NoPull (Note 4)	High-Z, NoPull	Input, PD	Input, PD	Input; NoPull (Note 4)	BT_VDDO
BT_PCM_IN	I/O	Y	Input; NoPull (Note 4)	Input; NoPull (Note 4)	High-Z, NoPull	Input, PD	Input, PD	Input; NoPull (Note 4)	BT_VDDO
BT_PCM_OUT	I/O	Y	Input; NoPull (Note 4)	Input; NoPull (Note 4)	High-Z, NoPull	Input, PD	Input, PD	Input; NoPull (Note 4)	BT_VDDO
BT_PCM_SYNC	I/O	Y	Input; NoPull (Note 4)	Input; NoPull (Note 4)	High-Z, NoPull	Input, PD	Input, PD	Input; NoPull (Note 4)	BT_VDDO
BT_I2S_WS	I/O	Y	Input; NoPull (Note 5)	Input; NoPull (Note 5)	High-Z, NoPull	Input, PD	Input, PD	Input; NoPull (Note 5)	BT_VDDO
BT_I2S_CLK	I/O	Y	Input; NoPull (Note 5)	Input; NoPull (Note 5)	High-Z, NoPull	Input, PD	Input, PD	Input; NoPull (Note 5)	BT_VDDO
BT_I2S_DI	I/O	Y	Input; NoPull (Note 5)	Input; NoPull (Note 5)	High-Z, NoPull	Input, PD	Input, PD	Input; NoPull (Note 5)	BT_VDDO
BT_I2S_DO	I/O	Y	Input; NoPull (Note 5)	Input; NoPull (Note 5)	High-Z, NoPull	Input, PD	Input, PD	Input; NoPull (Note 5)	BT_VDDO

Table 25. I/O States (Cont.)

Name	*I/O*	*Keeper*	*Active Mode*	*Low Power State/ Sleep (All Power Present)*	*Power-down (BT_REG_ON and WL_REG_ON Held Low)*	*Out-of-Reset; Before SW Download (BT_REG_ON=1; WL_REG_ON=1)*	*(WL_REG_ON=1 and BT_REG_ON=0) and VDDIOs Are Present*	*(WL_REG_ON=0 and BT_REG_ON=1) and VDDIOs Are Present*	*Power Rail*
JTAG_SEL	I	Y	PD	PD	PD	PD	PD	PD	WL_VDDIO
WL_GPIO_0	I/O	Y	PD	PD	NoPull	PD	PD	NoPull	WL_VDDIO
WL_GPIO_1	I/O	Y	NoPull	NoPull	NoPull	NoPull	NoPull	NoPull	WL_VDDIO
WL_GPIO_2	I/O	Y	PU	PU	NoPull	PU	PU	PU	WL_VDDIO
WL_GPIO_3	I/O	Y	JTAG_SEL = 1 PU; jtag_sel=0 PD	jtag_sel=1 PU; jtag_sel=0 PD	NoPull	jtag_sel=1 PU; jtag_sel=0 PD	jtag_sel=1 PU; jtag_sel=0 PD	PU	WL_VDDIO
WL_GPIO_4	I/O	Y	jtag_sel=1 PU; jtag_sel=0 PD	jtag_sel=1 PU; jtag_sel=0 PD	NoPull	jtag_sel=1 PU; jtag_sel=0 PD	jtag_sel=1 PU; jtag_sel=0 PD	PU	WL_VDDIO
WL_GPIO_5	I/O	Y	NoPull	NoPull	NoPull	NoPull	NoPull	NoPull	WL_VDDIO
WL_GPIO_6	I/O	Y	PU	PU	NoPull	PU	PU	NoPull	WL_VDDIO
WL_GPIO_7	I/O	Y	PU	PU	NoPull	PU	PU	NoPull	WL_VDDIO
WL_GPIO_8	I/O	Y	PU	PU	NoPull	PU	PU	PU	WL_VDDIO
WL_GPIO_9	I	Y	NoPull	NoPull	NoPull	NoPull	NoPull	NoPull	WL_VDDIO
WL_GPIO_10	I	Y	NoPull	NoPull	NoPull	NoPull	NoPull	NoPull	WL_VDDIO
WL_GPIO_11	O	Y	PD	PD	PD	PD	PD	PD	WL_VDDIO
WL_GPIO_12	I/O	Y	jtag_sel=1 PU; jtag_sel=0 PD	jtag_sel=1 PU; jtag_sel=0 PD	PD	jtag_sel=1 PU; jtag_sel=0 PD	jtag_sel=1 PU; jtag_sel=0 PD	PD	WL_VDDIO
WL_GPIO_13	I/O	Y	PD	PD	NoPull	PD	PD	PD	WL_VDDIO
WL_GPIO_14	O	Y	NoPull	NoPull	NoPull	NoPull	NoPull	NoPull	WL_VDDIO
WL_GPIO_15	I	Y	NoPull	NoPull	NoPull	NoPull	NoPull	NoPull	WL_VDDIO
RF_SW_CTRL_X	O	N	Output; no pulls	Output; no pulls	High-Z	Output; no pulls	Output; no pulls	Output; no pulls	VDDIO_RF

Table 25. I/O States (Cont.)

Name	*I/O*	*Keeper*	*Active Mode*	*Low Power State/ Sleep (All Power Present)*	*Power-down (BT_REG_ON and WL_REG_ON Held Low)*	*Out-of-Reset; Before SW Download (BT_REG_ON=1; WL_REG_ON=1)*	*(WL_REG_ON=1 and BT_REG_ON=0) and VDDIOs Are Present*	*(WL_REG_ON=0 and BT_REG_ON=1) and VDDIOs Are Present*	*Power Rail*

Note:

1. Keeper column: N=pad has no keeper. Y=pad has a keeper. Keeper is always active except in Power-down state.
2. If there is no keeper, and it is an input and there is Nopull, then the pad should be driven to prevent leakage due to floating pad (e.g., SDIO_CLK).
3. In the Power-down state (xx_REG_ON=0): High-Z; NoPull => the pad is disabled because power is not supplied.
4. Depending on whether the PCM interface is enabled and the configuration of PCM is in master or slave mode, it can be either output or input.
5. Depending on whether the I^2S interface is enabled and the configuration of I^2S is in master or slave mode, it can be either output or input.
6. GPIO_6, 7, 8, and 13 are input-only during the Low-Power and Deep-Sleep modes.
7. GPIO_0 through GPIO_5 and GPIO_12 can be configured to operate as inputs or outputs in Deep-Sleep mode before entering the mode.
8. The GPIO pull states for the Active and Low-Power states are hardware defaults. They can all be subsequently programmed as pull-ups or pull-downs.
9. Regarding GPIO pins, the following are the pull-up and pull-down values for both 3.3V and 1.8V VDDIO:

	Minimum (kΩ)	Typical (kΩ)	Maximum (kΩ)
3.3V VDDIO, Pull-downs:	51.5	44.5	38
3.3V VDDIO, Pull-ups:	37.4	39.5	44.5
1.8V VDDIO, Pull-downs:	64	83	116
1.8V VDDIO, Pull-ups:	65	86	118

14. DC Characteristics

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

14.1 Absolute Maximum Ratings

Caution! The absolute maximum ratings in Table 26 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 26. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
DC supply for VBAT and PA driver supply:	VBAT	–0.5 to +6.0	V
DC supply voltage for digital I/O	VDDIO	–0.5 to 3.9	V
DC supply voltage for RF switch I/Os	VDDIO_RF	–0.5 to 3.9	V
DC input supply voltage for CLDO and LNLDO1	–	–0.5 to 1.575	V
DC supply voltage for RF analog	VDDRF	–0.5 to 1.32	V
DC supply voltage for core	VDDC	–0.5 to 1.32	V
WRF_TCXO_VDD, LPO_IN	–	–0.5 to 3.63	V
Maximum undershoot voltage for I/O[a]	$V_{undershoot}$	–0.5	V
Maximum overshoot voltage for I/O[a]	$V_{overshoot}$	VDDIO + 0.5	V
Maximum Junction Temperature	T_j	125	°C

a. Duration not to exceed 25% of the duty cycle.

14.2 Environmental Ratings

The environmental ratings are shown in Table 27 .

Table 27. Environmental Ratings

Characteristic	Value	Units	Conditions/Comments
Ambient Temperature (T_A)	–30 to +85	°C	Functional operation[a]
Storage Temperature	–40 to +125	°C	–
Relative Humidity	Less than 60	%	Storage
	Less than 85	%	Operation

a. Functionality is guaranteed but specifications require derating at extreme temperatures; see the specification tables for details.

14.3 Electrostatic Discharge Specifications

Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices. Always store unused material in its antistatic packaging.

Table 28. ESD Specifications

Pin Type	Symbol	Condition	ESD Rating		Unit
			WLCSP	WLBGA	
ESD, Handling Reference: NQY00083, Section 3.4, Group D9, Table B	ESD_HAND_HBM	Human body model contact discharge per JEDEC EID/JESD22-A114	±1.5 kV	±1 kV	V
CDM	ESD_HAND_CDM	Charged device model contact discharge per JEDEC EIA/JESD22-C101	±500V	±500V[a]	V

a. Excludes WRF_RFOUT pin, which is ±250V.

14.4 Recommended Operating Conditions and DC Characteristics

Caution! Functional operation is not guaranteed outside of the limits shown in Table 29 and operation outside these limits for extended periods can adversely affect long-term reliability of the device.

Table 29. Recommended Operating Conditions and DC Characteristics

Parameter	Symbol	Value			Unit
		Minimum	Typical	Maximum	
DC supply voltage for VBAT	VBAT	2.3[a]	–	4.8[b]	V
DC supply voltage for core	VDD	1.14	1.2	1.26	V
DC supply voltage for RF blocks in chip	VDDRF	1.14	1.2	1.26	V
DC supply voltage for TCXO input buffer	WRF_TCXO_VDD	1.62	1.8	1.98	V
DC supply voltage for digital I/O	VDDIO, VDDIO_SD	1.71	–	3.63	V
DC supply voltage for RF switch I/Os	VDDIO_RF	3.13	3.3	3.46	V
External TSSI input	TSSI	0.15	–	0.95	V
Internal POR threshold	Vth_POR	0.4	–	0.7	V
SDIO Interface I/O Pins					
For VDDIO_SD = 1.8V:					
Input high voltage	VIH	1.27	–	–	V
Input low voltage	VIL	–	–	0.58	V
Output high voltage @ 2 mA	VOH	1.40	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.45	V
For VDDIO_SD = 3.3V:					
Input high voltage	VIH	0.625 × VDDIO_SD_SD	–	–	V
Input low voltage	VIL	–	–	0.25 × VDDIO_SD	V
Output high voltage @ 2 mA	VOH	0.75 × VDDIO_SD	–	-	V
Output low voltage @ 2 mA	VOL	–	–	0.125 × VDDIO_SD	V

Table 29. Recommended Operating Conditions and DC Characteristics (Cont.)

Parameter	Symbol	Value			Unit
		Minimum	Typical	Maximum	
Other Digital I/O Pins					
For VDDIO = 1.8V:					
Input high voltage	VIH	0.65 × VDDIO	–	–	V
Input low voltage	VIL	-	–	0.35 × VDDIO	V
Output high voltage @ 2 mA	VOH	VDDIO – 0.45	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.45	V
For VDDIO = 3.3V:					
Input high voltage	VIH	2.00	–	–	V
Input low voltage	VIL	–	–	0.80	V
Output high voltage @ 2 mA	VOH	VDDIO – 0.4	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.40	V
RF Switch Control Output Pins[c]					
For VDDIO_RF = 3.3V:					
Output high voltage	VOH	VDDIO_RF – 0.4	–	–	V
Output low voltage	VOL	–	–	0.40	V
Load capacitance	C_load	–	–	5	pF

a. The CYW4334W is functional across this range of voltages. Optimal RF performance specified in the data sheet, however, is guaranteed only for 3.0V < VBAT < 4.8V.
b. The maximum continuous voltage is 4.8V. Voltages up to 5.5V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.0V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.
c. Programmable 2 mA to 16 mA drive strength. Default is 10 mA.

15. Bluetooth RF Specifications

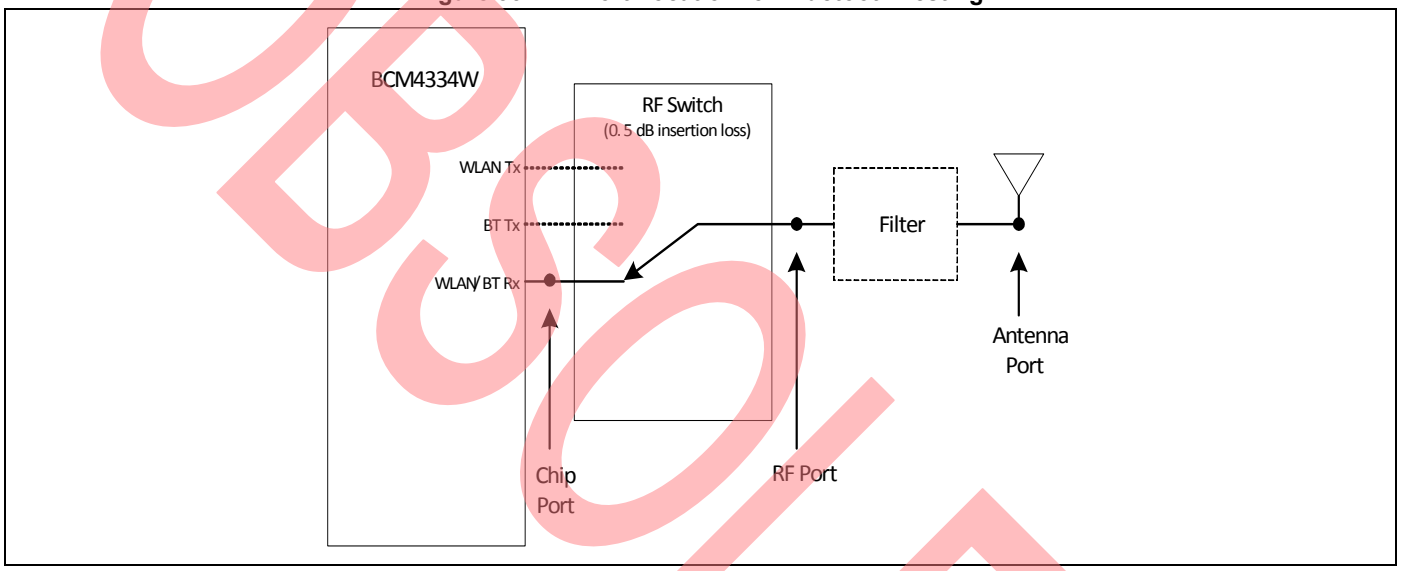
Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, limit values apply for the conditions specified in Table 27: “Environmental Ratings,” on page 72 and Table 29: “Recommended Operating Conditions and DC Characteristics,” on page 73.

Typical values apply to the following conditions:

- VBAT = 3.6V
- Ambient temperature +25°C

Figure 35. RF Port Location for Bluetooth Testing



Note: All Bluetooth specifications are measured at the Chip port unless otherwise specified.

Table 30. Bluetooth Receiver RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Note: The specifications in this table are measured at the Chip port output unless otherwise specified.					
General					
Frequency range	–	2402	–	2480	MHz
RX sensitivity	GFSK, 0.1% BER, 1 Mbps	–	–93.5	–	dBm
	π/4–DQPSK, 0.01% BER, 2 Mbps	–	–95.5	–	dBm
	8–DPSK, 0.01% BER, 3 Mbps	–	–89.5	–	dBm
Input IP3	–	–16	–	–	dBm
Maximum input at antenna	–	–	–	–20	dBm
Interference Performance[a]					
C/I co-channel	GFSK, 0.1% BER	–	8	–	dB
C/I 1-MHz adjacent channel	GFSK, 0.1% BER	–	–7	–	dB
C/I 2-MHz adjacent channel	GFSK, 0.1% BER	–	–38	–	dB
C/I ≥ 3-MHz adjacent channel	GFSK, 0.1% BER	–	–56	–	dB
C/I image channel	GFSK, 0.1% BER	–	–31	–	dB
C/I 1-MHz adjacent to image channel	GFSK, 0.1% BER	–	–46	–	dB
C/I co-channel	π/4–DQPSK, 0.1% BER	–	9	–	dB
C/I 1-MHz adjacent channel	π/4–DQPSK, 0.1% BER	–	–11	–	dB
C/I 2-MHz adjacent channel	π/4–DQPSK, 0.1% BER	–	–39	–	dB
C/I ≥ 3-MHz adjacent channel	π/4–DQPSK, 0.1% BER	–	–55	–	dB
C/I image channel	π/4–DQPSK, 0.1% BER	–	–23	–	dB
C/I 1-MHz adjacent to image channel	π/4–DQPSK, 0.1% BER	–	–43	–	dB
C/I co-channel	8–DPSK, 0.1% BER	–	17	–	dB
C/I 1 MHz adjacent channel	8–DPSK, 0.1% BER	–	–4	–	dB
C/I 2 MHz adjacent channel	8–DPSK, 0.1% BER	–	–37	–	dB
C/I ≥ 3-MHz adjacent channel	8–DPSK, 0.1% BER	–	–53	–	dB
C/I Image channel	8–DPSK, 0.1% BER	–	–16	–	dB
C/I 1-MHz adjacent to image channel	8–DPSK, 0.1% BER	–	–37	–	dB
Out-of-Band Blocking Performance (CW)					
30–2000 MHz	0.1% BER	–	–10.0	–	dBm
2000–2399 MHz	0.1% BER	–	–27	–	dBm
2498–3000 MHz	0.1% BER	–	–27	–	dBm
3000 MHz–12.75 GHz	0.1% BER	–	–10.0	–	dBm
Out-of-Band Blocking Performance, Modulated Interferer (LTE)					
GFSK (1 Mbps)[b]					
2310Mhz	LTE band40 TDD 20M BW	–	–23.8	–	dBm
2330MHz	LTE band40 TDD 20M BW	–	–24.2	–	dBm
2350MHz	LTE band40 TDD 20M BW	–	–25.7	–	dBm
2370MHz	LTE band40 TDD 20M BW	–	–28.4	–	dBm
2510MHz	LTE band7 FDD 20M BW	–	–26.6	–	dBm
2530MHz	LTE band7 FDD 20M BW	–	–22.8	–	dBm

Table 30. Bluetooth Receiver RF Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
2550MHz	LTE band7 FDD 20M BW	–	–22.3	–	dBm
2570MHz	LTE band7 FDD 20M BW	–	–21.4	–	dBm
π/4 DPSK (2 Mbps)[b]					
2310Mhz	LTE band40 TDD 20M BW	–	–22.2	–	dBm
2330MHz	LTE band40 TDD 20M BW	–	–24.5	–	dBm
2350MHz	LTE band40 TDD 20M BW	–	–25.4	–	dBm
2370MHz	LTE band40 TDD 20M BW	–	–27.5	–	dBm
2510MHz	LTE band7 FDD 20M BW	–	–25.3	–	dBm
2530MHz	LTE band7 FDD 20M BW	–	–24.7	–	dBm
2550MHz	LTE band7 FDD 20M BW	–	–21.9	–	dBm
2570MHz	LTE band7 FDD 20M BW	–	–21.1	–	dBm
8DPSK (3 Mbps)[b]					
2310Mhz	LTE band40 TDD 20M BW	–	–22.9	–	dBm
2330MHz	LTE band40 TDD 20M BW	–	–24.2	–	dBm
2350MHz	LTE band40 TDD 20M BW	–	–25.6	–	dBm
2370MHz	LTE band40 TDD 20M BW	–	–27.3	–	dBm
2510MHz	LTE band7 FDD 20M BW	–	–25.6	–	dBm
2530MHz	LTE band7 FDD 20M BW	–	–22.8	–	dBm
2550MHz	LTE band7 FDD 20M BW	–	–21.9	–	dBm
2570MHz	LTE band7 FDD 20M BW	–	–21.4	–	dBm
Out-of-Band Blocking Performance, Modulated Interferer (Non-LTE)					
GFSK (1 Mbps)[b]					
698–716 MHz	WCDMA	–	–7.0	–	dBm
776–849 MHz	WCDMA	–	–7.6	–	dBm
824–849 MHz	GSM850	–	–7.9	–	dBm
824–849 MHz	WCDMA	–	–7.9	–	dBm
880–915 MHz	E-GSM	–	–7.8	–	dBm
880–915 MHz	WCDMA	–	–7.7	–	dBm
1710–1785 MHz	GSM1800	–	–12.7	–	dBm
1710–1785 MHz	WCDMA	–	–11.9	–	dBm
1850–1910 MHz	GSM1900	–	–12.5	–	dBm
1850–1910 MHz	WCDMA	–	–11.6	–	dBm
1880–1920 MHz	TD-SCDMA	–	–11.5	–	dBm
1920–1980 MHz	WCDMA	–	–11.3	–	dBm
2010–2025 MHz	TD–SCDMA	–	–13.8	–	dBm
2500–2570 MHz	WCDMA	–	–26.1	–	dBm
π/4 DPSK (2 Mbps)[b]					
698–716 MHz	WCDMA	–	–6.9	–	dBm
776–794 MHz	WCDMA	–	–7.6	–	dBm
824–849 MHz	GSM850	–	–8.0	–	dBm

Table 30. Bluetooth Receiver RF Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
824–849 MHz	WCDMA	–	–7.9	–	dBm
880–915 MHz	E-GSM	–	–7.7	–	dBm
880–915 MHz	WCDMA	–	–7.8	–	dBm
1710–1785 MHz	GSM1800	–	–12.7	–	dBm
1710–1785 MHz	WCDMA	–	–11.9	–	dBm
1850–1910 MHz	GSM1900	–	–12.4	–	dBm
1850–1910 MHz	WCDMA	–	–11.6	–	dBm
1880–1920 MHz	TD-SCDMA	–	–12.0	–	dBm
1920–1980 MHz	WCDMA	–	–11.2	–	dBm
2010–2025 MHz	TD-SCDMA	–	–14.1	–	dBm
2500–2570 MHz	WCDMA	–	–25.1	–	dBm
8DPSK (3 Mbps)[b]					
698-716 MHz	WCDMA	–	–8.1	–	dBm
776-794 MHz	WCDMA	–	–8.1	–	dBm
824-849 MHz	GSM850	–	–8.0	–	dBm
824-849 MHz	WCDMA	–	–8.0	–	dBm
880-915 MHz	E-GSM	–	–8.0	–	dBm
880-915 MHz	WCDMA	–	–7.9	–	dBm
1710-1785 MHz	GSM1800	–	–12.9	–	dBm
1710-1785 MHz	WCDMA	–	–11.4	–	dBm
1850-1910 MHz	GSM1900	–	–10.8	–	dBm
1850-1910 MHz	WCDMA	–	–9.7	–	dBm
1880-1920 MHz	TD-SCDMA	–	–11.0	–	dBm
1920-1980 MHz	WCDMA	–	–9.2	–	dBm
2010-2025 MHz	TD-SCDMA	–	–13.6	–	dBm
2500-2570 MHz	WCDMA	–	–25.2	–	dBm
Rx LO Leakage					
2.4 GHz band	–	–	–90.0	–80.0	dBm
Spurious Emissions					
30 MHz–1 GHz		–	–95	–62	dBm
1–12.75 GHz		–	–70	–47	dBm
869–894 MHz		–	–147	–	dBm/Hz
925–960 MHz		–	–147	–	dBm/Hz
1805–1880 MHz		–	–147	–	dBm/Hz
1930–1990 MHz		–	–147	–	dBm/Hz
2110–2170 MHz		–	–147	–	dBm/Hz

a. The maximum value represents the actual Bluetooth specification required for Bluetooth qualification as defined in the version 4.0 specification.
b. Bluetooth reference level is taken at the 3dB Rx desense on each of the modulation schemes.

Note: Unless otherwise specified, the specifications in Table 31: "Bluetooth Transmitter Rf Specifications," on page 79 are measured at the chip output port and output power specifications are with the temperature correction algorithm and TSSI enabled.

Table 31. Bluetooth Transmitter Rf Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
General					
Frequency range	–	2402	–	2480	MHz
Basic rate (GFSK) Tx power at Bluetooth	–	11.0	13.0	–	dBm
QPSK Tx Power at Bluetooth	–	8.0	10.0	–	dBm
8PSK Tx Power at Bluetooth	–	8.0	10.0	–	dBm
Power control step	–	2	4	6	dB
GFSK In-Band Spurious Emissions					
–20 dBc BW	–	–	.93	1	MHz
EDR In-Band Spurious Emissions					
1.0 MHz < |M – N| < 1.5 MHz	M – N = the frequency range for which the spurious emission is measured relative to the transmit center frequency.	–	–38	–26.0	dBc
1.5 MHz < |M – N| < 2.5 MHz		–	–31	–20.0	dBm
|M – N| ≥ 2.5 MHz[a]		–	–43	–40.0	dBm
Out-of-Band Spurious Emissions					
30 MHz to 1 GHz	–	–	–	–36.0 [b, c]	dBm
1 GHz to 12.75 GHz	–	–	–	–30.0 [c, d, e]	dBm
1.8 GHz to 1.9 GHz	–	–	–	–47.0	dBm
5.15 GHz to 5.3 GHz	–	–	–	–47.0	dBm
GPS Band Spurious Emissions					
Spurious emissions	–	–	–103	–	dBm
Out-of-Band Noise Floor[f]					
65–108 MHz	FM Rx	–	–147	–	dBm/Hz
776–794 MHz	CDMA2000	–	–147	–	dBm/Hz
869–960 MHz	cdmaOne, GSM850	–	–147	–	dBm/Hz
925–960 MHz	E-GSM	–	–147	–	dBm/Hz
1570–1580 MHz	GPS	–	–146	–	dBm/Hz
1805–1880 MHz	GSM1800	–	–145	–	dBm/Hz
1930–1990 MHz	GSM1900, cdmaOne, WCDMA	–	–144	–	dBm/Hz
2110–2170 MHz	WCDMA	–	–141	–	dBm/Hz

a. Typically measured at an offset of ±3 MHz.
b. The maximum value represents the value required for Bluetooth qualification as defined in the v4.0 specification.
c. The spurious emissions during Idle mode are the same as specified in Table 31 on page 79.
d. Specified at the Bluetooth Antenna port.
e. Meets this specification using a front-end band-pass filter.
f. Transmitted power in cellular and FM bands at the Bluetooth antenna port. See Figure 35 on page 75 for location of the port.

Table 32. Local Oscillator Performance

Parameter	Minimum	Typical	Maximum	Unit
LO Performance				
Lock time	–	72	–	µs
Initial carrier frequency tolerance	–	±25	±75	kHz
Frequency Drift				
DH1 packet	–	±8	±25	kHz
DH3 packet	–	±8	±40	kHz
DH5 packet	–	±8	±40	kHz
Drift rate	–	5	20	kHz/50 µs
Frequency Deviation				
00001111 sequence in payload[a]	140	155	175	kHz
10101010 sequence in payload[b]	115	140	–	kHz
Channel spacing	–	1	–	MHz

a. This pattern represents an average deviation in payload.
b. Pattern represents the maximum deviation in payload for 99.9% of all frequency deviations.

Table 33. BLE RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Frequency range	–	2402		2480	MHz
Rx sense[a]	GFSK, 0.1% BER, 1 Mbps	–	–95.5	–	dBm
Tx power[b]	–	11	13	–	dBm
Mod Char: delta f1 average	–	225	255	275	kHz
Mod Char: delta f2 max[c]	–	99.9	–	–	%
Mod Char: ratio	–	0.8	0.95	–	%

a. The Bluetooth tester is set so that Dirty Tx is on.
b. The BLE Tx power cannot exceed the 10 dBm EIRP specification limit. The front-end losses and antenna gain/loss must be factored in so as not to exceed the limit.
c. At least 99.9% of all delta F2 max frequency values recorded over 10 packets must be greater than 185 kHz.

16. WLAN RF Specifications

16.1 Introduction

This section describes the RF characteristics of the integrated single-band direct conversion radio that supports the 2.4 GHz band.

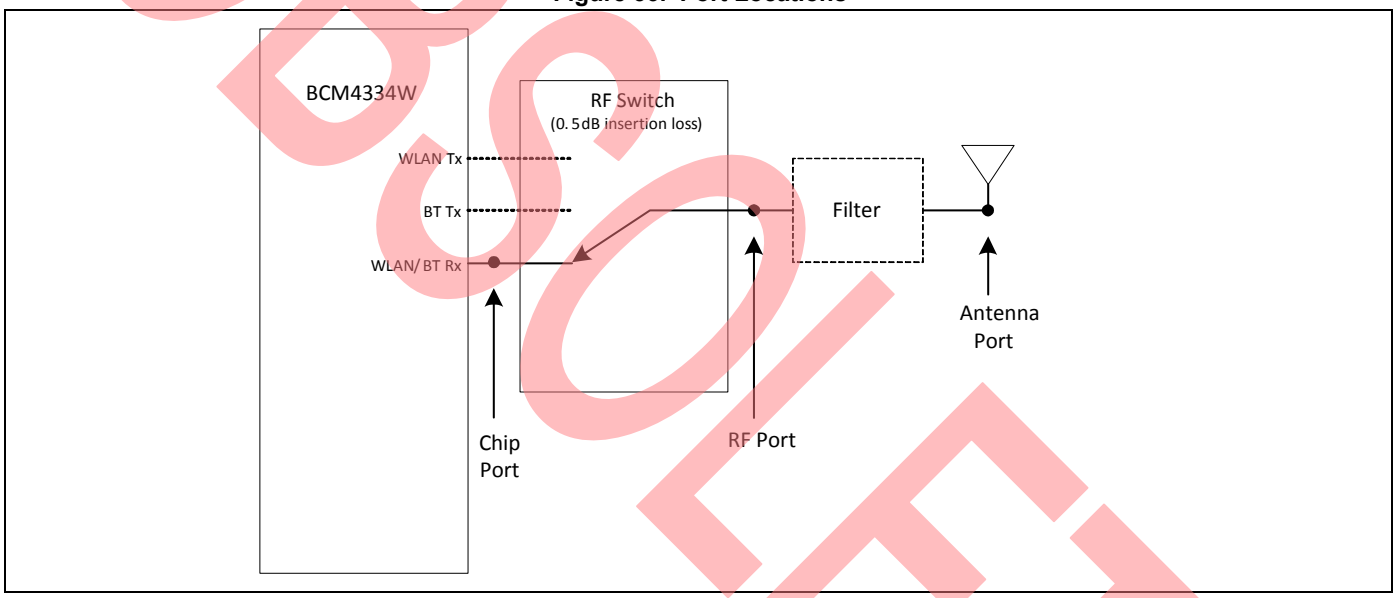
Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, limit values apply for the conditions specified inTable 27: “Environmental Ratings,” on page 72 and Table 29: “Recommended Operating Conditions and DC Characteristics,” on page 73. Typical values apply for the following conditions:

- VBAT = 3.6V
- Ambient temperature +25°C

Note: All WLAN specifications are measured at the chip port, unless otherwise specified.

Figure 36. Port Locations



16.2 2.4 GHz Band General RF Specifications

Table 34. 2.4 GHz Band General RF Specifications

Item	Condition	Minimum	Typical	Maximum	Unit
Tx/Rx switch time	Including TX ramp down	–	–	5	µs
Rx/Tx switch time	Including TX ramp up	–	–	2	µs
Power-up and power-down ramp time	DSSS/CCK modulations	–	–	< 2	µs

16.3 WLAN 2.4 GHz Receiver Performance Specifications

Note: The specifications in Table 35 are measured at the chip port, unless otherwise specified.

Table 35. WLAN 2.4 GHz Receiver Performance Specifications

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
Frequency range	–	2400	–	2500	MHz
RX sensitivity (8% PER for 1024 octet PSDU)[a]	1 Mbps DSSS	–	–98.9	–	dBm
	2 Mbps DSSS	–	–95.9	–	dBm
	5.5 Mbps DSSS	–	–93.5	–	dBm
	11 Mbps DSSS	–	–91.7	–	dBm
RX sensitivity (10% PER for 1024 octet PSDU)[a]	6 Mbps OFDM	–	–93.7	–	dBm
	9 Mbps OFDM	–	–92.4	–	dBm
	12 Mbps OFDM	–	–90	–	dBm
	18 Mbps OFDM	–	–88.4	–	dBm
	24 Mbps OFDM	–	–85.4	–	dBm
	36 Mbps OFDM	–	–82.7	–	dBm
	48 Mbps OFDM	–	–79.3	–	dBm
	54 Mbps OFDM	–	–78.1	–	dBm
RX sensitivity (10% PER for 4096 octet PSDU)[a,b.] Defined for default parameters: GF, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates	(GF)			
	MCS0	–	–93.6	–	dBm
	MCS 1	–	–90.6	–	dBm
	MCS 2	–	–88.3	–	dBm
	MCS 3	–	–85.7	–	dBm
	MCS 4	–	–83	–	dBm
	MCS 5	–	–79.4	–	dBm
	MCS 6	–	–77.9	–	dBm
	MCS 7	–	–76	–	dBm
RX sensitivity (10% PER for 4096 octet PSDU)[a,b.] Defined for default parameters: GF, 800 ns GI, and non-STBC.	40 MHz channel spacing for all MCS rates	(GF)			
	MCS 0	–	–92	–	dBm
	MCS 1	–	–88.5	–	dBm
	MCS 2	–	–86.5	–	dBm
	MCS 3	–	–84	–	dBm
	MCS 4	–	–81	–	dBm
	MCS 5	–	–76	–	dBm
	MCS 6	–	–74.5	–	dBm
	MCS 7	–	–73	–	dBm
RX sensitivity (10% PER for 4096 octet PSDU)[a,c.] Defined for default parameters: Mixed mode, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates (Mixed mode)				
	MCS0	–	–93.0	–	dBm
	MCS 1	–	–89.9	–	dBm
	MCS 2	–	–87.5	–	dBm
	MCS 3	–	–84.8	–	dBm
	MCS 4	–	–81.9	–	dBm
	MCS 5	–	–78.2	–	dBm
	MCS 6	–	–76.6	–	dBm
	MCS 7	–	–74.6	–	dBm

Table 35. WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
RX sensitivity (10% PER for 4096 octet PSDU)[a,b.] Defined for default parameters: Mixed mode, 800 ns GI, and non-STBC.	40 MHz channel spacing for all MCS rates (Mixed mode)					
	MCS 0		–	–91.0	–	dBm
	MCS 1		–	–87.4	–	dBm
	MCS 2		–	–85.2	–	dBm
	MCS 3		–	–82.6	–	dBm
	MCS 4		–	–79.4	–	dBm
	MCS 5		–	–74.3	–	dBm
	MCS 6		–	–72.6	–	dBm
	MCS 7		–	–71.0	–	dBm
Blocking level for 1dB Rx sensitivity degradation (without external filtering)[d]	776–794 MHz	CDMA2000	–20	–	–	dBm
	824–849 MHz[e]	cdmaOne	–24.5	–	–	dBm
	824–849 MHz	GSM850	–20	–	–	dBm
	880–915 MHz	E-GSM	–18	–	–	dBm
	1710–1785 MHz	GSM1800	–20	–	–	dBm
	1850–1910 MHz	GSM1800	–22	–	–	dBm
	1850–1910 MHz	cdmaOne	–32	–	–	dBm
	1850–1910 MHz	WCDMA	–29	–	–	dBm
	1920–1980 MHz	WCDMA	–32	–	–	dBm
In-band static CW jammer immunity (fc – 8 MHz < fcw < + 8 MHz)	Rx PER < 1%, 54 Mbps OFDM, 1000 octet PSDU for: (RxSens + 23 dB < Rxlevel < max input level)		–80	–	–	dBm
Input In-Band IP3[a]	Maximum LNA gain		–	–15.5	–	dBm
	Minimum LNA gain		–	–1.5	–	dBm
Maximum Receive Level @ 2.4 GHz	@ 1, 2 Mbps (8% PER, 1024 octets)		–3.5	–	–	dBm
	@ 5.5, 11 Mbps (8% PER, 1024 octets)		–9.5	–	–	dBm
	@ 6–54 Mbps (10% PER, 1024 octets)		–19.5	–	–	dBm
	@ MCS0–7 rates (10% PER, 4095 octets)		–19.5	–	–	dBm
LPF 3 dB Bandwidth	–		9	–	10	MHz
Adjacent channel rejection-DSSS (Difference between interfering and desired signal at 8% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	**Desired and interfering signal 30 MHz apart**					
	1 Mbps DSSS	–74 dBm	35	–	–	dB
	2 Mbps DSSS	–74 dBm	35	–	–	dB
	Desired and interfering signal 25 MHz apart					
	5.5 Mbps DSSS	–70 dBm	35	–	–	dB
	11 Mbps DSSS	–70 dBm	35	–	–	dB
Adjacent channel rejection-OFDM (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–79 dBm	16	–	–	dB
	9 Mbps OFDM	–78 dBm	15	–	–	dB
	12 Mbps OFDM	–76 dBm	13	–	–	dB
	18 Mbps OFDM	–74 dBm	11	–	–	dB
	24 Mbps OFDM	–71 dBm	8	–	–	dB
	36 Mbps OFDM	–67 dBm	4	–	–	dB
	48 Mbps OFDM	–63 dBm	0	–	–	dB
	54 Mbps OFDM	–62 dBm	–1	–	–	dB

Table 35. WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Adjacent channel rejection MCS0–7 (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/Notes)	MCS7	–61 dBm	–2	–	–	dB
	MCS6	–62 dBm	–1	–	–	dB
	MCS5	–63 dBm	0	–	–	dB
	MCS4	–67 dBm	4	–	–	dB
	MCS3	–71 dBm	8	–	–	dB
	MCS2	–74 dBm	11	–	–	dB
	MCS1	–76 dBm	13	–	–	dB
	MCS0	–79 dBm	16	–	–	dB
Maximum receiver gain	–	–	–	105	–	dB
Gain control step	–	–	–	3	–	dB
RSSI accuracy[f]	Range –98 dBm to –30 dBm		–5	–	5	dB
	Range above –30 dBm		–8	–	8	dB
Return loss	Z_o = 50Ω, across the dynamic range		6	10	–	dB
Receiver cascaded NF	At maximum gain		–	3.5	–	

a. Derate by 1.5 dB for –30 °C to –10°C and 55°C to 85°C.
b. Sensitivity degradations for alternate settings in MCS modes. MM: 0.5 dB drop, SGI: 2 dB drop, and STBC: 0.75 dB drop.
c. Sensitivity degradations for alternate settings in MCS modes. MM: 0.5 dB drop, SGI: 2 dB drop, and STBC: 0.75 dB drop.
d. The cellular standard listed for each band indicates the type of modulation used to generate the interfering signal in that band for the purpose of this test. It is not intended to indicate any specific usage of each band in any specific country.
e. The blocking levels are valid for channels 1 to 11. (For higher channels, the performance may be lower due to third harmonic signals (3 × 824 MHz) falling within band.)
f. The minimum and maximum values shown have a 95% confidence level.

16.4 WLAN 2.4 GHz Transmitter Performance Specifications

Note: The specifications in Table 36 are measured at the chip port output, unless otherwise specified.

Table 36. WLAN 2.4 GHz Transmitter Performance Specifications

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		2400	–	2500	MHz
Transmitted power in cellular and FM bands (at –5 dBm, 90% duty cycle, OFDM)[a]	76–108 MHz	FM Rx	–	–171	–	dBm/Hz
	776–794 MHz	–	–	–171	–	dBm/Hz
	869–960 MHz	cdmaOne, GSM850	–	–171	–	dBm/Hz
	925–960 MHz	E-GSM	–	–171	–	dBm/Hz
	1570–1580 MHz	GPS	–	–170	–	dBm/Hz
	1805–1880 MHz	GSM, WCDMA, LTE	–	–165	–	dBm/Hz
	1930–1990 MHz	GSM, WCDMA, LTE	–	–162	–	dBm/Hz
	2110–2170 MHz	WCDMA, LTE	–	–155	–	dBm/Hz
Harmonic level (–5 dBm output power; 100% duty cycle)	4.8–5.0 GHz	2nd harmonic	–	–41	–	dBm/1 MHz
	7.2–7.5 GHz	3rd harmonic	–	–69.5	–	dBm/1 MHz
OFDM EVM[b]	OFDM, BPSK	0 dBm	–29	–31	–	dB
OFDM EVM[b]	OFDM, 64 QAM	–3 dBm	–31.9	–33.9	–	dB
OFDM EVM[b]	MCS7	–6 dBm	–33	–35	–	dB
Phase noise	37.4 MHz Crystal, Integrated from 10 kHz to 10 MHz		–	0.5	–	Degrees
Tx power control dynamic range	–		20	–	–	dB
Carrier suppression	–		15	–	–	dBc
Gain control step	–		–	0.25	–	dB
Return loss at Chip port Tx	Z_o = 50Ω		4	6	–	dB

a. The cellular standards listed indicate only typical usages of that band in some countries. Other standards may also be used within those bands.
b. Derate power by 2 dB for temperatures less than –10C° or more than +55C°.

16.5 General Spurious Emissions Specifications

Table 37. General Spurious Emissions Specifications

Parameter	Condition/Notes		Min	Typ	Max	Unit
Frequency range	–		2400	–	2500	MHz
General Spurious Emissions						
Tx Emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	–	–	–62	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	–	–	–47	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	–	–	–53	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	–	–	–53	dBm

Table 37. General Spurious Emissions Specifications (Cont.)

Parameter	Condition/Notes		Min	Typ	Max	Unit
Rx/standby Emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	–	–78	–63	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	–	–68.5[a]	–53	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	–	–96	–53	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	–	–96	–53	dBm

a. For frequencies other than 3.2 GHz, the emissions value is –96 dBm. The value presented in table is the result of LO leakage at 3.2 GHz.

Table 38. General Spurious Emissions Specifications[a]

Spurious Frequency	Power (dBm)	*Frequency (Fch) (MHz)*							
		2412[b]		*5180[c]*		*5500[c]*		*5825[c]*	
		Typical (dBm)	Worst (dBm)	Typical (dBm)	Worst (dBm)	Typical (dBm)	Worst (dBm)	Typical (dBm)	Worst (dBm)
2 × VCO	–5	–60.95	–59.55	–62.17	–60.67	–64.87	–61.67	–57.97	–55.17
	–10	–64.65	–62.55	–63.27	–61.17	–64.07	–62.57	–59.07	–57.07
	–15	–64.75	–62.85	–63.47	–62.17	–63.47	–62.07	–60.27	–58.87
HD3	–5	–60.43	–59.03	–50.23	–47.03	–48.03	–45.93	–46.73	–44.63
	–10	–63.93	–62.63	–54.23	–51.93	–53.13	–50.43	–53.43	–49.93
	–15	–65.03	–63.73	–57.03	–54.53	–55.43	–53.83	–56.23	–54.13
HD2	–5	–43.57	–42.97	–40.95	–37.05	–42.75	–39.45	–40.75	–37.95
	–10	–47.87	–47.47	–45.55	–42.15	–47.45	–44.35	–46.45	–42.65
	–15	–50.87	–50.57	–49.35	–46.35	–52.15	–48.65	–50.75	–47.55
VCO/2	–5	–69.77	–68.47	–66.9	–65.2	–66.1	–64.3	–64.5	–63.3
	–10	–70.67	–69.47	–67.4	–65.8	–65.8	–65.5	–67.1	–64.7
	–15	–70.27	–69.57	–67.7	–66.5	–67.1	–66	–67.4	–65.1
5 × VCO/2	–5	–67.04	–65.64	–61.43	–59.03	–61.13	–58.73	–58.03	–56.13
	–10	–67.04	–66.34	–63.03	–60.93	–62.33	–60.93	–60.13	–58.23
	–15	–67.04	–65.44	–63.23	–61.93	–64.23	–62.23	–62.43	–60.13
VCO	–5	–49.84	–49.04	–50.03	–49.13	–50.13	–49.03	–49.63	–48.93
	–10	–49.84	–48.84	–50.03	–49.23	–50.23	–49.13	–49.73	–48.83
	–15	–49.84	–49.04	–50.13	–49.33	–50.23	–49.23	–49.63	–48.93
VCO/16	–5	–70.65	–69.45	–71.22	–69.62	–72.12	–70.52	–72.02	–70.92
	–10	–71.25	–69.75	–71.42	–69.72	–71.62	–70.72	–71.52	–70.72
	–15	–71.25	–70.15	–71.42	–69.52	–71.22	–70.42	–71.42	–70.62
5 × VCO/16	–5	–71.43	–68.63	–69.97	–68.77	–71.37	–70.17	–70.97	–70.27
	–10	–71.53	–70.73	–69.57	–69.07	–70.97	–69.87	–70.97	–69.77
	–15	–71.33	–70.03	–70.07	–68.37	–71.37	–69.77	–71.17	–70.07

a. RBW = 1 MHz, VBW = 1 MHz, sweep = auto, span = 100 MHz, detector = max peak, trace = max hold, and modulation = OFDM.
b. VCO = 1.5 × Fch, where Fch is the center frequency of the channel.
c. VCO = (2/3) × Fch, where Fch is the center frequency of the channel.

17. Internal Regulator Electrical Specifications

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Functional operation is not guaranteed outside of the specification limits provided in this section.

17.1 Core Buck Switching Regulator

Table 39. Core Buck Switching Regulator (CBUCK) Specifications

Specification	Notes	Min	Typ	Max	Units
Input supply voltage (DC), VBAT	DC voltage range inclusive of disturbances.	2.3	3.6	4.8[a]	V
PWM mode switching frequency, Fsw	Forced PWM without FLL enabled.	2.8	4	5.2	MHz
	Forced PWM with FLL enabled.	3.6	4	4.4	MHz
PWM output current	–	–	–	372	mA
Output current limit	–	–	1390	–	mA
Output voltage range	Programmable, 30 mV steps. Default = 1.35V (bits = 0000).	1.2	1.35	1.5	V
PWM output voltage DC accuracy	Includes load and line regulation. Forced PWM mode.	–4	–	4	%
	Total DC accuracy after trim.	–2	–	2	%
PWM ripple voltage, static	Measure with 20 MHz BW limit. Static Load. Max ripple based on: VBAT < 4.8V, Vout = 1.35V, Fsw = 4 MHz, 2.2 µH inductor, L > 0.6 µH, capacitor + Board total-ESR < 20 mΩ, Cout > 1.9 µF, ESL < 200 pH.	–	7	20	mVpp
PWM mode peak efficiency (Peak efficiency is at 200 mA load. The following conditions apply to all inductor types: Forced PWM, 200 mA, Vout = 1.35V, VBAT = 3.6V, Fsw = 4 MHz, at 25°C.)	2.5 x 2 mm LQM2HPN2R2NG0, L = 2 µH, DCR = 80 mΩ ±25%, ACR < 1Ω.	79	85	–	%
	0805-size LQM21PN2R2NGC, L = 2.1 µH, DCR=230 mΩ ±25%, ACR < 2Ω.	78	84	–	%
	0603-size MIPSTZ1608D2R2B, L = 2.2 µH, DCR = 390 mΩ ±30%, ACR < 2Ω.	74	81	–	%
PFM mode efficiency	10 mA load current, Vout = 1.35V, VBAT = 3.6V, 20C Cap + Board total-ESR < 20 mΩ, Cout = 4.7 µF, ESL < 200 pH, FLL= OFF 0603-size LQM18PN2R5ND0, L = 2.2 µH, DCR = 240 mΩ ±25%, ACR < 2Ω.	67	77	–	%
LPOM efficiency	1 mA load current, Vout = 1.35V, VBAT = 3.6V, 20C Cap + board total-ESR < 20 mΩ, Cout = 4.7 µF, ESL < 200 pH, FLL = OFF 0603-size LQM18PN2R5ND0, L = 2.2 µH, DCR = 240Ω ±25%, ACR < 2Ω.	55	65	–	%
Start-up time from power down	VIO already on and steady. Time from REG_ON rising edge to CLDO reaching 1.2V. Includes 256 µsec typical Vddc_ok_o delay.	–	903	1106	µs

Table 39. Core Buck Switching Regulator (CBUCK) Specifications (Cont.)

Specification	Notes	Min	Typ	Max	Units
External inductor, L[b]	–	–	2.2	–	µH
External output capacitor, Cout[b]	Ceramic, X5R, 0402, ESR < 30 mΩ at 4 MHz, ±20%, 6.3V, 4.7 µF, Murata GRM155R60J475M	2[c]	4.7	–	µF
External input capacitor, Cin[b]	For SR_VDDBATP5V pin. Ceramic, X5R, 0603, ESR < 30 mΩ at 4 MHz, ±20%, 6.3V, 4.7 µF, Murata GRM155R60J475M.	0.67[c]	4.7	–	µF
Input supply voltage ramp-up time	0 to 4.3V	40	–	–	µs

a. The maximum continuous voltage is 4.8V. Voltages up to 5.5V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.0V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.
b. Refer to *PCB Layout Guidelines and Component Selection for Optimized PMU Performance* (4334-AN200-R) for component selection details.
c. The minimum value refers to the residual capacitor value after taking into account part-to-part tolerance, DC-bias, temperature, and aging.

17.2 3.3V LDO (LDO3P3)

Table 40. LDO3P3 Specifications

Specification	Notes	Min	Typ	Max	Units
Input supply voltage	Min = 3.3 + 0.1V = 3.4V. Dropout voltage requirement must be met under maximum load for performance specifications.	2.3	3.6	4.8[a]	V
Output current	–	–	–	50	mA
Output voltage, V_o	Default = 3.3V.	2.4	3.3	3.4	V
Dropout voltage	At maximum load.	–	–	100	mV
Output voltage DC accuracy	Includes line/load regulation.	–5	–	+5	%
Quiescent current	No load.	–	8	–	µA
Line regulation	V_{in} from (V_o + 0.1V) to 4.8V, maximum load.	-0.2		+0.2	$\%V_o/V$
Load regulation	Load from 1 mA to 50 mA.	–	0.02	0.05	$\%V_o$/mA
Leakage current	Power-down mode.	–	–	5	µA
PSRR	VBAT ≥ 3.6V, V_o = 2.5V, C_o = 1 µF, maximum load, 100 Hz to 100 kHz.	20	–	–	dB
LDO turn-on time	Chip already powered up.	–	–	100	µs
In-rush current during turn-on	From its output capacitor in a fully-discharged state	–	–	70	mA
External output capacitor, C_o[b]	Ceramic, X5R, 0402, (ESR: 30–200 mΩ), ±10%, 10V	0.44[c]	1	–	µF
External input capacitor[b]	For SR_VDDBATA5V pin (shared with Bandgap) ceramic, X5R, 0402, (ESR: 30–200 mΩ), ±10%, 10V. Not needed if sharing VBAT 4.7 µF capacitor with SR_VDDBATP5V.	–	1	–	µF

a. The maximum continuous voltage is 4.8V. Voltages up to 5.5V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.0V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.
b. Refer to *PCB Layout Guidelines and Component Selection for Optimized PMU Performance* (4334-AN200-R) for component selection details.
c. The minimum value refers to the residual capacitor value after taking into account part-to-part tolerance, DC-bias, temperature, and aging.

17.3 2.5V LDO (LDO2P5)

Table 41. LDO2P5 Specifications

Specification	Notes	Min	Typ	Max	Units
Input supply voltage	Min = 2.5V + 0.15V = 2.65V. Dropout voltage requirement must be met under maximum load for performance specifications.	2.3	3.6	4.8[a]	V
Nominal output voltage	Default = 2.5V.	–	2.5	–	V
Output voltage programmability	Range	2.3	2.5	2.8	V
	Accuracy at any step (including line/load regulation), load > 0.1 mA.	–8	–	8	%
Dropout voltage	At maximum load.	–	–	150	mV
Output current	–	0.1	–	70	mA
Quiescent current	No load.[b]	–	18	27	µA
	Maximum load.	–	1000	1200	µA
Leakage current	Power-down mode.	–	1.5	5	µA
Line regulation	V_{in} from (V_o + 0.15V) to 4.8V, maximum load.	–	–	4.88	mV/V
Load regulation	Load from 1 mA to 70 mA, V_{in} = 3.6V.	–	0.4	0.6	mV/mA
Load step error	Load from 1 mA to 70 mA in 1 µs and 70 mA to 1 mA in 1 µs, $V_{in} \geq V_o$ + 0.15V, Co=2.2 µF.	–	–	70	mV
PSRR	VBAT ≥ 3.6V, V_o = 2.5V, C_o = 2.2 µF, maximum load, 100 Hz to 100 kHz.	20	–	–	dB
LDO turn-on time	Chip already powered up.	–	–	200	µs
In-rush current	V_{in} = V_o + 0.15V to 4.8V, C_o = 2.2 µF, No load.	–	–	250	mA
External output capacitor, C_o[c]	Ceramic, X5R, 0402, (ESR: 5–240 mΩ), ±10%, 10V	0.57[d]	2.2	4.7	µF
External input capacitor[b]	For SR_VDDBATA5V pin (shared with Bandgap) ceramic, X5R, 0402, (ESR: 30–200 mΩ), ±10%, 10V. Not needed if sharing VBAT 4.7 µF capacitor with SR_VDDBATP5V.	0.14[d]	1	–	µF

a. The maximum continuous voltage is 4.8V. Voltages up to 5.5V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.0V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.
b. Includes BT min-PMU support current bias.
c. Refer to *PCB Layout Guidelines and Component Selection for Optimized PMU Performance* (4334-AN200-R) for component selection details.
d. The minimum value refers to the residual capacitor value after taking into account part-to-part tolerance, DC-bias, temperature, and aging.

17.4 CLDO

Table 42. CLDO Specifications

Specification	Notes	Min	Typ	Max	Units
Input supply voltage, V_{in}	Min = 1.2 + 0.1V = 1.3V. Dropout voltage requirement must be met under maximum load.	1.2	1.35	1.5	V
Output current	–	0.1	–	150	mA
Output voltage, V_o	Programmable in 25 mV steps. Default = 1.2.V	1.1	1.2	1.275	V
Dropout voltage	At max load	–	–	100	mV
Output voltage DC accuracy[a]	Includes line/load regulation	–4	–	+4	%
	After trim. Includes line/load regulation. $V_{in} > V_o + 0.1V$.	–2	–	+2	%
Quiescent current	No load	–	10	–	µA
Line regulation	V_{in} from (V_o + 0.1V) to 1.5V, maximum load	–	–	7	mV/V
Load regulation	Load from 1 mA to 150 mA	–	15	25	µV/mA
Leakage current	Power-down	–	–	10	µA
PSRR	@1 kHz, Vin ≥ 1.5V, C_o = 1 µF	20	–		dB
Start-up time of PMU	VIO up and steady. Time from the REG_ON rising edge to the CLDO reaching 1.2V. Includes 256 µs vddc_ok_o delay.	–	–	1106	µs
LDO turn-on time	Chip already powered up.	–	–	180	µs
In-rush current during turn-on	From its output capacitor in a fully-discharged state	–	–	150	mA
External output capacitor, C_o[b]	Total ESR: 30 mΩ–200 mΩ	0.67[c]	1	–	µF
External input capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from the CBUCK output. Total ESR (trace/capacitor): 30 mΩ–200 mΩ	–	1	–	µF

a. Load from 0.1 to 150 mA.
b. Refer to *PCB Layout Guidelines and Component Selection for Optimized PMU Performance* (4334-AN200-R) for component selection details.
c. The minimum value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

17.5 LNLDO

Table 43. LNLDO Specifications

Specification	Notes	Min	Typ	Max	Units
Input supply voltage, Vin	Min = $1.2V_o$ + 0.1V = 1.3V. Dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Output current	–	0.1	–	104	mA
Output voltage, V_o	Programmable in 25 mV steps. Default = 1.2V	1.1	1.2	1.275	V
Dropout voltage	At maximum load	–	–	100	mV
Output voltage DC accuracy[a]	includes line/load regulation	–4	–	+4	%
Quiescent current	No load	–	44	–	µA
Line regulation	V_{in} from (V_o + 0.1V) to 1.5V, max load	–	–	7	mV/V
Load regulation	Load from 1 mA to 104 mA	–	15	25	µV/mA
Leakage current	Power-down	–	–	10	µA
Output noise	@30 kHz, 60 mA load, C_o = 1 µF @100 kHz, 60 mA load, C_o = 1 µF	–	–	60 35	nV/root-Hz nV/root-Hz
PSRR	@ 1kHz, input > 1.3V, C_o= 1 µF, V_o = 1.2V	20	–	–	dB
Start-up time of PMU	VIO up and steady. Time from the REG_ON rising edge to the LNLDO reaching 1.2V. Includes 256 µs vddc_ok_o delay.	–	–	1106	µs
LDO turn-on time	Chip already powered up.	–	–	180	µs
In-rush current during turn-on	From its output capacitor in a fully-discharged state	–	–	150	mA
External output capacitor, C_o[b]	Total ESR (trace/capacitor): 30–200 mΩ	0.67[c]	1	–	µF
External input capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from the CBUCK output. Total ESR (trace/capacitor): 30–200 mΩ	–	1	–	µF

a. Load from 0.1 to 104 mA.
b. Refer to *PCB Layout Guidelines and Component Selection for Optimized PMU Performance* (4334-AN200-R) for component selection details.
c. The minimum value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

18. System Power Consumption

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization. Unless otherwise stated, these values apply for the conditions specified in Table 29: "Recommended Operating Conditions and DC Characteristics," on page 73.

18.1 WLAN Current Consumption

The WLAN current consumption measurements are shown in Table 44 . All values are with the Bluetooth core in reset (that is, Bluetooth is off).

Table 44. Typical WLAN Power Consumption

Mode	Bandwidth (MHz)	Band (GHz)	*VBAT = 3.6V, VDDIO = 1.8V, T_A 25°C*	
			Vbat, mA	Vio[a], µA
Sleep Modes				
OFF[b]	–	–	0.003	3
SLEEP[c]	–	–	0.003	80
IEEE Power Save, DTIM 1[d]	–	–	0.525	80
IEEE Power Save DTIM 3[d]	–	–	0.185	80
Active Modes				
Transmit, –5 dBm[e,f]	20	2.4	53	3
Receive[g,f]	20	2.4	39	3
CRS[h]	20	2.4	37	3
Transmit, –5 dBm[e,f]	40	2.4	60	3
Receive[g,f]	40	2.4	48	3
CRS[h]	40	2.4	44	3

a. VIO is specified with all pins idle (not switching) and not driving any loads.
b. WL_REG_ON and BT_REG_ON low.
c. Idle, not associated, or inter-beacon.
d. Beacon Interval = 102.4 ms. Beacon duration = 1 ms @1 Mbps. Average current over 3 DTIM intervals.
e. Duty cycle is 100%. Excludes external PA contribution.
f. Measured using packet engine test mode.
g. Duty cycle is 100%. Carrier sense (CS) detect/packet receive.
h. Carrier sense (CCA) when no carrier present.

18.2 Bluetooth and BLE Current Consumption

The Bluetooth current consumption measurements are shown in Table 45 .

Note: The following conditions apply to the values provided in Table 45 :

- The WLAN core is in reset (WL_REG_ON = low) for all measurements.
- The BT current consumption numbers are measured based on GFSK Tx output power = 10 dBm.
- VBAT = 3.6V

VIO = 1.8V

Table 45. Bluetooth Current Consumption

Operating Mode	VBAT	VIO	Unit
Sleep	9	110	µA
SCO Master	10.18	–	mA
3DH5/3DH1 Master	27.7	–	mA
DM1/DH1 Master	21.12	–	mA
DM3/DH3 Master	25.89	–	mA
DM5/DH5 Master	26.49	–	mA
Standard 1.28s Inquiry scan	158	81	µA
Standard R1 page and 1.28 sec Inquiry scan	290	112	µA
ACL Link, Sniff mode, interval = 500 ms	126	84	µA
BLE Scan	160	82	µA
Adv—Unconnectable 1s	58	115	µA
Adv—Connectable 20 µs	2.32	0.102	mA
Connected 1s	43	108	µA

19. Interface Timing and AC Characteristics

19.1 SDIO/gSPI Timing

19.1.1 SDIO Default Mode Timing

SDIO default mode timing is shown by the combination of Figure 37 and Table 46 on page 95.

Figure 37. SDIO Bus Timing (Default Mode)

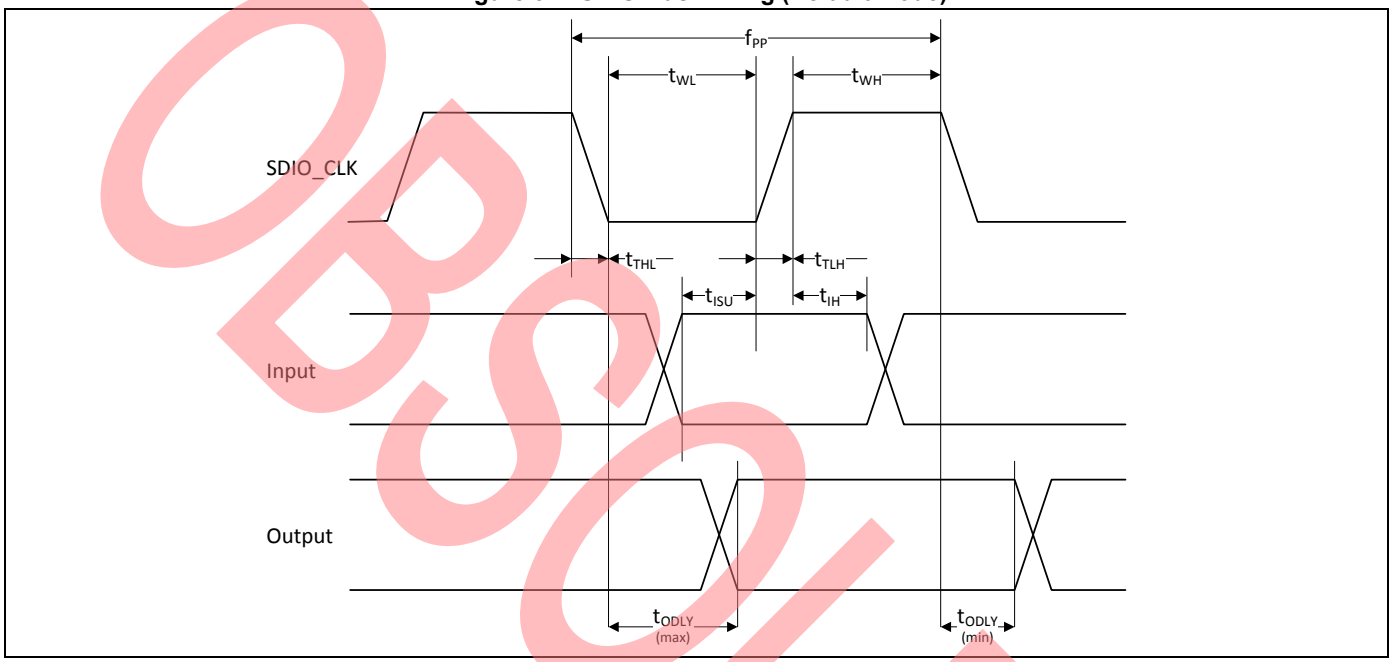


Table 46. SDIO Bus Timing[a] Parameters (Default Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer mode	fPP	0	–	25	MHz
Frequency – Identification mode	fOD	0	–	400	kHz
Clock low time	tWL	10	–	–	ns
Clock high time	tWH	10	–	–	ns
Clock rise time	tTLH	–	–	10	ns
Clock low time	tTHL	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	–	–	ns
Input hold time	tIH	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	–	14	ns
Output delay time – Identification mode	tODLY	0	–	50	ns

a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

19.1.2 SDIO High-Speed Mode Timing

SDIO high-speed mode timing is shown by the combination of Figure 38 and Table 47 .

Figure 38. SDIO Bus Timing (High-Speed Mode)

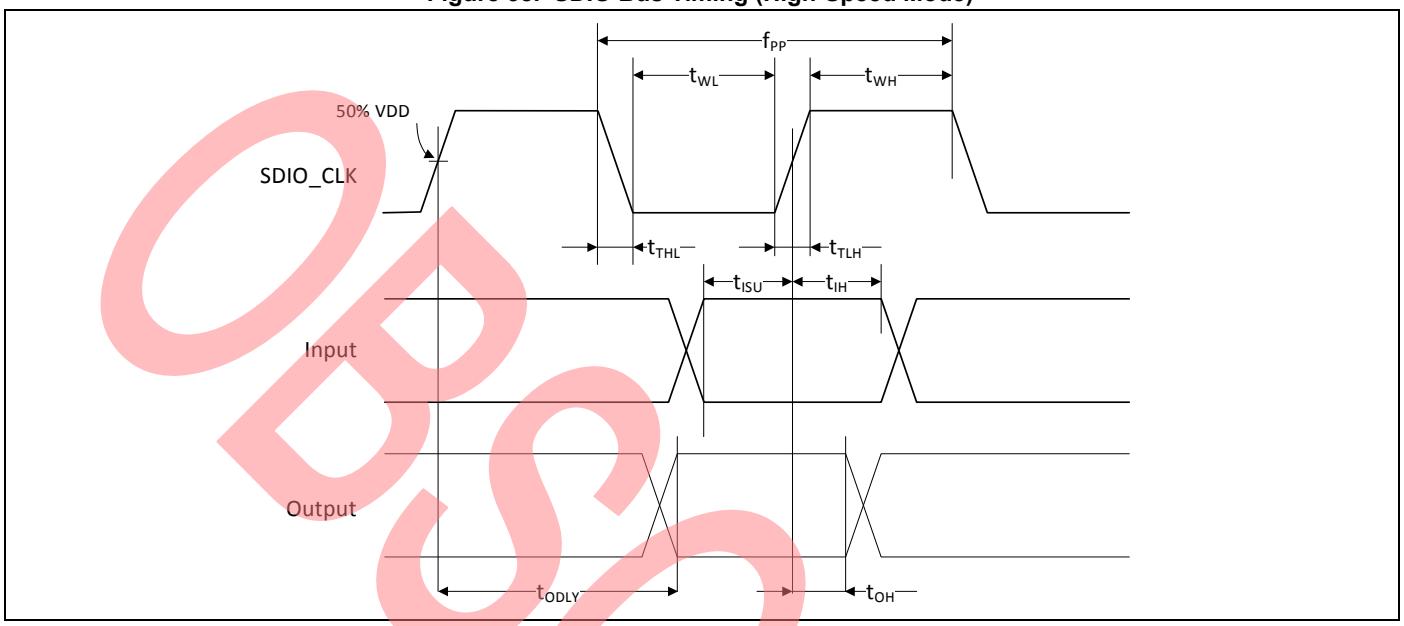


Table 47. SDIO Bus Timing[a] Parameters (High-Speed Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (all values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer Mode	fPP	0	–	50	MHz
Frequency – Identification Mode	fOD	0	–	400	kHz
Clock low time	tWL	7	–	–	ns
Clock high time	tWH	7	–	–	ns
Clock rise time	tTLH	–	–	3	ns
Clock low time	tTHL	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	tISU	6	–	–	ns
Input hold Time	tIH	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	tODLY	–	–	14	ns
Output hold time	tOH	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

19.1.3 gSPI Signal Timing

The gSPI host and device always use the rising edge of clock to sample data.

Figure 39. gSPI Timing

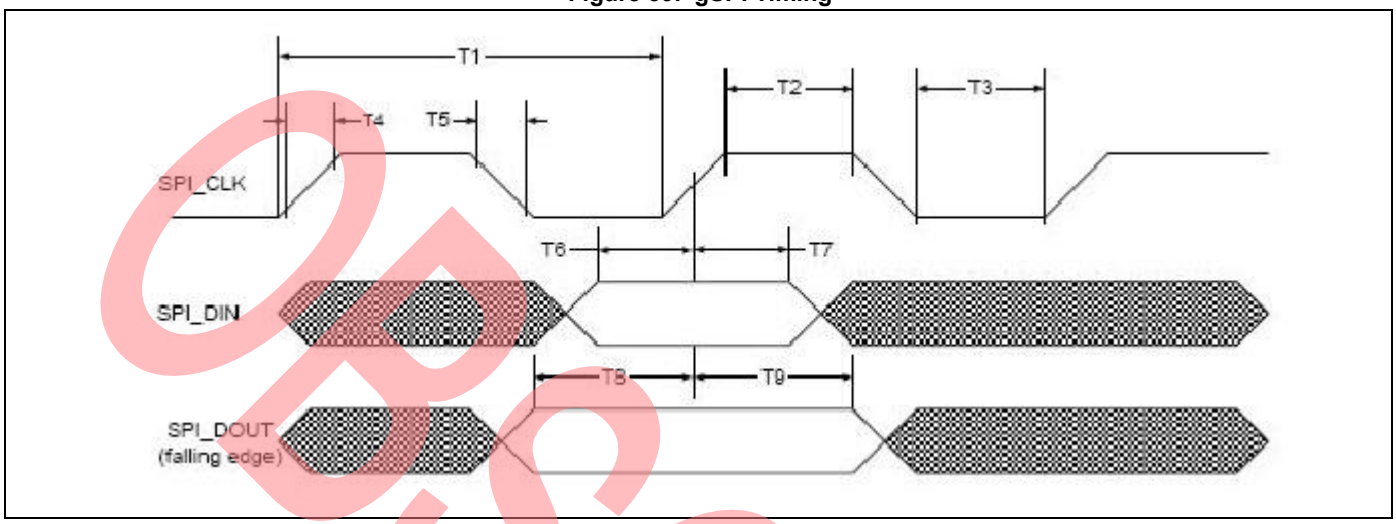


Table 48. gSPI Timing Parameters

Parameter	Symbol	Minimum	Maximum	Units	Note
Clock period	T1	20.8	–	ns	F_{max} = 48 MHz
Clock high/low	T2/T3	(0.45 × T1) – T4	(0.55 × T1) – T4	ns	–
Clock rise/fall time[a]	T4/T5	–	2.5	ns	Measured from 10% to 90% of VDDIO
Input setup time	T6	5.0	–	ns	Setup time, SIMO valid to SPI_CLK active edge
Input hold time	T7	5.0	–	ns	Hold time, SPI_CLK active edge to SIMO invalid
Output setup time	T8	5.0	–	ns	Setup time, SOMI valid before SPI_CLK rising
Output hold time	T9	5.0	–	ns	Hold time, SPI_CLK active edge to SOMI invalid
CSX to clock[b]	–	7.86	–	ns	CSX fall to 1st rising edge
Clock to CSX[a]	–	–	–	ns	Last falling edge to CSX high

a. Limit applies when SPI_CLK = Fmax. For slower clock speeds, longer rise/fall times are acceptable provided that the transitions are monotonic and the setup and hold time limits are complied with.
b. SPI_CSx remains active for entire duration of gSPI read/write/write-read transaction (overall words for multiple-word transaction)

19.2 JTAG Timing

Table 49. JTAG Timing Characteristics

Signal Name	Period	Output Maximum	Output Minimum	Setup	Hold
TCK	125 ns	–	–	–	–
TDI	–	–	–	20 ns	0 ns
TMS	–	–	–	20 ns	0 ns
TDO	–	100 ns	0 ns	–	–
JTAG_TRST	250 ns	–	–	–	–

20. Power-Up Sequence and Timing

20.1 Sequencing of Reset and Regulator Control Signals

The CYW4334W has three signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states (see Figure 40, Figure 41 on page 100, and Figure 42 and Figure 43 on page 101). The timing values indicated are minimum required values; longer delays are also acceptable.

Note:

- The WL_REG_ON and BT_REG_ON signals are ORed in the CYW4334W. The diagrams show both signals going high at the same time (as would be the case if both REG signals were controlled by a single host GPIO). If two independent host GPIOs are used (one for WL_REG_ON and one for BT_REG_ON), then only one of the two signals needs to be high to enable the CYW4334W regulators.
- The CYW4334W has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold (see Table 29: "Recommended Operating Conditions and DC Characteristics," on page 73). Wait at least 150 ms after VDDC and VDDIO are available before initiating SDIO accesses.

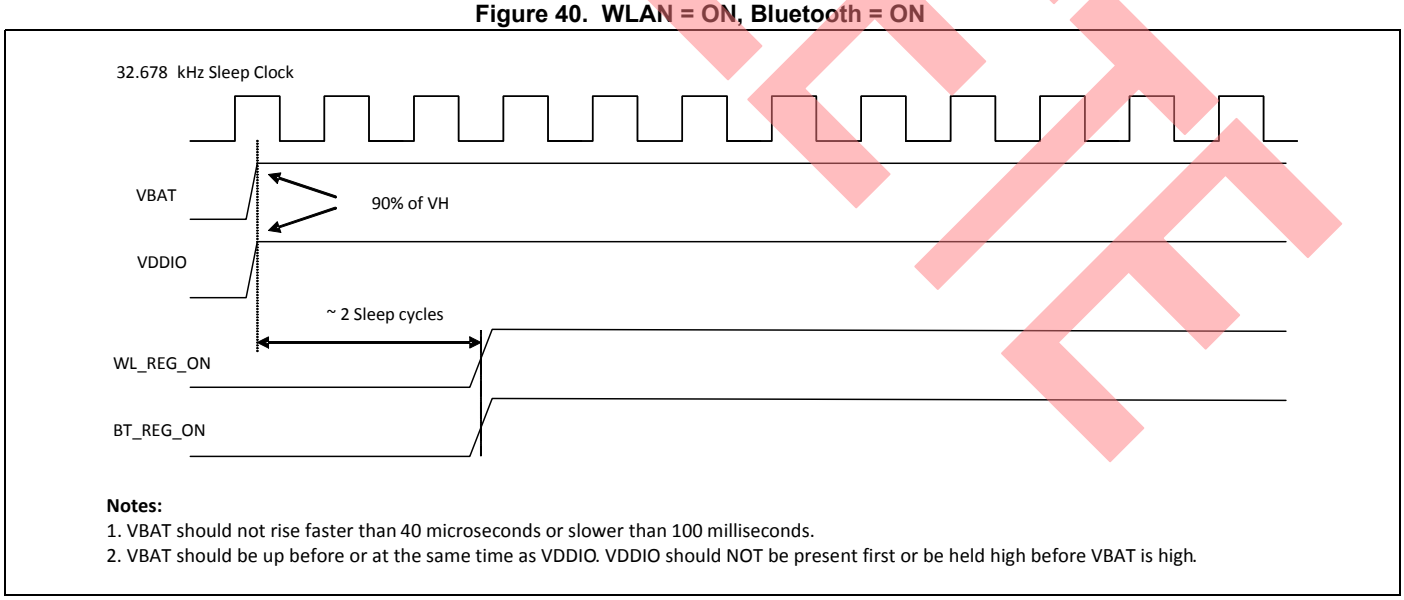
20.1.1 Description of Control Signals

- **WL_REG_ON**: Used by the PMU to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal CYW4334W regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled.
- **BT_REG_ON**: Used by the PMU (OR-gated with WL_REG_ON) to power up the internal CYW4334W regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled. When this pin is low and WL_REG_ON is high, the BT section is in reset.

Note: For both the WL_REG_ON and BT_REG_ON pins, there should be at least a 10 msec time delay between consecutive toggles (where both signals have been driven low). This is to allow time for the CBUCK regulator to discharge. If this delay is not followed, then there may be a VDDIO in-rush current on the order of 36 mA during the next PMU cold start.

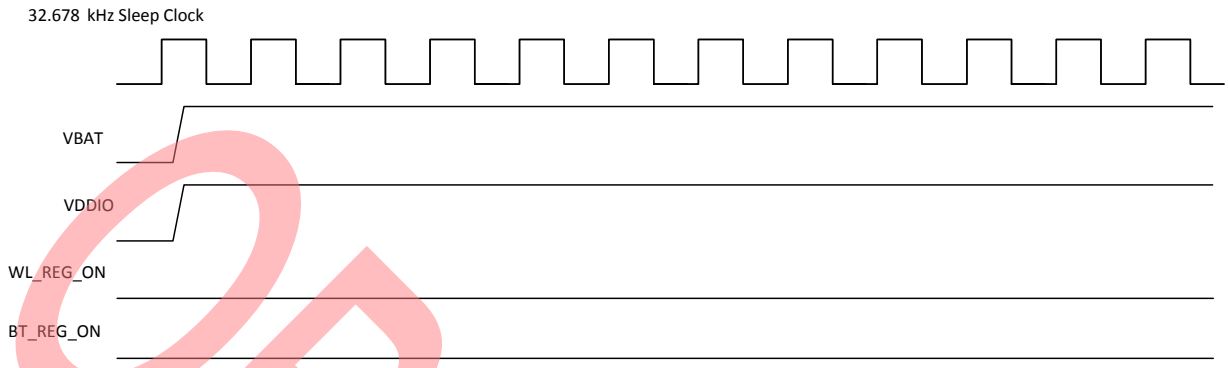
20.1.2 Control Signal Timing Diagrams

Figure 40. WLAN = ON, Bluetooth = ON



Notes:
1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

Figure 41. WLAN = OFF, Bluetooth = OFF

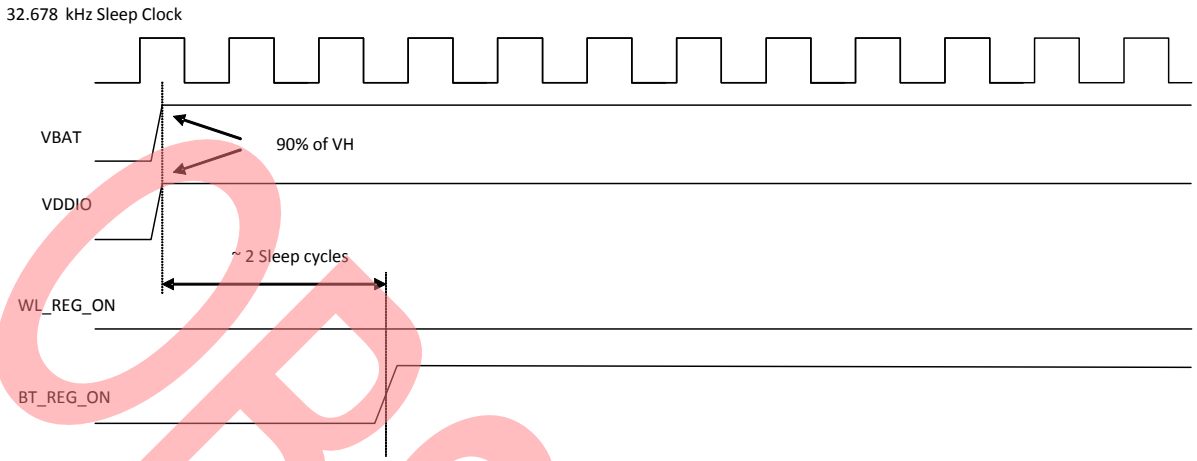


Notes:
1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

Figure 42. WLAN = ON, Bluetooth = OFF

Notes:
1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

Figure 43. WLAN = OFF, Bluetooth = ON



Notes:
1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

21. Package Information

21.1 Package Thermal Characteristics

Table 50. Package Thermal Characteristics[a]

Characteristic	WLBGA	WLSCP
θ_{JA} (°C/W) (value in still air)	40.59	40.26
θ_{JB} (°C/W)	1.82	1.60
θ_{JC} (°C/W)	0.50	0.50
Ψ_{JT} (°C/W)	0.98	0.39
Ψ_{JB} (°C/W)	12.73	9.34
Maximum Junction Temperature T_j	125°C	125°C
Maximum Power Dissipation (W)	0.87	0.87

a. No heat sink, TA = 70°C. This is an estimate, based on a 4-layer PCB that conforms to EIA/JESD51–7 (101.6 mm × 114.3 mm × 1.6 mm) and P = 0.87W continuous dissipation.

21.2 Junction Temperature Estimation and PSI$_{JT}$ Versus THETA$_{JC}$

Package thermal characterization parameter PSI–J_T (Ψ_{JT}) yields a better estimation of actual junction temperature (T_J) versus using the junction-to-case thermal resistance parameter Theta–J_C (θ_{JC}). The reason for this is that θ_{JC} assumes that all the power is dissipated through the top surface of the package case. In actual applications, some of the power is dissipated through the bottom and sides of the package. Ψ_{JT} takes into account power dissipated through the top, bottom, and sides of the package. The equation for calculating the device junction temperature is:

$$T_J = T_T + P \times \Psi_{JT}$$

Where:

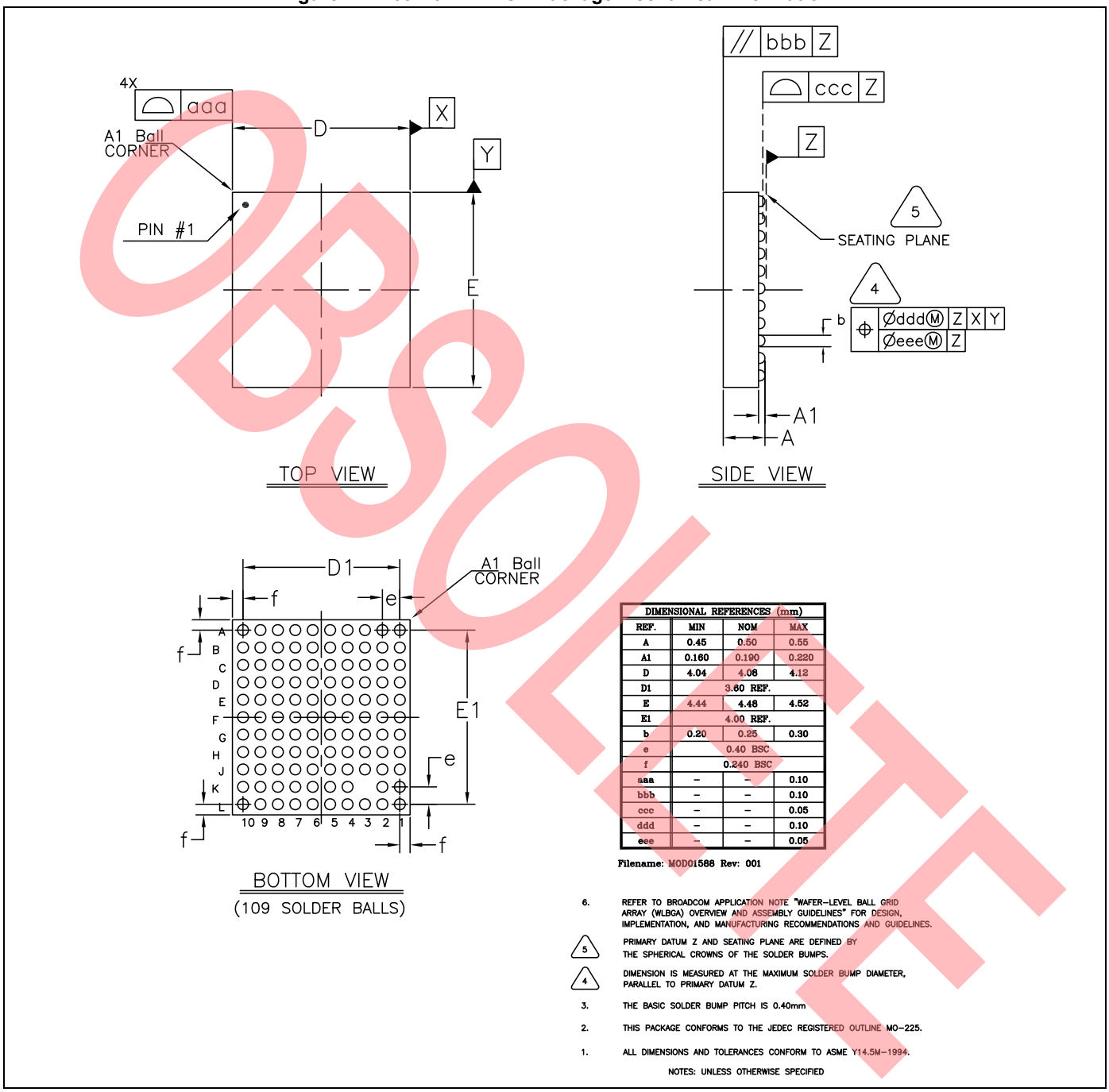
- T_J = Junction temperature at steady-state condition (°C)
- T_T = Package case top center temperature at steady-state condition (°C)
- P = Device power dissipation (Watts)
- Ψ_{JT} = Package thermal characteristics; no airflow (°C/W)

21.3 Environmental Characteristics

For environmental characteristics data, see Table 27: “Environmental Ratings,” on page 72.

22. Mechanical Information

Figure 44. 109-Ball WLBGA Package Mechanical Information



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.160	0.190	0.220
D	4.04	4.08	4.12
D1		3.60 REF.	
E	4.44	4.48	4.52
E1		4.00 REF.	
b	0.20	0.25	0.30
e		0.40 BSC	
f		0.240 BSC	
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.05
ddd	–	–	0.10
eee	–	–	0.05

Filename: MOD01588 Rev: 001

6. REFER TO BROADCOM APPLICATION NOTE "WAFER-LEVEL BALL GRID ARRAY (WLBGA) OVERVIEW AND ASSEMBLY GUIDELINES" FOR DESIGN, IMPLEMENTATION, AND MANUFACTURING RECOMMENDATIONS AND GUIDELINES.

5 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BUMPS.

4 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BUMP DIAMETER, PARALLEL TO PRIMARY DATUM Z.

3. THE BASIC SOLDER BUMP PITCH IS 0.40mm

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO-225.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Note: Top-layer metal is not allowed in the keep-out areas.

Figure 45. WLBGA Keep-Out Areas for PCB Layout—Bottom View

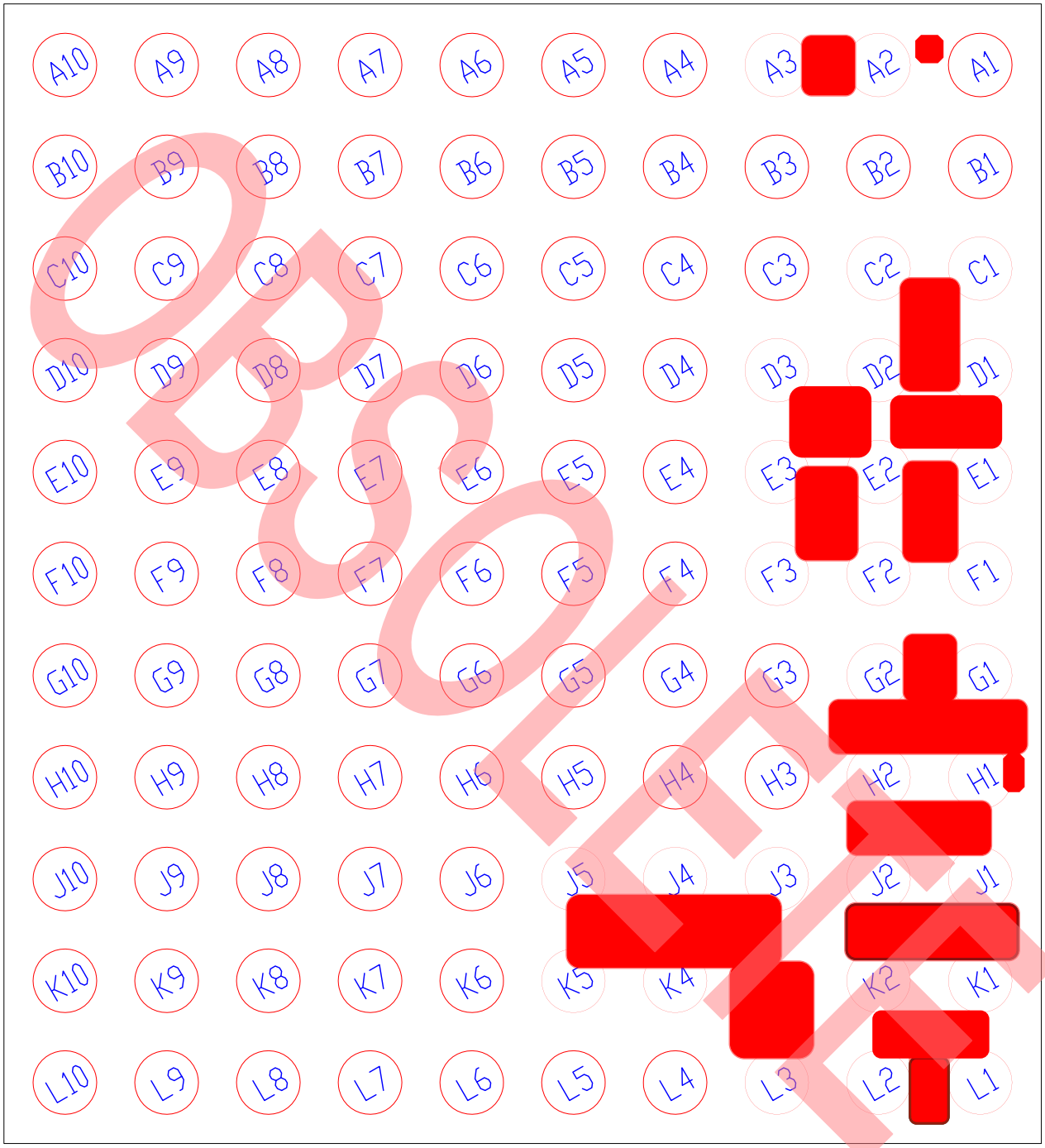
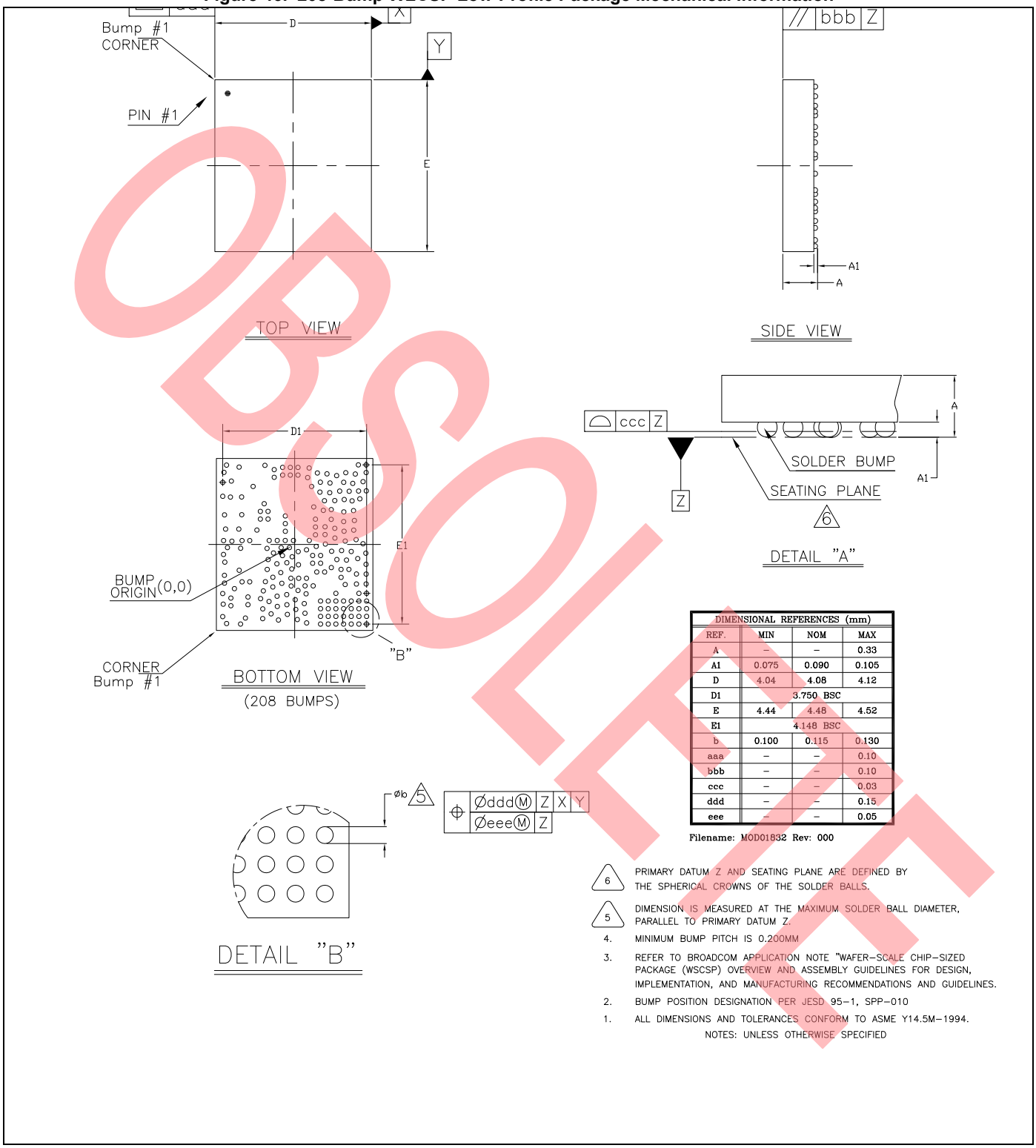
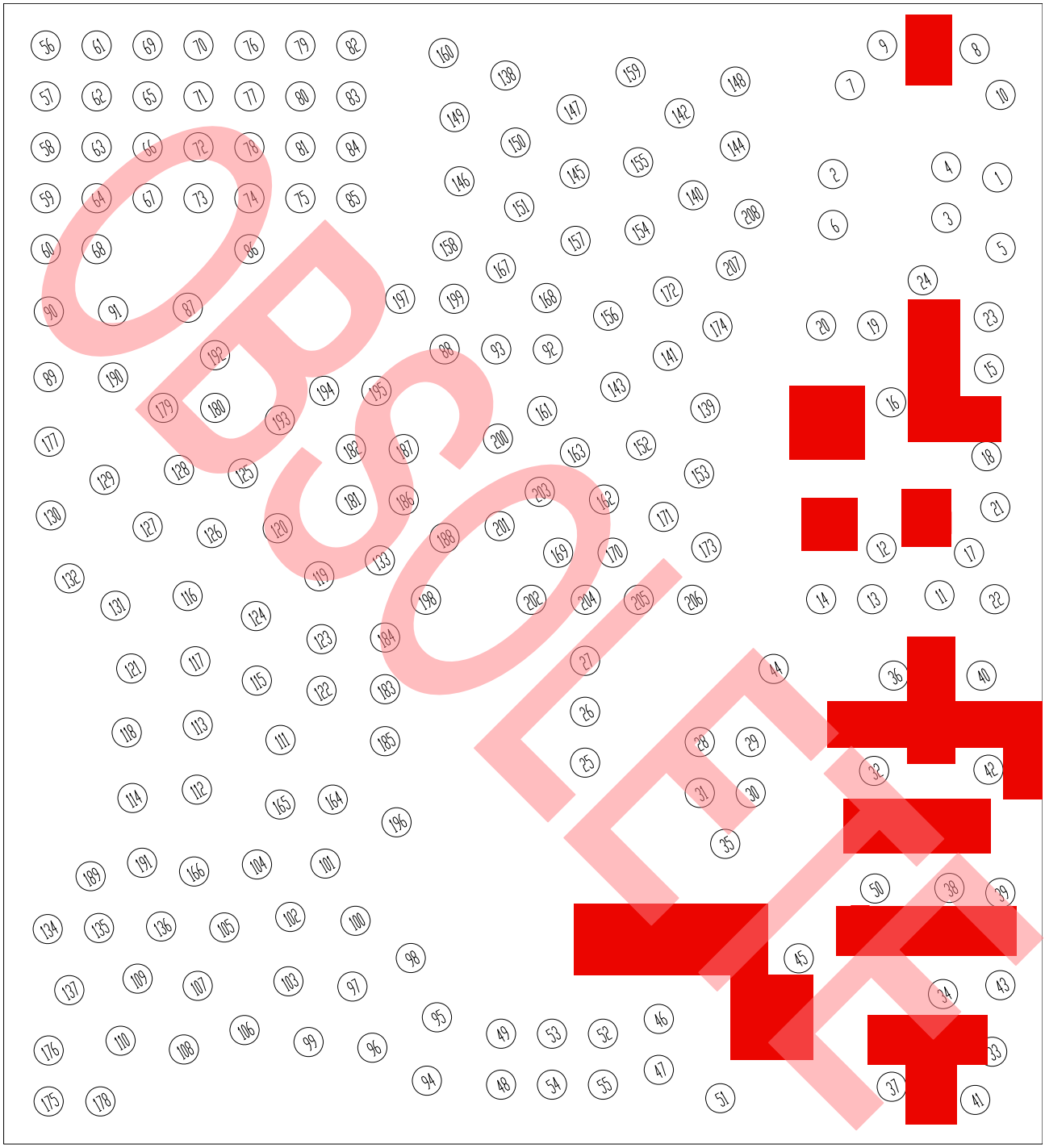


Figure 46. 208-Bump WLCSP Low-Profile Package Mechanical Information



Note: Top-layer metal is not allowed in the keep-out areas.

Figure 47. WLCSP Keep-Out Areas for PCB Layout—Bottom View with Bumps Facing Up



23. Ordering Information

Part Number	Package	Description	Operating Ambient Temperature
CYW4334WKWBG	208 bump WLCSP (4.08 mm × 4.48 mm, 0.2 mm pitch, 330 µm thickness)	Single-band 2.4 GHz WLAN + BT 4.0 low-profile package	–30°C to +85°C
CYW4334WKUBG	109 ball WLBGA (4.08 mm × 4.48 mm, 0.4 mm pitch)	Single-band 2.4 GHz WLAN + BT 4.0	–30°C to +85°C

Document History

Document Title: CYW4334W Single-Chip IEEE 802.11 b/g/n MAC/Baseband/ Radio with Integrated Bluetooth 4.0 Document Number: 002-14948				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	-	-	12/13/13	4334W-DS100-R: Initial release.
*A	-	-	1/10/2014	4334W-DS101-R: Updated: • Figure 31: "109-WLBGA Ball Map (Bottom View)," on page 59 • Figure 32: "208-WLCSP Bump Map (Bottom View)," on page 60 • Table 18: "WLCSP 208 – Bump Coordinates," on page 61 • Table 19: "WLBGA and WLCSP Signal Descriptions," on page 67
*B	-	-	3/19/2014	4334W-DS102-R: Updated: • Table 4, "External 32.768 kHz Sleep Clock Specifications," on page 14
*C	-	-	4/30/2014	4334W-DS103-R: Updated: • "External 32.768 kHz Low-Power Oscillator" on page 14 • Table 4, "External 32.768 kHz Sleep Clock Specifications," on page 14 • Table 26, "Absolute Maximum Ratings," on page 72
*D	5446871	UTSV	10/21/2016	Migrated to cypress template.
*E	5715511	UTSV	04/27/2017	Updated Cypress Logo and Copyright. Please Obsolete the Datasheet.

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