

Ordering Information

Part Numbers	Description	Device Vendor
SH5127RD451851SDV	512Mx72 (4GB), DDR4, 288-Pin Registered DIMM, Parity, ECC, VLP, 512Mx8 Based, DDR4-2133-15-15-15, 18.75mm, 1.2V, Halogen-Free (RoHS Compliant).	Samsung, Rev. D K4A4G085WD-BCPB

(All specifications of this module are subject to change without notice.)

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Part Number Decode

S	H	512	7	RD4	518	5	1	S	D	V
1	2	3	4	5	6	7	8	9	10	11

1	SMART Modular Technologies
2	Module Process Technology H: Halogen-Free (RoHS Compliant)
3	Module Address Depth 512: 512M
4	Module Data Bus Width 7: x72
5	Module Configuration RD4: 1.2V DDR4 288-Pin Registered DIMM
6	Device Configuration 518: 512Mx8 Based
7	CAS Latency 5: CL 15
8	Device Speed 1: DDR4-2133
9	Device Vendor S: Samsung
10	Device Revision D: Revision D
11	Module Characteristics V: VLP Module Height



Revision History

Date	Description
August 21, 2014	Datasheet released.

4GB (512Mx72) DDR4 SDRAM Module - 512Mx8 Based 288-Pin Registered DIMM, Parity, ECC, VLP

Features

- Standard = JEDEC
- Configuration = ECC
- Number of Module Ranks = 1
- Number of Devices = 9
- $V_{DD} = V_{DDQ} = 1.2V$
- $V_{PP} = 2.5V$
- $V_{DDSPD} = 2.25V$ to $2.75V$
- Cycle Time = 0.938ns
- \overline{CAS} Latency = 9, 11, 12, 13, 14, 15, 16
- \overline{CAS} Latency with Read DBI = TBD
- Additive Latency = 0, CL - 1, and CL - 2
- \overline{CAS} Write Latency (CWL) = 9, 10, 11, 12, 14
- Burst Length (BL) switch on-the-fly BL8 or BC4 (Burst Chop)
- Burst Type = Sequential & Interleave
- Bi-Directional Differential Data Strobe
- On-Die Termination (ODT)
- 8 bit pre-fetch
- Device Package = FBGA
- Lead Finish = $\geq 0.76\mu m$ Gold
- Length x Height = 133.35mm x 18.75mm
- No. of sides = Double-sided
- Mating Connector (Examples)
 - Vertical = Molex - 0787261002
 - Vertical = TE Connectivity - 2199154-2
- Bank Grouping is applied, and \overline{CAS} to \overline{CAS} latency (t_{CCD_L} , t_{CCD_S}) for the banks in the same or different bank group accesses are available
- Supports ECC error correction and detection
- Temperature sensor with integrated SPD
- Per DRAM Addressability is supported
- Internal V_{REF} DQ level generation is available
- Write CRC is supported at all speed grades
- DBI (Data Bus Inversion) is supported (x8)
- CA parity (Command/Address Parity) mode is supported

Addressing

Device Configuration	512Mx8
Number of Bank Groups	4
Bank Groups	BG0 - BG1
Bank Address	BA0 - BA1
Row Address	A0 - A14
Column Address	A0 - A9
Page size	1KB

Pin Description Table

Symbol	Type	Function
CK0-CK1, CK0-CK1	Input	Clock: CK and \overline{CK} are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of \overline{CK} .
CKE0	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After V_{REFCA} and Internal DQ V_{REF} have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, \overline{CK} , ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
$\overline{CS0}$	Input	Chip Select: All commands are masked when \overline{CS} is registered HIGH. \overline{CS} provides for external Rank selection on systems with multiple Ranks. \overline{CS} is considered part of the command code.
ODT0	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS, \overline{DQS} and $\overline{DM/DBI/TDQS}$, $\overline{NU/TDQS}$ (When TDQS is enabled via Mode Register A11=1 in MR1) signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
\overline{ACT}	Input	Activation Command Input: \overline{ACT} defines the Activation command being entered along with \overline{CS} . The input into RAS/A16, CAS/A15 and WE/A14 will be considered as Row Address A16, A15 and A14.
$\overline{RAS/A16}$, $\overline{CAS/A15}$, $\overline{WE/A14}$	Input	Command Inputs: $\overline{RAS/A16}$, $\overline{CAS/A15}$ and $\overline{WE/A14}$ (along with \overline{CS}) define the command being entered. Those pins have multi function. For example, for activation with \overline{ACT} Low, those are Addressing like A16, A15 and A14 but for non-activation command with \overline{ACT} High, those are Command pins for Read, Write and other command defined in command truth table.
$\overline{DM0/DBI0/}$ $\overline{TDQS0-}$ $\overline{DM8/DBI8/}$ $\overline{TDQS8}$	Input/ Output	Input Data Mask and Data Bus Inversion: \overline{DM} is an input mask signal for write data. Input data is masked when \overline{DM} is sampled LOW coincident with that input data during a Write access. \overline{DM} is sampled on both edges of DQS. \overline{DM} is muxed with DBI function by Mode Register A10, A11, A12 setting in MR5. The function of \overline{DM} or \overline{TDQS} is enabled by Mode Register A11 setting in MR1. \overline{DBI} is an input/output identifying whether to store/output the true or inverted data. If DBI is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI is HIGH.
BG0-BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle.
BA0-BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0-A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/ \overline{BC} , RAS/A16, $\overline{CAS/A15}$ and $\overline{WE/A14}$ have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is connected to the register for the CA parity check.
A10/AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Auto-precharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Auto-precharge; LOW: no Auto-precharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12/ \overline{BC}	Input	Burst Chop: A12/ \overline{BC} is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
\overline{RESET}	Input	Active Low Asynchronous Reset: Reset is active when \overline{RESET} is LOW, and inactive when \overline{RESET} is HIGH. \overline{RESET} must be HIGH during normal operation. \overline{RESET} is a CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DD} .

Pin Description Table (Continued)

Symbol	Type	Function
DQ0-DQ63 CB0-CB7	Input/ Output	Data Input/Output: Bi-directional data bus. If CRC is enabled via Mode register, then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal V_{REF} level during test via Mode Register Setting MR4 A4 = HIGH.
DQS0-DQS8 DQS0-DQS8	Input/ Output	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
$\overline{TDQS0-TDQS8}$ $\overline{TDQS0-TDQS8}$	Output	Termination Data Strobe: $\overline{TDQS}/\overline{TDQS}$ is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on $\overline{TDQS}/\overline{TDQS}$ that is applied to DQS/DQS. When disabled via mode register A11 = 0 in MR1, $\overline{DM}/\overline{DBI}/\overline{TDQS}$ will provide the data mask function or Data Bus Inversion depending on MR5; A11,12,10 and \overline{TDQS} is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
PARITY	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with \overline{ACT} , $\overline{RAS}/A16$, $\overline{CAS}/A15$, $\overline{WE}/A14$, BG0-BG1, BA0-BA1, A17-A0. Input parity should maintain at the rising edge of the clock and at the same time with command & address with \overline{CS} LOW.
\overline{ALERT}	Input/ Output	Alert: It has multiple functions, such as CRC error flag, or Command and Address Parity error flag. If there is error in the CRC, then \overline{ALERT} goes LOW for a period of time and goes back HIGH. If there is error in the Command Address Parity Check, then \overline{ALERT} goes LOW for a relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case it is not connected, \overline{ALERT} Pin must be connected to V_{DD} on the board.
SA0-SA2	Input	These signals are tied at the system to either V_{SS} or V_{DDSPD} to configure the serial SPD EEPROM address range.
SDA	Input/ Output	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. An external resistor may be connected from the SDA bus line to V_{DDSPD} to act as a pull-up on the system board.
SCL	Input	This signal is used to clock data into and out of the SPD EEPROM. An external resistor may be connected from the SCL bus tied to V_{DDSPD} to act as a pull-up on the system board.
\overline{EVENT}	Output	This signal indicates that a thermal event has been detected in the thermal sensing device. The system should guarantee the electrical level requirement is met for the \overline{EVENT} pin on TS/SPD part. No pull-up resistor is provided on DIMM.
NC	-	No Connect.
V_{DD}	Supply	Power Supply.
V_{SS}	Supply	Ground.
V_{PP}	Supply	DRAM Activating Power Supply.
V_{REFCA}	Supply	Reference voltage for address/command inputs.
V_{DDSPD}	Supply	Power supply for SPD EEPROM/Thermal Sensor.
V_{TT}	Supply	Termination voltage for address/command/control/clock nets.

DDR4 288-Pin Registered DIMM Pin List

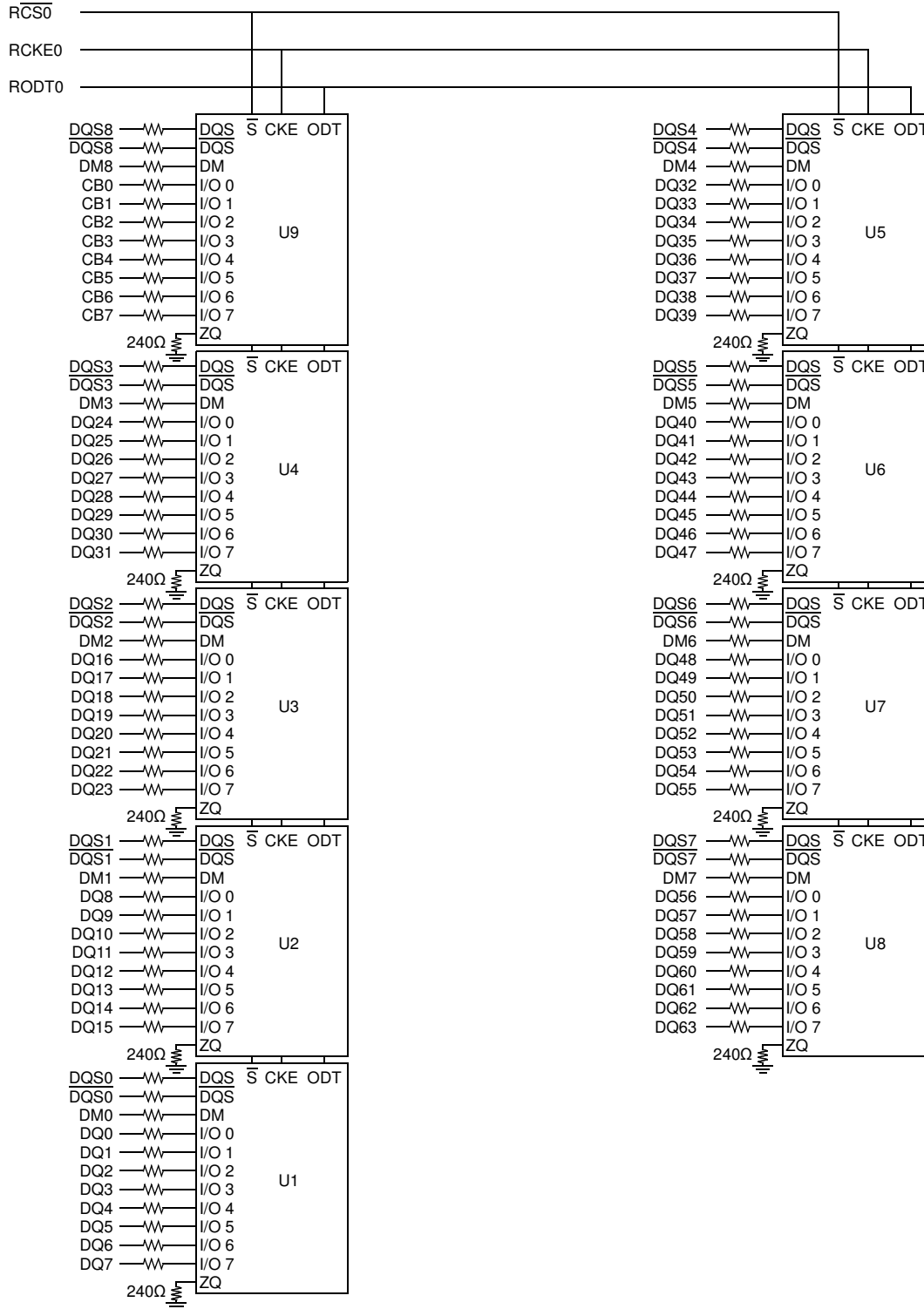
Front Side						Back Side					
Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	NC	49	CB0	97	DQ32	145	NC	193	V _{SS}	241	V _{SS}
2	V _{SS}	50	V _{SS}	98	V _{SS}	146	V _{REFCA}	194	CB1	242	DQ33
3	DQ4	51	DM3/DBI3/ TDQS17	99	DM4/DBI4/ TDQS13	147	V _{SS}	195	V _{SS}	243	V _{SS}
4	V _{SS}	52	NC/TDQS17	100	NC/TDQS13	148	DQ5	196	DQS8	244	DQS4
5	DQ0	53	V _{SS}	101	V _{SS}	149	V _{SS}	197	DQS8	245	DQS4
6	V _{SS}	54	CB6	102	DQ38	150	DQ1	198	V _{SS}	246	V _{SS}
7	DM0/DBI0/ TDQS9	55	V _{SS}	103	V _{SS}	151	V _{SS}	199	CB7	247	DQ39
8	NC/TDQS9	56	CB2	104	DQ34	152	DQS0	200	V _{SS}	248	V _{SS}
9	V _{SS}	57	V _{SS}	105	V _{SS}	153	DQS0	201	CB3	249	DQ35
10	DQ6	58	RESET	106	DQ44	154	V _{SS}	202	V _{SS}	250	V _{SS}
11	V _{SS}	59	V _{DD}	107	V _{SS}	155	DQ7	203	CKE1 (NC)	251	DQ45
12	DQ2	60	CKE0	108	DQ40	156	V _{SS}	204	V _{DD}	252	V _{SS}
13	V _{SS}	61	V _{DD}	109	V _{SS}	157	DQ3	205	RFU	253	DQ41
14	DQ12	62	ACT	110	DM5/DBI5/ TDQS14	158	V _{SS}	206	V _{DD}	254	V _{SS}
15	V _{SS}	63	BG0	111	NC/TDQS14	159	DQ13	207	BG1	255	DQS5
16	DQ8	64	V _{DD}	112	V _{SS}	160	V _{SS}	208	ALERT	256	DQS5
17	V _{SS}	65	A12/BC	113	DQ46	161	DQ9	209	V _{DD}	257	V _{SS}
18	DM1/DBI1/ TDQS10	66	A9	114	V _{SS}	162	V _{SS}	210	A11	258	DQ47
19	NC/TDQS10	67	V _{DD}	115	DQ42	163	DQS1	211	A7	259	V _{SS}
20	V _{SS}	68	A8	116	V _{SS}	164	DQS1	212	V _{DD}	260	DQ43
21	DQ14	69	A6	117	DQ52	165	V _{SS}	213	A5	261	V _{SS}
22	V _{SS}	70	V _{DD}	118	V _{SS}	166	DQ15	214	A4	262	DQ53
23	DQ10	71	A3	119	DQ48	167	V _{SS}	215	V _{DD}	263	V _{SS}
24	V _{SS}	72	A1	120	V _{SS}	168	DQ11	216	A2	264	DQ49
25	DQ20	73	V _{DD}	121	DM6/DBI6/ TDQS15	169	V _{SS}	217	V _{DD}	265	V _{SS}
26	V _{SS}	74	CK0	122	NC/TDQS15	170	DQ21	218	CK1	266	DQS6
27	DQ16	75	CK0	123	V _{SS}	171	V _{SS}	219	CK1	267	DQS6
28	V _{SS}	76	V _{DD}	124	DQ54	172	DQ17	220	V _{DD}	268	V _{SS}

DDR4 288-Pin Registered DIMM Pin List

Front Side						Back Side					
Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
29	DM2/DBI2/ TDQS11	77	V _{TT}	125	V _{SS}	173	V _{SS}	221	V _{TT}	269	DQ55
30	NC/TDQS11	78	EVENT	126	DQ50	174	DQS2	222	PARITY	270	V _{SS}
31	V _{SS}	79	A0	127	V _{SS}	175	DQS2	223	V _{DD}	271	DQ51
32	DQ22	80	V _{DD}	128	DQ60	176	V _{SS}	224	BA1	272	V _{SS}
33	V _{SS}	81	BA0	129	V _{SS}	177	DQ23	225	A10/AP	273	DQ61
34	DQ18	82	RAS/A16	130	DQ56	178	V _{SS}	226	V _{DD}	274	V _{SS}
35	V _{SS}	83	V _{DD}	131	V _{SS}	179	DQ19	227	RFU	275	DQ57
36	DQ28	84	CS0	132	DM7/DBI7/ TDQS16	180	V _{SS}	228	WE/A14	276	V _{SS}
37	V _{SS}	85	V _{DD}	133	NC/TDQS16	181	DQ29	229	V _{DD}	277	DQS7
38	DQ24	86	CAS/A15	134	V _{SS}	182	V _{SS}	230	NC	278	DQS7
39	V _{SS}	87	ODT0	135	DQ62	183	DQ25	231	V _{DD}	279	V _{SS}
40	DM3/DBI3/ TDQS12	88	V _{DD}	136	V _{SS}	184	V _{SS}	232	A13	280	DQ63
41	NC/TDQS12	89	CS1 (NC)	137	DQ58	185	DQS3	233	V _{DD}	281	V _{SS}
42	V _{SS}	90	V _{DD}	138	V _{SS}	186	DQS3	234	A17	282	DQ59
43	DQ30	91	ODT1 (NC)	139	SA0	187	V _{SS}	235	NC	283	V _{SS}
44	V _{SS}	92	V _{DD}	140	SA1	188	DQ31	236	V _{DD}	284	V _{DDSPD}
45	DQ26	93	CS2 (NC)	141	SCL	189	V _{SS}	237	CS3 (NC)	285	SDA
46	V _{SS}	94	V _{SS}	142	V _{PP}	190	DQ27	238	SA2	286	V _{PP}
47	CB4	95	DQ36	143	V _{PP}	191	V _{SS}	239	V _{SS}	287	V _{PP}
48	V _{SS}	96	V _{SS}	144	RFU	192	CB5	240	DQ37	288	V _{PP}

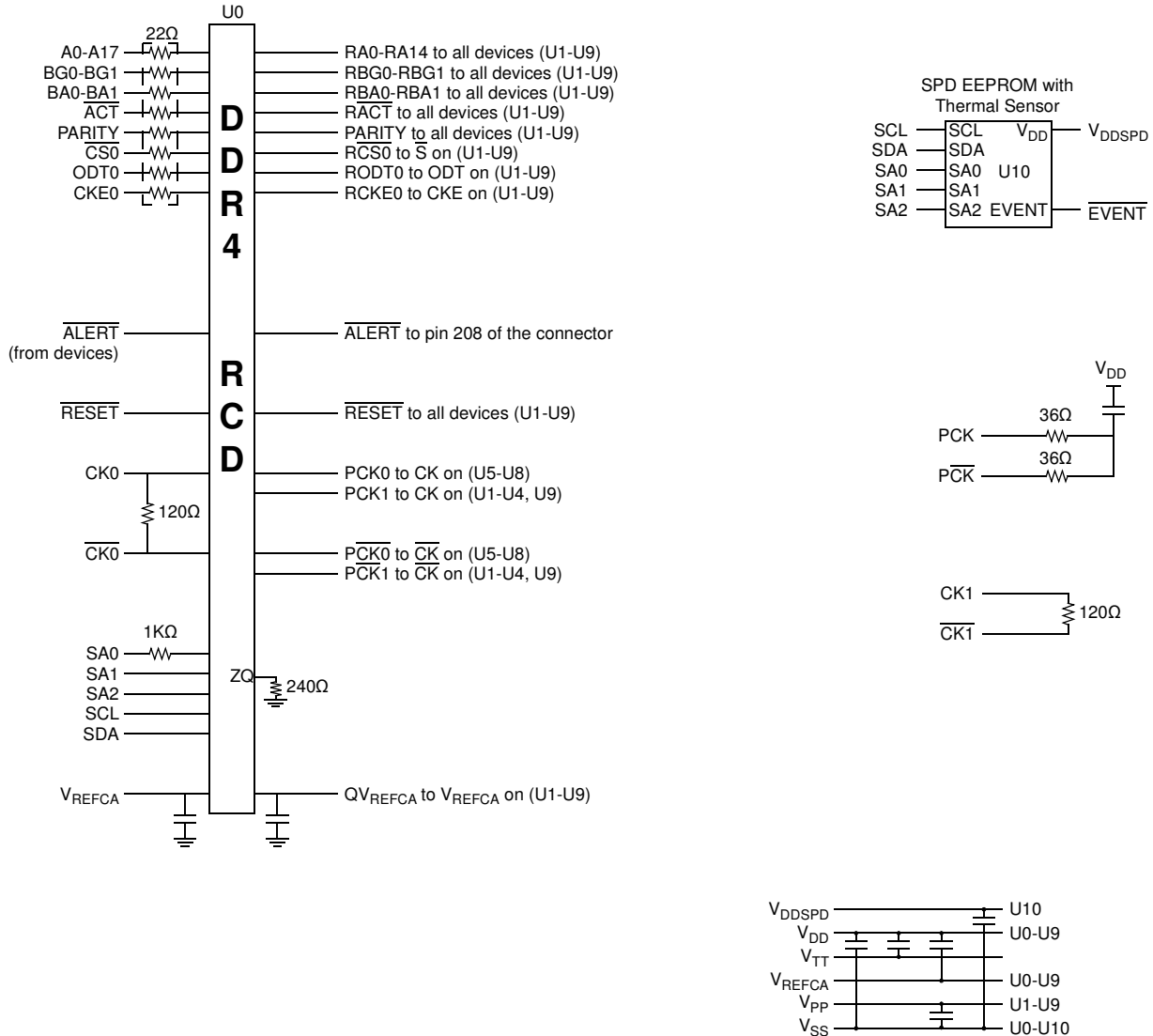


Block Diagram



Note: Unless otherwise noted, data resistor values are 15Ω ± 5%.

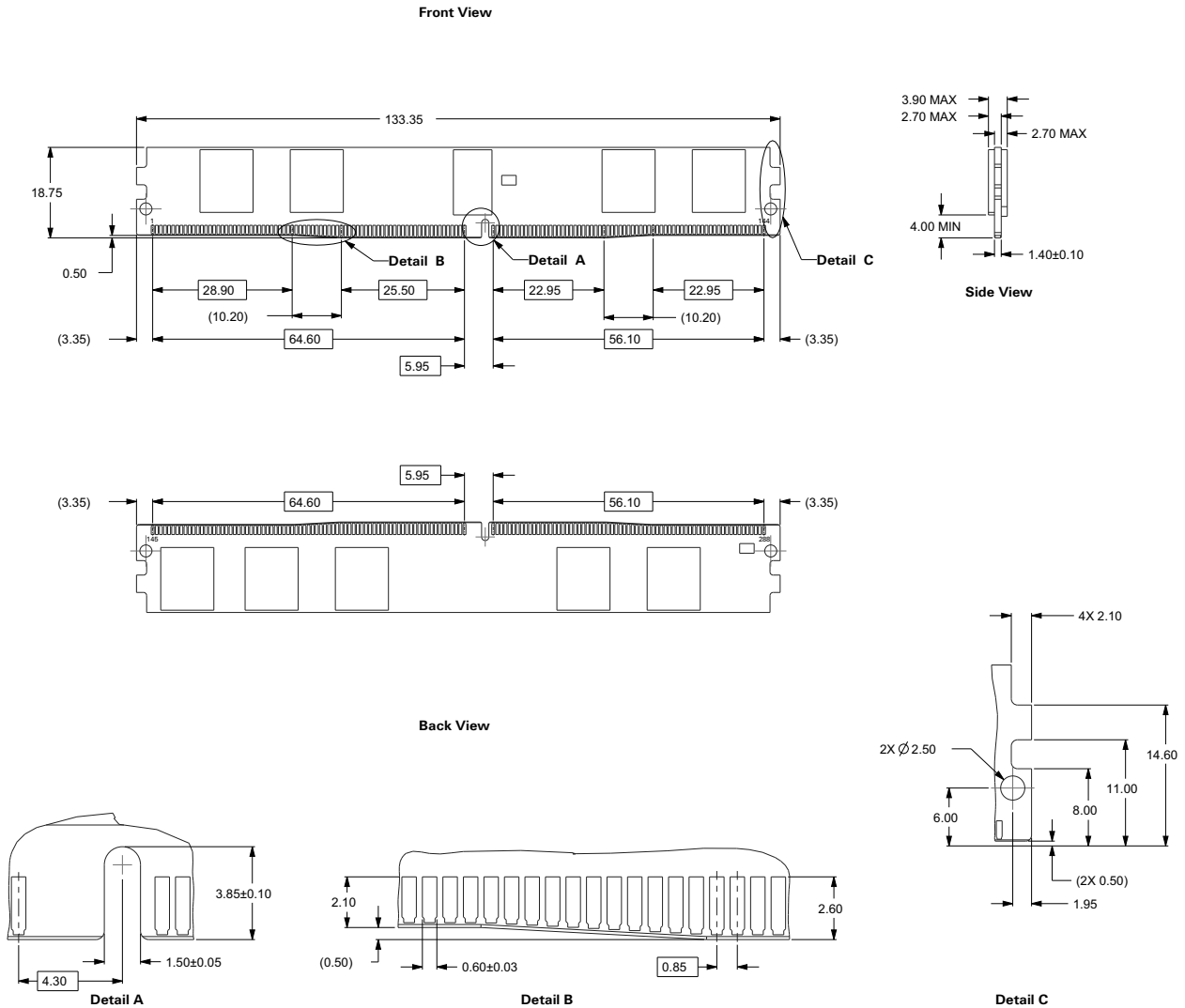
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Block Diagram (Continued)

Notes:

- Each address, command and control signal output line from the register is terminated through a 39Ω series resistor to V_{TT}.
- Data bits may be swapped within a device. However, DQ/DQS/DM relationship must be maintained as shown on page 9.

Physical Dimensions

288-Pin Registered DIMM Module



(All dimensions are in millimeters with $\pm 0.15\text{mm}$ tolerance unless specified otherwise.)

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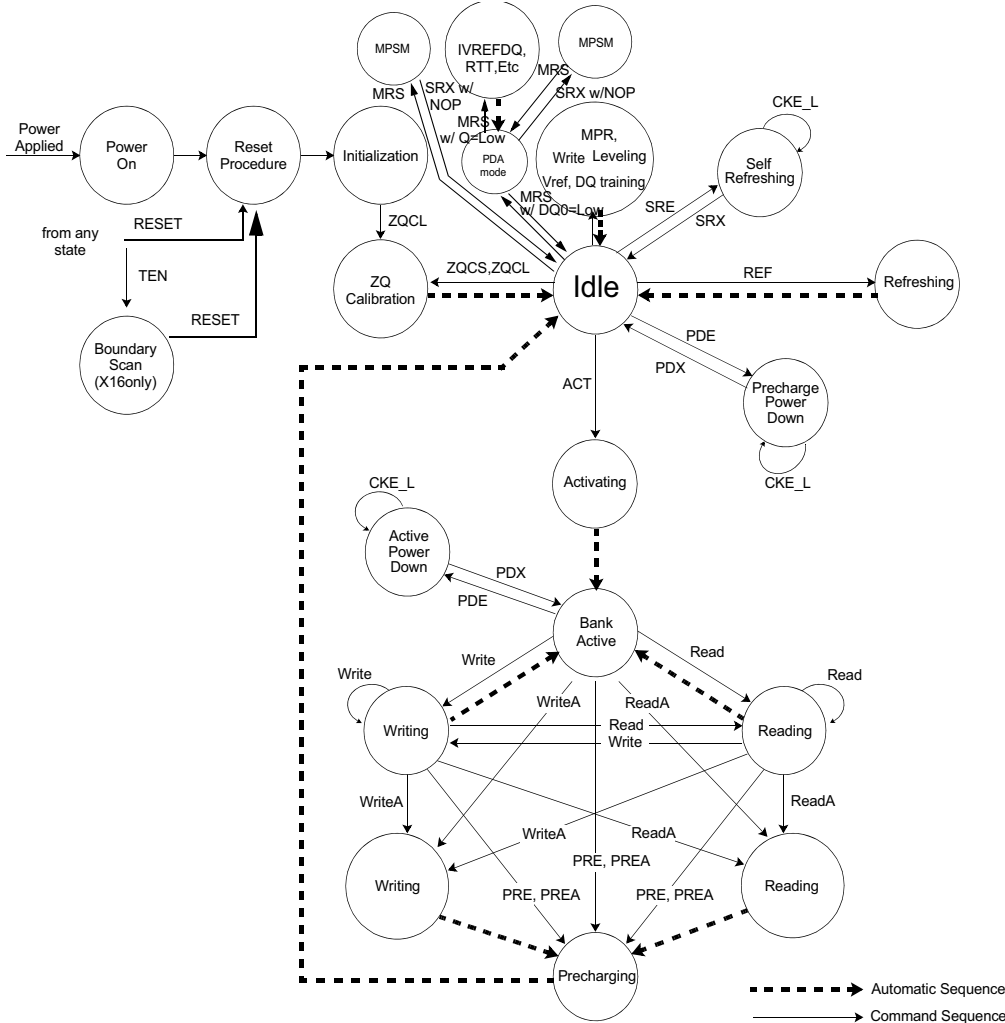
Control Words Programming

DDR4 registered modules (RDIMM) use a JEDEC standard registering clock driver device (RCD). This device features a set of control words that allows the device to be optimized for different RDIMM and motherboard designs. The recommended control word settings for each RDIMM design are programmed in the SPD from bytes 137-138. The control word values from the SPD must be programmed into the registering clock driver to ensure proper operation. This control word programming should be performed prior to the Mode Register programming.

The address & control parity must be generated correctly during the control word programming, otherwise the programming values will be ignored and the registering clock driver will maintain all zero default values. The $\overline{\text{ALERT}}$ signal from the RDIMM should be monitored during control word programming to ensure that the programming is successful.



State Diagram



Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Activate	Read	RD, RDS4, RDS8	PDE	Enter Power-Down
PRE	Precharge	Read A	RDA, RDAS4, RDAS8	PDX	Enter Power-Down
PREA	Precharge All	Write	WR, WRS4, WRS8 with/without CRC	SRE	Self-Refresh Entry
MRS	Mode Register Set	Write A	WRA, WRAS4, WRAS8 with/without CRC	SRX	Self-Refresh Exit
REF	Refresh, Fine Granularity Refresh	RESET	Start RESET Procedure	MPR	Multi Purpose Register
TEN	Boundary Scan Mode Enable				

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Mode Registers

MR0

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG, BA1-BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	RFU	0 = must be programmed to 0 during MRS
A11-A9	WR and RTP ^{2, 3}	Write Recovery and Read to Precharge for auto-precharge (See Write Recovery and Read to Precharge (cycles) table)
A8	DLL Reset	0 = No 1 = Yes
A7	TM	0 = Normal 1 = Test
A6-A4, A2	$\overline{\text{CAS}}$ Latency ⁴	(See $\overline{\text{CAS}}$ Latency table)
A3	Read Burst Type	0 = Sequential 1 = Interleave
A1-A0	Burst Length	00 = 8 (Fixed) 01 = BC4 or 8 (on the fly) 10 = BC4 (Fixed) 11 = Reserved

Notes:

- Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1-BA0 = 111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.
- WR_{min} (write recovery for auto-precharge) in clock cycles is calculated by dividing t_{WR} (in ns) by t_{CK} (in ns) and rounding up to the next integer: WR_{min} [cycles] = Roundup (t_{WR} [ns] / t_{CK} [ns]). The WR value in the mode register must be programmed to be equal or larger than WR_{min}. The programmed WR value is used with t_{RP} to determine t_{DAL}.
- The table shows the encodings for Write Recovery and internal Read command to Precharge command delay. For actual Write recovery timing, please refer to AC timing table.
- The table only shows the encodings for a given $\overline{\text{CAS}}$ Latency. For actual supported $\overline{\text{CAS}}$ Latencies, please refer to the Speed Bin tables.



Write Recovery and Read to Precharge (Cycles)

A11	A10	A9	WR	RTP	WR_CRC_DM
0	0	0	10	5	TBD
0	0	1	12	6	TBD
0	1	0	14	7	TBD
0	1	1	16	8	TBD
1	0	0	18	9	TBD
1	0	1	20	10	TBD
1	1	0	24	12	TBD
1	1	1	Reserved	Reserved	Reserved

CAS Latency

A11	A10	A9	WR	CAS Latency
0	0	0	0	9
0	0	0	1	10
0	0	1	0	11
0	0	1	1	12
0	1	0	0	13
0	1	0	1	14
0	1	1	0	15
0	1	1	1	16
1	0	0	0	18
1	0	0	1	20
1	0	1	0	22
1	0	1	1	24
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

MR1

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG, BA1-BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Qoff ²	0 = Output buffer enabled 1 = Output buffer disabled
A11	TDQS enable	0 = Disable 1 = Enable
A10-A8	RTT_NOM	(See RTT_NOM table)
A7	Write Leveling Enable	0 = Disable 1 = Enable
A6-A5	RFU	0 = must be programmed to 0 during MRS
A4-A3	Additive Latency	00 = 0 (AL disabled) 10 = CL - 2 01 = CL - 1 11 = Reserved
A2-A1	Output Driver Impedance Control	(See Output Driver Impedance Control table)
A0	DLL Enable	0 = Disable ³ 1 = Enable

Notes:

1. Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1-BA0 = 111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.
2. Outputs disabled - DQs, DQSs, \overline{DQSs} .
3. States reversed to "0 as Disable" with respect to DDR4.



RTT_NOM

A11	A10	A9	RTT_NOM
0	0	0	RTT_NOM Disable
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

Output Driver Impedance Control

A2	A1	Output Driver Impedance Control
0	0	RZQ/7
0	1	RZQ/5
1	0	Reserved
1	1	Reserved



MR2

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG, BA1-BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Write CRC	0 = Disable 1 = Enable
A11	RFU	0 = must be programmed to 0 during MRS
A10-A9	RTT_WR	(See RTT_WR table)
A8	RFU	0 = must be programmed to 0 during MRS
A7-A6	Low Power Array Self-Refresh (LP ASR)	00 = Manual Mode (Normal Operating Temperature Range) 01 = Manual Mode (Reduced Operating Temperature Range) 10 = Manual Mode (Extended Operating Temperature Range) 11 = ASR Mode (Auto Self-Refresh)
A5-A3	CAS Write Latency (CWL)	(See CAS Write Latency table)
A2-A0	RFU	0 = must be programmed to 0 during MRS

Notes:

1. Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1-BA0 = 111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.



RTT_WR

A10	A9	RTT_WR
0	0	Dynamic ODT off
0	1	RZQ/2
1	0	RZQ/1
1	1	Hi-Z

CWL (CAS Write Latency)

A5	A4	A3	CWL	Speed Bin (in MT/s)
0	0	0	9	1600
0	0	1	10	1866
0	1	0	11	2133, 1600
0	1	1	12	2400, 1866
1	0	0	14	2133
1	0	1	16	2400
1	1	0	18	
1	1	1	Reserved	

MR3

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG, BA1-BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12-A11	MPR Read Format	00 = Serial 10 = Staggered 01 = Parallel 11 = Reserved Temperature
A10-A9	Write CMD Latency when CRC and DM are enabled	(See Write Command Latency when CRC and DM are both Enabled table)
A8-A6	Fine Granularity Refresh Mode	(See Fine Granularity Refresh Mode table)
A5	Temperature Sensor Readout	0 = Disabled 1 = Enabled
A4	Per DRAM Addressability	0 = Disable 1 = Enable
A3	Geardown Mode	0 = 1/2 Rate 1 = 1/4 Rate
A2	MPR Operation	0 = Normal 1 = Dataflow from/to MPR
A1-A0	MPR Page Selection	00 = Serial 10 = Staggered 01 = Parallel 11 = Reserved Temperature (See MPR Data Format section)

Notes:

1. Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1-BA0 = 111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.



Fine Granularity Refresh Mode

A8	A7	A6	Fine Granularity Refresh
0	0	0	Normal (Fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Enable on the fly 2x
1	1	0	Enable on the fly 4x
1	1	1	Reserved

Write Command Latency when CRC and DM are both Enabled

A10	A9	CRC + DM Write Command Latency	Speed Bin (in MT/s)
0	0	4 nCK	1600
0	0	5 nCK	1866, 2133, 2400
0	1	6 nCK	TBD
0	1	RFU	RFU

MPR Data Format

MPR page 0 (Training Pattern)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note
BA1-BA0	00 = MPR0	0	1	0	1	0	1	0	1	Read/Write (default value)
	01 = MPR1	0	0	1	1	0	0	1	1	
	10 = MPR2	0	0	0	0	1	1	1	1	
	11 = MPR3	0	0	0	0	0	0	0	0	

MPR page 1 (C/A Parity Error Log)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note
BA1-BA0	00 = MPR0	A[7]	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]	Read-Only
	01 = MPR1	CAS/ A15	$\overline{WE}/A14$	A[13]	A[12]	A[11]	A[10]	A[9]	A[8]	
	10 = MPR2	PAR	\overline{ACT}	BG[1]	BG[0]	BA[1]	BA[0]	A[17]	RAS/ A16	
	11 = MPR3	CRC Error Status	C/A Parity Error Status	C/A Parity Latency ⁴			C[2]	C[1]	C[0]	
		MR5. A[2]	MR5. A[1]	MR5. A[0]						

Notes:

1. MPR used for C/A parity error log readout is enabled by setting A[2] in MR3.
2. For higher density of DRAM, where A[17] is not used, MPR2[1] should be treated as don't care.
3. If a device is used in monolithic application, where C[2:0] are not used, then MPR3[2:0] should be treated as don't care.
4. MPR3 bit 0~2 (C/A parity latency) reflects the latest programmed C/A parity latency values.

MPR page 2 (MRS Readout)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note	
BA1-BA0	00 = MPR0	RFU	RFU	RFU	Temperature Sensor Status (See table below)		CRC Write Enable	RTT_WR		Read-Only	
		-	-	-	-	-	MR2	MR2			
		-	-	-	-	-	A12	A10	A9		
	01 = MPR1	V _{REF} DQ Training Range	V _{REF} DQ Training Value						Gear- down Enable		
		MR6	MR6								
		A6	A5	A4	A3	A2	A1	A0	A3		
	10 = MPR2	CAS Latency			RFU		CAS Write Latency				
		MR0			-		MR2				
		A6	A5	A4	A2	-	A5	A4	A3		
	11 = MPR3	RTT_NOM			RTT_PARK			Driver Impedance			
		MR1			MR5			MR2			
		A10	A9	A6	A8	A7	A6	A2	A1		

MR bit for Temperature

MR3 bit A5=1: DRAM updates the temperature sensor status to MPR Page 2 (MPR0 bits A4:A3). Temperature data is guaranteed by the DRAM to be no more than 32ms old at the time of MPR Read of the Temperature Sensor Status bits.

MR3 bit A5=0: DRAM disables updates to the temperature sensor status in MPR Page 2(MPR0-bit A4:A3)

MPR0 bit A4	MPR0 bit A3	Refresh Rate Range
0	0	Sub 1X Refresh ($> t_{REFI}$)
0	1	1X Refresh Rate ($= t_{REFI}$)
1	0	2X Refresh Rate ($1/2 * t_{REFI}$)
1	1	Reserved

MPR page 3 (Vendor Use Only)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note
BA1-BA0	00 = MPR0	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Read-Only
	01 = MPR1	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	
	10 = MPR2	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	
	11 = MPR3	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	

Notes:

1. MPR page 3 is specifically assigned to DRAM. Actual encoding method is vendor specific.

MR4

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG, BA1-BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Write Preamble	0 = 1 nCK 1 = 2 nCK
A11	Read Preamble	0 = 1 nCK 1 = 2 nCK
A10	Read Preamble Training Mode	0 = Disable 1 = Enable
A9	Self-Refresh Abort	0 = Disable 1 = Enable
A8-A6	$\overline{\text{CS}}$ to CMD/ADDR Latency Mode (cycles)	000 = Disable 100 = 6 001 = 3 101 = 8 010 = 4 110 = Reserved 011 = 5 111 = Reserved (See $\overline{\text{CS}}$ to CMD/ADDR Latency Mode Setting table)
A5	RFU	0 = must be programmed to 0 during MRS
A4	Internal V _{REF} Monitor	0 = Disable 1 = Enable
A3	Temperature Controlled Refresh Mode	0 = Disable 1 = Enable
A2	Temperature Controlled Refresh Range	0 = Normal 1 = Extended
A1	Maximum Power Down Mode	0 = Disable 1 = Enable
A0	RFU	0 = must be programmed to 0 during MRS

Notes:

1. Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1-BA0 = 111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.



$\overline{\text{CS}}$ to CMD/ADDR Latency Mode Setting

A8	A7	A6	CAL
0	0	0	Disable
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	8
1	1	0	Reserved
1	1	1	Reserved

MR5

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG, BA1-BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Read DBI	0 = Disable 1 = Enable
A11	Write DBI	0 = Disable 1 = Enable
A10	Data Mask	0 = Disable 1 = Enable
A9	C/A Parity Persistent Error	0 = Disable 1 = Enable
A8-A6	RTT_PARK	(See RTT_PARK table)
A5	ODT Input Buffer during Power Down Mode	0 = ODT Input Buffer is activated 1 = ODT Input Buffer is deactivated
A4	C/A Parity Error Status	0 = Clear 1 = Error
A3	CRC Error Clear	0 = Clear 1 = Error
A2-A0	C/A Parity Latency Mode	(See C/A Parity Latency Mode table)

Notes:

- Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1-BA0 = 111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.
- When RTT_NOM Disable is set in MR1, A5 of MR5 will be ignored.



RTT_PARK

A8	A7	A6	RTT_PARK
0	0	0	RTT_PARK Disable
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

C/A Parity Latency Mode

A5	A4	A3	PL	Speed Bin (in MT/s)
0	0	0	Disable	
0	0	1	4	1600, 1866, 2133
0	1	0	5	2400
0	1	1	6	RFU
1	0	0	8	RFU
1	0	1	Reserved	
1	1	0	Reserved	
1	1	1	Reserved	

Notes:

1. Parity latency must be programmed according to the timing parameters in the speed grade table.



MR6

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG, BA1-BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12-A10	t _{CCD_L}	(See t _{CCD_L} table)
A9-A8	RFU	0 = must be programmed to 0 during MRS
A7	V _{REFDQ} Training Enable	0 = Disable (Normal Operation Mode) 1 = Enable (Training Mode)
A6	V _{REFDQ} Training Range	(See V _{REFDQ} Training: Range table)
A5-A0	V _{REFDQ} Training Value	(See V _{REFDQ} Training: Values table)

Notes:

- Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1-BA0 = 111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

t_{CCD_L}

A12	A11	A10	t _{CCD_L} min (nCK) ¹	t _{DLLK} min (nCK) ¹	Note
0	0	0	4	597	≤ 1333Mbps
0	0	1	5		≤ 1866Mbps (1600/1866Mbps)
0	1	0	6	768	≤ 2400Mbps (2133/2400Mbps)
0	1	1	7	1024	≤ TBD
1	0	0	8		≤ TBD
1	0	1	Reserved		
1	1	0	Reserved		
1	1	1	Reserved		

Notes:

- t_{CCD_L}/t_{DLLK} should be programmed according to the value defined in AC parameter table per operating frequency.

V_{REFDQ} Training: Range

A6	V _{REFDQ} Range
0	Range 1
1	Range 1

V_{REFDQ} Training: Values

A5-A0	Range 1	Range 2		A5-A0	Range 1	Range 2
00 0000	60.00%	45.00%		01 1010	76.90%	61.90%
00 0001	60.65%	45.65%		01 1011	77.55%	62.55%
00 0010	61.30%	46.30%		01 1100	78.20%	63.20%
00 0011	61.95%	46.95%		01 1101	78.85%	63.85%
00 0100	62.60%	47.60%		01 1110	79.50%	64.50%
00 0101	63.25%	48.25%		01 1111	80.15%	65.15%
00 0110	63.90%	48.90%		10 0000	80.80%	65.80%
00 0111	64.55%	49.55%		10 0001	81.45%	66.45%
00 1000	65.20%	50.20%		10 0010	82.10%	67.10%
00 1001	65.85%	50.85%		10 0011	82.75%	67.75%
00 1010	66.50%	51.50%		10 0100	83.40%	68.40%
00 1011	67.15%	52.15%		10 0101	84.05%	69.05%
00 1100	67.80%	52.80%		10 0110	84.70%	69.70%
00 1101	68.45%	53.45%		10 0111	85.35%	70.35%
00 1110	69.10%	54.10%		10 1000	86.00%	71.00%
00 1111	69.75%	54.75%		10 1001	86.65%	71.65%
01 0000	70.40%	55.40%		10 1010	87.30%	72.30%
01 0001	71.05%	56.05%		10 1011	87.95%	72.95%
01 0010	71.70%	56.70%		10 1100	88.60%	73.60%
01 0011	72.35%	57.35%		10 1101	89.25%	74.25%
01 0100	73.00%	58.00%		10 1110	89.90%	74.90%
01 0101	73.65%	58.65%		10 1111	90.55%	75.55%
01 0110	74.30%	59.30%		11 0000	91.20%	76.20%
01 0111	74.95%	59.95%		11 0001	91.85%	76.85%
01 1000	75.60%	60.60%		11 0010	92.50%	77.50%
01 1001	76.25%	61.25%		11 0011 to 11 1111	Reserved	Reserved

Truth Tables

Command Truth Table

a. Notes 1-4 apply to the entire Command Truth Table.

b. Note 5 applies to all Read/Write command.

 [BG= Bank Group Address, BA= Bank Address, RA= Row Address, CA = Column Address, \overline{BC} = Burst chop, X = Don't care, V = Valid]

Command Truth Table

Function	Abbreviation	CKE		\overline{CS}	\overline{ACT}	$\overline{RAS}/A16$	$\overline{CAS}/A15$	$\overline{WE}/A14$	BG0-BG1	BA0-BA1	C2-C0	A12/ \overline{BC}	A17, A13, A11	A10/AP	A0-A9	Notes
		Previous Cycle	Current Cycle													
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V	OP Code			12	
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V		
Self-Refresh Entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	7, 9
Self-Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	7, 8, 9, 10
				L	H	H	H	H	H	V	V	V	V	V	V	
Single Bank Pre-charge	PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	L	V	
Precharge All Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	V	H	V	
RFU	RFU	H	H	L	H	L	H	H	RFU							
Bank Activate	ACT	H	H	L	L	Row Address (RA)			BG	BA	V	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA	
Write with Auto-Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA	
Write with Auto-Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA	
Write with Auto-Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA	
Read with Auto-Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	H	CA	
Read with Auto-Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA	

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Command Truth Table

Function	Abbreviation	CKE		\overline{CS}	\overline{ACT}	$\overline{RAS}/A16$	$\overline{CAS}/A15$	$\overline{WE}/A14$	BG0-BG1	BA0-BA1	C2-C0	A12/ \overline{BC}	A17, A13, A11	A10/AP	A0-A9	Notes
		Previous Cycle	Current Cycle													
Read with Auto-Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA	
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	
Power-Down Entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	6
Power-Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	6
ZQ Calibration Long	ZQCL	H	H	L	H	H	H	L	V	V	V	V	V	H	V	
ZQ Calibration Short	ZQCS	H	H	L	H	H	H	L	V	V	V	V	V	L	V	

Notes:

- All DDR4 SDRAM commands are defined by states of \overline{CS} , \overline{ACT} , $\overline{RAS}/A16$, $\overline{CAS}/A15$, $\overline{WE}/A14$ and CKE at the rising edge of the clock. The MSB of BG, BA, RA and CA are device density and configuration dependant. When $\overline{ACT} = H$; pins $\overline{RAS}/A16$, $\overline{CAS}/A15$, and $\overline{WE}/A14$ are used as command pins RAS, CAS, and WE respectively. When $\overline{ACT} = L$; pins RAS/A16, CAS/A15, and WE/A14 are used as address pins A16, A15, and A14 respectively
- \overline{RESET} is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
- Bank Group addresses (BG) and Bank addresses (BA) determine which bank within a bank group to be operated upon. For MRS commands the BG and BA selects the specific Mode Register location.
- "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level".
- Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.
- The Power Down Mode does not perform any refresh operation.
- The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.
- Controller guarantees Self-Refresh exit to be synchronous.
- $V_{REF}(V_{REFCA})$ must be maintained during Self-Refresh operation. The first Write Leveling Activity may not occur earlier than TBD nCK after exit from Self-Refresh.
- The No Operation command should be used in cases when the DDR4 SDRAM is in Gear Down Mode and Max Power Saving Mode Exit
- Refer to the CKE Truth Table for more detail with CKE transition.
- During a MRS command A17 is Reserved for Future Use and is device density and configuration dependent.

CKE Truth Table

Current State ²	CKE		Command (N) ³ RAS, CAS, WE, CS	Action (N) ³	Notes
	Previous Cycle ¹ (N-1)	Current Cycle ¹ (N)			
Power-Down	L	L	X	Maintain Power-Down	14, 15
	L	H	DESELECT	Power-Down Exit	11, 14
Self-Refresh	L	L	X	Maintain Self-Refresh	15, 16
	L	H	DESELECT	Self-Refresh Exit	8, 12, 16
Bank(s) Activate	H	L	DESELECT	Active Power-Down Entry	11, 13, 14
Reading	H	L	DESELECT	Power-Down Entry	11, 13, 14, 17
Writing	H	L	DESELECT	Power-Down Entry	11, 13, 14, 17
Precharging	H	L	DESELECT	Power-Down Entry	11, 13, 14, 17
Refreshing	H	L	DESELECT	Precharge Power-Down Entry	11
All Banks Idle	H	L	DESELECT	Precharge Power-Down Entry	11, 13, 14, 18
	H	L	REFRESH	Self-Refresh	9, 13, 18
For more details with all signals, see Command Truth Table on page 30.					10

Notes:

1. CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
2. Current state is defined as the state of the DDR4 SDRAM immediately prior to clock edge N.
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here.
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.
6. During any CKE transition (registration of CKE H->L or CKE L->H), the CKE level must be maintained until 1nCK prior to t_{CKEmin} being satisfied (at which time CKE may transition again).
7. DESELECT and NOP are defined in the Command Truth Table.
8. On Self-Refresh Exit DESELECT commands must be issued on every clock edge occurring during the t_{XS} period. Read or ODT commands may be issued only after t_{XSDDL} is satisfied.
9. Self-Refresh mode can only be entered from the All Banks Idle state.
10. Must be a legal command as defined in the Command Truth Table.
11. Valid commands for Power-Down Entry and Exit are DESELECT only.
12. Valid commands for Self-Refresh Exit are DESELECT only except for Gear Down mode and Max Power Saving exit. NOP is allowed for these 2 modes.
13. Self-Refresh can not be entered during Read or Write operations.
14. The Power-Down does not perform any refresh operations.
15. "X" means "don't care" (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.
16. V_{PP} and V_{REFCA} must be maintained during Self-Refresh operation. The first Write operation or first Write Leveling Activity may not occur earlier than TBD nCK after exit from Self-Refresh.
17. If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.
18. 'Idle state' is defined as all banks are closed (t_{RP}, t_{DAL}, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (t_{MRD}, t_{MOD}, t_{RFC}, t_{ZQinit}, t_{ZQoper}, t_{ZQCS}, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (t_{XS}, t_{XP}, etc.)

Absolute Maximum Ratings

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Voltage on V_{DD} relative to V_{SS}	-0.3 ~ 1.5	V	1, 3
V_{PP}	Voltage on V_{PP} relative to V_{SS}	-0.3 ~ 1.5	V	1, 4
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.3 ~ 1.5	V	1
V_{DDSPD}	Voltage on V_{DDSPD} relative to V_{SS}	-0.5 ~ 4.3	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1, 2

Notes:

- Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Storage Temperature is the case surface temperature on the center/top side of the DRAM.
- V_{REF} must be not greater than $0.6 * V_{DD}$. When V_{DD} is less than 500 mV, V_{REF} may be less than or equal to 300 mV.
- V_{PP} must be equal or greater than V_{DD} at all times.

Recommended DC Operating Conditions

Symbol	Parameter	Rating			Units	Notes
		Min	Typical	Max		
V_{DD}	Supply Voltage	1.14	1.2	1.26	V	1, 2
V_{PP}	Supply Voltage for Output	2.375	2.5	2.75	V	1
V_{DDSPD}	SPD Supply Voltage	2.25	2.5	2.75	V	
V_{TT}	Termination Voltage	0.57	0.6	0.63	V	2
V_{SS}	Ground	0	0	0	V	

Notes:

- DC bandwidth is limited to 20MHz.
- $V_{TT} = V_{DD}/2$

Operating Temperature Range

Symbol	Parameter	Range	Units	Notes
T _{OPER}	Normal Operating Temperature Range (Case)	0 to 85	°C	1, 2
	Extended Operating Temperature Range (Case)	85 to 95	°C	1, 3

Notes:

- Operating Temperature T_{OPER} is the case surface temperature on the center/top side of the DRAM.
- The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 °C and 85 °C under all operating conditions.
- Some applications require operation in the Extended Temperature Range between 85 °C and 95 °C. Full specifications are supported in this range, but the following additional conditions apply:
 - Refresh commands must be doubled in frequency, therefore reducing the Refresh interval t_{REFI} to 3.9µs. It is also possible to specify a component with 1X refresh (t_{REFI} to 7.8µs) in the Extended Temperature Range. Please refer to the SPD for option availability.
 - If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 1b and MR2 A7 = 0b). DDR4 SDRAMs support Auto Self-Refresh and Extended Temperature Range. Please refer to the DIMM SPD for t_{REFI} requirements in the Extended Temperature Range.

Temperature Sensor Characteristics

Symbol	Test Condition ²	Min	Typical	Max	Units
JEDEC B-Grade	+75 °C ≤ T _A ≤ +95 °C, Active Range	-	±0.5	±1	°C
	+40 °C ≤ T _A ≤ +125 °C, Monitor Range	-	±1	±2	°C
	-40 °C ≤ T _A ≤ +125 °C	-	±2	±3	°C
Resolution		-	0.25	-	°C
Conversion Time ¹	Worst Case Conversion Time	-	-	120	ms

Notes:

- Assuming 10-bit resolution. Conversion times may range from 62.5 ms for 9-bit to 500 ms for 12-bit accuracy.
- V_{DDSPDmin} ≤ V_{DDSPD} ≤ V_{DDSPDmax}

Refresh Parameters

Parameter	Symbol	4Gb	Units
Average periodic refresh interval	t _{REFI}	7.8	µs
		3.9	µs

Differential AC and DC Input Levels for CK- $\overline{\text{CK}}$

Symbol	Parameter	DDR4-2133		Units	Notes
		Min	Max		
V _{IHDIFF}	Differential input logic high	TBD	Note 3	V	1
V _{ILDIFF}	Differential input logic high	Note 3	TBD	V	1
V _{IHDIFF(AC)}	AC input logic high	2 * (V _{IH(AC)} - V _{REF})	Note 3	V	2
V _{ILDIFF(AC)}	AC input logic low	Note 3	2 * (V _{IL(AC)} - V _{REF})	V	2

Notes:

- Used to define a differential signal slew-rate.
- For CK/ $\overline{\text{CK}}$, use V_{IH}/V_{IL(AC)} of ADD/CMD and V_{REFCA}.
- These values are not defined, however the single-ended signals CK, $\overline{\text{CK}}$, need to be within the respective limits (V_{IH(DC)} max, V_{IL(DC)} min) for single-ended signals as well as the limitations for overshoot and undershoot.

Single-Ended Levels for CK- $\overline{\text{CK}}$

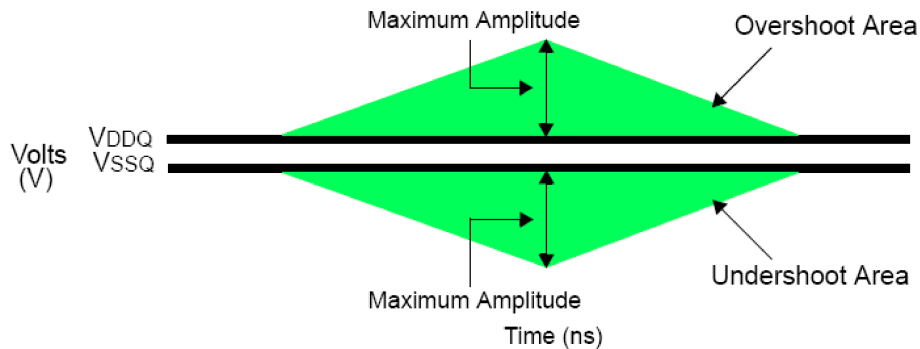
Symbol	Parameter	DDR4-2133		Units	Notes
		Min	Max		
V _{SEH}	Single-ended high-level for CK- $\overline{\text{CK}}$	TBD	Note 3	V	1, 2
V _{SEL}	Single-ended low-level for CK- $\overline{\text{CK}}$	Note 3	TBD	V	1, 2

Notes:

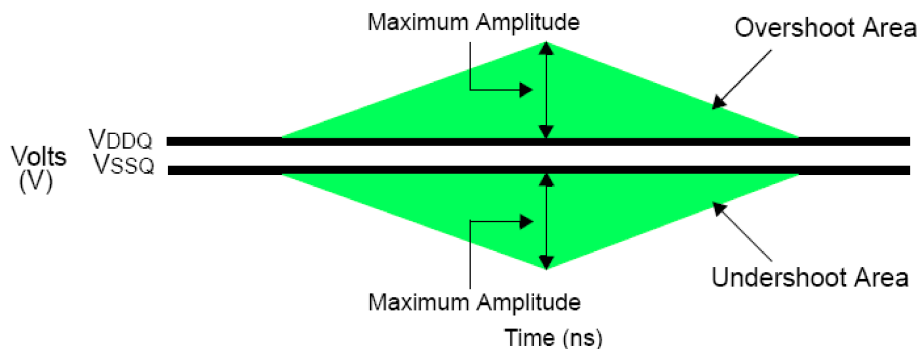
- For CK/ $\overline{\text{CK}}$, use V_{IH}/V_{IL(AC)} of ADD/CMD.
- V_{IH(AC)}/V_{IL(AC)} for ADD/CMD is based on V_{REFCA}.
- These values are not defined, however the single-ended signals CK, $\overline{\text{CK}}$, need to be within the respective limits (V_{IH(DC)} max, V_{IL(DC)} min) for single-ended signals as well as the limitations for overshoot and undershoot.

AC Overshoot/Undershoot Specification for Address and Control Pins

Parameter	DDR4-2133	Units
Maximum peak amplitude allowed for overshoot area.	0.3	V
Maximum peak amplitude allowed for undershoot area.	0.3	V
Maximum overshoot area above V_{DD} .	0.25	V-ns
Maximum undershoot area under V_{SS} .	0.25	V-ns
(A0-A13, A17, BG0-BG1, BA0-BA1, CS, RAS/A16, CAS/A15, WE/A14, CKE, ODT, C0-C2)		

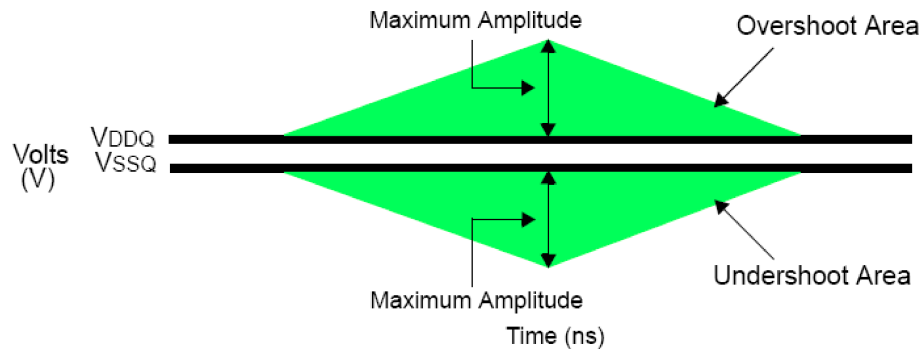

AC Overshoot/Undershoot Specification for Clock

Parameter	DDR4-2133	Units
Maximum peak amplitude allowed for overshoot area.	0.3	V
Maximum peak amplitude allowed for undershoot area.	0.3	V
Maximum overshoot area above V_{DD} .	0.10	V-ns
Maximum undershoot area under V_{SS} .	0.10	V-ns
(CK, \overline{CK})		



AC Overshoot/Undershoot Specification for Data, Strobe and Mask

Parameter	DDR4-2133	Units
Maximum peak amplitude allowed for overshoot area.	0.4	V
Maximum peak amplitude allowed for undershoot area.	0.32	V
Maximum overshoot area above V_{DD} .	0.2	V-ns
Maximum undershoot area under V_{SS} .	0.1	V-ns
(DQ, CB, DQS, DQS, DM/DBI)		


Cross Point Voltage for Differential Input Signals ($\overline{CK-CK}$)

Symbol	Parameter	DDR4-2133		Units	Notes
		Min	Max		
$V_{IX}(CK)$	Differential Input Cross Point Voltage relative to $V_{DD}/2$ for CK, \overline{CK}	-120	-120	mV	2
		TBD	TBD	mV	1
$V_{IX_DQS_ratio}$	DQS Differential input crosspoint voltage ratio	-	TBD	%	3, 4

Notes:

- Extended range for V_{IX} is only allowed for clock and if single-ended clock input signals CK and \overline{CK} are monotonic with a single-ended swing V_{SEL}/V_{SEH} of at least $V_{DD}/2 \pm$ TBD mV, and when the differential slew rate of $CK - \overline{CK}$ is larger than 3 V/ns.
- The relation between V_{IX} Min/Max and V_{SEL}/V_{SEH} should satisfy following.
 $(V_{DD}/2) + V_{IXmin} - V_{SEL} \geq 25mV$
 $V_{SEH} - ((V_{DD}/2) + V_{IXmax}) \geq 25mV$.
- Referenced to $V_{SWING}/2 = \text{average } 0.5(V_{DQS} + V_{\overline{DQS}})$ where the average is over TBD UI.
- Ratio of the V_{IX} pk voltage divided by V_{diff_DQS} :
 $V_{IX_DQS_ratio} = 100 * (V_{IX_DQS}/V_{diff_DQS} \text{ pk-pk})$ where $V_{diff_DQS} \text{ pk-pk} = 2 * |V_{DQS} - V_{\overline{DQS}}|$

Single-Ended AC & DC Output Levels

Symbol	Parameter	DDR4-2133	Units	Notes
V _{OH} (DC)	DC output high measurement level (for IV curve linearity)	1.1 * V _{DD}	V	
V _{OM} (DC)	DC output mid measurement level (for IV curve linearity)	0.8 * V _{DD}	V	
V _{OL} (DC)	DC output low measurement level (for IV curve linearity)	0.5 * V _{DD}	V	
V _{OH} (AC)	AC output high measurement level (for output SR)	(0.7 + 0.15) * V _{DD}	V	1
V _{OL} (AC)	AC output low measurement level (for output SR)	(0.7 - 0.15) * V _{DD}	V	1

Notes:

1. The swing of $\pm 0.15 * V_{DD}$ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7 Ω and an effective test load of 50 Ω to V_{TT} = V_{DD}.

Differential AC & DC Output Levels

Symbol	Parameter	DDR4-2133	Units	Notes
		Min		
V _{OHdiff} (AC)	AC differential output high measurement level (for output SR)	0.3 * V _{DD}	V	1
V _{OLdiff} (AC)	AC differential output low measurement level (for output SR)	-0.3 * V _{DD}	V	1

Notes:

1. The swing of $\pm 0.3 * V_{DD}$ is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of RZQ/7 Ω and an effective test load of 50 Ω to V_{TT} = V_{DD} at each of the differential outputs.

Device Standard Speed Bins
DDR4-2133 Speed Bins

Speed Bin			DDR4-2133		Units	Notes	
CL - nRCD - nRP			15-15-15				
Parameter	Symbol		Min	Max			
Internal read command to first data	t_{AA}		13.5	18	ns	7	
Internal read command to first data with read DBI enabled	t_{AA_DBI}		TBD	TBD	ns		
ACT to internal read or write delay time	t_{RCD}		13.5	-	ns	7	
PRE command period	t_{RP}		13.5	-	ns	7	
ACT to ACT or REF command period	t_{RC}		46.5	-	ns	7	
ACT to PRE command period	t_{RAS}		33	$9 * t_{REFI}$	ns		
	Normal	Read DBI	$t_{CK(avg)}$				
CWL = 9	CL = 9	CL = 11	$t_{CK(avg)}$	1.5	1.6	ns	1, 2, 3, 5, 6, 8
	CL = 10	CL = 12		Reserved		ns	4
CWL = 9, 11	CL = 11	CL = 13	$t_{CK(avg)}$	Reserved		ns	4
	CL = 12	CL = 14		1.25	< 1.5	ns	1, 2, 3, 5
CWL = 10, 12	CL = 13	CL = 15	$t_{CK(avg)}$	1.071	< 1.25	ns	1, 2, 3, 5
	CL = 14	CL = 16		1.071	< 1.25	ns	1, 2, 3, 5
CWL = 11, 14	CL = 14	CL = TBD	$t_{CK(avg)}$	Reserved		ns	4
	CL = 15	CL = TBD		0.938	< 1.071	ns	1, 2, 3
	CL = 14	CL = TBD		0.938	< 1.071	ns	1, 2, 3
Supported CL Settings			9, 11, 12, 13, 14, 15, 16		n_{CK}		
Supported CL Settings with read DBI			TBD		n_{CK}		
Supported CWL Settings			9, 10, 11, 12, 14		n_{CK}		

Speed Bin Tables Notes

Absolute Specification

- $V_{DD} = 1.20V \pm 0.06 V$
- $V_{PP} = 2.5V +0.25/-0.125 V$
- The values defined with the above mentioned table are the case where DLL ON.
- DDR4-2133 Speed Bin Table is valid only when Geardown Mode is disabled.

1. The CL setting and CWL setting result in $t_{CK(avg)min}$ and $t_{CK(avg)max}$ requirements. When making a selection of $t_{CK(avg)}$, both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. $t_{CK(avg)min}$ limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard $t_{CK(avg)}$ value (1.5, 1.25, 1.071, 0.938 or 0.833 ns) when calculating $CL [nCK] = t_{AA} [ns] / t_{CK(avg)} [ns]$, rounding up to the next 'Supported CL', where $t_{AA} = 12.5ns$ and $t_{CK(avg)} = 1.3 ns$ should only be used for $CL = 10$ calculation.
3. $t_{CK(avg)max}$ limits: Calculate $t_{CK(avg)} = t_{AA}max / CL$ SELECTED and round the resulting $t_{CK(avg)}$ down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.938 ns or 0.833 ns). This result is $t_{CK(avg)max}$ corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
6. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
7. For devices supporting optional down binning to $CL = 9$, $CL = 11$ and $CL = 13$, $t_{AA}/t_{RCD}/t_{RPmin}$ must be 13.5ns or lower. SPD settings must be programmed to match. For example, DDR4-1600K devices supporting down binning to 1333MT/s should program 13.5ns in SPD bytes for t_{AAmin} (Byte 24), t_{RCDmin} (Byte 25), and t_{RPmin} (Byte 26). DDR4-2133P devices supporting down binning to 1333MT/s or DDR4-1600K or DDR4-1866M should program 13.5ns in SPD bytes for t_{AAmin} (Byte 24), t_{RCDmin} (Byte 25), and t_{RPmin} (Byte 26). t_{RCmin} (Byte 27, 29) also should be programmed accordingly. For example, 48.5ns ($t_{RASmin} + t_{RPmin} = 35ns + 13.5ns$) is set to supporting optional down binning $CL = 9$ and $CL = 11$.
8. DDR4 SDRAM supports $CL = 9$ as long as a system meets $t_{AA}(min)$.

Device Timing Parameters by Speed Bin

Parameter	Symbol	DDR4-2133		Units	Notes
		Min	Max		
Clock Timing					
Minimum Clock Cycle Time (DLL off mode)	$t_{CK(DLL_OFF)}$	8	-	t_{CK}	22
Average Clock Period	$t_{CK(avg)}$	TBD		ps	
Average HIGH Pulse Width	$t_{CH(avg)}$	0.48	0.52	$t_{CK(avg)}$	
Average LOW Pulse Width	$t_{CL(avg)}$	0.48	0.52	$t_{CK(avg)}$	
Absolute Clock Period	$t_{CK(abs)}$	$t_{CK(avg)min} + t_{JIT(per_tot)min}$	$t_{CK(avg)max} + t_{JIT(per_tot)max}$	ps	
Absolute Clock HIGH Pulse Width	$t_{CH(abs)}$	0.45	-	$t_{CK(avg)}$	23
Absolute Clock LOW Pulse Width	$t_{CL(abs)}$	0.45	-	$t_{CK(avg)}$	24
Clock Period Jitter - Total	$t_{JIT(per_tot)}$	-0.1	0.1	UI	23
Clock Period Jitter - Deterministic	$t_{JIT(per_dj)}$	TBD	TBD	UI	26
Clock Period Jitter during DLL Locking Period	$t_{JIT(per, lck)}$	TBD	TBD	UI	
Cycle to Cycle Period Jitter - Total	$t_{JIT(CC_total)}$	0.2		UI	25
Cycle to Cycle Period Jitter - Deterministic	$t_{JIT(CC_dj)}$	TBD		UI	26
Cycle to Cycle Period Jitter during DLL Locking Period	$t_{JIT(CC, lck)}$	TBD		UI	
Duty Cycle Jitter	$t_{JIT(duty)}$	TBD	TBD	UI	
Cumulative Error across 2 Cycles	$t_{ERR(2per)}$	TBD	TBD	UI	
Cumulative Error across 3 Cycles	$t_{ERR(3per)}$	TBD	TBD	UI	
Cumulative Error across 4 Cycles	$t_{ERR(4per)}$	TBD	TBD	UI	
Cumulative Error across 5 Cycles	$t_{ERR(5per)}$	TBD	TBD	UI	
Cumulative Error across 6 Cycles	$t_{ERR(6per)}$	TBD	TBD	UI	
Cumulative Error across 7 Cycles	$t_{ERR(7per)}$	TBD	TBD	UI	
Cumulative Error across 8 Cycles	$t_{ERR(8per)}$	TBD	TBD	UI	
Cumulative Error across 9 Cycles	$t_{ERR(9per)}$	TBD	TBD	UI	
Cumulative Error across 10 Cycles	$t_{ERR(10per)}$	TBD	TBD	UI	
Cumulative Error across 11 Cycles	$t_{ERR(11per)}$	TBD	TBD	UI	
Cumulative Error across 12 Cycles	$t_{ERR(12per)}$	TBD	TBD	UI	
Cumulative Error across n = 13-50 Cycles	$t_{ERR(nper)}$	TBD		UI	
Command and Address Timing					
\overline{CAS} to \overline{CAS} Command Delay for Same Bank Group	t_{CCD_L}	6	-	nCK	
\overline{CAS} to \overline{CAS} Command Delay for Different Bank Group	t_{CCD_S}	4	-	nCK	

Device Timing Parameters by Speed Bin (Continued)

Parameter	Symbol	DDR4-2133		Units	Notes
		Min	Max		
Command and Address Timing					
ACTIVATE to ACTIVATE Command Delay to Same Bank Group for 2 KB Page Size	$t_{RRD_L(2K)}$	Max(4nCK, 6.4ns)	-	nCK	14, 16, 18
ACTIVATE to ACTIVATE Command Delay to Same Bank Group for 1 KB Page Size	$t_{RRD_L(1K)}$	Max(4nCK, 5.3ns)	-	nCK	
ACTIVATE to ACTIVATE Command Delay to Same Bank Group for 1/2 KB Page Size	$t_{RRD_L(1/2K)}$	Max(4nCK, 5.3ns)	-	nCK	
ACTIVATE to ACTIVATE Command Delay to Different Bank Group for 2 KB Page Size	$t_{RRD_S(2K)}$	Max(4nCK, 5.3ns)	-	nCK	
ACTIVATE to ACTIVATE Command Delay to Different Bank Group for 1 KB Page Size	$t_{RRD_S(1K)}$	Max(4nCK, 3.7ns)	-	nCK	
ACTIVATE to ACTIVATE Command Delay to Different Bank Group for 1/2 KB Page Size	$t_{RRD_S(1/2K)}$	Max(4nCK, 3.7ns)	-	nCK	
Four Activate Window for 2 KB Page Size	$t_{FAW(2K)}$	35	-	ns	
Four Activate Window for 1 KB Page Size	$t_{FAW(1K)}$	25	-	ns	
Four Activate Window for 1/2 KB Page Size	$t_{FAW(1/2K)}$	20	-	ns	
Delay from Start of Internal Write Transaction to Internal READ Command for Same Bank Group	t_{WTR_S}	Max(2nCK, 2.5ns)	-		1, 2
Delay from Start of Internal Write Transaction to Internal READ Command for Different Bank Group	t_{WTR_L}	Max(4nCK, 7.5ns)	-		1
Internal READ Command to PRECHARGE Command Delay	t_{RTP}	Max(4nCK, 7.5ns)	-		
WRITE Recovery Time	t_{WR}	15	-	ns	1
WRITE Recovery Time when Both CRC and DM are Enabled	$t_{WR_CRC_DM}$	$t_{WR} + \text{Max}(4nCK, 3.75ns)$	-	ns	1, 9
Delay from Start of Internal Write Transaction to Internal READ Command for Same Bank Group when Both CRC and DM are Enabled	$t_{WTR_S_CRC_DM}$	$t_{WTR_S} + \text{Max}(4nCK, 3.75ns)$	-	ns	2, 10
Delay from Start of Internal Write Transaction to Internal READ Command for Different Bank Group when Both CRC and DM are Enabled	$t_{WTR_L_CRC_DM}$	$t_{WTR_L} + \text{Max}(4nCK, 3.75ns)$	-	ns	3, 11
DLL locking time	t_{DLLK}	TBD	-	nCK	
Mode Register Set Command Cycle Time	t_{MRD}	8	-	nCK	
Mode Register Set Command Update Delay	t_{MOD}	Max(24nCK, 15ns)	-		
Multi-Purpose Register Recovery Time	t_{MPRR}	1	-	nCK	29
Multi-Purpose Register Write Recovery Time	t_{WR_MPR}	t_{MODmin}	-		

Device Timing Parameters by Speed Bin (Continued)

Parameter	Symbol	DDR4-2133		Units	Notes
		Min	Max		
CS to Command Address Latency					
$\overline{\text{CS}}$ to Command Address Latency	t_{CAL}	4	-	nCK	
DRAM Data Timing					
DQS, $\overline{\text{DQS}}$ to DQ Skew, Per Group, Per Access	t_{DQSQ}	-	TBD	UI	13, 18
DQS, $\overline{\text{DQS}}$ to DQ Skew Deterministic, Per Group, Per Access	t_{DQSQ}	-	TBD	UI	14, 16, 18
DQ Output Hold Time from DQS, $\overline{\text{DQS}}$	t_{QH}	TBD	-	UI	13, 17, 18
DQ Output Hold Time Deterministic from DQS, $\overline{\text{DQS}}$	t_{QH}	TBD	-	UI	14, 16, 18
DQS, $\overline{\text{DQS}}$ to DQ Skew Total, Per Group, Per Access; DBI Enabled	t_{DQSQ}	-	TBD	UI	13, 19
DQ Output Hold Time Total from DQS, $\overline{\text{DQS}}$; DBI Enabled	t_{QH}	TBD	-	UI	13, 19
$\overline{\text{DQ}}$ to DQ Offset, Per Group, Per Access Referenced to DQS, $\overline{\text{DQS}}$	t_{DQSQ}	TBD	TBD	UI	15, 16
Data Strobe Timing					
DQS, $\overline{\text{DQS}}$ Differential Output High Time	t_{QSH}	TBD	TBD	UI	21
DQS, $\overline{\text{DQS}}$ Differential Output Low Time	t_{QSL}	TBD	TBD	UI	20
MPSM Timing					
Command Path Disable Delay upon MPSM Entry	t_{MPED}	$t_{\text{MODmin}} + t_{\text{CPDEDmin}}$	-		
Valid Clock Requirement after MPSM Entry	t_{CKMPE}	$t_{\text{MODmin}} + t_{\text{CPDEDmin}}$	-		
Valid Clock Requirement before MPSM Exit	t_{CKMPX}	t_{CKSRXmin}	-		
Exit MPSM to Commands not Requiring a Locked DLL	t_{XMP}	TBD	-		
Exit MPSM to Commands Requiring a Locked DLL	t_{XMPDLL}	$t_{\text{XMPmin}} + t_{\text{XSDLLmin}}$	-		
$\overline{\text{CS}}$ Setup Time to CKE	t_{MPX_S}	TBD	-		
$\overline{\text{CS}}$ Hold Time to CKE	t_{MPX_H}	TBD	-		
Calibration Timing					
Power-up and $\overline{\text{RESET}}$ Calibration Time	t_{zQinit}	1024	-	nCK	
Normal Operation Full Calibration Time	t_{zQoper}	512	-	nCK	
Normal Operation Short Calibration Time	t_{zQCS}	128	-	nCK	

Device Timing Parameters by Speed Bin (Continued)

Parameter	Symbol	DDR4-2133		Units	Notes
		Min	Max		
RESET/Self-Refresh Timing					
Exit $\overline{\text{RESET}}$ from CKE HIGH to a Valid Command	t_{XPR}	Max(5nCK, $t_{RFCmin} + 10ns$)	-		
Exit Self-Refresh to Commands not Requiring a Locked DLL	t_{XS}	$t_{RFCmin} + 10ns$	-		
SRX to Commands not Requiring a Locked DLL in Self-Refresh ABORT	t_{XS_ABORT}	$t_{RFC4min} + 10ns$	-		
Exit Self-Refresh to ZQCL, ZQCS and MRS (CL, CWL, WL, RTP and Geardown)	t_{XS_FAST}	$t_{RFC4min} + 10ns$	-		
Exit Self Refresh from to Commands Requiring a Locked DLL	t_{XSDLL}	$t_{DLLKmin}$	-		
Minimum CKE Low Width for Self-Refresh Entry to Exit Timing	t_{CKESR}	$t_{CKEmin} + 1nCK$	-		
Valid Clock Requirement after Self-Refresh Entry (SRE) or Power-Down Entry (PDE)	t_{CKSRE}	Max(5nCK, 10ns)	-		
Valid Clock Requirement after Self-Refresh Entry (SRE) or Power-Down Entry (PDE) when CA Parity us Enabled	t_{CKSRE_PAR}	Max(5nCK, 10ns) + PL	-		
Valid Clock Requirement before Self-Refresh Exit (SRX) or Power-Down Exit (PDX) or RESET Exit	t_{CKSRX}	Max(5nCK, 10ns)	-		
Power Down Timing					
Exit Power Down with DLL on to any Valid Command; Exit Precharge Power Down with DLL Frozen to Commands not Requiring a Locked DLL	t_{XP}	Max(4nCK, 6ns)	-		
CKE Minimum Pulse Width	t_{CKE}	Max(3nCK, 5ns)	-		27, 28
Command Pass Disable Delay	t_{CPDED}	4	-	nCK	
Power Down Entry to Exit Timing	t_{PD}	t_{CKEmin}	$9 * t_{REFI}$		6
Timing of ACT Command to Power Down Entry	$t_{ACTPDEN}$	2	-	nCK	7
Timing of PRE or PREA Command to Power Down Entry	t_{PRPDEN}	2	-	nCK	7
Timing of RD/RDA Command to Power Down Entry	t_{RDPDEN}	RL + 4 + 1	-	nCK	
Timing of WR Command to Power Down Entry (BL8OTF, BL8MRS, BC4OTF)	t_{WRPDEN}	WL + 4 + ($t_{WR} / t_{CK(avg)}$)	-	nCK	4
Timing of WRA Command to Power Down Entry (BL8OTF, BL8MRS, BC4OTF)	$t_{WRAPDEN}$	WL + 4 + WR + 1	-	nCK	5
Timing of WR Command to Power Down Entry (BC4MRS)	$t_{WRPBC4DEN}$	WL + 2 + ($t_{WR} / t_{CK(avg)}$)	-	nCK	4
Timing of WRA Command to Power Down Entry (BC4MRS)	$t_{WRAPBC4DEN}$	WL + 2 + WR + 1	-	nCK	5
Timing of REF Command to Power Down Entry	$t_{REFPDEN}$	2	-	nCK	7
Timing of MRS Command to Power Down Entry	$t_{MRSPDEN}$	t_{MODmin}	-		

Device Timing Parameters by Speed Bin (Continued)

Parameter	Symbol	DDR4-2133		Units	Notes
		Min	Max		
PDA Timing					
Mode Register Set Command Cycle Time in PDA Mode	t_{MRD_PDA}	Max(16nCK, 10ns)	-		
Mode Register Set Command Update Delay in PDA Mode	t_{MOD_PDA}	t_{MOD}			
ODT Timing					
Asynchronous RTT Turn-On Delay (Power Down with DLL Frozen)	t_{AONAS}	1	9	ns	
Asynchronous RTT Turn-Off Delay (Power Down with DLL Frozen)	t_{AOFAS}	1	9	ns	
RTT Dynamic Change Skew	t_{ADC}	0.3	0.7	$t_{CK(avg)}$	
Write Leveling Timing					
First DQS/ \overline{DQS} Rising Edge after Write Leveling Mode is Programmed	t_{WLMRD}	40	-	nCK	12
DQS/ \overline{DQS} Delay after Write Leveling Mode is Programmed	$t_{WLDQSEN}$	25	-	nCK	12
Write Leveling Setup Time from Rising CK, \overline{CK} Crossing to Rising DQS, \overline{DQS} Crossing	t_{WLS}	0.13	-	$t_{CK(avg)}$	
Write Leveling Hold Time from Rising CK, \overline{CK} Crossing to Rising DQS, \overline{DQS} Crossing	t_{WLH}	0.13	-	$t_{CK(avg)}$	
Write Leveling Output Delay	t_{WLO}	0	9.5	ns	
Write Leveling Output Error	t_{WLOE}			ns	
CA Parity Timing					
Commands not Guaranteed to be Executed during this Time	$t_{PAR_UNKNOWN}$	-	Max(2nCK, 3ns)		
Delay from Errant Command to \overline{ALERT} Assertion	$t_{PAR_ALERT_ON}$	-	PL + 6ns		
Pulse Width of \overline{ALERT} Signal when Asserted	$t_{PAR_ALERT_PW}$	64	128	nCK	
Time from when \overline{ALERT} is Asserted until Controller Must Start Providing DES Commands in Persistent CA Parity Mode	$t_{PAR_ALERT_RSP}$	-	57	nCK	
Parity Latency	PL	4		nCK	
CRC Error Reporting					
CRC Error to \overline{ALERT} Latency	t_{CRC_ALERT}	-	13	ns	
CRC \overline{ALERT} Pulse Width	$t_{CRC_ALERT_PW}$	6	10	nCK	
Refresh Timing					
1x Refresh Cycle Time - 4Gb	t_{RFC1}	260	-	ns	
2x Refresh Cycle Time - 4Gb	t_{RFC2}	160	-	ns	
4x Refresh Cycle Time - 4Gb	t_{RFC4}	110	-	ns	

Device Timing Parameters Notes

1. Start of internal write transaction is defined as follows:
 For BL8 (Fixed by MRS and on-the-fly): Rising clock edge 4 clock cycles after WL.
 For BC4 (on-the-fly): Rising clock edge 4 clock cycles after WL.
 For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.
2. A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled.
3. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
4. t_{WR} is defined in ns, for calculation of t_{WRPDEN} it is necessary to round up t_{WR}/t_{CK} to the next integer.
5. WR in clock cycles as programmed in MRO.
6. t_{REFI} depends on t_{OPER} .
7. CKE is allowed to be registered low while operations such as row activation, precharge, auto-precharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
8. For these parameters, the DDR4 SDRAM device supports $t_{nPARAM} [nCK] = RU \{t_{PARAM} [ns]/t_{CK(avg)} [ns]\}$, which is in clock cycles assuming all input clock jitter specifications are satisfied.
9. When CRC and DM are both enabled, $t_{WR_CRC_DM}$ is used in place of t_{WR} .
10. When CRC and DM are both enabled $t_{WTR_S_CRC_DM}$ is used in place of t_{WTR_S} .
11. When CRC and DM are both enabled $t_{WTR_L_CRC_DM}$ is used in place of t_{WTR_L} .
12. The max values are system dependent.
13. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are TBD.
14. The deterministic component of the total timing. Measurement method is TBD.
15. DQ to DQ static offset relative to strobe per group. Measurement method is TBD.
16. This parameter will be characterized and guaranteed by design.
17. When the device is operated with the input clock jitter, this parameter needs to be derated by the actual $t_{jit(per)}_{total}$ of the input clock (output deratings are relative to the SDRAM input clock). Example TBD.
18. DRAM DBI mode is off.
19. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
20. t_{QSL} describes the instantaneous differential output low pulse width on DQS - \overline{DQS} , as measured from on falling edge to the next consecutive rising edge.
21. t_{QSH} describes the instantaneous differential output high pulse width on DQS - \overline{DQS} , as measured from on falling edge to the next consecutive rising edge.
22. There is no maximum cycle time limit besides the need to satisfy the refresh interval t_{REFI} .
23. $t_{CH(abs)}$ is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
24. $t_{CL(abs)}$ is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are TBD.
26. The deterministic jitter component out of the total jitter. This parameter is characterized and guaranteed by design.
27. After CKE is registered LOW, CKE signal level shall be maintained below $V_{IL}(DC)$ for t_{CKE} specification (LOW Pulse Width).
28. After CKE is registered HIGH, CKE signal level shall be maintained above $V_{IH}(DC)$ for t_{CKE} specification (HIGH Pulse Width).
29. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.

$$UI = t_{CK(avg)} \min/2$$

I_{DD} and I_{PP} Measurement-Loop Patterns Timing

Speed Bin		DDR4-2133	Units
Parameter		15-15-15	
t _{CK}		0.938	ns
CL		15	nCK
CWL		14	nCK
nRCD		15	nCK
nRC		51	nCK
nRAS		36	nCK
nRP		15	nCK
nFAW	x4	16	nCK
	x8	23	
	x16	32	
nRRDS	x4	4	nCK
	x8	4	
	x16	6	
nRRDL	x4	6	nCK
	x8	6	
	x16	7	
nRFC		278	nCK

I_{DD} and I_{PP} Measurement Conditions

- I_{DD} currents (such as I_{DD0}, I_{DD0A}, I_{DD1}, I_{DD1A}, I_{DD2N}, I_{DD2NA}, I_{DD2NL}, I_{DD2NT}, I_{DD2P}, I_{DD2Q}, I_{DD3N}, I_{DD3NA}, I_{DD3P}, I_{DD4R}, I_{DD4RA}, I_{DD4W}, I_{DD4WA}, I_{DD5B}, I_{DD5F2}, I_{DD5F4}, I_{DD6N}, I_{DD6E}, I_{DD6R}, I_{DD6A}, I_{DD7} and I_{DD8}) are measured as time-averaged currents with all V_{DD} balls of the DDR4 SDRAM under test tied together. Any I_{PP} current is not included in I_{DD} currents.
- I_{PP} currents have the same definition as I_{DD} except that the current on the V_{PP} supply is measured.
- “0” and “LOW” is defined as V_{IN} ≤ V_{IL(AC)}max.
- “1” and “HIGH” is defined as V_{IN} ≥ V_{IH(AC)}min.
- “MID-LEVEL” is defined as inputs that are V_{REF} = V_{DD}/2.
- Timings used for I_{DD} and I_{PP} Measurement-Loop Patterns are provided in the I_{DD} and I_{PP} Measurement-Loop Patterns Timing on page 47.
- Basic I_{DD} and I_{PP} Measurement Conditions are described on pages 49-54.
- Detailed I_{DD} and I_{PP} Measurement-Loop Patterns are described on pages 56-64.
- I_{DD} and I_{PP} Measurements are done after properly initializing the DDR4 SDRAM. This includes but is not limited to setting:
 - RON = RZQ/7 (34 Ohm in MR1);
 - RTT_NOM = RZQ/6 (40 Ohm in MR1);
 - RTT_WR = RZQ/2 (120 Ohm in MR2);
 - RTT_PARK = Disable;
 - Qoff = 0B (Output Buffer enabled) in MR1;
 - TDQS disabled in MR1;
 - CRC disabled in MR2;
 - CA parity feature disabled in MR5;
 - Gear down mode disabled in MR3;
 - Read/Write DBI disabled in MR5;
 - DM disabled in MR5
- Attention: The I_{DD} and I_{PP} Measurement-Loop Patterns need to be executed at least one time before actual I_{DD} and I_{PP} measurement is started.
- Define $\overline{D} = \{\overline{CS}, \overline{ACT}, \overline{RAS}, \overline{CAS}, \overline{WE}\} = \{\text{HIGH}, \text{LOW}, \text{LOW}, \text{LOW}, \text{LOW}\}$
- Define $\overline{D} = \{\overline{CS}, \overline{ACT}, \overline{RAS}, \overline{CAS}, \overline{WE}\} = \{\text{HIGH}, \text{HIGH}, \text{HIGH}, \text{HIGH}, \text{HIGH}\}$



Basic I_{DD} and I_{PP} Measurement Conditions

Symbol	Description
I _{DD0}	Operating One Bank Active-Precharge Current (AL = 0) CKE: HIGH; External Clock: On; t_{CK}, nRC, nRAS, CL: See I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 47; BL: 8 ¹ ; AL: 0; CS: HIGH between ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: Partially toggling according to I _{DD0} , I _{DD0A} and I _{PP0} Measurement-Loop Pattern on page 56; Data I/O: V _{DD} ; DM: Stable at 1; Bank Activity: Cycling with one bank active at a time: 0, 0, 1, 1, 2, 2,... (See I _{DD0} , I _{DD0A} and I _{PP0} Measurement-Loop Pattern on page 56); Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: Stable at 0; Pattern Details: See I _{DD0} , I _{DD0A} and I _{PP0} Measurement-Loop Pattern on page 56
I _{DD0A}	Operating One Bank Active-Precharge Current (AL = CL - 1) AL: CL-1; Other conditions: See I _{DD0}
I _{PP0}	Operating One Bank Active-Precharge IPP Current Same conditions as I _{DD0}
I _{DD1}	Operating One Bank Active-Read-Precharge Current (AL = 0) CKE: HIGH; External Clock: On; t_{CK}, nRC, nRAS, CL: See I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 47; BL: 8 ¹ ; AL: 0; CS: HIGH between ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data I/O: Partially toggling according to I _{DD1} , I _{DD1A} and I _{PP1} Measurement-Loop Pattern on page 57; DM: Stable at 1; Bank Activity: Cycling with one bank active at a time: 0, 0, 1, 1, 2, 2,... (See I _{DD1} , I _{DD1A} and I _{PP1} Measurement-Loop Pattern on page 57); Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: Stable at 0; Pattern Details: See I _{DD1} , I _{DD1A} and I _{PP1} Measurement-Loop Pattern on page 57
I _{DD1A}	Operating One Bank Active-Read-Precharge Current (AL = CL - 1) AL: CL - 1; Other Conditions: See I _{DD1}
I _{PP1}	Operating One Bank Active-Read-Precharge IPP Current Same Conditions as I _{DD1}
I _{DD2N}	Precharge Standby Current (AL = 0) CKE: HIGH; External Clock: On; t_{CK}, CL: See I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 47; BL: 8 ¹ ; AL: 0; CS: Stable at 1; Command, Address, Bank Group Address, Bank Address Inputs, Data I/O: Partially Toggling according to I _{DD2N} , I _{DD2NA} , I _{PP2N} , I _{DD2NL} , I _{DD2NG} , I _{DD2ND} , I _{DD2N_par} , I _{DD3N} , I _{DD3NA} and I _{PP3N} Measurement-Loop Pattern on page 58; DM: Stable at 1; Bank Activity: All Banks Closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: Stable at 0; Pattern Details: See I _{DD2N} , I _{DD2NA} , I _{PP2N} , I _{DD2NL} , I _{DD2NG} , I _{DD2ND} , I _{DD2N_par} , I _{DD3N} , I _{DD3NA} and I _{PP3N} Measurement-Loop Pattern on page 58
I _{DD2NA}	Precharge Standby Current (AL = CL - 1) AL: CL - 1; Other conditions: See I _{DD2N}
I _{PP2N}	Precharge Standby IPP Current Same Conditions as I _{DD2N}



Basic I_{DD} and I_{PP} Measurement Conditions (Continued)

Symbol	Description
I _{DD2NT}	Precharge Standby ODT Current CKE: HIGH; External Clock: On; t_{CK}, CL: See I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 47; BL: 8 ¹ ; AL: 0; CS: Stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: Partially Toggling according to I _{DD2NT} Measurement-Loop Pattern on page 59; Data I/O: V _{SS} ; DM: Stable at 1; Bank Activity: All Banks Closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: Toggling according to I _{DD2NT} Measurement-Loop Pattern on page 59; Pattern Details: See I _{DD2NT} Measurement-Loop Pattern on page 59
I _{DD2NL}	Precharge Standby Current with CAL Enabled Same Conditions as I _{DD2N} ; CAL Enabled ³
I _{DD2NG}	Precharge Standby Current with Geardown Mode Enabled Same Conditions as I _{DD2N} ; Geardown Mode Enabled ³
I _{DD2ND}	Precharge Standby Current with DLL Disabled Same Conditions as I _{DD2N} ; DLL Disabled ³
I _{DD2N_par}	Precharge Standby Current with CA Parity Enabled Same Conditions as I _{DD2N} ; CA Parity Enabled ³
I _{DD2P}	Precharge Power-Down Current CKE: LOW; External Clock: On; t_{CK}, CL: See I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 47; BL: 8 ¹ ; AL: 0; CS: Stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: Stable at 0; DATA I/O: V _{DD} ; DM: Stable at 1; Bank Activity: All Banks Closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: Stable at 0
I _{PP2P}	Precharge Power-Down IPP Current Same Conditions as I _{DD2P}
I _{DD2Q}	Precharge Quiet Standby Current CKE: High; External Clock: On; t_{CK}, CL: See I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 47; BL: 8 ¹ ; AL: 0; CS: Stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: Stable at 0; DATA I/O: V _{DD} ; DM: Stable at 1; Bank Activity: All Banks Closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: Stable at 0
I _{DD3N}	Active Standby Current (AL = 0) CKE: HIGH; External Clock: On; t_{CK}, CL: See I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 47; BL: 8 ¹ ; AL: 0; CS: Stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: Partially Toggling according to I _{DD2N} , I _{DD2NA} , I _{PP2N} , I _{DD2NL} , I _{DD2NG} , I _{DD2ND} , I _{DD2N_par} , I _{DD3N} , I _{DD3NA} and I _{PP3N} Measurement-Loop Pattern on page 58; DATA I/O: V _{DD} ; DM: Stable at 1; Bank Activity: All Banks Closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: Stable at 0; Pattern Details: See I _{DD2N} , I _{DD2NA} , I _{PP2N} , I _{DD2NL} , I _{DD2NG} , I _{DD2ND} , I _{DD2N_par} , I _{DD3N} , I _{DD3NA} and I _{PP3N} Measurement-Loop Pattern on page 58



Basic I_{DD} and I_{PP} Measurement Conditions (Continued)

Symbol	Description
I _{DD3NA}	Active Standby Current (AL = CL - 1) AL: CL - 1; Other conditions: See I _{DD3N}
I _{PP3N}	Active Standby IPP Current Same Conditions as I _{DD3N}
I _{DD3P}	Active Power-Down Current CKE: LOW; External Clock: On; t _{CK} , CL: See I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 47; BL: 8 ¹ ; AL: 0; $\overline{\text{CS}}$: Stable at 1; Command, Address, Bank Group Address, Bank Address Inputs : Stable at 0; DATA I/O : V _{DD} ; DM : Stable at 1; Bank Activity : All Banks Open; Output Buffer and RTT : Enabled in Mode Registers ² ; ODT Signal : Stable at 0
I _{PP3P}	Active Power-Down IPP Current Same Conditions as I _{DD3P}
I _{DD4R}	Operating Burst Read Current (AL = 0) CKE: HIGH; External Clock: On; t _{CK} , CL: See I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 47; BL: 8 ¹ ; AL: 0; $\overline{\text{CS}}$: HIGH between RD; Command, Address, Bank Group Address, Bank Address Inputs : Partially Toggling according to I _{DD4R} , I _{DD4RA} , I _{DD4RB} and I _{PP4R} Measurement-Loop Pattern on page 60; DATA I/O : Seamless Read Data Burst with Different Data between One Burst and the Next One according to I _{DD4R} , I _{DD4RA} , I _{DD4RB} and I _{PP4R} Measurement-Loop Pattern on page 60; DM : Stable at 1; Bank Activity : All Banks Open, RD Commands Cycling through Banks: 0, 0, 1, 1, 2, 2,... (See I _{DD4R} , I _{DD4RA} , I _{DD4RB} and I _{PP4R} Measurement-Loop Pattern on page 60); Output Buffer and RTT : Enabled in Mode Registers ² ; ODT Signal : Stable at 0; Pattern Details : See I _{DD4R} , I _{DD4RA} , I _{DD4RB} and I _{PP4R} Measurement-Loop Pattern on page 60
I _{DD4RA}	Operating Burst Read Current (AL = CL - 1) AL: CL - 1; Other conditions: See I _{DD4R}
I _{DD4RB}	Operating Burst Read Current with Read DBI Same Conditions as I _{DD4R} ; Read DBI Enabled ³
I _{PP4R}	Operating Burst Read IPP Current Same Conditions as I _{DD4R}



Basic I_{DD} and I_{PP} Measurement Conditions (Continued)

Symbol	Description
I _{DD4W}	Operating Burst Write Current (AL = 0) CKE: HIGH; External Clock: On; t_{CK}, CL: See I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 47; BL: 8 ¹ ; AL: 0; CS: HIGH between WR; Command, Address, Bank Group Address, Bank Address Inputs: Partially Toggling according to I _{DD4W} , I _{DD4WA} , I _{DD4WB} , I _{DD4W_par} and I _{PP4W} Measurement-Loop Pattern on page 61; DATA I/O: Seamless Write Data Burst with Different Data between One Burst and the Next One according to I _{DD4W} , I _{DD4WA} , I _{DD4WB} , I _{DD4W_par} and I _{PP4W} Measurement-Loop Pattern on page 61; DM: Stable at 1; Bank Activity: All Banks Open, WR Commands Cycling through Banks: 0, 0, 1, 1, 2, 2,... (See I _{DD4W} , I _{DD4WA} , I _{DD4WB} , I _{DD4W_par} and I _{PP4W} Measurement-Loop Pattern on page 61); Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: Stable at HIGH; Pattern Details: See I _{DD4W} , I _{DD4WA} , I _{DD4WB} , I _{DD4W_par} and I _{PP4W} Measurement-Loop Pattern on page 61
I _{DD4WA}	Operating Burst Write Current (AL = CL - 1) AL: CL - 1; Other conditions: See I _{DD4W}
I _{DD4WB}	Operating Burst Write Current with Write DBI Same Conditions as I _{DD4W} ; Write DBI Enabled ³
I _{DD4WC}	Operating Burst Write Current with Write CRC CKE: HIGH; External Clock: On; t_{CK}, CL: See I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 47; BL: 8 ¹ ; AL: 0; CS: HIGH between WR; Command, Address, Bank Group Address, Bank Address Inputs: Partially Toggling according to I _{DD4WC} Measurement-Loop Pattern on page 62; DATA I/O: Seamless Write Data Burst with Different Data between One Burst and the Next One according to I _{DD4WC} Measurement-Loop Pattern on page 62; DM: Stable at 1; Bank Activity: All Banks Open, WR Commands Cycling through Banks: 0, 0, 1, 1, 2, 2,... (See I _{DD4WC} Measurement-Loop Pattern on page 62); Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: Stable at HIGH; Pattern Details: See I _{DD4WC} Measurement-Loop Pattern on page 62 Measurement-Loop Pattern on page 61; Write CRC Enabled ³
I _{DD4W_par}	Operating Burst Write Current with CA Parity Same Conditions as I _{DD4W} ; CA Parity Enabled ³
I _{PP4W}	Operating Burst Write IPP Current Same Conditions as I _{DD4W}



Basic I_{DD} and I_{PP} Measurement Conditions (Continued)

Symbol	Description
I _{DD5B}	Burst Refresh Current (1X REF) CKE: HIGH; External Clock: On; t_{CK}, CL, nRFC: See I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 47; BL: 8 ¹ ; AL: 0; CS: HIGH between REF; Command, Address, Bank Group Address, Bank Address Inputs: Partially Toggling according to I _{DD5B} , I _{PP5B} , I _{DD5F2} , I _{PP5F2} , I _{DD5F4} , and I _{PP5F4} Measurement-Loop Pattern on page 63; DATA I/O: V _{DD} ; DM: Stable at 1; Bank Activity: REF Command Every nRFC (See I _{DD5B} , I _{PP5B} , I _{DD5F2} , I _{PP5F2} , I _{DD5F4} , and I _{PP5F4} Measurement-Loop Pattern on page 63); Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: Stable at 0; Pattern Details: See I _{DD5B} , I _{PP5B} , I _{DD5F2} , I _{PP5F2} , I _{DD5F4} , and I _{PP5F4} Measurement-Loop Pattern on page 63
I _{PP5B}	Burst Refresh IPP Current (1X REF) Same Conditions as I _{DD5B}
I _{DD5F2}	Burst Refresh Current (2X REF) Same Conditions as I _{DD5B} ; t _{RFC} = t _{RFC2}
I _{PP5F2}	Burst Refresh IPP Current (2X REF) Same Conditions as I _{DD5F2} ; t _{RFC} = t _{RFC2}
I _{DD5F4}	Burst Refresh Current (4X REF) Same Conditions as I _{DD5B} ; t _{RFC} = t _{RFC4}
I _{PP5F4}	Burst Refresh IPP Current (4X REF) Same Conditions as I _{DD5F4} ; t _{RFC} = t _{RFC4}
I _{DD6N}	Self-Refresh Current: Normal Temperature Range T _{CASE} : 0 - 85 °C; Low Power Array Self Refresh (LP ASR): Normal ⁴ ; CKE: LOW; External Clock: Off; CK and CK: LOW; CL: I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 47; BL: 8 ¹ ; AL: 0; CS, Command, Address, Bank Group Address, Bank Address, Data I/O: HIGH; DM: Stable at 1; Bank Activity: Self-Refresh Operation; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: MID-LEVEL
I _{PP6N}	Self-Refresh IPP Current: Normal Temperature Range Same Conditions as I _{DD6N}
I _{DD6E}	Self-Refresh Current: Extended Temperature Range T _{CASE} : 0 - 95 °C; Low Power Array Self Refresh (LP ASR): Extended ⁴ ; CKE: LOW; External Clock: Off; CK and CK: LOW; CL: I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 47; BL: 8 ¹ ; AL: 0; CS, Command, Address, Bank Group Address, Bank Address, Data I/O: HIGH; DM: Stable at 1; Bank Activity: Extended Temperature Self-Refresh Operation; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: MID-LEVEL
I _{PP6E}	Self-Refresh IPP Current: Extended Temperature Range Same Conditions as I _{DD6E}



Basic I_{DD} and I_{PP} Measurement Conditions (Continued)

Symbol	Description
I _{DD6R}	Self-Refresh Current: Extended Temperature Range T _{CASE} : 0 - TBD (~35-45)°C; Low Power Array Self Refresh (LP ASR) : Reduced ⁴ ; CKE : LOW; External Clock : Off; CK and CK : LOW; CL : I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 47; BL : 8 ¹ ; AL : 0; CS, Command, Address, Bank Group Address, Bank Address, Data I/O : HIGH; DM : Stable at 1; Bank Activity : Reduced Temperature Self-Refresh Operation; Output Buffer and RTT : Enabled in Mode Registers ² ; ODT Signal : MID-LEVEL
I _{PP6R}	Self-Refresh IPP Current: Reduced Temperature Range Same Conditions as I _{DD6R}
I _{DD6A}	Auto Self-Refresh Current T _{CASE} : 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Auto ⁴ ; Partial Array Self-Refresh (PASR) : Full Array; CKE : LOW; External Clock : Off; CK and CK : LOW; CL : I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 47; BL : 8 ¹ ; AL : 0; CS, Command, Address, Bank Group Address, Bank Address, Data I/O : HIGH; DM : Stable at 1; Bank Activity : Auto Self-Refresh Operation; Output Buffer and RTT : Enabled in Mode Registers ² ; ODT Signal : MID-LEVEL
I _{PP6A}	Auto Self-Refresh IPP Current Same Conditions as I _{DD6A}
I _{DD7}	Operating Bank Interleave Read Current CKE : HIGH; External Clock : On; t _{CK} , nRAS, nRCD, nRRD, nFAW, CL : See I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 47; BL : 8 ¹ ; AL : CL - 1; CS : HIGH between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs : Partially Toggling according to I _{DD7} and I _{PP7} Measurement-Loop Pattern on page 64; Data I/O : Read Data Bursts with Different Data between One Burst and the Next One according to I _{DD7} and I _{PP7} Measurement-Loop Pattern on page 64; DM : Stable at 1; Bank Activity : Two Times Interleaved Cycling through Banks (0, 1,...7) with Different Addressing, See I _{DD7} and I _{PP7} Measurement-Loop Pattern on page 64; Output Buffer and RTT : Enabled in Mode Registers ² ; ODT Signal : Stable at 0; Pattern Details : See I _{DD7} and I _{PP7} Measurement-Loop Pattern on page 64
I _{PP7}	Operating Bank Interleave Read IPP Current Same Conditions as I _{DD7}
I _{DD8}	Maximum Power-Down Read Current TBD
I _{PP8}	Maximum Power-Down IPP Current Same Conditions as I _{DD8}



Notes:

1. Burst Length: BL8 fixed by MRS: set MR0 [A1:0=00].
2. Output Buffer Enabled:
 - Set MR1 [A12 = 0]: Qoff = Output buffer enabled
 - Set MR1 [A2:1 = 00]: Output Driver Impedance Control = RZQ/7RTT_Nom Enabled:
 - Set MR1 [A10:8 = 011]: RTT_NOM = RZQ/6RTT_WR Enabled:
 - Set MR2 [A10:9 = 01]: RTT_WR = RZQ/2RTT_PARK Disabled:
 - Set MR5 [A8:6 = 000]
3. CAL Enabled:
 - Set MR4 [A8:6 = 001]: 1600MT/s
 - Set MR4 [A8:6 = 010]: 1866MT/s, 2133MT/s
 - Set MR4 [A8:6 = 011]: 2400MT/sGeardown Mode Enabled:
 - Set MR3 [A3 = 1]: 1/4 RateDLL Disabled:
 - Set MR1 [A0 = 0]CA Parity Enabled:
 - Set MR5 [A2:0 = 001]: 1600MT/s,1866MT/s, 2133MT/s
 - Set MR5 [A2:0 = 010]: 2400MT/sRead DBI Enabled:
 - Set MR5 [A12 = 1]Write DBI Enabled:
 - Set MR5 [A11 = 1]
4. Low Power Array Self Refresh (LP ASR):
 - Set MR2 [A7:6 = 00]: Normal Temperature Range
 - Set MR2 [A7:6 = 01]: Reduced Temperature Range
 - Set MR2 [A7:6 = 10]: Extended Temperature Range
 - Set MR2 [A7:6 = 11]: Auto Self Refresh.



I_{DD0}, I_{DD0A} and I_{PP0} Measurement-Loop Pattern¹

CK, \overline{CK}	CKE	Sub-Loop	Cycle Number	Command	\overline{CS}	\overline{ACT}	$\overline{RAS/A16}$	$\overline{CAS/A15}$	$\overline{WE/A14}$	ODT	C[2:0] ³	BG[1:0] ²	BA[2:0]	A[12] \overline{BC}	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴			
Toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-		
			1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
			3, 4	$\overline{D}, \overline{D}$	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	0	7	F	0	-	
			...	Repeat pattern 1-4 until nRAS - 1. Truncate if Necessary																			
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			...	Repeat pattern 1-4 until nRC - 1. Truncate if Necessary																			
		1	1*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 1 and BA[1:0] = 1 instead																			
		2	2*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 2 instead																			
		3	3*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 1 and BA[1:0] = 3 instead																			
		4	4*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 1 instead																			
		5	5*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 1 and BA[1:0] = 2 instead																			
		6	6*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 3 instead																			
		7	7*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 1 and BA[1:0] = 0 instead																			
		8	8*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 0 instead																			
		9	9*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 3 and BA[1:0] = 1 instead																			
10	10*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 2 instead																					
11	11*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 3 and BA[1:0] = 3 instead																					
12	12*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 1 instead																					
13	13*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 3 and BA[1:0] = 2 instead																					
14	14*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 3 instead																					
15	15*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 3 and BA[1:0] = 0 instead																					

For x4 and x8 only



I_{DD1}, I_{DD1A} and I_{PP1} Measurement-Loop Pattern¹

CK, \overline{CK}	CKE	Sub-Loop	Cycle Number	Command	\overline{CS}	\overline{ACT}	RAS/A16	CAS/A15	$\overline{WE}/A14$	ODT	C[2:0] ³	BG[1:0] ²	BA[2:0]	A[12]/ \overline{BC}	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴				
Toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-			
			1-2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
			3-4	\overline{D} , \overline{D}	1	1	1	1	1	1	0	0	0	3 ²	3	0	0	0	0	7	F	0	-	
			...	Repeat pattern 1-4 until nRCD - 1. Truncate if Necessary																				
			nRCD - AL	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D0 = 00, D1 = FF D2 = FF, D3 = 00 D4 = FF, D5 = 00 D6 = 00, D7 = FF
			...	Repeat pattern 1-4 until nRAS - 1. Truncate if Necessary																				
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			...	Repeat pattern 1-4 until nRC - 1. Truncate if Necessary																				
			1*nRC + 0	ACT	0	0	0	1	1	0	0	1	1	0	1	1	0	0	0	0	0	0	0	-
			1*nRC + 1-2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
		1*nRC + 3-4	\overline{D} , \overline{D}	1	1	1	1	1	1	0	0	0	3 ²	3	0	0	0	0	7	F	0	-		
		...	Repeat pattern nRC + 1-4 until 1*nRC + nRCD - 1. Truncate if Necessary																					
		1*nRC + nRCD - AL	RD	0	1	1	0	1	0	0	1	1	0	1	1	0	0	0	0	0	0	0	D0 = FF, D1 = 00 D2 = 00, D3 = FF D4 = 00, D5 = FF D6 = FF, D7 = 00	
		...	Repeat pattern 1-4 until nRAS - 1. Truncate if Necessary																					
		1*nRC + nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
		...	Repeat pattern nRC + 1-4 until 2*nRC - 1. Truncate if Necessary																					
		2	2*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 2 instead																				
		3	3*nRC	Repeat Sub-Loop 1, but BG[1:0] ² = 1 and BA[1:0] = 3 instead																				
		4	4*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 1 instead																				
		5	5*nRC	Repeat Sub-Loop 1, but BG[1:0] ² = 1 and BA[1:0] = 2 instead																				
		6	6*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 3 instead																				
		7	7*nRC	Repeat Sub-Loop 1, but BG[1:0] ² = 1 and BA[1:0] = 0 instead																				
		8	8*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 0 instead																				
		9	9*nRC	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 1 instead																				
		10	10*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 2 instead																				
11	11*nRC	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 3 instead																						
12	12*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 1 instead																						
13	13*nRC	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 2 instead																						
14	14*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 3 instead																						
15	15*nRC	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 0 instead																						

For x4 and x8 only

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**I_{DD2N}, I_{DD2NA}, I_{PP2N}, I_{DD2NL}, I_{DD2NG}, I_{DD2ND}, I_{DD2N_par}, I_{DD3N}, I_{DD3NA} and I_{PP3N}
Measurement-Loop Pattern¹**

CK, \overline{CK}	CKE	Sub-Loop	Cycle Number	Command	\overline{CS}	\overline{ACT}	RAS/A16	CAS/A15	$\overline{WE}/A14$	ODT	C[2:0] ³	BG[1:0] ²	BA[2:0]	A[12]/BC	A[7,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴		
Toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			2	\overline{D} , \overline{D}	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	7	F	0	0	0
			3	\overline{D} , \overline{D}	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	7	F	0	0	0
		1	4-7	Repeat Sub-Loop 0, but BG[1:0] ² = 1 and BA[1:0] = 1 instead																		
		2	8-11	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 2 instead																		
		3	12-15	Repeat Sub-Loop 0, but BG[1:0] ² = 1 and BA[1:0] = 3 instead																		
		4	16-19	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 1 instead																		
		5	20-23	Repeat Sub-Loop 0, but BG[1:0] ² = 1 and BA[1:0] = 2 instead																		
		6	24-27	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 3 instead																		
		7	28-31	Repeat Sub-Loop 0, but BG[1:0] ² = 1 and BA[1:0] = 0 instead																		
		8	32-35	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 0 instead																		
		9	36-39	Repeat Sub-Loop 0, but BG[1:0] ² = 3 and BA[1:0] = 1 instead																		
		10	40-43	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 2 instead																		
		11	44-47	Repeat Sub-Loop 0, but BG[1:0] ² = 3 and BA[1:0] = 3 instead																		
12	48-51	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 1 instead																				
13	52-55	Repeat Sub-Loop 0, but BG[1:0] ² = 3 and BA[1:0] = 2 instead																				
14	56-59	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 3 instead																				
15	60-63	Repeat Sub-Loop 0, but BG[1:0] ² = 3 and BA[1:0] = 0 instead																				

For x4 and x8 only



I_{DD2NT} Measurement-Loop Pattern

CK, \overline{CK}	CKE	Sub-Loop	Cycle Number	Command	\overline{CS}	\overline{ACT}	$\overline{RAS/A16}$	$\overline{CAS/A15}$	$\overline{WE/A14}$	ODT	$C[2:0]^3$	$BG[1:0]^2$	$BA[2:0]$	$A[12]/\overline{BC}$	$A[17,13,11]$	$A[10]/AP$	$A[9:7]$	$A[6:3]$	$A[2:0]$	Data ⁴			
Toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-		
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
			2	$\overline{D}, \overline{D}$	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	7	F	0	0	-	
			3	$\overline{D}, \overline{D}$	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	7	F	0	0	-	
		1	4-7	Repeat Sub-Loop 0, but ODT = 1, $BG[1:0]^2 = 1$ and $BA[1:0] = 1$ instead																			
		2	8-11	Repeat Sub-Loop 0, but ODT = 0, $BG[1:0]^2 = 0$ and $BA[1:0] = 2$ instead																			
		3	12-15	Repeat Sub-Loop 0, but ODT = 1, $BG[1:0]^2 = 1$ and $BA[1:0] = 3$ instead																			
		4	16-19	Repeat Sub-Loop 0, but ODT = 0, $BG[1:0]^2 = 0$ and $BA[1:0] = 1$ instead																			
		5	20-23	Repeat Sub-Loop 0, but ODT = 1, $BG[1:0]^2 = 1$ and $BA[1:0] = 2$ instead																			
		6	24-27	Repeat Sub-Loop 0, but ODT = 0, $BG[1:0]^2 = 0$ and $BA[1:0] = 3$ instead																			
		7	28-31	Repeat Sub-Loop 0, but ODT = 1, $BG[1:0]^2 = 1$ and $BA[1:0] = 0$ instead																			
		8	32-35	Repeat Sub-Loop 0, but ODT = 0, $BG[1:0]^2 = 2$ and $BA[1:0] = 0$ instead																			For x4 and x8 only
		9	36-39	Repeat Sub-Loop 0, but ODT = 1, $BG[1:0]^2 = 3$ and $BA[1:0] = 1$ instead																			
		10	40-43	Repeat Sub-Loop 0, but ODT = 0, $BG[1:0]^2 = 2$ and $BA[1:0] = 2$ instead																			
		11	44-47	Repeat Sub-Loop 0, but ODT = 1, $BG[1:0]^2 = 3$ and $BA[1:0] = 3$ instead																			
12	48-51	Repeat Sub-Loop 0, but ODT = 0, $BG[1:0]^2 = 2$ and $BA[1:0] = 1$ instead																					
13	52-55	Repeat Sub-Loop 0, but ODT = 1, $BG[1:0]^2 = 3$ and $BA[1:0] = 2$ instead																					
14	56-59	Repeat Sub-Loop 0, but ODT = 0, $BG[1:0]^2 = 2$ and $BA[1:0] = 3$ instead																					
15	60-63	Repeat Sub-Loop 0, but ODT = 1, $BG[1:0]^2 = 3$ and $BA[1:0] = 0$ instead																					



I_{DD4R}, I_{DD4RA}, I_{DD4RB} and I_{PP4R} Measurement-Loop Pattern¹

CK, \overline{CK}	CKE	Sub-Loop	Cycle Number	Command	\overline{CS}	\overline{ACT}	RAS/A16	$\overline{CAS}/A15$	$\overline{WE}/A14$	ODT	C[2:0] ³	BG[1:0] ²	BA[2:0]	A[12]/ \overline{BC}	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴		
Toggling	Static High	0	0	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	D0 = 00, D1 = FF D2 = FF, D3 = 00 D4 = FF, D5 = 00 D6 = 00, D7 = FF	
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
			2-3	$\overline{D}, \overline{D}$	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	7	F	0	-	
		1	4	RD	0	1	1	0	1	0	0	0	1	1	0	0	0	7	F	0	0	D0 = FF, D1 = 00 D2 = 00, D3 = FF D4 = 00, D5 = FF D6 = FF, D7 = 00
			5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			6-7	$\overline{D}, \overline{D}$	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	7	F	0	-	
		2	8-11	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 2 instead																		
		3	12-15	Repeat Sub-Loop 1, but BG[1:0] ² = 1 and BA[1:0] = 3 instead																		
		4	16-19	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 1 instead																		
		5	20-23	Repeat Sub-Loop 1, but BG[1:0] ² = 1 and BA[1:0] = 2 instead																		
		6	24-27	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 3 instead																		
		7	28-31	Repeat Sub-Loop 1, but BG[1:0] ² = 1 and BA[1:0] = 0 instead																		
		8	32-35	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 0 instead																		
		9	36-39	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 1 instead																		
		10	40-43	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 2 instead																		
11	44-47	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 3 instead																				
12	48-51	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 1 instead																				
13	52-55	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 2 instead																				
14	56-59	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 3 instead																				
15	60-63	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 0 instead																				

For x4 and x8 only



I_{DD4W}, I_{DD4WA}, I_{DD4WB}, I_{DD4W_par} and I_{PP4W} Measurement-Loop Pattern¹

CK, \overline{CK}	CKE	Sub-Loop	Cycle Number	Command	\overline{CS}	\overline{ACT}	RAS/A16	$\overline{CAS}/A15$	$\overline{WE}/A14$	ODT	C[2:0] ³	BG[1:0] ²	BA[2:0]	A[12]/ \overline{BC}	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴			
Toggling	Static High	0	0	WR	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	D0 = 00, D1 = FF D2 = FF, D3 = 00 D4 = FF, D5 = 00 D6 = 00, D7 = FF		
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
			2-3	$\overline{D}, \overline{D}$	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	7	F	0	0	-	
		1	4	WR	0	1	1	0	1	0	0	0	1	1	0	0	0	7	F	0	0	D0 = FF, D1 = 00 D2 = 00, D3 = FF D4 = 00, D5 = FF D6 = FF, D7 = 00	
			5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
			6-7	$\overline{D}, \overline{D}$	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	7	F	0	0	-	
		2	8-11	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 2 instead																			
		3	12-15	Repeat Sub-Loop 1, but BG[1:0] ² = 1 and BA[1:0] = 3 instead																			
		4	16-19	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 1 instead																			
		5	20-23	Repeat Sub-Loop 1, but BG[1:0] ² = 1 and BA[1:0] = 2 instead																			
		6	24-27	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 3 instead																			
		7	28-31	Repeat Sub-Loop 1, but BG[1:0] ² = 1 and BA[1:0] = 0 instead																			
		8	32-35	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 0 instead																			
		9	36-39	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 1 instead																			
		10	40-43	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 2 instead																			
11	44-47	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 3 instead																					
12	48-51	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 1 instead																					
13	52-55	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 2 instead																					
14	56-59	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 3 instead																					
15	60-63	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 0 instead																					
																				For x4 and x8 only			



I_{DD4WC} Measurement-Loop Pattern¹

CK, \overline{CK}	CKE	Sub-Loop	Cycle Number	Command	\overline{CS}	\overline{ACT}	RAS/A16	$\overline{CAS/A15}$	$\overline{WE/A14}$	ODT	C[2:0] ³	BG[1:0] ²	BA[2:0]	A[12]/ \overline{BC}	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴		
Toggling	Static High	0	0	WR	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	D0 = 00, D1 = FF D2 = FF, D3 = 00 D4 = FF, D5 = 00 D6 = 00, D7 = FF D8 = CRC	
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
			2-3	$\overline{D}, \overline{D}$	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	7	F	0	-	
		1	4	WR	0	1	1	0	1	0	0	0	1	1	0	0	0	7	F	0	0	D0 = FF, D1 = 00 D2 = 00, D3 = FF D4 = 00, D5 = FF D6 = FF, D7 = 00 D8 = CRC
			5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			6-7	$\overline{D}, \overline{D}$	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	7	F	0	-	
		2	8-11	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 2 instead																		
		3	12-15	Repeat Sub-Loop 1, but BG[1:0] ² = 1 and BA[1:0] = 3 instead																		
		4	16-19	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 1 instead																		
		5	20-23	Repeat Sub-Loop 1, but BG[1:0] ² = 1 and BA[1:0] = 2 instead																		
		6	24-27	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 3 instead																		
		7	28-31	Repeat Sub-Loop 1, but BG[1:0] ² = 1 and BA[1:0] = 0 instead																		
		8	32-35	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 0 instead																		
		9	36-39	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 1 instead																		
		10	40-43	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 2 instead																		
11	44-47	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 3 instead																				
12	48-51	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 1 instead																				
13	52-55	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 2 instead																				
14	56-59	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 3 instead																				
15	60-63	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 0 instead																				

For x4 and x8 only



I_{DD5B}, I_{PP5B}, I_{DD5F2}, I_{PP5F2}, I_{DD5F4} and I_{PP5F4} Measurement-Loop Pattern¹

CK, \overline{CK}	CKE	Sub-Loop	Cycle Number	Command	\overline{CS}	\overline{ACT}	RAS/A16	CAS/A15	$\overline{WE}/A14$	ODT	C[2:0] ³	BG[1:0] ²	BA[2:0]	A[12] \overline{BC}	A[17,13,11]	A[10] \overline{AP}	A[9:7]	A[6:3]	A[2:0]	Data ⁴		
toggling	Static High	0	0	REF	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
		1	1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
		2	2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
		3	3	$\overline{D}, \overline{D}$	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	7	F	0	0	-
		4	4	$\overline{D}, \overline{D}$	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	7	F	0	0	-
		4-7	Repeat Pattern 1-4, but BG[1:0] ² = 0 and BA[1:0] = 2 instead																			
		8-11	Repeat Pattern 1-4, but BG[1:0] ² = 0 and BA[1:0] = 2 instead																			
		12-15	Repeat Pattern 1-4, but BG[1:0] ² = 1 and BA[1:0] = 3 instead																			
		16-19	Repeat Pattern 1-4, but BG[1:0] ² = 0 and BA[1:0] = 1 instead																			
		20-23	Repeat Pattern 1-4, but BG[1:0] ² = 1 and BA[1:0] = 2 instead																			
		24-27	Repeat Pattern 1-4, but BG[1:0] ² = 0 and BA[1:0] = 3 instead																			
		28-31	Repeat Pattern 1-4, but BG[1:0] ² = 1 and BA[1:0] = 0 instead																			
		32-35	Repeat Pattern 1-4, but BG[1:0] ² = 2 and BA[1:0] = 0 instead																			
		36-39	Repeat Pattern 1-4, but BG[1:0] ² = 3 and BA[1:0] = 1 instead																			
		40-43	Repeat Pattern 1-4, but BG[1:0] ² = 2 and BA[1:0] = 2 instead																			
		44-47	Repeat Pattern 1-4, but BG[1:0] ² = 3 and BA[1:0] = 3 instead																			
		48-51	Repeat Pattern 1-4, but BG[1:0] ² = 2 and BA[1:0] = 1 instead																			
		52-55	Repeat Pattern 1-4, but BG[1:0] ² = 3 and BA[1:0] = 2 instead																			
		56-59	Repeat Pattern 1-4, but BG[1:0] ² = 2 and BA[1:0] = 3 instead																			
		60-63	Repeat Pattern 1-4, but BG[1:0] ² = 3 and BA[1:0] = 0 instead																			
		2	64-nRFC - 1 Repeat Sub-Loop 1. Truncate if Necessary																			

For x4 and x8 only



I_{DD7} and I_{PP7} Measurement-Loop Pattern¹

CK, \overline{CK}	CKE	Sub-Loop	Cycle Number	Command	\overline{CS}	\overline{ACT}	RAS/A16	CAS/A15	$\overline{WE}/A14$	ODT	C[2:0] ³	BG[1:0] ²	BA[2:0]	A[12]/ \overline{BC}	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴			
Toggling	Static High	0	0	ACT	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	-			
			1	RDA	0	0	1	0	1	0	0	0	0	0	0	0	1	0	0	0	D0 = 00, D1 = FF D2 = FF, D3 = 00 D4 = FF, D5 = 00 D6 = 00, D7 = FF		
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-		
			3	\overline{D}	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	7	F	0	-		
			...	Repeat pattern 2-3 until nRRD - 1, if nRCD > 4. Truncate if Necessary																			
		1	nRRD	ACT	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	-		
			nRRD + 1	RDA	0	1	1	0	1	0	0	0	1	1	0	0	1	0	0	0	D0 = FF, D1 = 00 D2 = 00, D3 = FF D4 = 00, D5 = FF D6 = FF, D7 = 00		
			...	Repeat pattern 2-3 until 2*nRRD - 1, if nRCD > 4. Truncate if Necessary																			
		2	2*nRRD	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 2 instead																			
		3	3*nRRD	Repeat Sub-Loop 1, but BG[1:0] ² = 1 and BA[1:0] = 3 instead																			
		4	4*nRRD	Repeat pattern 2-3 until nFAW - 1, if nFAW > 4*nRCD. Truncate if Necessary																			
		5	nFAW	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 1 instead																			
		6	nFAW + nRRD	Repeat Sub-Loop 1, but BG[1:0] ² = 1 and BA[1:0] = 2 instead																			
		7	nFAW + 2*nRRD	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 3 instead																			
		8	nFAW + 3*nRRD	Repeat Sub-Loop 1, but BG[1:0] ² = 1 and BA[1:0] = 0 instead																			
		9	nFAW + 4*nRRD	Repeat Sub-Loop 4																			
		10	2*nFAW	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 0 instead																			
		11	2*nFAW + nRRD	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 1 instead																			
		12	2*nFAW + 2*nRRD	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 2 instead																			
		13	2*nFAW + 3*nRRD	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 3 instead																			
14	2*nFAW + 4*nRRD	Repeat Sub-Loop 4																					
15	3*nFAW	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 1 instead																					
16	3*nFAW + nRRD	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 2 instead																					
17	3*nFAW + 2*nRRD	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 3 instead																					
18	3*nFAW + 3*nRRD	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 0 instead																					
19	3*nFAW + 4*nRRD	Repeat Sub-Loop 4																					
20	4*nFAW	Repeat pattern 2-3 until nRC - 1, if nRC > 4*nFAW. Truncate if Necessary																					

For x4 and x8 only

Notes:

1. DQS, $\overline{\text{DQS}}$ are V_{DD} .
2. BG1 is don't care for a x16 device.
3. C[2:0] are used only for a 3DS device.
4. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are V_{DD} .

I_{DD} Specifications

Parameter	DDR4-2133	Units
	15-15-15	
I _{DD0}	TBD	mA
I _{DD0A}	TBD	mA
I _{DD1}	TBD	mA
I _{DD1A}	TBD	mA
I _{DD2N}	TBD	mA
I _{DD2NA}	TBD	mA
I _{DD2NT}	TBD	mA
I _{DD2NL}	TBD	mA
I _{DD2NG}	TBD	mA
I _{DD2ND}	TBD	mA
I _{DD2N_par}	TBD	mA
I _{DD2P}	TBD	mA
I _{DD2Q}	TBD	mA
I _{DD3N}	TBD	mA
I _{DD3NA}	TBD	mA
I _{DD3P}	TBD	mA
I _{DD4R}	TBD	mA
I _{DD4RA}	TBD	mA
I _{DD4RB}	TBD	mA
I _{DD4W}	TBD	mA
I _{DD4WA}	TBD	mA
I _{DD4WB}	TBD	mA



I_{DD} Specifications (Continued)

Parameter	DDR4-2133	Units
	15-15-15	
I _{DD4WC}	TBD	mA
I _{DD4W_PAR}	TBD	mA
I _{DD5B}	TBD	mA
I _{DD5F2}	TBD	mA
I _{DD5F4}	TBD	mA
I _{DD6N}	TBD	mA
I _{DD6E}	TBD	mA
I _{DD6R}	TBD	mA
I _{DD6A}	TBD	mA
I _{DD7}	TBD	mA
I _{DD8}	TBD	mA



I_{pp} Specifications

Parameter	DDR4-2133	Units
	15-15-15	
I _{PP0}	TBD	mA
I _{PP1}	TBD	mA
I _{PP2N}	TBD	mA
I _{PP2P}	TBD	mA
I _{PP3N}	TBD	mA
I _{PP3P}	TBD	mA
I _{PP4R}	TBD	mA
I _{PP4W}	TBD	mA
I _{PP5B}	TBD	mA
I _{PP5F2}	TBD	mA
I _{PP5F4}	TBD	mA
I _{PP5TC}	TBD	mA
I _{PP6N}	TBD	mA
I _{PP6E}	TBD	mA
I _{PP6R}	TBD	mA
I _{PP6A}	TBD	mA
I _{PP7}	TBD	mA
I _{PP8}	TBD	mA

Input/Output Capacitance

Parameter	Symbol	DDR4-2133		Units	Notes
		Min	Max		
Input/output capacitance	C_{IO}	0.7	1.4	pF	1, 2
Input/output capacitance delta	C_{DIO}	-0.1	0.1	pF	1, 2, 8
Input/output capacitance delta, DQS and \overline{DQS}	C_{DDQS}	-	0.05	pF	1, 2, 4
Input capacitance, CK and \overline{CK}	C_{CK}	0.8	1.1	pF	1
Input capacitance delta, CK and \overline{CK}	C_{DCK}	-	0.1	pF	1, 3
Input capacitance, ADD, CMD, CTRL input-only pins	C_I	0.8	1.1	pF	1, 5
Input capacitance delta, ADD, CMD, CTRL input-only pins	C_{DI}	-	0.2	pF	1, 6, 7
Input capacitance of ALERT	C_{ALERT}	0.5	2	pF	1

Notes:

- This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by de-embedding the package L & C parasitic. The capacitance is measured with V_{DD} , V_{DDQ} , V_{SS} , V_{SSQ} applied with all other signal pins floating. Measurement procedure TBD.
- DQ, DM, DQS, \overline{DQS} , TDQS, \overline{TDQS} . Although the DM, TDQS and \overline{TDQS} pins have different functions, the loading matches DQ and DQS
- Absolute value CK - \overline{CK}
- Absolute value of $C_{IO}(DQS) - C_{IO}(\overline{DQS})$
- C_I applies to ODT, \overline{CS} , CKE, A0-A17, BA0-BA1, BG0-BG1, $\overline{RAS}/A16$, $\overline{CAS}/A15$, $\overline{WE}/A14$, \overline{ACT} and PAR.
- C_{DI} applies to ODT, \overline{CS} , CKE, A0-A17, BA0-BA1, BG0-BG1, $\overline{RAS}/A16$, $\overline{CAS}/A15$, $\overline{WE}/A14$, \overline{ACT} and PAR.
- $C_{DI} = C_I - 0.5 * (C_I(\overline{CLK}) + C_I(\overline{CLK}))$
- $C_{DIO} = C_{IO}(DQ, DM) - 0.5 * (C_{IO}(DQS) + C_{IO}(\overline{DQS}))$.

Serial Presence Detect (SPD)

Serial Presence Detect Table

Byte No.	Byte Description	Supported Value	Hex Value
0	Number of Serial PD Bytes Written / SPD Device Size / CRC Coverage	512 Total Bytes / 384 Bytes Used	23h
1	SPD Revision	Revision 1.0	10h
2	Key Byte / DRAM Device Type	DDR4 SDRAM	0Ch
3	Key Byte / Module Type	RDIMM	01h
4	SDRAM Density and Banks	4 Bank Groups / 4 Banks / 4 Gb	84h
5	SDRAM Addressing	15 Row / 10 Column	19h
6	SDRAM Package Type	Monolithic	00h
7	SDRAM Optional Features	tMAW = 8192*tREFI / MAC = Unlimited	08h
8	SDRAM Thermal and Refresh Options	Reserved	00h
9	Other SDRAM Optional Features	PPR supported	40h
10	Reserved	-	00h
11	Module Nominal Voltage (VDD)	1.2V	03h
12	Module Organization	1 Rank / x8	01h
13	Module Memory Bus Width	ECC / 64 bits	0Bh
14	Module Thermal Sensor	Thermal Sensor	80h
15-16	Reserved	-	00h
17	Timebases	MTB = 125 ps / FTB = 1 ps	00h
18	SDRAM Minimum Cycle Time (tCKAVGmin)	0.938 ns	08h
19	SDRAM Maximum Cycle Time (tCKAVGmax)	1.6 ns	0Dh
20	CAS Latencies Supported (First Byte)	9 / 11 / 12 / 13 / 14	F4h
21	CAS Latencies Supported (Second Byte)	15 / 16	03h
22	CAS Latencies Supported (Third Byte)	-	00h
23	CAS Latencies Supported (Fourth Byte)	-	00h
24	Minimum CAS Latency Time (tAAmin)	13.5 ns	6Ch
25	Minimum RAS to CAS Delay Time (tRCDmin)	13.5 ns	6Ch
26	Minimum Row Precharge Delay Time (tRPmin)	13.5 ns	6Ch



Byte No.	Byte Description	Supported Value	Hex Value
27	Upper Nibbles for tRASmin and tRCmin	tRAS = 33 ns / tRC = 46.5 ns	11h
28	Minimum Active to Precharge Delay Time (tRASmin) (LSB)	33 ns	08h
29	Minimum Active to Active/Refresh Delay Time (tRCmin) (LSB)	46.5 ns	74h
30	Minimum Refresh Recovery Delay Time (tRFC1min) (LSB)	260 ns	20h
31	Minimum Refresh Recovery Delay Time (tRFC1min) (MSB)	260 ns	08h
32	Minimum Refresh Recovery Delay Time (tRFC2min) (LSB)	160 ns	00h
33	Minimum Refresh Recovery Delay Time (tRFC2min) (MSB)	160 ns	05h
34	Minimum Refresh Recovery Delay Time (tRFC4min) (LSB)	110 ns	70h
35	Minimum Refresh Recovery Delay Time (tRFC4min) (MSB)	110 ns	03h
36	Minimum Four Activate Window Time (tFAWmin) (MSB)	21 ns	00h
37	Minimum Four Activate Window Time (tFAWmin) (LSB)	21 ns	A8h
38	Minimum Activate to Activate Delay Time (tRRD_Smin) (different bank group)	3.7 ns	1Eh
39	Minimum Activate to Activate Delay Time (tRRD_Lmin) (same bank group)	5.3 ns	2Bh
40	Minimum CAS to CAS Delay Time (tCCD_Lmin) (same bank group)	5.625 ns	2Dh
41-59	Reserved	-	00h
60	Connector to SRAM Bit Mapping	DQ0-DQ3	24h
61	Connector to SRAM Bit Mapping	DQ4-DQ7	03h
62	Connector to SRAM Bit Mapping	DQ8-DQ11	15h
63	Connector to SRAM Bit Mapping	DQ12-DQ15	2Ch
64	Connector to SRAM Bit Mapping	DQ16-DQ19	24h
65	Connector to SRAM Bit Mapping	DQ20-DQ23	03h
66	Connector to SRAM Bit Mapping	DQ24-DQ27	15h
67	Connector to SRAM Bit Mapping	DQ28-DQ31	2Ch
68	Connector to SRAM Bit Mapping	CB0-CB3	24h

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Byte No.	Byte Description	Supported Value	Hex Value
69	Connector to SRAM Bit Mapping	CB4-CB7	03h
70	Connector to SRAM Bit Mapping	DQ32-DQ35	24h
71	Connector to SRAM Bit Mapping	DQ36-DQ39	03h
72	Connector to SRAM Bit Mapping	DQ40-DQ43	15h
73	Connector to SRAM Bit Mapping	DQ44-DQ47	2Ch
74	Connector to SRAM Bit Mapping	DQ48-DQ51	24h
75	Connector to SRAM Bit Mapping	DQ52-DQ55	03h
76	Connector to SRAM Bit Mapping	DQ56-DQ59	15h
77	Connector to SRAM Bit Mapping	DQ60-DQ63	2Ch
78-116	Reserved	-	00h
117	Fine Offset for Minimum CAS to CAS Delay Time (tCCD_Lmin) (same bank group)	5.625 ns	00h
118	Fine Offset for Minimum Activate to Activate Delay Time (tRRD_Lmin) (same bank group)	5.3 ns	B5h
119	Fine Offset for Minimum Activate to Activate Delay Time (tRRD_Smin) (different bank group)	3.7 ns	CEh
120	Fine Offset for Minimum Activate to Activate/Refresh Delay Time (tRCmin)	46.5 ns	00h
121	Fine Offset for Minimum Row Precharge Delay Time (tRPmin)	13.5 ns	00h
122	Fine Offset for Minimum RAS to CAS Delay Time (tRCDmin)	13.5 ns	00h
123	Fine Offset for Minimum CAS Latency Time (tAAmin)	13.5 ns	00h
124	Fine Offset for SDRAM Maximum Cycle Time (tCKAVG-max)	1.6 ns	E7h
125	Fine Offset for SDRAM Minimum Cycle Time (tCKAVG-min)	0.938 ns	C2h
126	CRC for Base Configuration Section (LSB)	CRC for bytes 0-125	9Bh
127	CRC for Base Configuration Section (MSB)	CRC for bytes 0-125	08h
128	Raw Card Extension / Module Nominal Height	18.75mm	04h
129	Module Maximum Thickness	Front = 1.3mm / Back = 1.2 mm	11h
130	Reference Raw Card Used	R/C G / Revision 0	06h
131	DIMM Module Attributes	1 Row / 1 Register	05h
132	RDIMM Thermal Heat Spreader Solution	No Heatspreader	80h

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Byte No.	Byte Description	Supported Value	Hex Value
133	Register Manufacturer ID Code (LSB)	Generic	00h
134	Register Manufacturer ID Code (MSB)	Generic	00h
135	Register Revision Number	Generic	FFh
136	Address Mapping from Register to DRAM	Standard	00h
137	Register Output Drive Strength for Control	Address/Control Drive Strength	00h
138	Register Output Drive Strength for CK	CK Drive Strength	00h
139-253	Reserved	-	00h
254	CRC for Module Specific Section (LSB)	CRC for bytes 128-253	C0h
255	CRC for Module Specific Section (MSB)	CRC for bytes 128-253	69h
256-319	Reserved	-	00h
320	Module Manufacturer's ID Code (LSB)	1 Continuation Code	01h
321	Module Manufacturer's ID Code (MSB)	SMART's ID Code	94h
322	Module Manufacturing Location	See Note 1	xxh
323	Module Manufacturing Date	Date (Year)	xxh
324	Module Manufacturing Date	Date (Week)	xxh
325-328	Module Serial Number	Serial Number	xxh
329	Module Part Number	S	53h
330	Module Part Number	H	48h
331	Module Part Number	5	35h
332	Module Part Number	1	31h
333	Module Part Number	2	32h
334	Module Part Number	7	37h
335	Module Part Number	R	52h
336	Module Part Number	D	44h
337	Module Part Number	4	34h
338	Module Part Number	5	35h
339	Module Part Number	1	31h
340	Module Part Number	8	38h
341	Module Part Number	5	35h
342	Module Part Number	1	31h
343	Module Part Number	S	53h

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Byte No.	Byte Description	Supported Value	Hex Value
344	Module Part Number	D	44h
345	Module Part Number	V	56h
346	Module Part Number		20h
347	Module Part Number		20h
348	Module Part Number		20h
349	Module Revision Code	Revision 0	00h
350	DRAM Manufacturer's ID Code (LSB)	Samsung	80h
351	DRAM Manufacturer's ID Code (MSB)	Samsung	CEh
352	DRAM Stepping	Revision D	00h
353	Module Manufacturer's Specific Data	S	53h
354	Module Manufacturer's Specific Data	M	4Dh
355	Module Manufacturer's Specific Data	A	41h
356	Module Manufacturer's Specific Data	R	52h
357	Module Manufacturer's Specific Data	T	54h
358	Module Manufacturer's Specific Data	M	4Dh
359	Module Manufacturer's Specific Data	o	6Fh
360	Module Manufacturer's Specific Data	d	64h
361	Module Manufacturer's Specific Data	u	75h
362	Module Manufacturer's Specific Data	l	6Ch
363	Module Manufacturer's Specific Data	a	61h
364	Module Manufacturer's Specific Data	r	72h
365	Module Manufacturer's Specific Data	T	54h
366	Module Manufacturer's Specific Data	e	65h
367	Module Manufacturer's Specific Data	c	63h
368	Module Manufacturer's Specific Data	h	68h
369	Module Manufacturer's Specific Data	n	6Eh
370	Module Manufacturer's Specific Data	o	6Fh
371	Module Manufacturer's Specific Data	l	6Ch
372	Module Manufacturer's Specific Data	o	6Fh
373	Module Manufacturer's Specific Data	g	67h
374	Module Manufacturer's Specific Data	i	69h
375	Module Manufacturer's Specific Data	e	65h

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Byte No.	Byte Description	Supported Value	Hex Value
376	Module Manufacturer's Specific Data	s	73h
377	Module Manufacturer's Specific Data	For Internal Use	xxh
378-381	Module Manufacturer's Specific Data	-	00h
382-383	Reserved	-	00h
384-511	End User Programmable	-	00h

Notes:

1. Manufacturing Location:
00h - Undefined,
01h - Newark, CA, USA,
02h - Aguada, Puerto Rico,
03h - East Kilbride, Scotland,
04h - Penang, Malaysia,
05h - Bangalore, India,
06h - Sao Paulo, Brazil,
07h - Aguadilla, Puerto Rico,
08h - Mayaguez, Puerto Rico,
09h - Santo Domingo, Dominican Republic,
0Ah - Dongguan, China,



Declaration of Conformity



Responsible Party Name: SMART Modular Technologies, Inc.
Address: 39870 Eureka Drive
Newark, CA 94560-4809, USA
Phone: +1-510-623-1231

hereby declares that the products:

SH5127RD451851SDV

to which this declaration relates are in conformity with the following Directives and other normative documents:

RoHS Directive 2011/65/EU

Restriction of the use of certain hazardous substances in electrical and electronic equipment

• **EN 50581:2012**

Technical documentation for the assessment of electrical and electronic products with respect to the restriction of hazardous substances

Name: Jeffrey Milano
Title: Director, Worldwide Quality
Date: August 21, 2014

Representative in the European Union (for regulatory topics only):

Mr. Graham Kyle
SMART Modular Technologies (Europe) Ltd.
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