

## 24-V Input Voltage, 150-mA, Ultralow $I_Q$ Low-Dropout Regulators

### FEATURES

- **Wide Input Voltage Range: 2.5 V to 24 V**
- **Low 3.2- $\mu$ A Quiescent Current**
- **Ground Pin Current: 3.4  $\mu$ A at 100-mA  $I_{OUT}$**
- **Stable with Any Capacitor (> 0.47  $\mu$ F)**
- **Operating Junction Temperature:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$**
- **Available in SOT23-5 Package**
  - See *Package Option Addendum* at end of this document for complete list of available voltage options

### APPLICATIONS

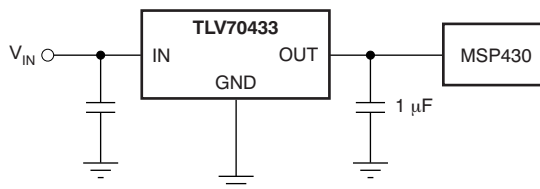
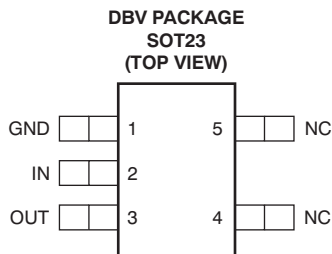
- **Ultralow Power Microcontrollers**
- **E-Meters**
- **Fire Alarms/Smoke Detector Systems**
- **Handset Peripherals**
- **Industrial/Automotive Applications**
- **Remote Controllers**
- **Zigbee™ Networks**
- **PDA's**
- **Portable, Battery-Powered Equipment**

### DESCRIPTION

The TLV704xx series of low dropout (LDO) regulators are ultralow quiescent current devices designed for extremely power-sensitive applications. Quiescent current is virtually constant over the complete load current and ambient temperature range. These devices are an ideal power management attachment to low-power microcontrollers, such as the [MSP430](#).

The TLV704xx operate over a wide operating input voltage of 2.5 V to 24 V. Thus, it is an excellent choice for both battery-powered systems as well as industrial applications that see large line transients.

The TLV704xx is available in a 3-mm  $\times$  3-mm SOT23-5 package, which is ideal for cost-effective board manufacturing.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### AVAILABLE OPTIONS<sup>(1)</sup>

PRODUCT	V <sub>OUT</sub>
TLV704xxyyyz	<b>XX</b> is nominal output voltage (for example 33 = 3.3 V) <b>YYY</b> is Package Designator <b>Z</b> is Package Quantity

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Over operating free-air temperature range, unless otherwise noted.

		VALUE		UNIT
		MIN	MAX	
Voltage <sup>(2)</sup>	IN	-0.3	24	V
Current source	OUT	Internally limited		
Temperature	Operating junction, T <sub>J</sub>	-40	+150	°C
	Storage, T <sub>stg</sub>	-65	+150	°C
Electrostatic Discharge Rating <sup>(3)</sup>	Human body model (HBM) QSS 009-105 (JEDEC22-A114A)		2	kV
	Charge device model (CDM) QSS 009-147 (JEDEC22-C101B.01)		500	V

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network ground terminal.
- (3) ESD testing is performed according to the respective JEDEC standard.

### THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		TLV70433DBV	UNITS
		DBV	
		5 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance	213.1	°C/W
$\theta_{JcTop}$	Junction-to-case (top) thermal resistance	110.9	
$\theta_{JB}$	Junction-to-board thermal resistance	97.4	
$\psi_{JT}$	Junction-to-top characterization parameter	22.0	
$\psi_{JB}$	Junction-to-board characterization parameter	78.4	
$\theta_{JcBot}$	Junction-to-case (bottom) thermal resistance	n/a	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](http://www.ti.com/lit/spr953).

### POWER DISSIPATION RATING TABLE

BOARD	PACKAGE	R <sub>θJA</sub>	T <sub>A</sub> ≤ 25°C POWER RATING	T <sub>A</sub> = +70°C POWER RATING	T <sub>A</sub> = +85°C POWER RATING
High-K <sup>(1)</sup>	DBV	213.1 °C/W	470 mW	258 mW	188 mW

- (1) The JEDEC High-K (2s2p) board design used to derive this data was a 3-inch × 3-inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

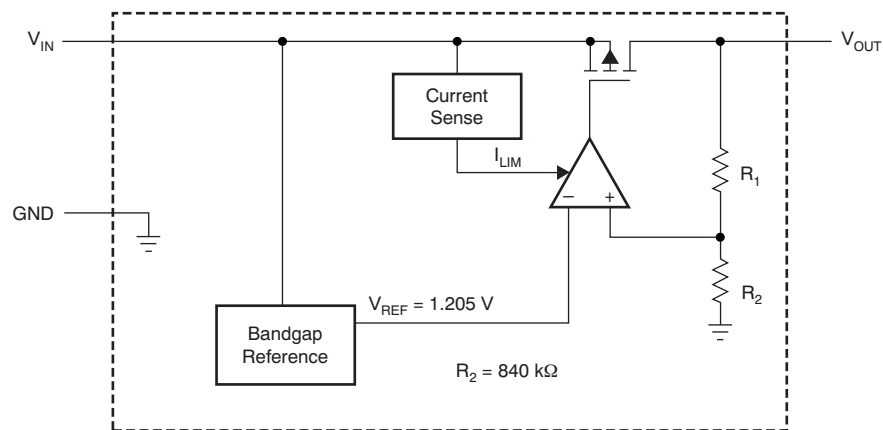
## ELECTRICAL CHARACTERISTICS

All values are at  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(\text{nom})} + 1\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$ , and  $C_{OUT} = 1\text{ }\mu\text{F}$ , unless otherwise noted.

PARAMETER	TEST CONDITIONS	TLV704xx			UNIT	
		MIN	TYP	MAX		
$V_O$	Input voltage range			24	V	
	Output voltage range	1.2		5	V	
$V_{OUT}$	DC output accuracy	-2		2	%	
$\Delta V_O$ for $\Delta V_{IN}$	Line regulation	$V_{OUT(\text{NOM})} + 1\text{ V} < V_{IN} < 24\text{ V}$		20	50	mV
$\Delta V_O$ for $\Delta I_{OUT}$	Load regulation	$V_{OUT} \leq 3.3\text{ V}$	$0\text{ mA} < I_{OUT} < 10\text{ mA}$	10		mV
			$0\text{ mA} < I_{OUT} < 50\text{ mA}$	25		mV
			$0\text{ mA} < I_{OUT} < 100\text{ mA}$	33	50	mV
		$V_{OUT} \geq 3.3\text{ V}$	$0\text{ mA} < I_{OUT} < 10\text{ mA}$	7		mV
			$0\text{ mA} < I_{OUT} < 50\text{ mA}$	35		mV
			$0\text{ mA} < I_{OUT} < 100\text{ mA}$	50	75	mV
$V_{DO}$	Dropout voltage <sup>(1)</sup>	$I_{OUT} = 10\text{ mA}$		75		mV
		$I_{OUT} = 50\text{ mA}$		400		mV
		$I_{OUT} = 100\text{ mA}$		850	1100	mV
$I_{CL}$	Output current limit	$V_{OUT} = 0\text{ V}$	160		1000	mA
$I_{GND}$	Ground pin current	$I_{OUT} = 0\text{ mA}$		3.2	4.5	$\mu\text{A}$
		$I_{OUT} = 100\text{ mA}$		3.4	5.5	$\mu\text{A}$
PSRR	Power-supply rejection ratio	$f = 100\text{ kHz}$ , $C_{OUT} = 10\text{ }\mu\text{F}$		60		dB
$T_J$	Operating junction temperature		-40		+125	$^\circ\text{C}$

(1)  $V_{IN} = V_{OUT(\text{NOM})} - 0.1\text{ V}$ .

### FUNCTIONAL BLOCK DIAGRAM



**Table 1. Pin Descriptions**

TLV704xx		DESCRIPTION
NAME	DBV	
GND	1	Ground
IN	2	Unregulated input voltage.
OUT	3	Regulated output voltage. Any capacitor greater than 1 $\mu\text{F}$ between this pin and ground is needed for stability.
NC	4, 5	No connection. This pin can be left open or tied to ground for improved thermal performance.

TYPICAL CHARACTERISTICS

LINE REGULATION

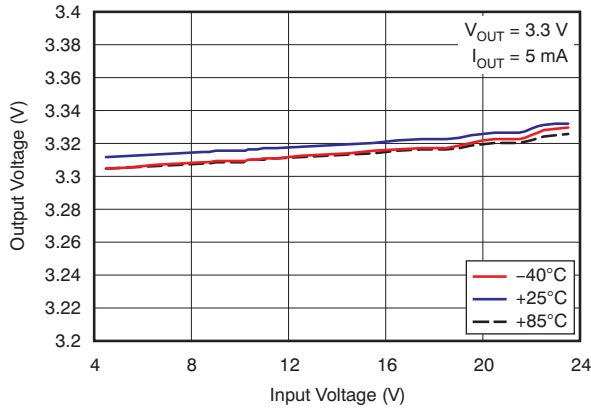


Figure 1.

LOAD REGULATION  
( $V_{OUT} = 3.3\text{ V}$ )

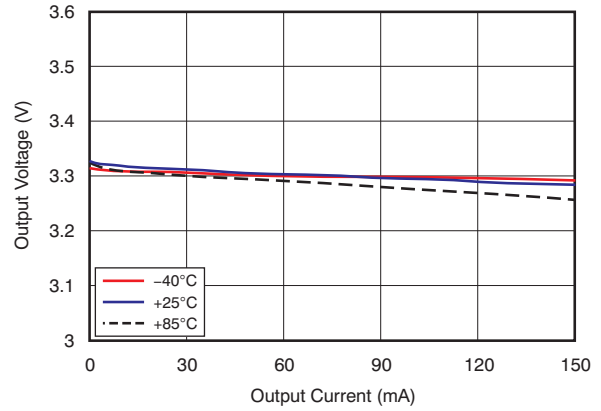


Figure 2.

OUTPUT VOLTAGE vs  
JUNCTION TEMPERATURE

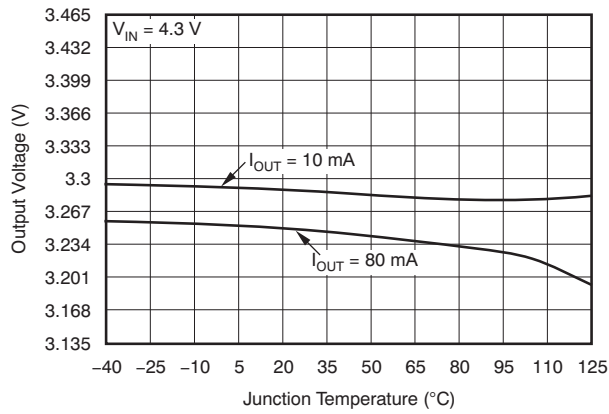


Figure 3.

DROPOUT VOLTAGE vs INPUT VOLTAGE  
TLV70433

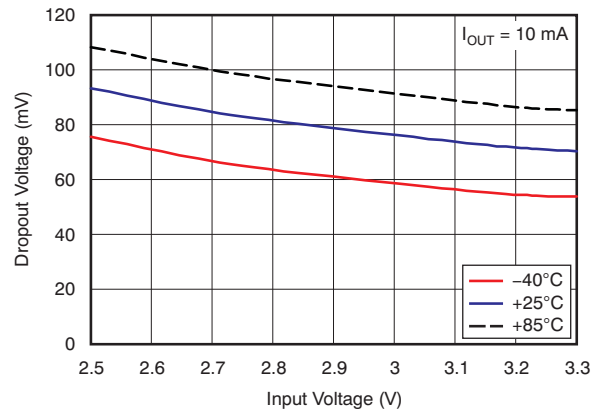


Figure 4.

DROPOUT VOLTAGE vs OUTPUT CURRENT

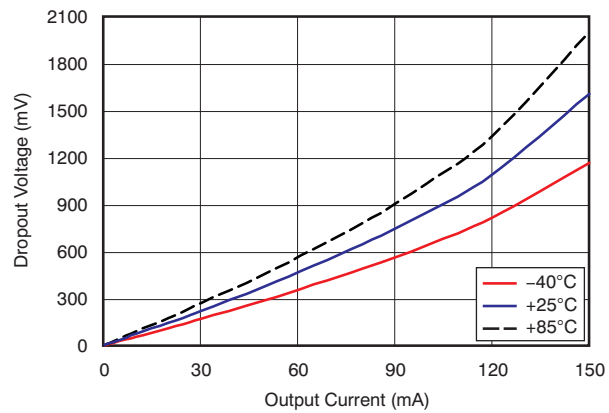


Figure 5.

GROUND CURRENT vs JUNCTION TEMPERATURE

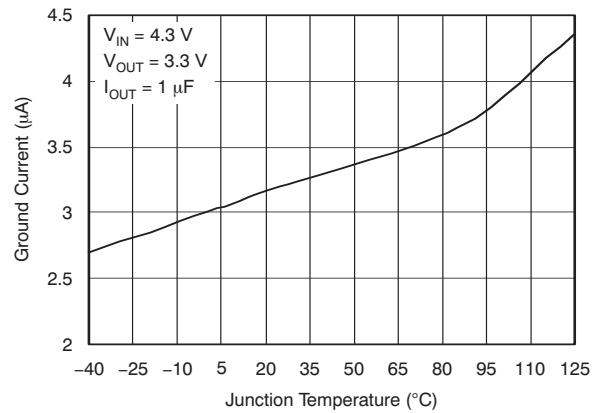


Figure 6.

TYPICAL CHARACTERISTICS (continued)

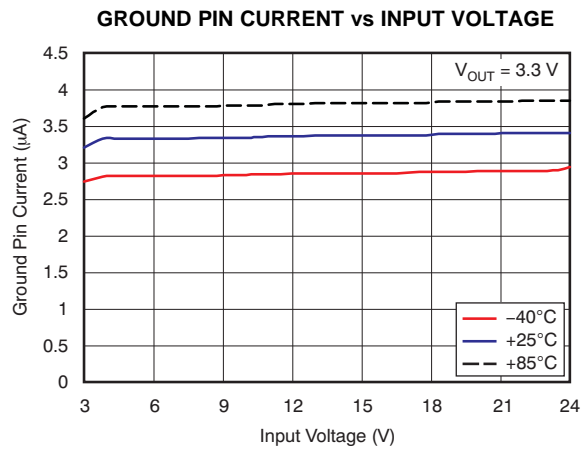


Figure 7.

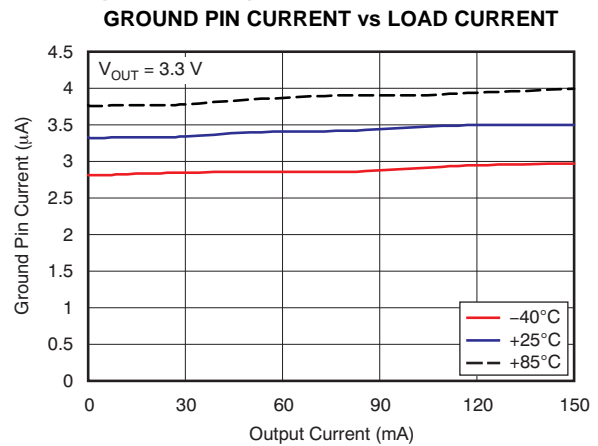


Figure 8.

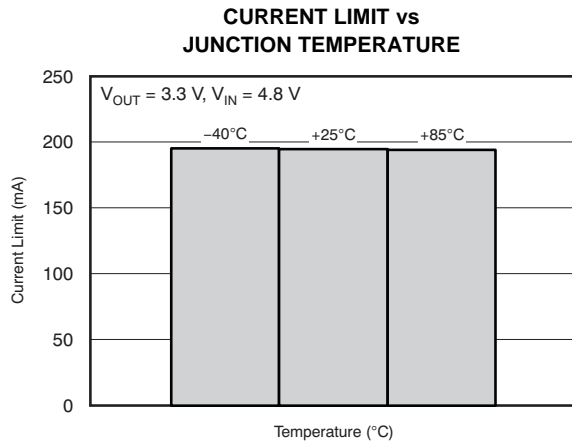


Figure 9.

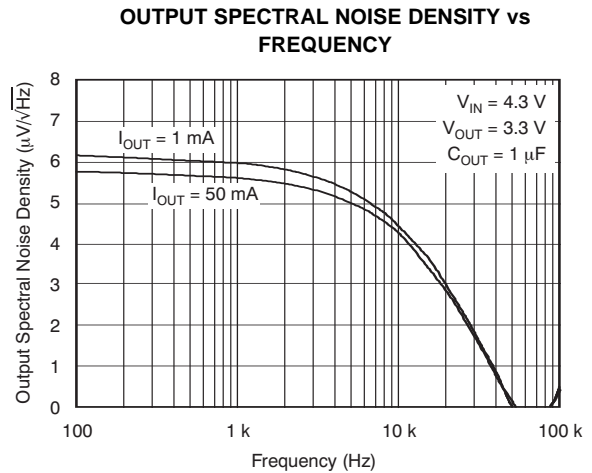


Figure 10.

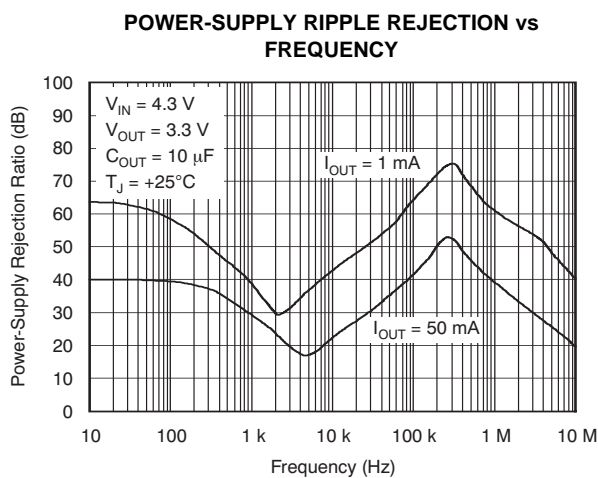


Figure 11.

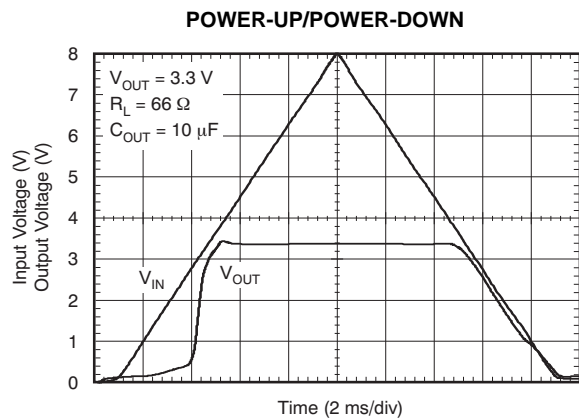
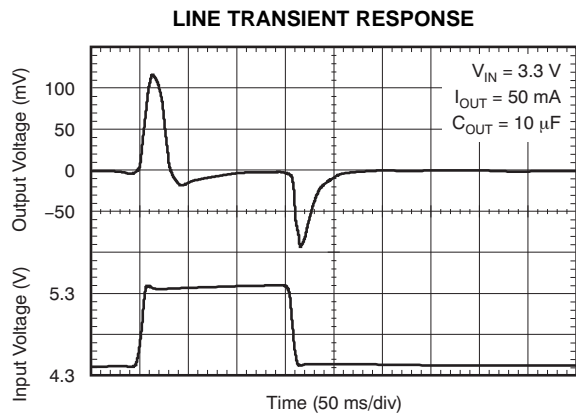
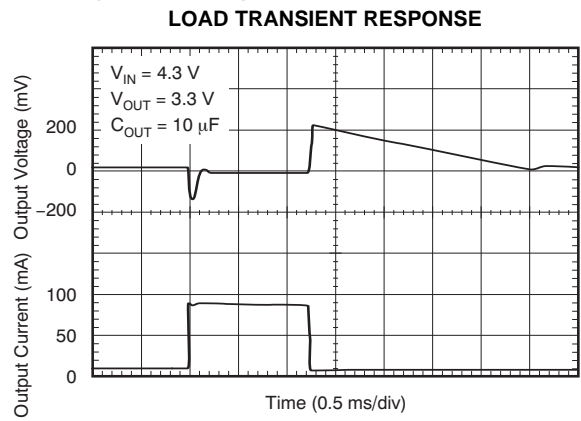


Figure 12.

**TYPICAL CHARACTERISTICS (continued)**



**Figure 13.**



**Figure 14.**

## APPLICATION INFORMATION

The TLV704xx series belong to a family of ultralow  $I_Q$  LDO regulators.  $I_Q$  remains fairly constant over the complete output load current and temperature range. The devices are ensured to operate over a temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

### INPUT AND OUTPUT CAPACITOR REQUIREMENTS

The TLV704 requires a  $1\text{-}\mu\text{F}$  or larger capacitor connected between OUT and GND for stability. Ceramic or tantalum capacitors can be used. Larger value capacitors result in better transient and noise performance.

Although an input capacitor is not required for stability, when a  $0.1\text{-}\mu\text{F}$  or larger capacitor is placed between IN and GND, it counteracts reactive input sources and improves transient and noise performance. Higher value capacitors are necessary if large, fast rise time load transients are anticipated.

### BOARD LAYOUT RECOMMENDATIONS

Input and output capacitors should be placed as close to the device pins as possible. To avoid interference of noise and ripple on the board, it is recommended that the board be designed with separate ground planes for  $V_{\text{IN}}$  and  $V_{\text{OUT}}$ , with the ground plane connected only at the device GND pin. In addition, the ground connection for the output capacitor should be connected directly to the device GND pin.

### POWER DISSIPATION AND JUNCTION TEMPERATURE

To ensure reliable operation, worst-case junction temperature should not exceed  $+125^{\circ}\text{C}$ . This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation,  $P_{\text{D(max)}}$ , and the actual dissipation,  $P_{\text{D}}$ , which must be less than or equal to  $P_{\text{D(max)}}$ .

The maximum power dissipation limit is determined using Equation 1:

$$P_{\text{D(max)}} = \frac{T_{\text{J max}} - T_{\text{A}}}{R_{\theta\text{JA}}} \quad (1)$$

where:

$T_{\text{J max}}$  is the maximum allowable junction temperature.

$R_{\theta\text{JA}}$  is the thermal resistance junction-to-ambient for the package (see the [Power Dissipation Rating](#) table).

$T_{\text{A}}$  is the ambient temperature.

The regulator dissipation is calculated using Equation 2:

$$P_{\text{D}} = (V_{\text{IN}} - V_{\text{OUT}}) \times I_{\text{OUT}} \quad (2)$$

Power dissipation resulting from quiescent current is negligible.

### REGULATOR PROTECTION

The TLV704xx series of LDO regulators use a PMOS-pass transistor that has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power-down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TLV704xx features internal current limiting. During normal operation, the TLV704xx limits output current to approximately 250 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. Take care not to exceed the rated maximum operating junction temperature of  $+125^{\circ}\text{C}$ . Continuously running the device under conditions where the junction temperature exceeds  $+125^{\circ}\text{C}$  degrades device reliability.

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC high-K boards are given in the [Power Dissipation Rating](#) table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heatsink effectiveness. Power dissipation depends on input voltage and load conditions. Power dissipation ( $P_{\text{D}}$ ) is equal to the product of the output current and the voltage drop across the output pass element, as shown in Equation 2.

### PACKAGE MOUNTING

Solder pad footprint recommendations for the TLV704xx are available from the Texas Instruments web site at [www.ti.com](http://www.ti.com) through the [TLV704 series product folders](#). The recommended land pattern for the DBV package is appended to this data sheet.

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (November, 2010) to Revision C	Page
• Revised document to reflect PK package option removal .....	1
• Removed SOT89 (PK) package from front-page figure .....	1
• Revised <i>Thermal Information</i> table and <i>Power Dissipation Rating</i> table .....	2
• Added load regulation specifications for $V_{OUT} \geq 3.3$ V .....	3
• Deleted PK package information from <i>Pin Descriptions</i> table .....	3
• Removed Figure 15 and Figure 16 .....	7

Changes from Revision A (October, 2010) to Revision B	Page
• Updated document to reflect availability of PK package option .....	1
• Corrected typo in front-page figure .....	1
• Changed <i>Pin Descriptions</i> table to correct pin numbering for PK package option .....	3
• Revised <i>Typical Characteristics</i> section; added and removed graphs .....	4
• Updated format of <i>Application Information</i> section .....	7
• Added <i>Package Mounting</i> section and .....	7



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TLV70430DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	QUQ	<a href="#">Samples</a>
TLV70430DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	QUQ	<a href="#">Samples</a>
TLV70433DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAO	<a href="#">Samples</a>
TLV70433DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAO	<a href="#">Samples</a>
TLV70436DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAW	<a href="#">Samples</a>
TLV70436DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAW	<a href="#">Samples</a>
TLV70450DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAX	<a href="#">Samples</a>
TLV70450DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAX	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV70430DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV70430DBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70433DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV70433DBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70436DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV70436DBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70450DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV70450DBVT	SOT-23	DBV	5	250	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV70430DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV70430DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV70433DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV70433DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV70436DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV70436DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV70450DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV70450DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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