

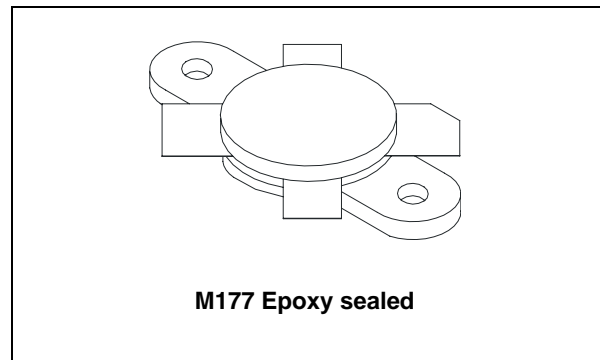
## HF/VHF/UHF RF power N-channel MOSFETs

### Features

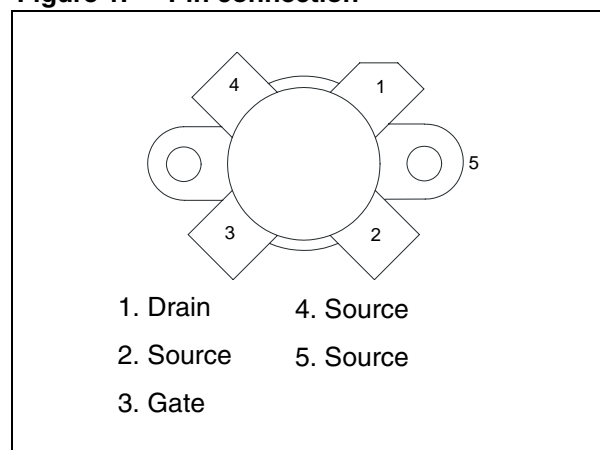
- High power capability
- $P_{OUT} = 350\text{ W}$  min. with 22dB gain @ 30 MHz
- $P_{SAT} = 450\text{ W}$
- Low  $R_{DS(on)}$
- Thermally enhanced packaging for lower junction temperatures
- Gold metallization
- Excellent thermal stability
- Common source configuration

### Description

The SD2943 is a gold metallized N-channel MOS field-effect RF power transistor. It is intended for use in 50 V dc large signal applications up to 150 MHz. The SD2943 offers a 20% higher power saturation than the SD2933, and is ideal for ISM applications where reliability and ruggedness are critical factors.



**Figure 1. Pin connection**



**Table 1. Device summary**

Order code	Marking	Base qty.	Package	Packaging <sup>(1)</sup>
SD2943W	SD2943 <sup>(1)</sup>	25 pcs	M177	Plastic tray

1. For more details please refer to [Chapter 7: Marking, packing and shipping specifications](#)..

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# 1 Electrical data

( $T_{CASE} = 25^{\circ}C$ )

**Table 2. Absolute maximum rating**

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}^{(1)}$	Drain source voltage	130	V
$V_{DGR}$	Drain-gate voltage ( $R_{GS} = 1M\Omega$ )	130	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current	40	A
$P_{DISS}$	Power dissipation	648	W
$T_j$	Max. operating junction temperature	200	$^{\circ}C$
$E_{AS}$	Avalanche energy, single pulse ( $I_D = 53A$ , $800\mu H$ coil)	1100	mJ
$T_{STG}$	Storage temperature	-65 to +150	$^{\circ}C$

1.  $T_j = 150^{\circ}C$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Junction to case thermal resistance	0.27	$^{\circ}C/W$

## 2 Electrical characteristics

( $T_{CASE} = 25^{\circ}C$ )

**Table 4. Static**

Symbol	Test conditions		Min.	Typ.	Max.	Unit
$V_{(BR)DSS}^{(1)}$	$V_{GS} = 0 V$	$I_{DS} = 200 mA$	130			V
$I_{DSS}$	$V_{GS} = 0 V$	$V_{DS} = 50 V$			200	$\mu A$
$I_{GSS}$	$V_{GS} = 20 V$	$V_{DS} = 0 V$			500	nA
$V_{GS(Q)}$	$V_{DS} = 10 V$	$I_D = 250 mA$	2		4	V
$V_{DS(ON)}$	$V_{GS} = 10 V$	$I_D = 20 A$			2	V
$G_{FS}^{(2)}$	$V_{DS} = 10 V$	$I_D = 10 A$	10			mho
$C_{ISS}$	$V_{GS} = 0 V$	$V_{DS} = 50 V$		830		pF
$C_{OSS}$	$V_{GS} = 0 V$	$V_{DS} = 50 V$		470		pF
$C_{RSS}$	$V_{GS} = 0 V$	$V_{DS} = 50 V$		35		pF

1.  $T_J = 150^{\circ}C$

2.  $G_{FS}$  sorts for each unit see [Table](#) .

**Table 5. Dynamic**

Symbol	Test conditions		Min.	Typ.	Max.	Unit
$P_{OUT}$	$V_{DD} = 50 V$	$I_{DQ} = 250 mA$ $f = 30 MHz$	350	450		W
$G_{PS}$	$V_{DD} = 50 V$	$I_{DQ} = 250 mA$ $P_{OUT} = 350 W$ $f = 30 MHz$	22	25		dB
$h_D$	$V_{DD} = 50 V$	$I_{DQ} = 250 mA$ $P_{OUT} = 350 W$ $f = 30 MHz$	60	65		%
Load Mismatch	$V_{DD} = 50 V$	$I_{DQ} = 250 mA$ $P_{OUT} = 350 W$ $f = 30 MHz$ All Phase Angles	3:1			VSWR

**Table 6.  $G_{FS}$  sorts**

Symbol	Value
A	10 ÷ 10.99
B	11 ÷ 11.99
C	12 ÷ 12.99
D	13 ÷ 13.99
E	14 ÷ 14.99
F	15 ÷ 15.99
G	16 ÷ 16.99
H	17 ÷ 18

### 3 Impedance

Figure 2. Impedance Data Schematic

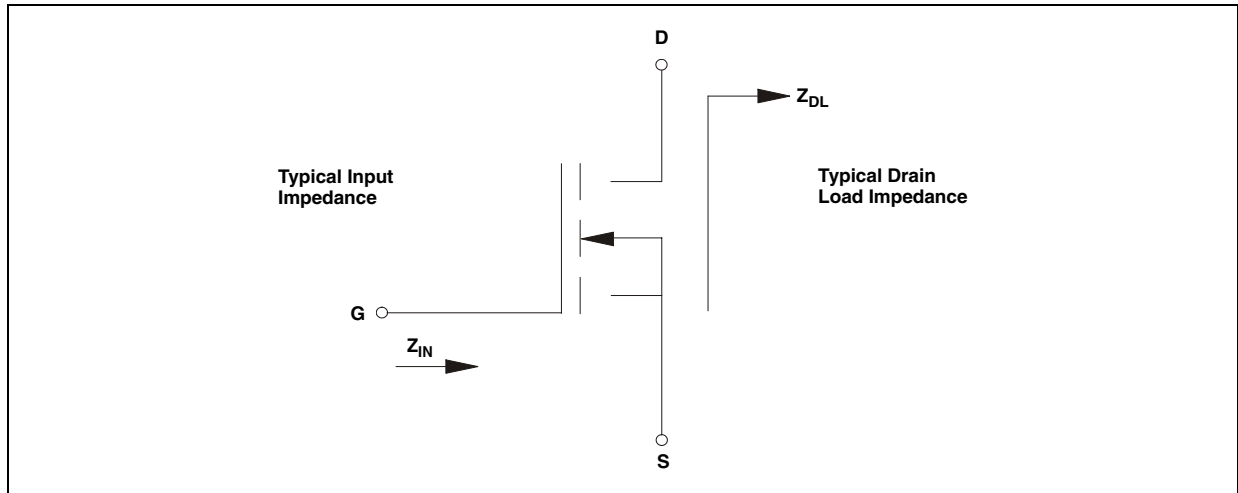
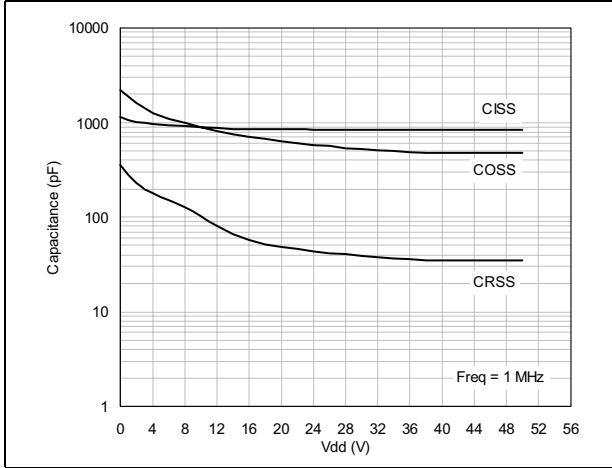


Table 7. Impedance data

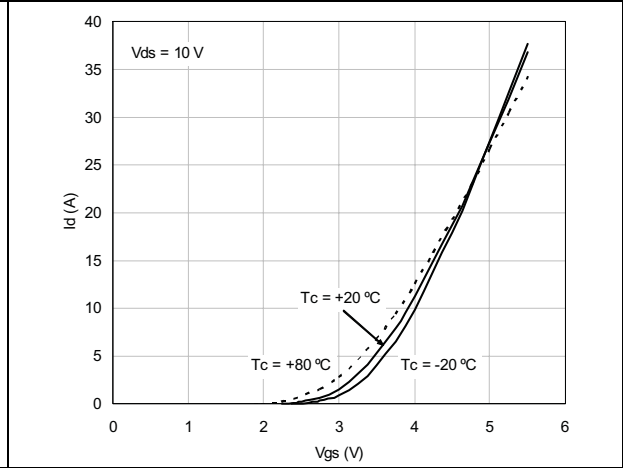
f	$Z_{IN}$ ( $\Omega$ )	$Z_{DL}$ ( $\Omega$ )
30 MHz	$1.3 - j 2.9$	$3.1 + j 2.3$
108 MHz	$1.4 - j 2.4$	$1.9 + j 1.4$
175 MHz	$1.4 - j 2.2$	$1.7 + j 1.6$

# 4 Typical performance

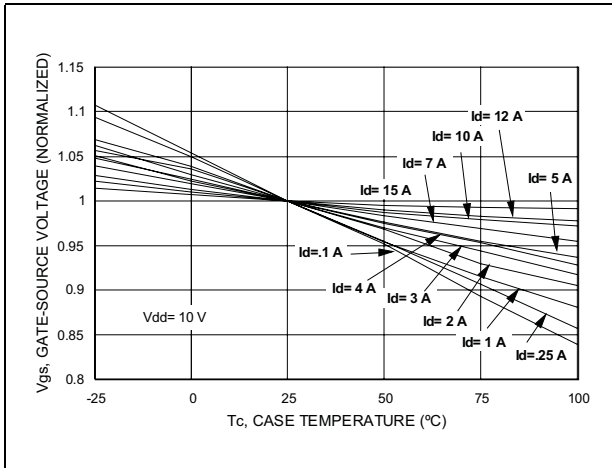
**Figure 3. Capacitance vs drain voltage**



**Figure 4. Drain current vs gate voltage**



**Figure 5. Gate-source voltage vs case temperature**



**Figure 6. Maximum thermal resistance vs. case temperature**

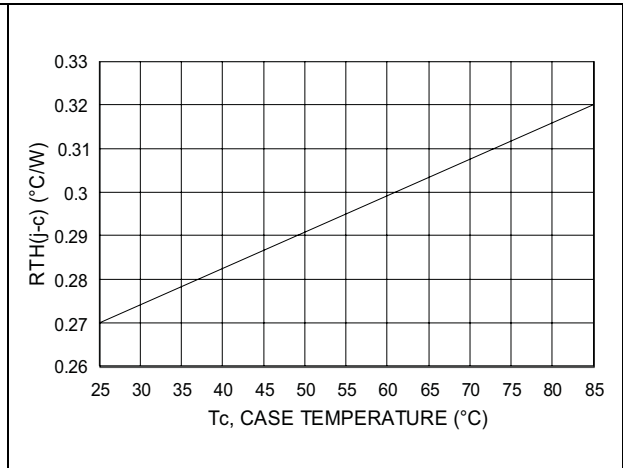


Figure 7. Output power vs input power

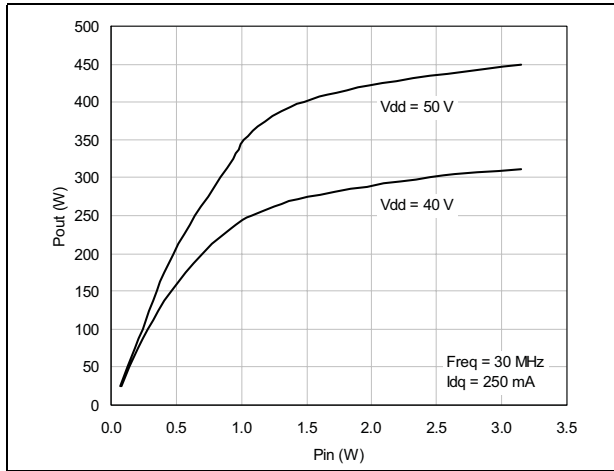


Figure 8. Output power vs input power (at different temperature)

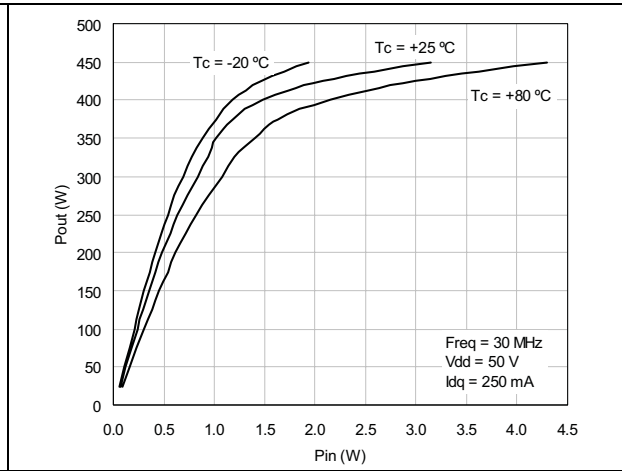


Figure 9. Power gain vs output power

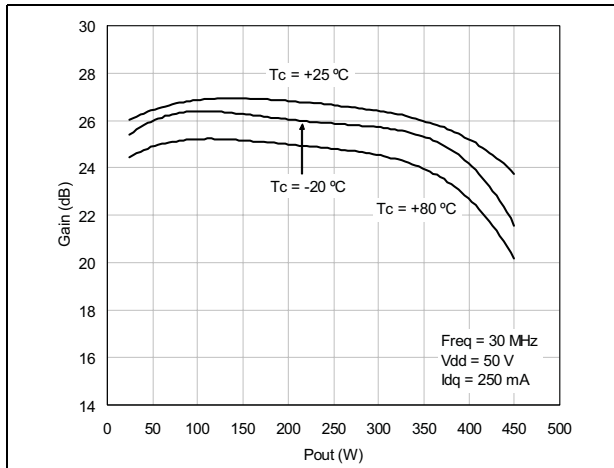


Figure 10. Efficiency vs output power

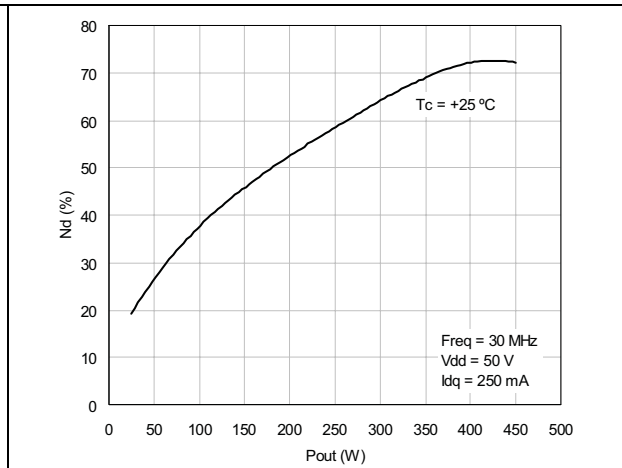


Figure 11. Output power vs supply voltage

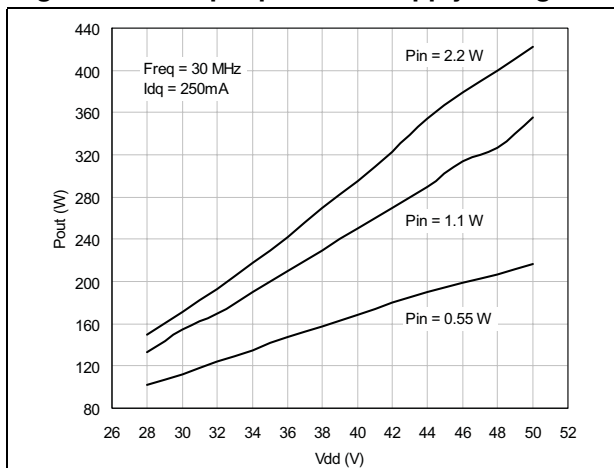
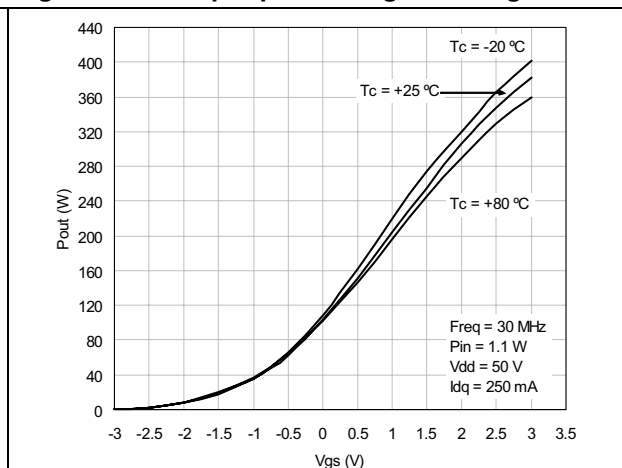
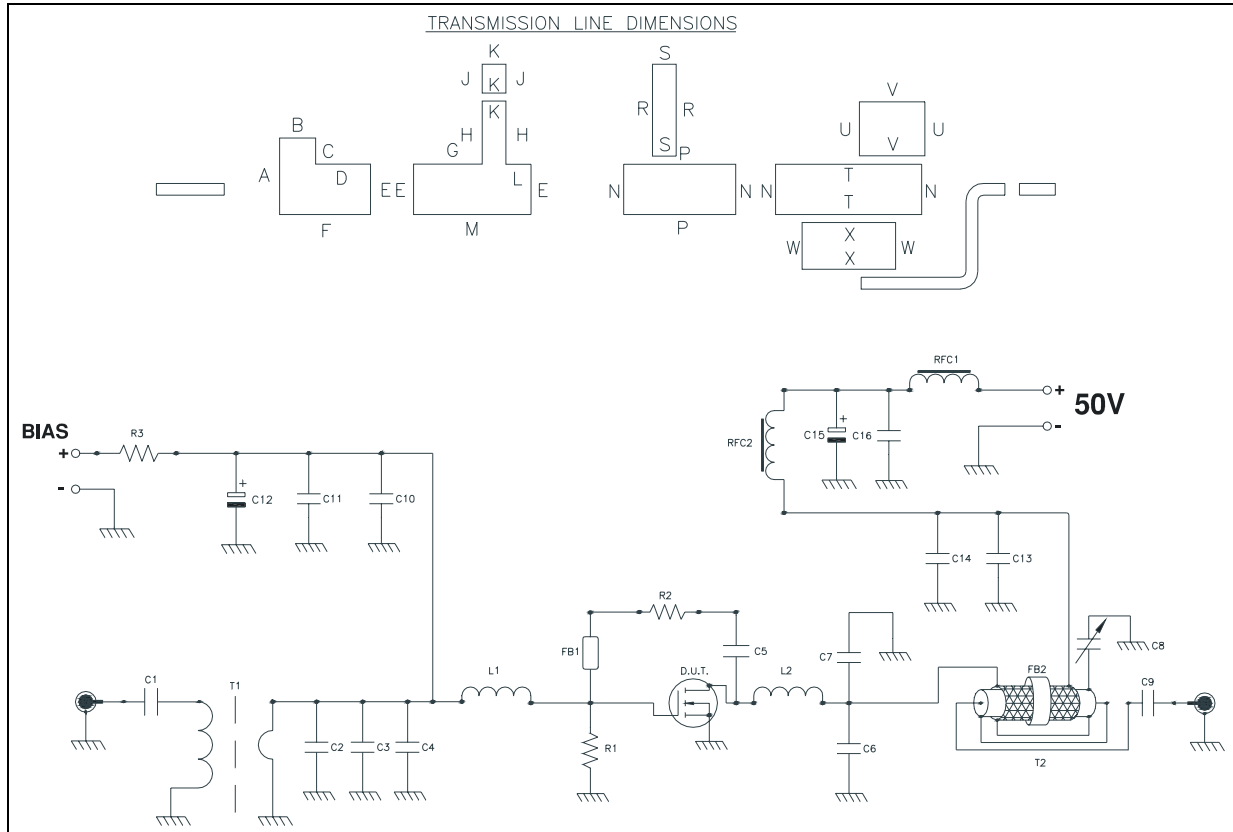


Figure 12. Output power vs gate voltage



## 5 Test Circuit

Figure 13. 30 MHz test circuit schematic



- Note:
- 1 Dimension at component symbol are reference for component placement.
  - 2 Gap between group and trasmission files are 0.056[1.42] typ.
  - 3 Transmission lime are not 1:1 scale.
  - 4 Input and output trasmission line are 50Ω

Table 8. 30 MHz test circuit component part list

Symbol	Description
C1,C9	0.01 μF / 500 V surface mount ceramic chip capacitor
C2, C3	750 pF ATC 700B surface mount ceramic chip capacitor
C4	300 pF ATC 700B surface mount ceramic chip capacitor
C5,C10,C11,C14,C16	10000 pF ATC 200B surface mount ceramic chip capacitor
C6	510 pF ATC 700B surface mount ceramic chip capacitor
C7	300 pF ATC 700B surface mount ceramic chip capacitor
C8	175-680 pF TYPE 46 standard trimmer capacitor
C12	47 μF / 63 V aluminum electrolytic radial lead capacitor



**Table 8. 30 MHz test circuit component part list (continued)**

Symbol	Description
C13	1200 pF ATC 700B surface mount ceramic chip capacitor
C15	100 $\mu$ F / 63 V aluminum electrolytic radial lead capacitor
R1,R3	1 K $\Omega$ 1 W surface mount chip resistor
R2	560 $\Omega$ 2 W wire-wound axils lead resistor
T1	HF 2-30 MHz surface mount 9:1 transformer
T2	RG - 142B/U 50 $\Omega$ coaxial cable OD = 0.165[4.18] L 15"[381.00] covered with 15"[381.00] tinned copper tubular brand 13/65" [5.1] width
L1	1 3/4 turn air-wound 16 AWG ID = 0.219 [5.56] poly-coated magnet wire
L2	1 3/4 turn air-wound 12 AWG ID = 0.250 [6.34] bus bar wire
RFC1,RFC2	3 turns 14 AWG wire through fair rite toroid
FB1	surface mount emi shield bead
FB2	toroid
PCB	ULTRALAM 2000. 0.030" THK, $\epsilon_r = 2.55$ , 2 Oz ED CU both sides

**Figure 14. 30 MHz test circuit photomaster**

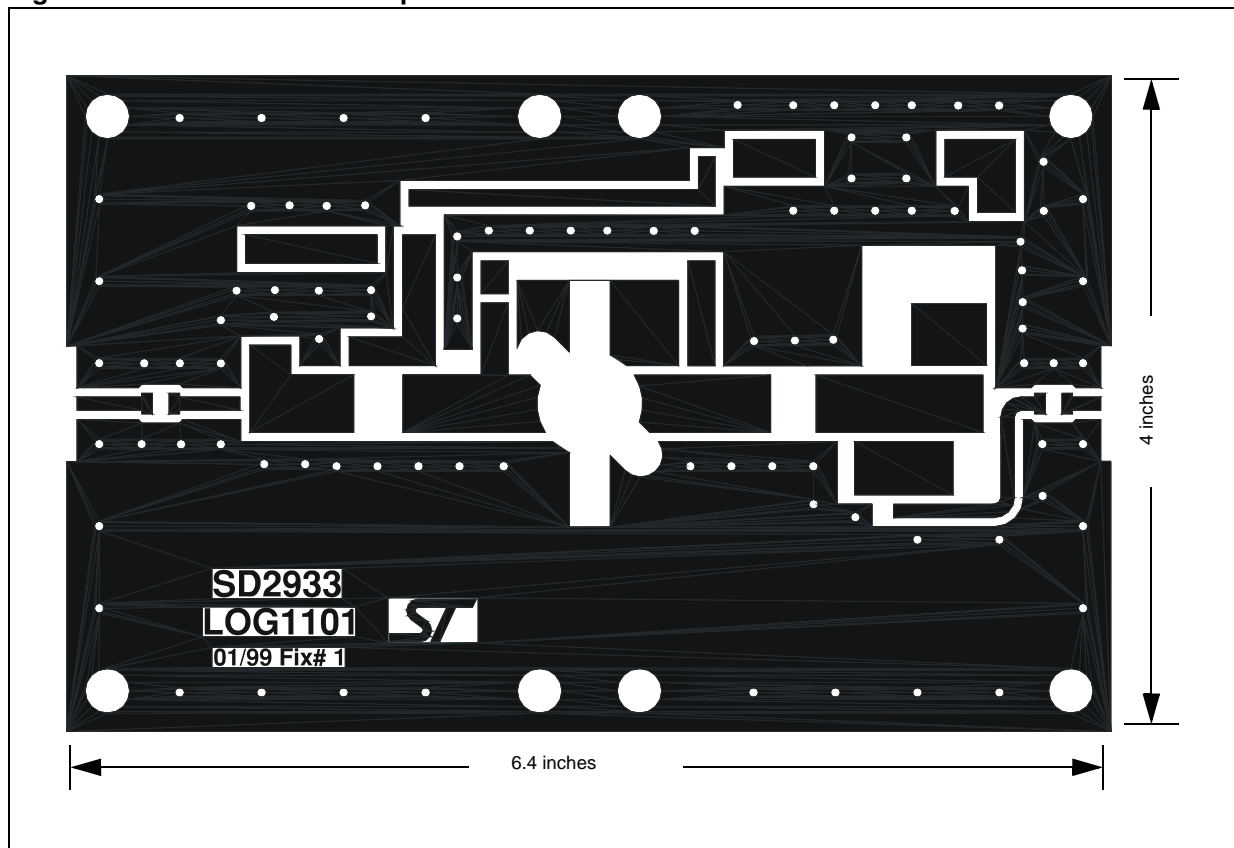
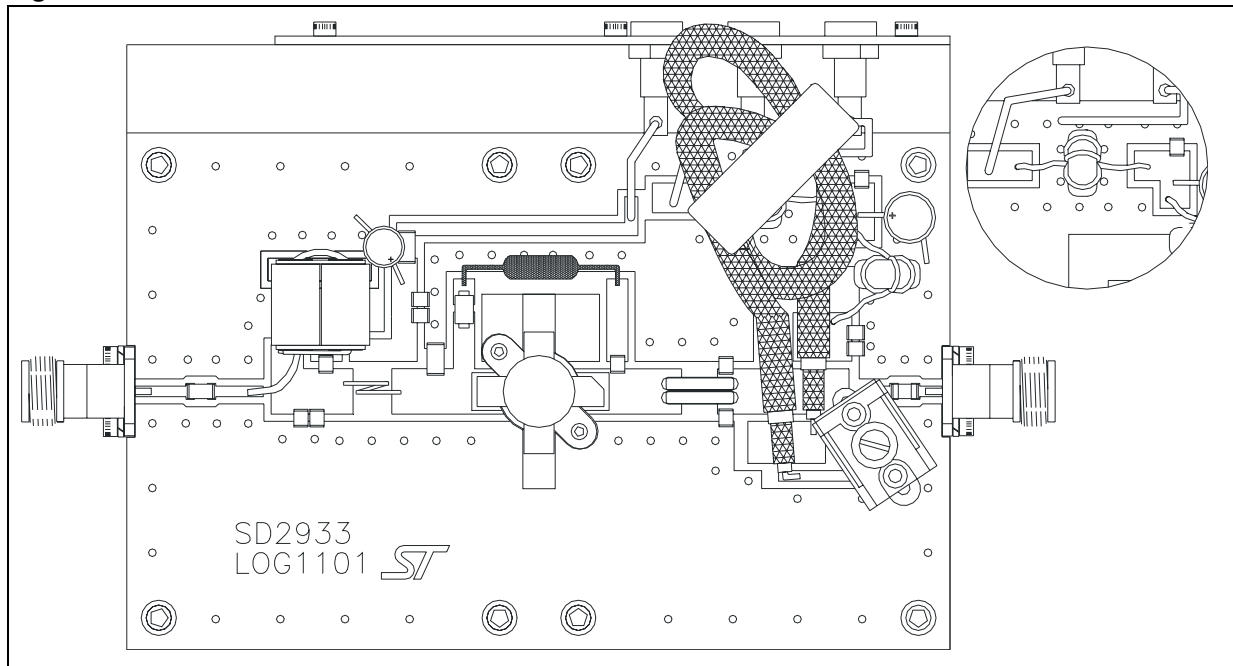


Figure 15. 30 MHz test circuit



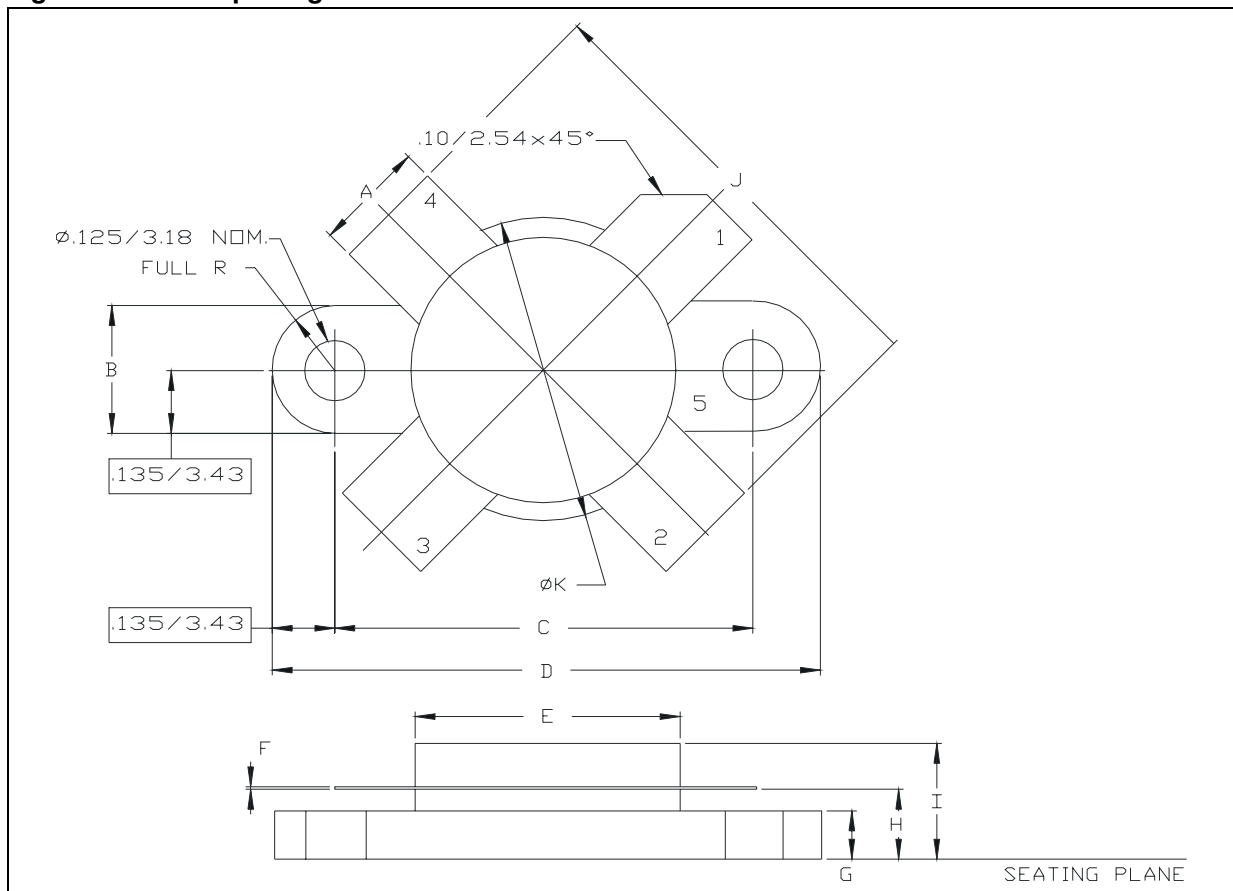
## 6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

**Table 9. M177 (.550 DIA 4/L N/HERM W/FLG)**

DIM.	mm.		inch			
	Min.	Typ	Max.	Min.	Typ	Max.
A	5.72		-	5.97	0.225	-
B	6.73	6.96		0.265	0.275	
C	21.84	22.10		0.860	0.870	
D	28.70	28.96		1.130	1.140	
E	13.84	14.10		0.545	0.555	
F	0.08	0.18		0.003	0.007	
G	2.49	2.74		0.098	0.108	
H	3.81	4.32		0.150	0.170	
I		7.11			0.280	
J	27.43	28.45		1.080	1.120	
K	15.88	16.13		0.625	0.635	

Figure 16. M177 package dimensions

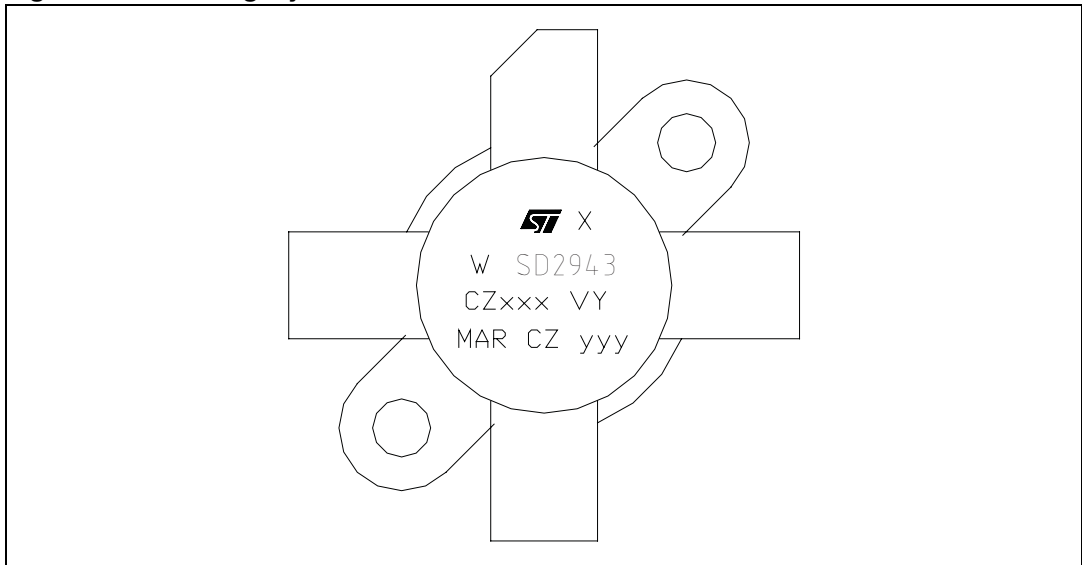


## 7 Marking, packing and shipping specifications

**Table 10. Packing and shipping specifications**

Order code	Packaging	Pcs per tray	Dry pack humidity	GFS code	Lot code
SD2943W	Plastic tray	25	< 10 %	Not mixed	Not mixed

**Figure 17. Marking layout**



**Table 11. Marking specifications**

Symbol	Description
W	Wafer process code
X	G <sub>FS</sub> sort
CZ	Assy plant
xxx	Last 3 digit of diffusion lot
VY	Diffusion plant
MAR	Country of origin
CZ	Test and finishing plant
y	Assy year
yy	Assy week

## 8 Revision history

**Table 12. Document revision history**

Date	Revision	Description of Changes
18-Oct-2005	1	First Issue.
04-Jan-2006	2	Complete version
24-Aug-2011	3	Inserted <i>Chapter 7: Marking, packing and shipping specifications</i> . Minor text changes.

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