KAF-0402

768 (H) x 512 (V) Full Frame CCD Image Sensor

ON Semiconductor®

www.onsemi.com

Description

The KAF−0402 Image Sensor is a high performance area CCD (charge-coupled device) image sensor with 768 (H) × 512 (V) photoactive pixels designed for a wide range of image sensing applications.

The sensor incorporates true two-phase CCD technology, simplifying the support circuits required to drive the sensor as well as reducing dark current without compromising charge capacity. The sensor also utilizes the TRUESENSE Transparent Gate Electrode to improve sensitivity compared to the use of a standard front side illuminated polysilicon electrode.

Optional microlenses focus the majority of the light through the transparent gate, increasing the optical response further.

Table 1. GENERAL SPECIFICATIONS

Parameter	Typical Value
Architecture	Full Frame CCD, Enhanced Response
Total Number of Pixels	784 (H) × 520 (V)
Number of Active Pixels	768 (H) × 512 (V) = approx. 0.4 Mp
Pixel Size	9.0 μm (H) × 9.0 μm (V)
Active Image Size	6.91 mm (H) × 4.6 mm (V) 8.3 mm (Diagonal) 1/2″ Optical Format
Die Size	8.4 mm (H) × 5.5 mm (V)
Aspect Ratio	3:2
Saturation Signal	100,000 electrons
Quantum Efficiency (with Microlens)	Peak: 77% 400 nm: 45%
Quantum Efficiency (No Microlens)	Peak: 65% 400 nm: 30%
Output Sensitivity	10 μV/e^-
Read Noise	15 electrons
Dark Current	< 10 pA/cm^2 at 25°C
Dark Current Doubling Temperature	6.3°C
Dynamic Range	76 dB
Charge Transfer Efficiency	> 0.99999
Blooming Suppression	None
Maximum Date Rate	10 MHz
Package	CERDIP Package (Sidebrazed)
Cover Glass	Clear or AR Coated, 2 Sides

NOTE: Parameters above are specified at T = 25°C unless otherwise noted.

Figure 1. KAF−0402 Full Frame CCD Image Sensor

Applications

- Digitization
- Medical
- Scientific

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Table 2. ORDERING INFORMATION − KAF−0402 IMAGE SENSOR

Part Number	Description	Marking Code
KAF−0402−AAA−CB−B1	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass (No Coatings), Grade 1	KAF−0402−AAA Serial Number
KAF−0402−AAA−CB−AE	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass (No Coatings), Engineering Sample	
KAF−0402−AAA−CP−B1	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass (No Coatings), Grade 1	
KAF−0402−AAA−CP−B2	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass (No Coatings), Grade 2	
KAF−0402−AAA−CP−AE	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass (No Coatings), Engineering Sample	
KAF−0402−ABA−CD−B1	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coating (Both Sides), Grade 1	KAF−0402−ABA Serial Number
KAF−0402−ABA−CD−B2	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coating (Both Sides), Grade 2	
KAF−0402−ABA−CD−AE	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coating (Both Sides), Engineering Sample	
KAF−0402−ABA−CP−B1	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass (No Coatings), Grade 1	
KAF−0402−ABA−CP−B2	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass (No Coatings), Grade 2	
KAF−0402−ABA−CP−AE	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass (No Coatings), Engineering Sample	

Table 3. ORDERING INFORMATION − EVALUATION SUPPORT

Part Number	Description
KAF−0402−12−5−A−EVK	Evaluation Board (Complete Kit)

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

DEVICE DESCRIPTION

Architecture

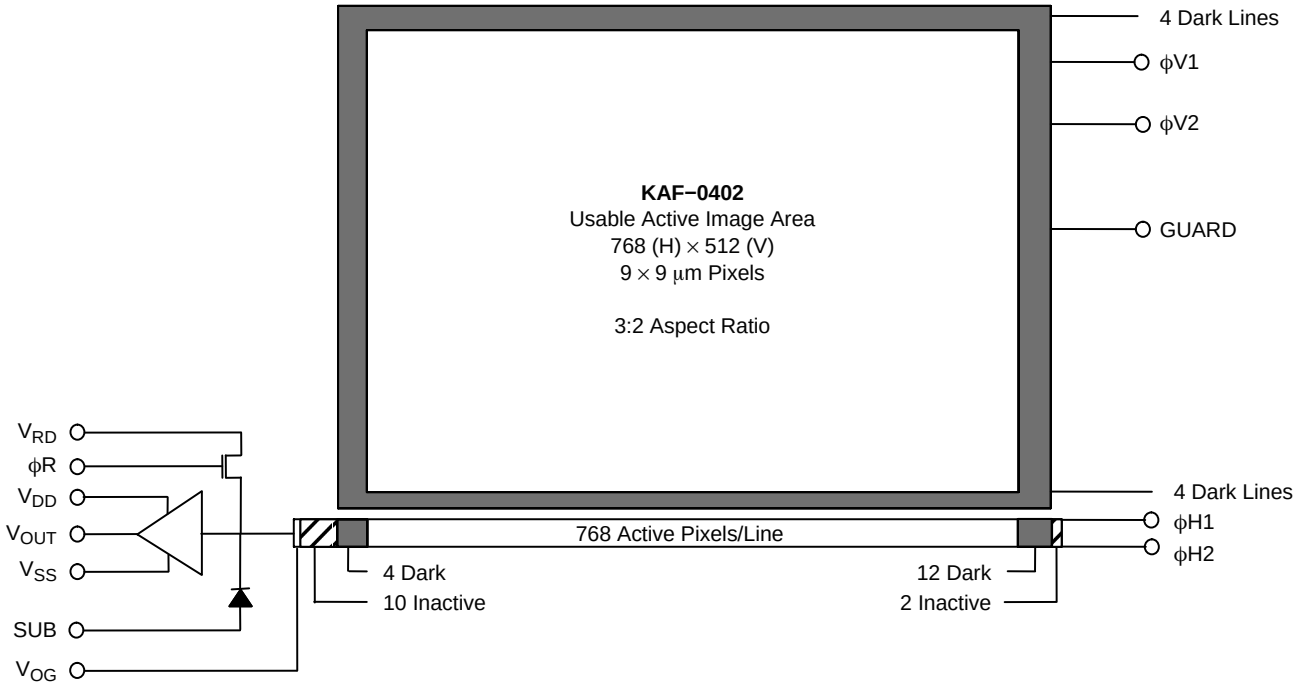


Figure 2. Block Diagram

The sensor consists of 784 parallel (vertical) CCD shift registers each 520 elements long. These registers act as both the photosensitive elements and as the transport circuits that allow the image to be sequentially read out of the sensor. The parallel (vertical) CCD registers transfer the image one line at a time into a single 796-element (horizontal) CCD shift register. The horizontal register transfers the charge to a single output amplifier. The output amplifier is a two-stage source follower that converts the photo-generated charge to a voltage for each pixel.

Microlenses

Microlenses are formed along each row. They are effectively half of a cylinder centered on the transparent gates, extending continuously in the row direction. They act to direct the photons away from the polysilicon gate and through the transparent gate. This increases the response, especially at the shorter wavelengths (< 600 nm).

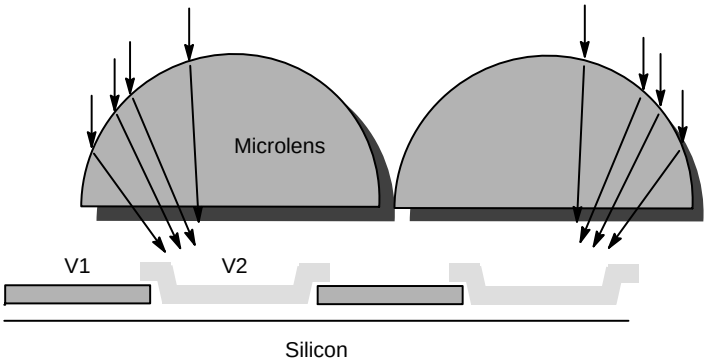


Figure 3. Microlens

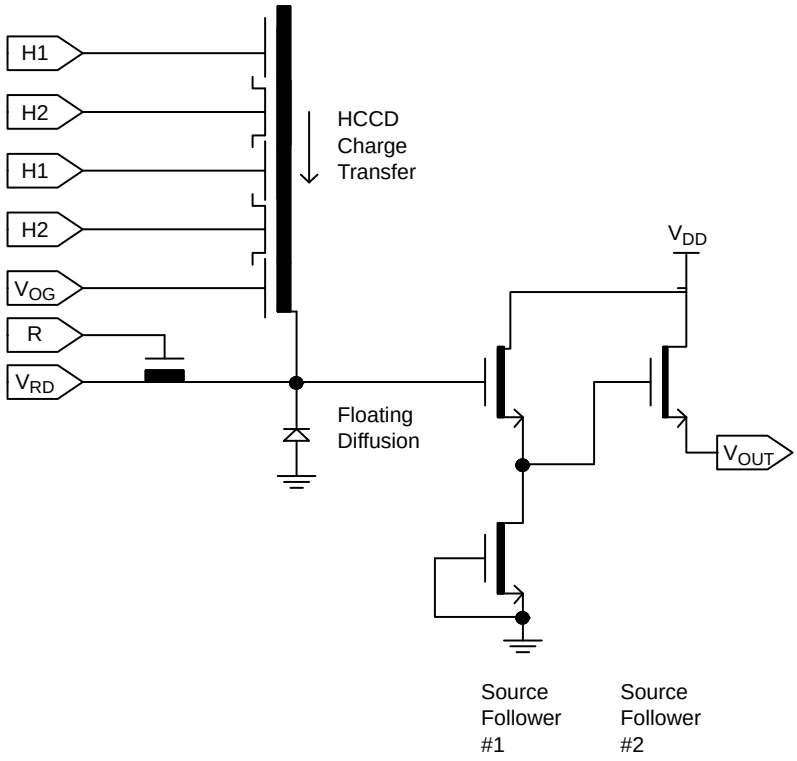


Figure 4. Output Schematic

Output Structure

Charge presented to the floating diffusion is converted into a voltage and current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the floating diffusion. Once the signal has been sampled by the system electronics, the reset gate (ϕR) is clocked to remove the signal and the floating diffusion is reset to the potential applied by Vrd (see Figure 4). More signal at the floating diffusion reduces the voltage seen at the output pin. In order to activate the output structure, an off-chip load must be added to the Vout pin of the device such as shown in Figure 8.

Dark Reference Pixels

There are 4 light shielded pixels at the beginning of each line, and 12 at the end. There are 4 dark lines at the start of every frame and 4 dark lines at the end of each frame. Under normal circumstances, these pixels do not respond to light. However, dark reference pixels in close proximity to an active pixel can scavenge signal depending on light intensity and wavelength and therefore will not represent the true dark signal.

Dummy Pixels

Within the horizontal shift register are 10 leading additional pixels that are not associated with a column of pixels within the vertical register. These pixels contain only horizontal shift register dark current signal and do not respond to light. A few leading dummy pixels may scavenge false signal depending on operating conditions. There are two more dummy pixels at the end of each line.

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the sensor. These photon induced electrons are collected locally by the formation of potential wells at each photogate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons will leak into the adjacent pixels within the same column. This is termed blooming. During the integration period, the ϕV1 and ϕV2 register clocks are held at a constant (low) level. See Figure 9.

Charge Transport

Referring again to Figure 10, the integrated charge from each photogate is transported to the output using a two-step process. Each line (row) of charge is first transported from the vertical CCD to the horizontal CCD register using the ϕV1 and ϕV2 register clocks. The horizontal CCD is presented a new line on the falling edge of ϕV2 while ϕH1 is held high. The horizontal CCD then transports each line, pixel by pixel, to the output structure by alternately clocking the ϕH1 and ϕH2 pins in a complementary fashion. On each falling edge of ϕH2 a new charge packet is transferred onto a floating diffusion and sensed by the output amplifier.

Physical Description

Pin Description and Device Orientation

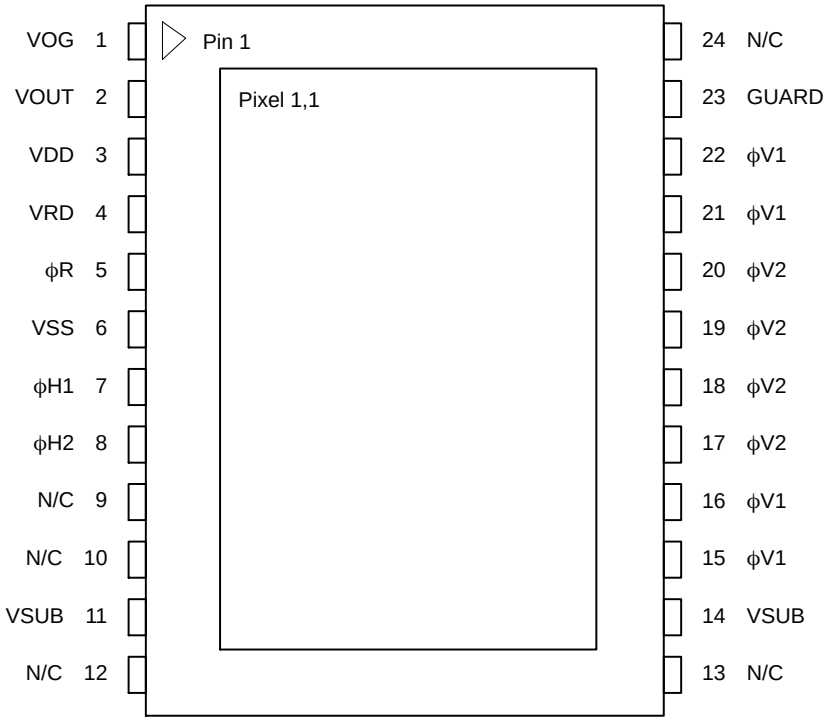


Figure 5. Pinout Diagram

Table 4. PIN DESCRIPTION

Pin	Name	Description
1	VOG	Output Gate
2	VOUT	Video Output
3	VDD	Amplifier Supply
4	VRD	Reset Drain
5	ϕR	Reset Clock
6	VSS	Amplifier Supply Return
7	ϕH1	Horizontal CCD Clock − Phase 1
8	ϕH2	Horizontal CCD Clock − Phase 2
9	N/C	No Connection
10	N/C	No Connection
11	VSUB	Substrate
12	N/C	No Connection

Pin	Name	Description
13	N/C	No Connection
14	VSUB	Substrate
15	ϕV1	Vertical CCD Clock − Phase 1
16	ϕV1	Vertical CCD Clock − Phase 1
17	ϕV2	Vertical CCD Clock − Phase 2
18	ϕV2	Vertical CCD Clock − Phase 2
19	ϕV2	Vertical CCD Clock − Phase 2
20	ϕV2	Vertical CCD Clock − Phase 2
21	ϕV1	Vertical CCD Clock − Phase 1
22	ϕV1	Vertical CCD Clock − Phase 1
23	GUARD	Guard Ring
24	N/C	No Connection

IMAGING PERFORMANCE

Specifications

Electro-Optical

All values measured at 25°C and nominal operating conditions. These parameters exclude defective pixels.

Table 5. SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max.	Units	Notes	Verification Plan
Saturation Signal Vertical CCD Capacity Horizontal CCD Capacity Output Node Capacity	N_{SAT}	 85,000 170,000 190,000	 100,000 200,000 220,000	 − 240,000 −	e^-/pix	1	Design[9]
Quantum Efficiency (see Figure 6)		−	−	−			Design[9]
Photoresponse Non-Linearity	PRNL	−	1.0	2.0	%	2	
Photoresponse Non-Uniformity	PRNU	−	0.8	−	%	3	Die[8]
Dark Signal	J_{DARK}	− −	15 6	30 10	e^-/pix/sec pA/cm^2	4	Die[8]
Dark Signal Doubling Temperature		−	6.3	7	°C		Design[9]
Dark Signal Non-Uniformity	DSNU	−	15	30	e^-/pix/sec	5	Die[8]
Dynamic Range	DR	72	76	−	dB	6	Design[9]
Charge Transfer Efficiency	CTE	0.99997	0.99999	−			Die[8]
Output Amplifier DC Offset	V_{ODC}	V_{RD}	V_{RD} + 0.5	V_{RD} + 1.0	V		Design[9]
Output Amplifier Sensitivity	V_{OUT}/N_{e^-}	9	10	−	$\mu V/e^-$		Design[9]
Output Amplifier Output Impedance	Z_{OUT}	180	200	220	Ω		Design[9]
Noise Floor	n_{e^-}	−	15	20	electrons	7	

1. For pixel binning applications, electron capacity up to 330,000 can be achieved with modified CCD inputs.
2. Worst case deviation from straight line fit, between 2% and 90% of V_{SAT}.
3. One Sigma deviation of a 128 × 128 sample when CCD illuminated uniformly at half of saturation.
4. Average of all pixels with no illumination at 25°C.
5. Average dark signal of any of 11 × 8 blocks within the sensor (each block is 128 × 128 pixels).
6. 20LOG (N_{SAT} / n_{e^-}) at nominal operating frequency and 25°C.
7. Noise floor is specified at the nominal pixel frequency and excludes any dark or pattern noises. It is dominated by the output amplifier power spectrum with a bandwidth = 5 · pixel rate.
8. A parameter that is measured on every sensor during production testing.
9. A parameter that is quantified during the design verification activity.

TYPICAL PERFORMANCE CURVES

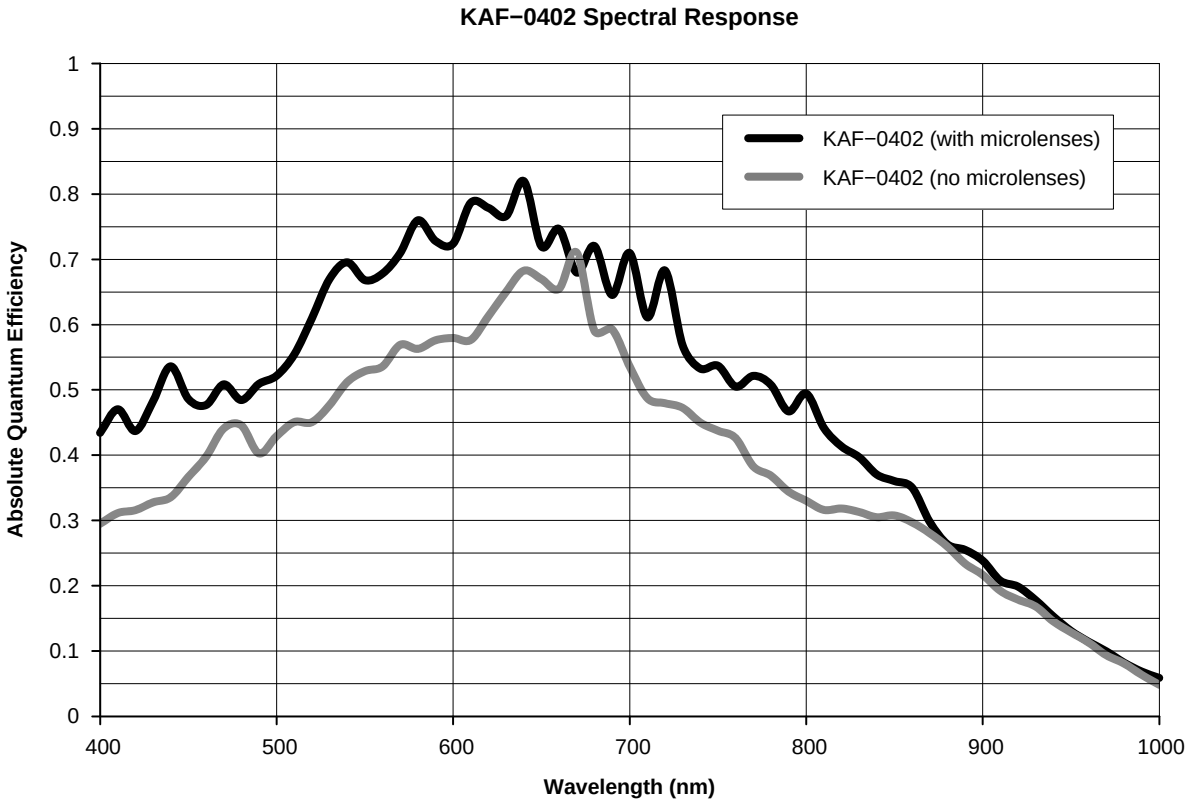


Figure 6. Typical Spectral Response

DEFECT DEFINITIONS

Table 6. SPECIFICATIONS (Defect tests performed at T = 25°C)

Grade	Point Defect	Cluster Defect	Column Defect
C1	< 5	0	0
C2	< 10	< 4	0

Point Defects

Dark: A pixel which deviates by more than 6% from neighboring pixels when illuminated to 70% of saturation.

Bright: A pixel whose dark current > 5,000 e^-/pix/sec at 25°C.

Cluster Defect

A grouping of not more than 5 adjacent point defects.

Column Defect

A grouping of > 5 contiguous point defects along a single column.

A column containing a pixel with dark current > 12,000 e^-/pix/sec at 25°C (Bright column).

A column that does not meet the minimum vertical CCD charge capacity (Low charge capacity column).

A column that loses > 250 e^- under 2 ke^- (Trap defect).

Neighboring Pixels

The surrounding 128 × 128 pixels or ±64 columns/rows.

Defect Separation

Column and cluster defects are separated by no less than 2 pixels in any direction (excluding single pixel defects).

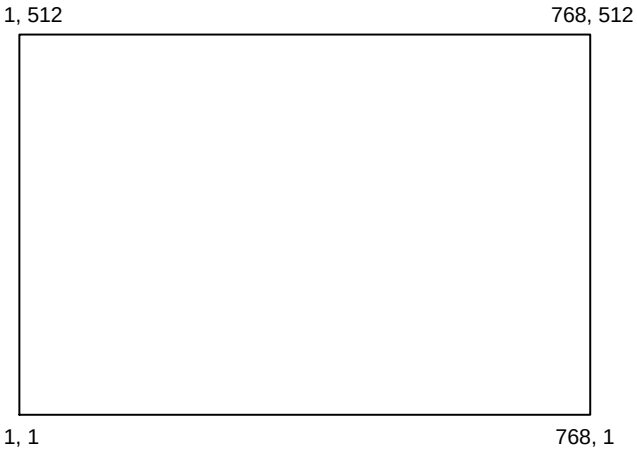


Figure 7. Active Pixel Region

OPERATION

Table 7. ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Units	Notes
Diode Pin Voltages	V_{DIODE}	0	20	V	1, 2
Gate Pin Voltages	V_{GATE1}	−16	16	V	1, 3, 5
Output Bias Current	I_{OUT}	−	−10	mA	4
Output Load Capacitance	C_{LOAD}	−	15	pF	4

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Referenced to pin VSUB or between each pin in this group.
2. Includes pins: VRD, VDD, VSS, VOUT.
3. Includes pins: ϕV1, ϕV2, ϕH1, ϕH2, VOG, VLG, ϕR.
4. Avoid shorting output pins to ground or any low impedance source during operation.
5. This sensor contains gate protection circuits to provide some protection against ESD events. The circuits will turn on when greater than 16 V appears between any two gate pins. Permanent damage can result if excessive current is allowed to flow under these conditions.

Table 8. DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Reset Drain	V_{RD}	10	11.0	11.5	V	0.01	
Output Amplifier Return	V_{SS}	1.5	2.0	2.5	V	−0.5	
Output Amplifier Supply	V_{DD}	14.75	15	15.5	V	I_{OUT}	
Substrate	V_{SUB}	0	0	0	V	0.01	
Output Gate	V_{OG}	3.75	4	5	V	0.01	
Guard Ring	GUARD	8.0	9.0	12.0	V	0.01	
Video Output Current	I_{OUT}	−	−5	−10	mA	−	1

1. An output load sink must be applied to V_{OUT} to activate output amplifier − see Figure 8.

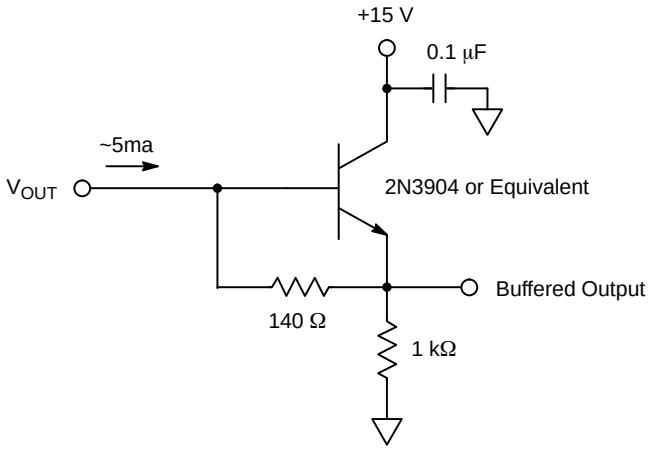


Figure 8. Example Output Structure Load Diagram

AC Operating Conditions

Table 9. CLOCK LEVELS

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Effective Capacitance
Vertical CCD Clock − Phase 1	ϕV1	Low	−10.5	−10	−9.5	V	6 nF (All ϕV1 Pins)
Vertical CCD Clock − Phase 1	ϕV1	High	−0.5	0	1.0	V	6 nF (All ϕV1 Pins)
Vertical CCD Clock − Phase 2	ϕV2	Low	−10.5	−10.0	−9.5	V	6 nF (All ϕV2 Pins)
Vertical CCD Clock − Phase 2	ϕV2	High	−0.5	0	1.0	V	6 nF (All ϕV2 Pins)
Horizontal CCD Clock − Phase 1	ϕH1	Low	−4.5	−4.0	−3.5	V	50 pF
Horizontal CCD Clock − Phase 1	ϕH1	Amplitude	9.5	10.0	10.5	V	50 pF
Horizontal CCD Clock − Phase 2	ϕH2	Low	−4.5	−4.0	−3.5	V	50 pF
Horizontal CCD Clock − Phase 2	ϕH2	Amplitude	9.5	10.0	10.5	V	50 pF
Reset Clock	ϕR	Low	−3.0	−2.0	−1.75	V	5 pF
Reset Clock	ϕR	Amplitude	5.0	6.0	7.0	V	5 pF

1. All pins draw less than 10 μA DC current.
2. Capacitance values relative to V_{SUB}.

TIMING

Table 10. REQUIREMENTS AND CHARACTERISTICS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
ϕH1, ϕH2 Clock Frequency	f_H	−	4	10	MHz	1, 2, 3
Pixel Period (1 Count)	t_{PIX}	100	250	−	ns	
ϕH1, ϕH2 Set-up Time	$t_{\phi HS}$	0.5	1	−	μs	
ϕV1, ϕV2 Clock Pulse Width	$t_{\phi V}$	1.5	2	−	μs	2
Reset Clock Pulse Width	$t_{\phi R}$	10	20	−	ns	4
Readout Time	$t_{READOUT}$	43.7	107	−	ms	5
Integration Time	t_{INT}	−	−	−		6
Line Time	t_{LINE}	84.1	206	−	μs	7

1. 50% duty cycle values.
2. CTE may degrade above the nominal frequency.
3. Rise and fall times (10/90% levels) should be limited to 5−10% of clock period. Crossover of register clocks should be between 40−60% of amplitude.
4. ϕR should be clocked continuously.
5. $t_{READOUT} = (520 \cdot t_{LINE})$
6. Integration time (t_{INT}) is user specified. Longer integration times will degrade noise performance due to dark signal fixed pattern and shot noise.
7. $t_{LINE} = (3 \cdot t_{\phi V}) + t_{\phi HS} + (796 \cdot t_{PIX}) + t_{PIX}$

Frame Timing

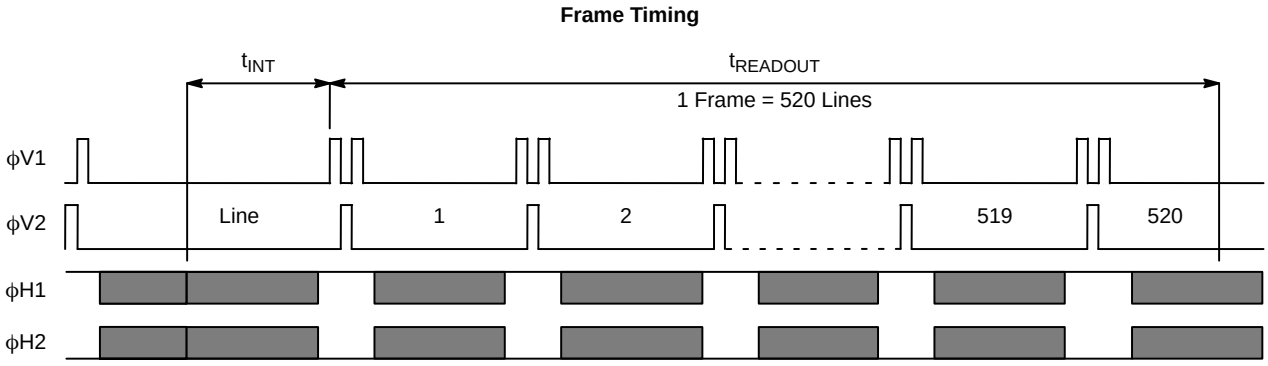
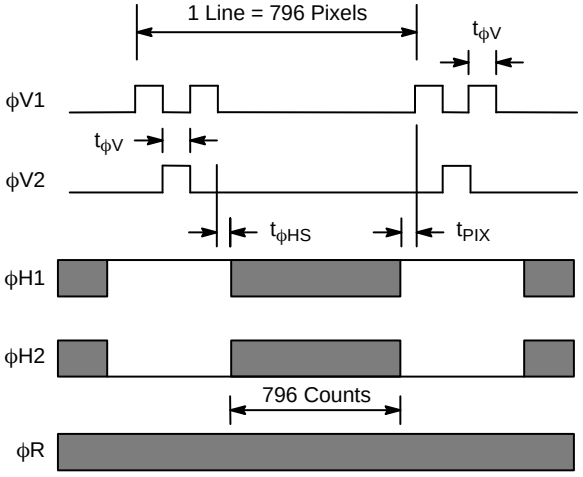


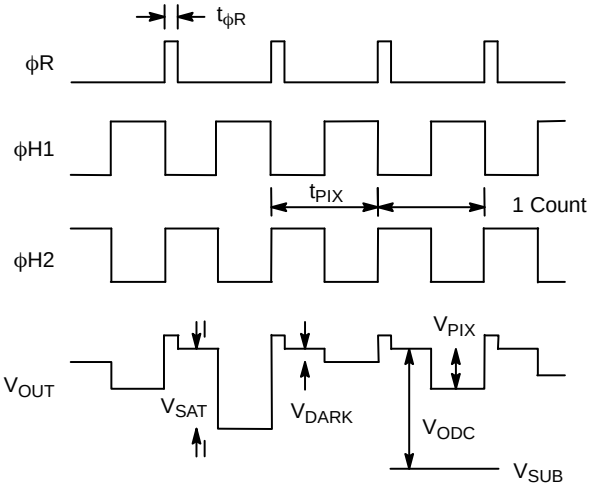
Figure 9. Frame Timing Diagram

Line Timing and Pixel Timing

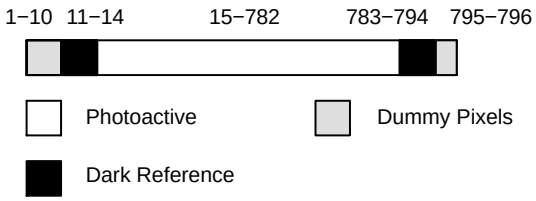
Line Timing Detail



Pixel Timing Detail



Line Content



V_{SAT}	Saturated pixel video output signal
V_{DARK}	Video output signal in no-light situation, not zero due to J_{DARK}
V_{PIX}	Pixel video output signal level, more electrons = more negative
V_{ODC}	Video level offset with respect to V_{SUB}*
V_{SUB}	Analog ground

* See Image Acquisition section.

Figure 10. Line and Pixel Timing Diagrams

STORAGE AND HANDLING

Table 11. STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	−	100	°C	
Humidity	RH	5	90	%	1

1. T = 25°C. Excessive humidity will degrade MTTF.

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from www.onsemi.com.

For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

MECHANICAL INFORMATION

Completed Assembly

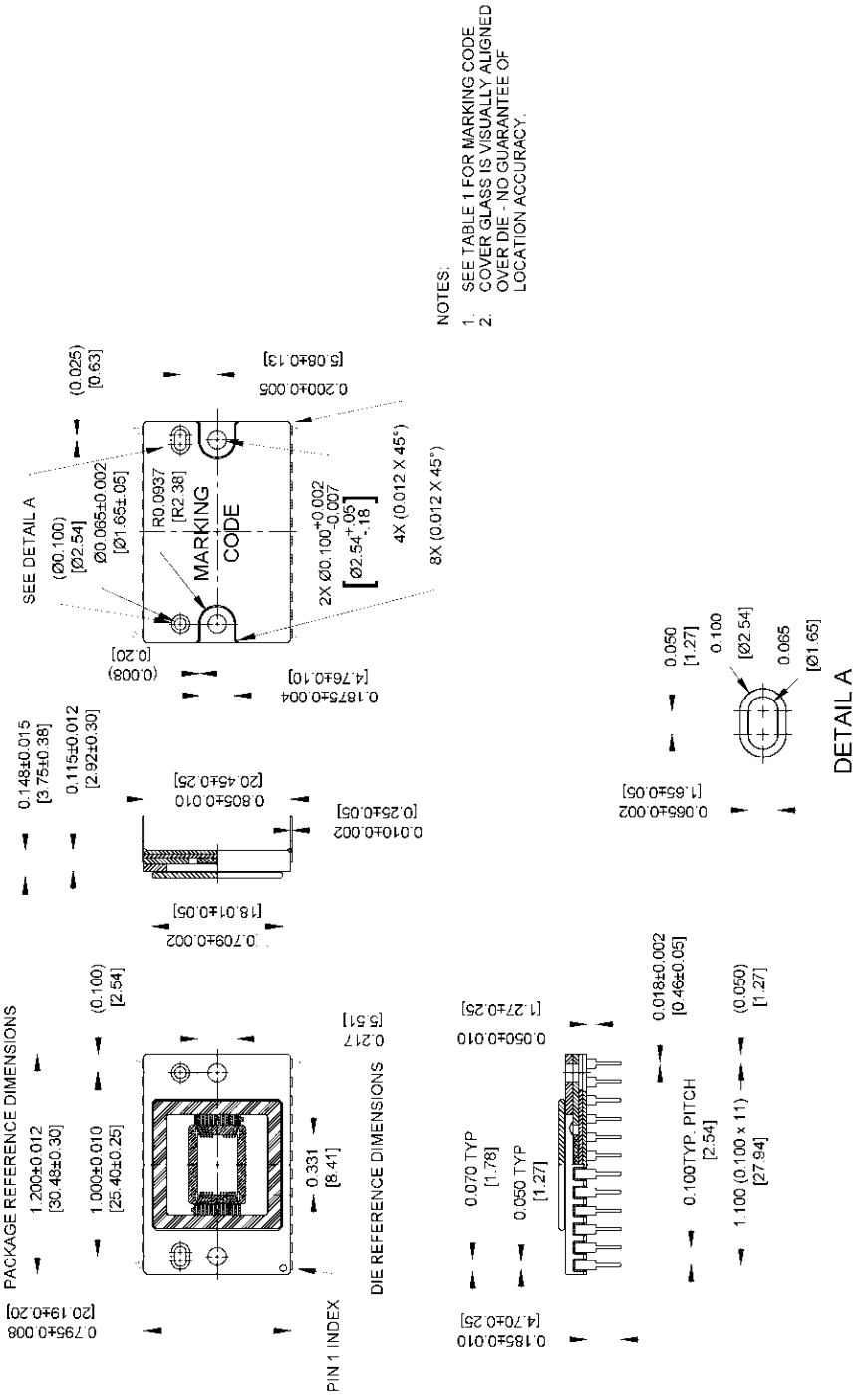


Figure 11. Completed Assembly (1 of 2)

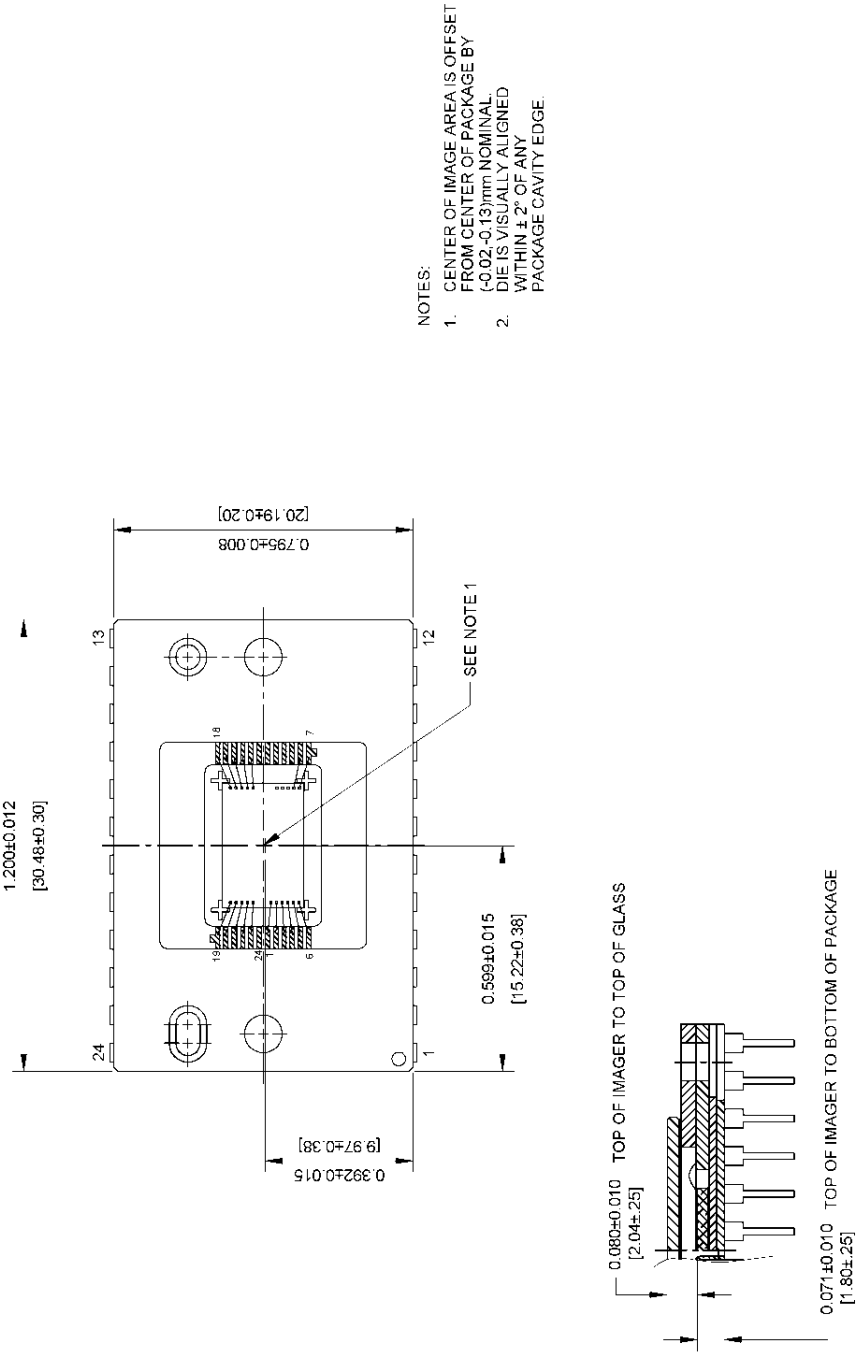


Figure 12. Completed Assembly (2 of 2)

PUBLICATION ORDERING INFORMATION

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Email: orderlit@onsemi.com

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