STD840DN40

Dual NPN high voltage transistors in a single package

Datasheet — production data

Features

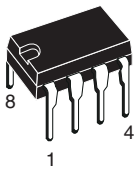
- Low $V_{CE(sat)}$
- Simplified circuit design
- Reduced component count
- Fast switching speed

Applications

- Compact fluorescent lamp (CFL) 220 V mains
- Electronic ballast for fluorescent lighting

Description

This device is a dual NPN high voltage power transistor manufactured using multi-epitaxial planar technology. It is housed in a dual-island DIP-8 package, with separated terminals for a high degree of mounting flexibility.



DIP-8

Figure 1. Internal schematic diagram

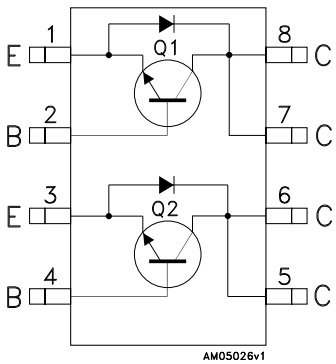


Table 1. Device summary

Order code	Marking	Package	Packaging
STD840DN40	D840DN40	DIP-8	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-base voltage (I_E = 0)	700	V
V_{CEO}	Collector-emitter voltage (I_B = 0)	400	V
V_{EBO}	Emitter-base voltage (I_C = 0, I_B = 1.5 A, t_p < 10 ms)	$V_{(BR)EBO}$	V
I_C	Collector current	4	A
I_{CM}	Collector peak current (t_P < 5 ms)	8	A
I_B	Base current	1.5	A
I_{BM}	Base peak current (t_P < 5 ms)	3	A
P_{TOT}	Total dissipation at T_{amb} = 25 °C single transistor	3	W
	Total dissipation at T_{case} = 25 °C single transistor	45	W
T_{STG}	Storage temperature	-65 to 150	°C
T_J	Max. operating junction temperature	150	°C

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA} (1)	Thermal resistance junction-ambient (single transistor)	42	°C/W
R_{thJC}	Thermal resistance junction-case (single transistor)	2.7	°C/W

1. Device mounted on PCB area of 25 mm².

2 Electrical characteristics

T_{case} = 25 °C unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector cut-off current (V_{BE} = 0)	V_{CE} = 700 V V_{CE} = 700 V T_c = 125 °C			100 500	µA µA
I_{CEO}	Collector cut-off current (I_B = 0)	V_{CE} = 400 V			250	µA
$V_{(BR)EBO}$	Emitter-base breakdown voltage (I_C = 0)	I_E = 10 mA	9		18	V
$V_{CEO(sus)}$(1)	Collector-emitter sustaining voltage (I_B = 0)	I_C = 10 mA	400			V
$V_{CE(sat)}$(1)	Collector-emitter saturation voltage	I_C = 1 A I_B = 0.2 A I_C = 2 A I_B = 0.4 A			0.5 1	V V
$V_{BE(sat)}$(1)	Base-emitter saturation voltage	I_C = 1 A I_B = 0.2 A I_C = 2 A I_B = 0.4 A			1.2 1.3	V V
h_{FE}(1)	DC current gain	I_C = 10 mA V_{CE} = 5 V I_C = 2 A V_{CE} = 5 V	10 8		 24	
V_F	Diode forward voltage	I_F = 1 A			2.5	V
 t_s t_f	Resistive load Storage time Fall time	 I_C = 1 A I_{B1} = - I_{B2} = 0.2 A V_{CC} = 125 V t_p = 20 µs		 2.5 0.2		 µs µs

1. Pulse test: pulse duration ≤300 µs, duty cycle ≤ 2 %.

2.1 Electrical characteristics (curves)

Figure 2. DC current gain (V_{CE} = 1 V)

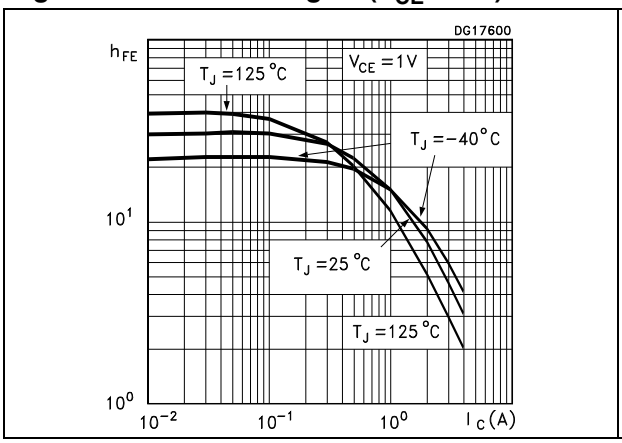


Figure 3. DC current gain (V_{CE} = 5 V)

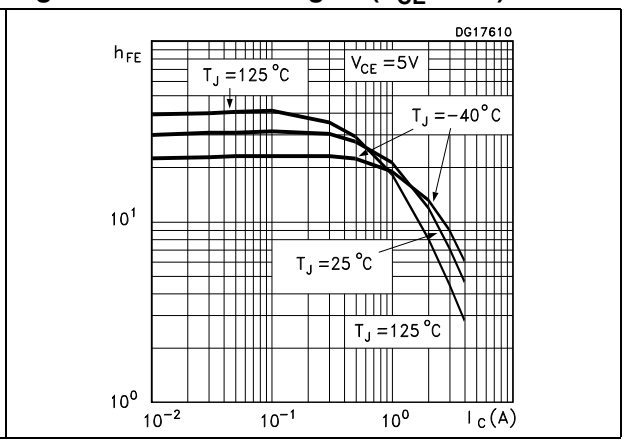


Figure 4. Collector-emitter saturation voltage

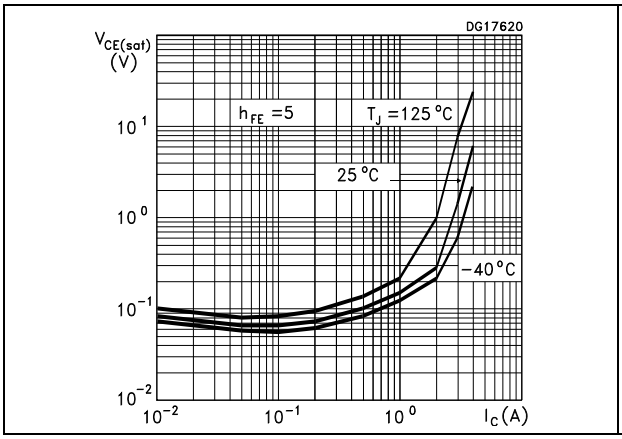


Figure 5. Base-emitter saturation voltage

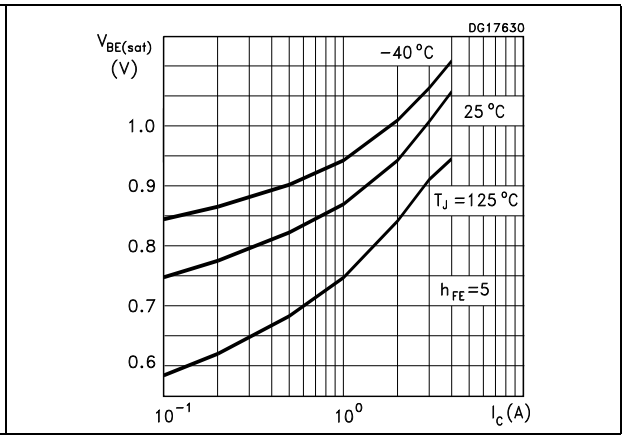


Figure 6. Freewheel diode forward voltage

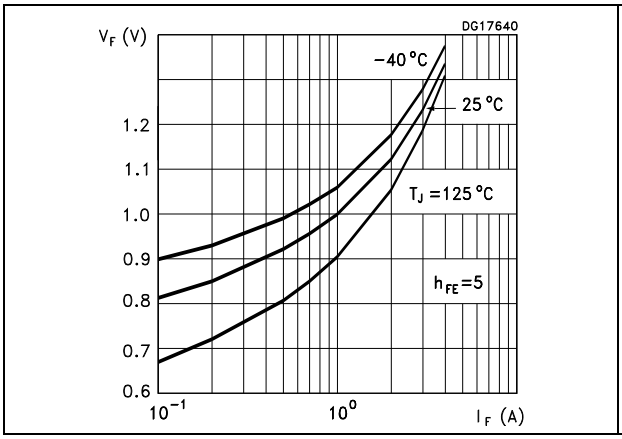
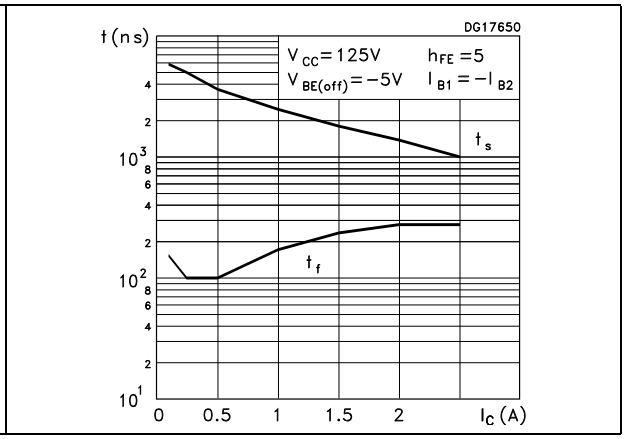
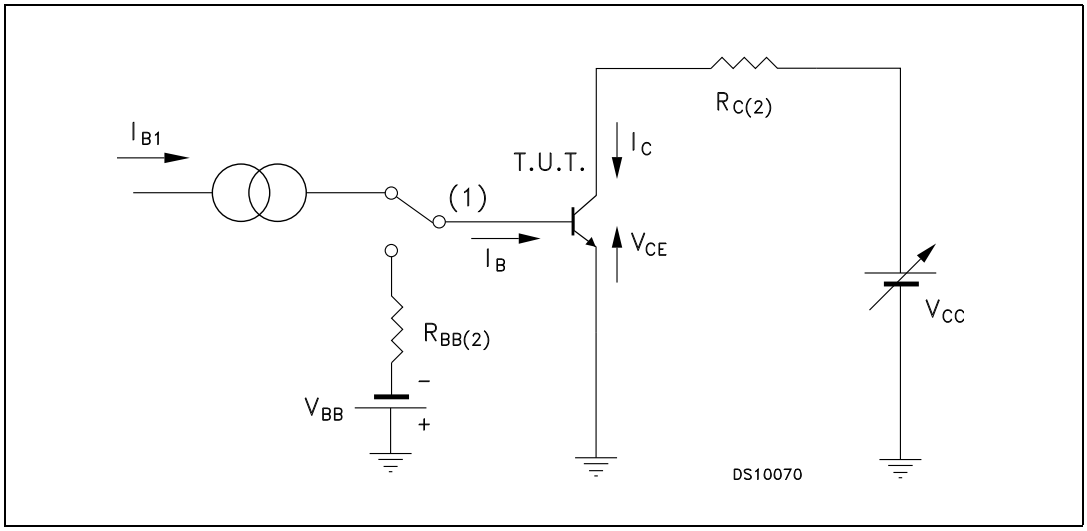


Figure 7. Resistive load switching time



3 Test circuit

Figure 8. Resistive load switching test circuit



1. Fast electronic switch
2. Non-inductive resistor

4 Package mechanical data

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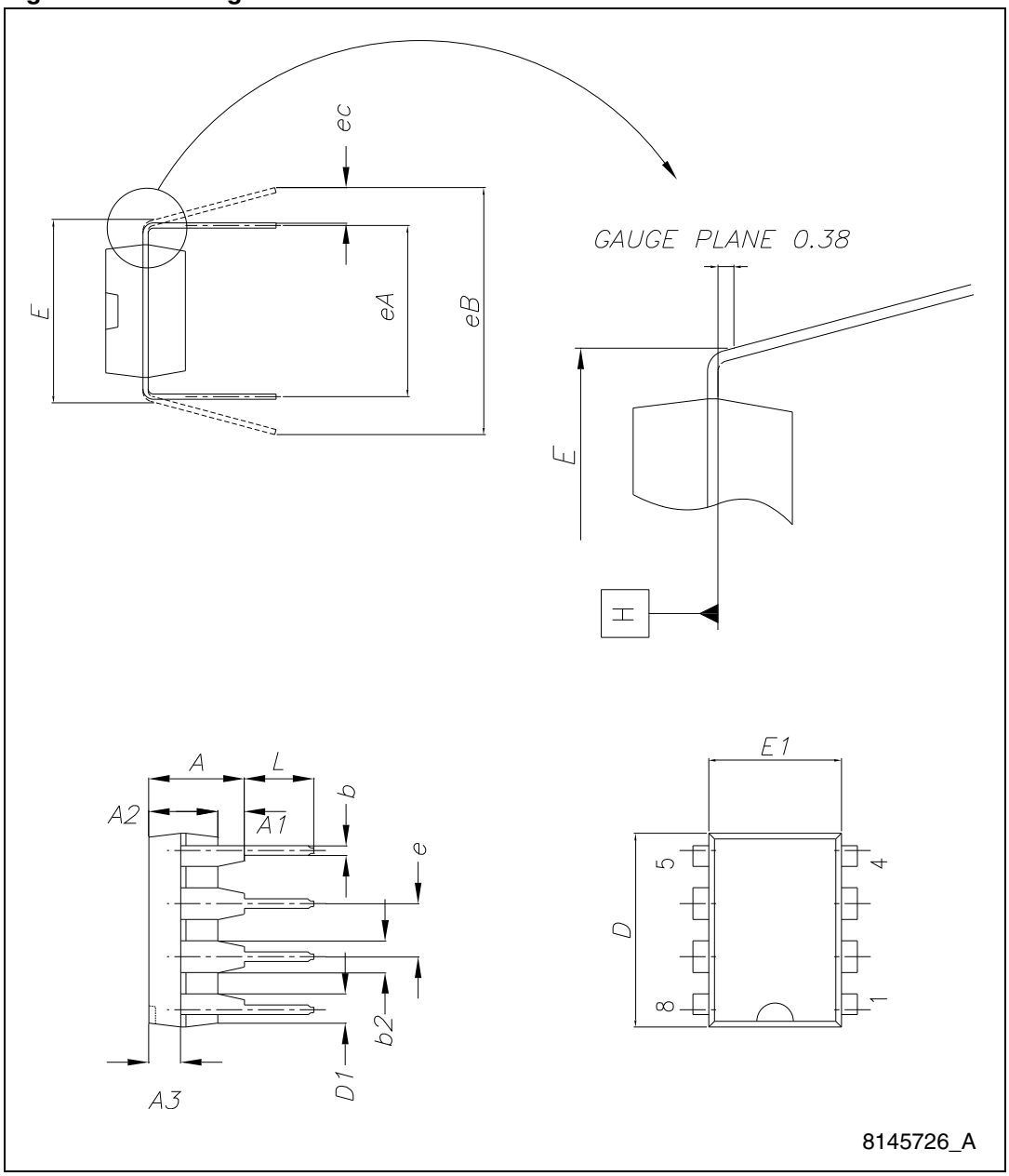
Table 5. DIP-8 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A			4.80
A1	0.50		
A2	3.10		3.50
A3	1.40		1.60
b	0.38		0.55
b1	0.38		0.51
b2	1.47		1.57
b3	0.89		1.09
c	0.21		0.35
c1	0.20		0.30
D	9.10		9.30
D1	0.13		
E	7.62		8.25
E1	6.25		6.45
e		2.54	
eA		7.62	
eB	7.62		10.90
eC	0		1.52
L	2.92		3.81

Figure 9. Drawing dimension DIP-8



5 Revision history

Table 6. Document revision history

Date	Revision	Changes
18-Nov-2009	1	Initial release.
16-Apr-2010	2	Inserted P_{TOT} and R_{thJA} values *Table 2* and *Table 3 on page 2*.
23-Oct-2012	3	Modified P_{TOT} and R_{thJA} values in *Table 2* and *Table 3 on page 2*. Minor text changes.

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