

March 2012

SG6846A Highly Integrated Green-Mode PWM Controller

Features

- Low Startup Current: 8µA
- Low Operating Current: 3.7mA
- Peak-Current Mode of Operation with Cycle-by-Cycle Current Limiting
- PWM Frequency Continuously Decreasing with Burst Mode at Light Loads
- V_{DD} Over-Voltage Protection (OVP)
- AC Input Brownout Protection with Hysteresis
- Constant Output Power Limit (Full AC Input Range)
- Internal Latch Circuit for OVP, OTP, and OCP
- Two-level OCP Delay: 1600ms
- Output Short-Circuited Delay Time: 100ms
- Programmable PWM Frequency with Frequency Hopping
- OCP Threshold is Half Peak Current Limit
- Feedback Open-loop Protection with 1700ms Delay
- Built-in Soft-Start

Applications

General-purpose switch-mode power supplies and flyback power converters, including:

- Power Adapters
- Open-frame SMPS
- SMPS with Surge-current Output, such as for Printers, Scanners, Motor Drivers

Description

The SG6846A is especially designed for SMPS with surge-current output, incorporated with a two-level OCP function. Besides the cycle-by-cycle current limiting, if the switching current is higher than two thirds the peak-current threshold for 1700ms, over-current protection is activated such that the SG6846A is latched off.

If the switching current is higher than two thirds of the peak-current threshold for 100ms, and the voltage on the V_{DD} is still higher than $V_{DD\text{-}OFF}$ + 1V, the PWM pulses are latched off immediately once the V_{DD} voltage is lower than $V_{DD\text{-}OFF}$ + 1V. This is useful when an output short circuit occurs.

SG6846A also integrates a frequency-hopping function internally to reduce EMI emission of a power supply with minimum line filters. Its built-in synchronized slope compensation provides proprietary internal compensation for constant output power limit over universal AC input range. Also, the gate output is clamped at 18V to protect the external MOSFET from over-voltage damage. Internal soft-start is built-in to soften the stress on the MOSFET and startup current during power on period.

Other protection functions include AC input brownout protection with hysteresis, V_{DD} over-voltage protection, and over-temperature protection. For over-temperature protection, an external NTC thermistor can be applied to sense the ambient temperature. When OCP, V_{DD} OVP, or OTP is activated, an internal latch circuit latches off the controller. The PWM pulses stay latched off until the power supply is disconnected from the mains outlet.

SG6846A controller is available in 8-pin SOP package.

Ordering Information

Part Number	Operating Temperature Range	OCP Latch	Package	
SG6846ALSY	-40 to +105°C	Yes	8-Pin Small Outline Package (SOP)	Tape & Reel
SG6846ALSZ	-40 to +105°C	Yes	8-Pin Small Outline Package (SOP)	Tape & Reel
SG6846ACSY	-40 to +105°C	No	8-Pin Small Outline Package (SOP)	Tape & Reel

Typical Application

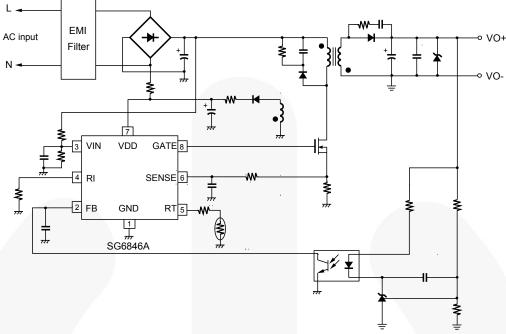


Figure 1. Typical Application

Block Diagram

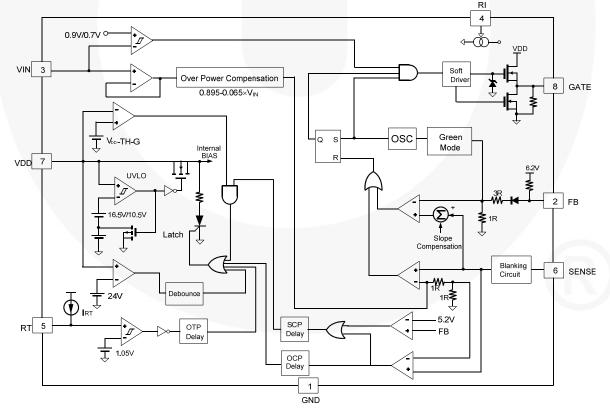


Figure 2. Block Diagram

Marking Information



Marking for SG6846ALSZ (Pb-Free)

F: L = OCP Latch

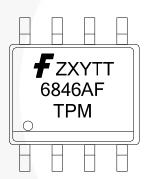
T: S = SOP

P: Z = Lead Free + ROHS Compatible Null = regular package

XXXXXXXX: Wafer Lot Y: Year; WW: Week

V: Assembly Location

Figure 3. Top Mark 1



f: Fairchild logo

Z: Plant Code

X: Year Code

Y: Week Code

TT: Die Run Code

F: L = OCP Latch, C = OCP auto-recovery

T: Package type, S = SOP

P: Y = Green Package

M: Manufacturing flow code

Marking for SG6846ALSY (Green-compound), SG6846ACSY (Green-compound)

Figure 4. Top Mark 2

Pin Configuration

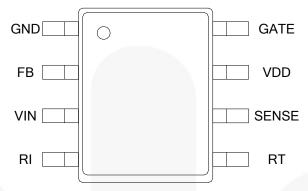


Figure 5. Pin Configuration

Pin Definitions

	1			
Pin #	Name	Function	Description	
1	GND	Ground	Ground.	
2	FB	Feedback	The signal from the external compensation circuit is fed into this pin. The PWM duty cycle is determined in response to the signal from this pin and the current-sense signal from pin 6.	
3	VIN	Line-voltage Detection	Line-voltage detection is used for brownout protection with hysteresis. Constant output power limit over universal AC input range is achieved using this pin. Add a low-pass filter to filter out line ripple on the bulk capacitor.	
4	RI	Reference Setting	A resistor from the RI pin to ground generates a reference current source that determines the switching frequency. Increasing the resistance reduces the switching frequency. A $26k\Omega$ resistor results in a $65kHz$ switching frequency.	
5	RT	Temperature Detection	For over-temperature protection, an external NTC thermistor is connected from this pin to the GND pin. The impedance of the NTC decreases at high temperatures. Once the voltage of the RT pin drops below a threshold, PWM output is disabled.	
6	SENSE	Current Sense	The sensed voltage is used for peak-current-mode control and cycle-by-cycle current limiting. If the switching current is higher than OCP threshold and lasts for 1700ms, SG6846A turns off immediately. This two-level OCP feature is especially suitable for SMPS with surge current output.	
7	VDD	Power Supply	If an open-circuit failure occurs in the feedback loop, the internal protection circuit disables PWM output as long as V_{DD} exceeds a threshold.	
8	GATE	Driver Output	The totem-pole output driver for the power MOSFET; internally clamped below 18V.	

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. All voltage values, except differential voltages, are given with respect to GND pin.

Symbol	Parameter	Min.	Max.	Unit	
V_{DD}	Supply Voltage			25	V
V_L	Input Voltage to FB, SENSE, VIN, RT, RI F	Pins	-0.3	7.0	V
P _D	Power Dissipation at T _A <50°C	SOP		400	mW
Θ _{JC}	Thermal Resistance (Junction-to-Case)	SOP		54.4	°C/W
T_J	Operating Junction Temperature	-40	+150	°C	
T _{STG}	Storage Temperature Range	-65	+150	°C	
T _L	Lead Temperature, Wave Soldering, 10 Se		+260	°C	
ESD	Human Body Model, JESD22-A114			5.0	kV
ESD	Charge Device Model, JESD22-C101			1.5	K V

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T _A	Operating Ambient Temperature	-40	+105	°C

Electrical Characteristics

 V_{DD} = 15V and T_A = 25°C unless otherwise noted.

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
V _{DD} Section	1					
$V_{\text{DD-OP}}$	Continuously Operating Voltage				20	V
V_{DD-ON}	Turn-on Threshold Voltage		15.5	16.5	17.5	V
$V_{DD\text{-}OFF}$	Turn-off Voltage		9.5	10.5	11.5	V
$V_{\text{DD-SCP}}$	Threshold voltage on VDD for Short-Circuit Protection		V _{DD-OFF} +0.5V	V _{DD-OFF} +1.0V	V _{DD-OFF} +1.5V	٧
$V_{\text{DD-LH}}$	Threshold Voltage for Latch-off Release		3	4	5	V
I _{DD-ST}	Startup Current	V _{DD-ON} – 0.16V		8	30	μA
I _{DD-OP}	Operating Supply Current	GATE Open		3.7	5.0	mA
V _{DD-OVP}	V _{DD} Over-Voltage Protection (Latch off)		22.6	23.6	24.6	V
t _{D-VDDOVP}	V _{DD} OVP Debounce Time	$R_I = 26k\Omega$	60	100	140	μs
I _{DD-OVP}	V _{DD} OVP Latch-off Holding Current	V _{DD} = 5V	30	50	70	μA
V _{IN} Section						
V _{IN-OFF}	PWM Turn-off Threshold Voltage		0.65	0.70	0.75	V
V _{IN-ON}	PWM Turn-on Threshold Voltage		V _{IN-OFF} +0.18	V _{IN-OFF} +0.20	V _{IN-OFF} +0.22	V
Feedback I	nput Section					
A _V	Input-Voltage to Current-Sense Attenuation		1/3.5	1/4.0	1/4.5	V/V
Z _{FB}	Input Impedance		4.0	5.5	7.0	kΩ
V_{FBO}	FB Pin Open Voltage		5.2	6.2	6.6	V
V_{FB-OLP}	Threshold Voltage of Open-loop Protection		4.7	5.2	5.7	V
t _{D-OLP}	Open-loop Protection Delay Time	$R_1 = 26k\Omega$	1600	1700	1800	ms
Current Se	nse Section			•	1.7	
Z _{SENSE}	Input Impedance			12		kΩ
t _{PD}	Delay to Output			100	250	ns
t _{LEB}	Leading-edge Blanking Time		270	360	У	ns
V _{SLOPE}	Slope Compensation	Duty = DCY _{MAX}	0.30	0.33	0.36	V
V _{STH1V}	Threshold Voltage for Current Limit	V _{IN} = 1V	0.80	0.83	0.86	V
V _{STH3V}	Threshold Voltage for Current Limit	V _{IN} = 3V	0.67	0.70	0.73	V
V _{STH1V-2/3}	OCP Threshold Voltage for Current Limit	V _{IN} = 1V	0.58	0.61	0.64	V
V _{STH3V-2/3}	OCP Threshold Voltage for Current Limit	V _{IN} = 3V	0.48	0.51	0.54	V
t _{D-OCP}	Delay Time for Over-Current Protection	$R_I = 26k\Omega$	1600	1700	1800	ms
t _{D-SCP}	Delay Time for Output Short-Circuited Protection	$R_{I} = 26k\Omega;$ $V_{DD} < V_{DD-SCP}$	90	100	110	ms
t _{SS-65KHz}	Resided Business Of a first Time	$R_I = 26k\Omega$	4.5	5.0	5.5	ms
t _{SS-130KHz}	Period During Startup Time	$R_{l} = 13k\Omega$	2.25	2.50	2.75	ms

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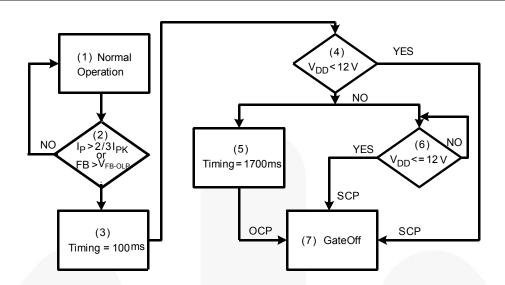


Figure 6. SG6846A OCP/SCP Logic Flow Diagram

Electrical Characteristics (Continued)

 V_{DD} = 15V and T_A = 25°C unless otherwise noted.

Symbol	Parameter			Test Condition	Min.	Тур.	Max.	Unit
Oscillator Section								
f _{OSC}	Normal PWM Frequency		Center Frequency	$R_I = 26k\Omega, V_{FB}>V_N$	62	65	68	kHz
000	·		Jitter Range		±3.7	±4.2	±4.7	
f _{OSC,MAX}	Maximum PWM		Center Frequency	$R_{I} = 13k\Omega, V_{FB}>V_{N}$	124	130	136	kHz
000,	Frequency	Frequency Jitter Range			±7.4	±8.4	±9.4	1
f _{OSC,MIN}	f _{OSC.MIN} Minimum PWM Freque		Center Frequency	$R_{I} = 36k\Omega, V_{FB} > V_{N}$	44.8	47.0	49.2	kHz
	Jitter Range			±2.54	±2.90	±3.26		
t _{hop-1}	Jitter Period	Pitter De de la		$R_I = 26k\Omega, V_{FB} \ge V_N$	3.9	4.4	4.9	ms
t _{hop-3}	- Jitter Period			$R_I = 26k\Omega$, $V_{FB} = V_G$	10.2	11.5	12.8	1115
f _{OSC-G}	Green-Mode Minimum	r Frequ	uency	$R_1 = 26k\Omega$	18.0	22.5	25.0	kHz
W	FB Pin Frequency	Pin, F	B voltage	D = 20k0 \/ = \/	1.9	2.1	2.3	V
V_{FB-N}	Reduction Threshold	Jitter	Range	$R_{I} = 26k\Omega, V_{FB} = V_{N}$	3.7	4.2	4.7	KHz
.,	ED Vallage at 6	Pin, F	B voltage		1.4	1.6	1.8	V
V_{FB-G}	FB Voltage at f _{OSC-G} Jitter Range		Range	$R_{I} = 26k\Omega, V_{FB} = V_{G}$	1.27	1.45	1.62	KHz
S _G	Slope for Green-Mode	Modulation		$R_1 = 26k\Omega$		85		Hz/mV
f_{DV}	Frequency Variation v	s. V _{DD} Deviation		V _{DD} = 11.5V to 20V			5	%
f _{DT}	Frequency Variation v Deviation	s. Tem	nperature	T _A = -30 to 85°C		1.5	5.0	%

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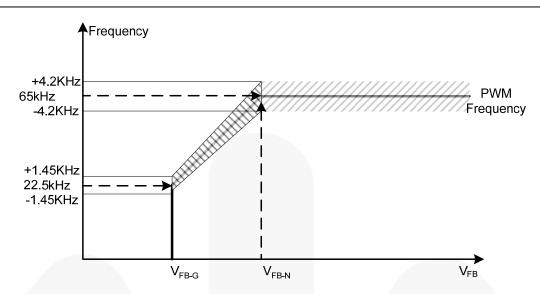


Figure 7. PWM Frequency

Electrical Characteristics (Continued)

 V_{DD} = 15V and T_A = 25°C unless otherwise noted.

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
PWM Outpu	ut Section					
DCY _{MAX}	Maximum Duty Cycle		80	85	90	%
V _{OL}	Output Voltage Low	$V_{DD} = 15V, I_{O} = 50mA$			1.5	٧
V _{OH}	Output Voltage High	$V_{DD} = 12V, I_{O} = 50mA$	8			V
t _R	Rising Time	GATE = 1nF		350		ns
t _F	Falling Time	GATE = 1nF		50		ns
V_{CLAMP}	Gate Output Clamping Voltage	V _{DD} = 20V			18	V
Over-Temp	erature Protection (OTP) Section ⁽¹⁾		/			
I _{RT}	Output Current of RT Pin	$R_1 = 26k\Omega$	64	70	76	μA
V _{RTTH}	Threshold Voltage for OTP		1.015	1.065	1.115	V
t _{DOTP-LATCH}	Over-Temperature Latch-off Debounce	$R_1 = 26k\Omega$		100		ms
R _{RT-OFF}	Equivalent Impedance of RT for OTP ⁽¹⁾	$R_1 = 26k\Omega$	14	15	16	kΩ
R _I Section						
RI _{NOR}	R _I Operating Range		13		36	kΩ
RI _{MAX}	Maximum R _I Value for Protection		10			МΩ
RI _{MIN}	Minimum R _I Value for Protection				6	kΩ

Note:

1. The relationship between R_{RT-OFF} and R_I is: $R_{RT-OFF} = V_{OTP-LATCH-OFF} / I_{RT} = V_{RT} / (70 \mu A \times 26 / R_I (K\Omega))$ (1)

Typical Performance Characteristics

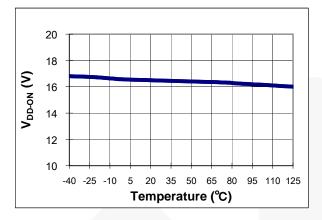


Figure 8. Turn-on Threshold Voltage (V_{DD-ON}) vs. Temperature

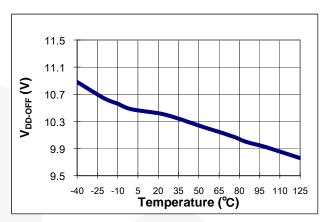


Figure 9. Turn-off Threshold Voltage (V_{DD-OFF}) vs. Temperature

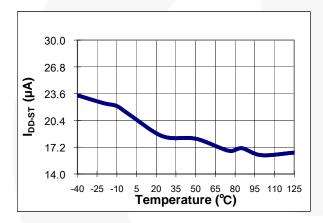


Figure 10. Startup Current (I_{DD-ST}) vs. Temperature

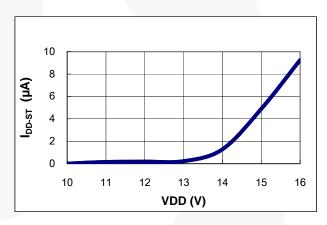


Figure 11. Startup Current vs. V_{DD} Voltage

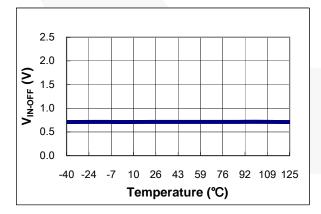


Figure 12. PWM Turn-off Threshold Voltage (V_{IN-OFF}) vs. Temperature

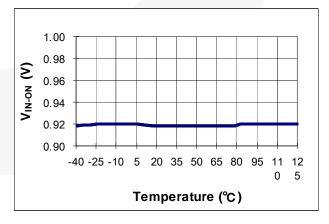


Figure 13. PWM Turn-on Threshold Voltage ($V_{\text{IN-ON}}$) vs. Temperature

Typical Performance Characteristics (Continued)

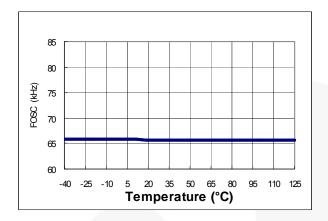
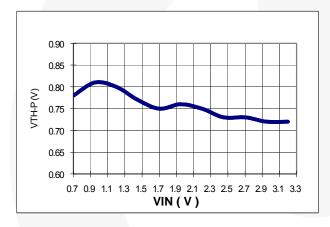


Figure 14. Normal PWM Frequency (fosc) vs. Temperature

Figure 15. PWM Frequency vs. FB Voltage



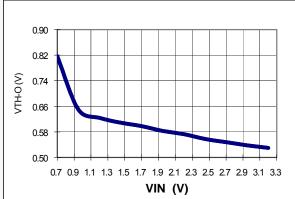
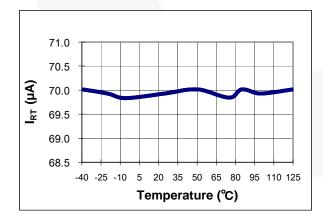


Figure 16. Current-Limit Threshold vs. V_{IN} Voltage

Figure 17. 2/3 Current-Limit Threshold vs. V_{IN} Voltage



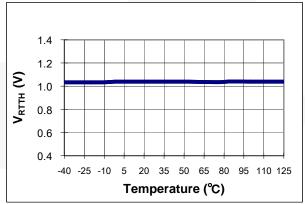


Figure 18. Output Current of RT Pin (I_{RT}) vs. Temperature

Figure 19. FB Output High Voltage (V_{RTTH}) vs. Temperature

Operation Description

Startup Operation

The turn-on/turn-off thresholds are fixed internally at 16.5V and 10.5V. To enable the SG6846A during startup, the hold-up capacitor must first be charged to 16.5V through the startup resistor.

The hold-up capacitor continues to supply V_{DD} before energy can be delivered from the auxiliary winding of the main transformer. The V_{DD} must not drop below 10.5V during this startup process. This UVLO hysteresis window ensures that the hold-up capacitor can adequately supply V_{DD} during startup.

The typical startup current is only 8µA, which allows a high-resistance, low-wattage startup resistor to be used. For constant output power limit over a universal inputvoltage range, the peak-current threshold is adjusted by the voltage of the VIN pin. Since the VIN pin is connected to the rectified AC input line voltage through the resistive divider, a higher line voltage generates a higher V_{IN} voltage. The threshold voltage decreases as the V_{IN} increases, making the maximum output power at high line input voltage equal to that at low line input. The value of R-C network should not be so large it affects the power limit (shown in Figure 20). R and C should put on less than 300Ω and 1000pF, respectively, to minimize power loss. A $1.5M\Omega/0.25W$ startup resistor and a 10µF/25V V_{DD} hold-up capacitor are sufficient for a universal input range.

The required operating current has been reduced to 3.7mA, which enables higher efficiency and reduces the V_{DD} hold-up capacitance requirement.

Green-Mode Operation

The proprietary green-mode function provides off-time modulation to continuously decrease the switching frequency under light-load conditions. Maximum on-time is limited to provide protection against abnormal conditions. To further reduce power consumption under zero-load condition, the PWM oscillator is completely turned off and the power supply enters burst-mode. This green mode dramatically reduces power consumption under light-load and zero-load conditions. Power supplies using SG6846A can meet restrictive international regulations regarding standby power consumption.

Oscillator Operation

A resistor connected from the RI pin to GND generates a reference current source, inside the SG6846A, used to determine the PWM frequency. Increasing the resistance decreases the amplitude of the current source and reduces the PWM frequency. Using a $26 k \Omega$ resistor results in a corresponding 65kHz switching frequency. The relationship between $R_{\rm I}$ and the switching frequency is:

$$f_{\text{PWM}}(kHz) = \frac{1690}{R_1 (k\Omega)}$$
 (2)

If an open-circuit or short-circuit to ground occurs at the RI pin, the internal protection circuit immediately shuts down the controller.

Two-level Over-current Protection (OCP)

The cycle-by-cycle current limiting shuts down the PWM immediately when the switching current is over the peak-current threshold. Additionally, when the switching current is higher than the over-current threshold, the internal counter counts down. When the total accumulated counting time is more than ~1600ms (R_I = $26k\Omega$), the controller is latched off and the internal counter counts up. When the switching current is lower than the over-current threshold, the internal counter counts down. When the total accumulated counting time is more than ~1600ms (R_I = $26k\Omega$), the controller is latched off.

This two-level OCP protection and up/down counter are especially designed for SMPS with surge current output, such as those for printers, scanners, and motor drivers.

Constant Output Power Limit

For constant output power limit over universal input-voltage range, the peak-current threshold is adjusted by the voltage of the VIN pin. Since the VIN pin is connected to the rectified AC input line voltage through the resistive divider, a higher line voltage generates a higher $V_{\rm IN}$ voltage. The threshold voltage decreases as $V_{\rm IN}$ increases, making the maximum output power at high-line input voltage equal to that at low-line input.

Brownout Protection

Since the VIN pin is connected through a resistive divider to the rectified AC input line voltage, it can also be used for brownout protection. If the V_{IN} voltage is less than 0.7V, the PWM output is shut off. If the V_{IN} is over 0.9V, the PWM output is turned on again. The hysteresis window for on/off is ~0.2V.

V_{DD} Over-voltage Protection (OVP)

 V_{DD} over-voltage protection is built in to prevent damage. If V_{DD} is over 23.6V, SG6846A is latched off.

Over-Temperature Protection (OTP)

An external NTC thermistor can be connected from the RT pin to GND. The impedance of the NTC decreases at high temperatures. When the voltage of the RT pin drops below 1.05V, the SG6846A is turned off. For protection-mode options, see Ordering Information.

Operation Description (Continued)

Noise Immunity

Noise from the current sense or the control signal may cause significant pulse-width jitter, particularly in continuous-conduction mode. Slope compensation helps alleviate this problem. Good placement and layout practices should be followed. Avoid long PCB traces and component leads. Compensation and filter components should be located near the SG6846A.

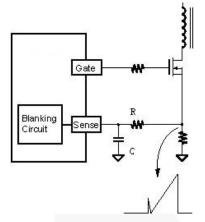


Figure 20. Current Sense R-C Filter

Reference Circuit

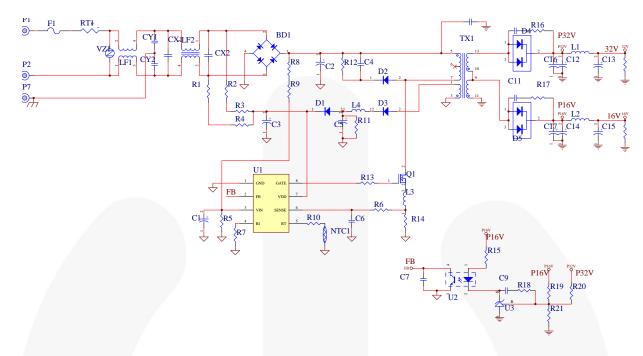
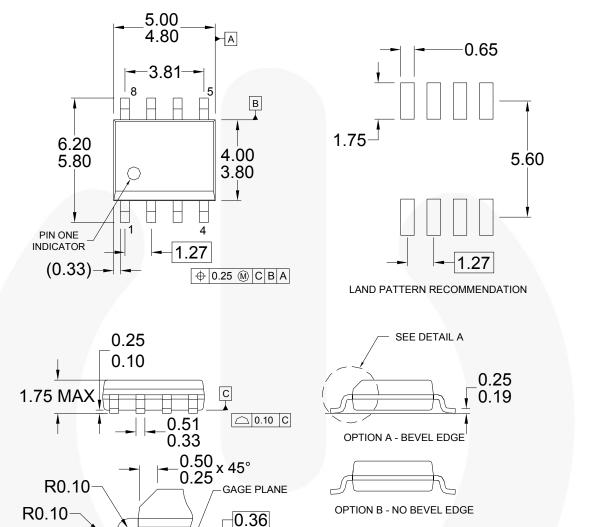


Figure 21. Application Circuit for 32V / 16V Output

Bill of Materials

Part No.	Value	Part No.	Value	Part No.	Value
R1, R2, R3, R4	470KΩ ±5%	C4	103 P 630V	D3	FR103 1.0A 200V
R8, R9	S1MΩ ±1%	C10,C11	102 P 1KV	BD1	DBL406G
R5	16K2Ω ±1%	C6,C7	102 P 50V	D4	BYT28-300
R15	1K5Ω ±5%	C9	222 P 50V	D5	BYV32-150
R13	10Ω ±5%	C14,C17	470μ 25V	F1	250V4A QUICK
R18	4K7Ω ±5%	C15	220µ 25V	L1,L2	1.8µH
R21	15KΩ ±1%	C13,C16	220μ 50V	L4	10μH
R7	27KΩ ±5%	C2	150µ 400V	U3	TL431 ±1%
R6	330Ω ±1%	C1	4.7µ 50V	U1	SG 6846
R19	102KΩ ±1%	C3	10μ 50V	U2	PC817
R14	0Ω22 ±5%	CX1	X1 0.47μ 275V	Q1	7NB60
R16, R17	1W 20Ω ±5%	C8	Y2 222P 250V	TX1	EI-33
R11	20KΩ ±5%	C5	100μ 50V	RT1	SCK053
R12	100KΩ ±5%	CX2	X2 0.1μF 275V	VZ1	14ψ 470V
R20	887KΩ ±1%	D1	1N4148		
R22	10KΩ ±1%	D2	BYV95C		

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA, ISSUE C,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M.
- E) DRAWING FILENAME: M08AREV13

Figure 22. 8-Pin Small Outline Package (SOP)

SEATING PLANE

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings: http://www.fairchildsemi.com/packaging/

-(1.04)

DETAIL A

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O°=

0.90

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	Political of Terms				
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