8-Channel Serial to Parallel Converter with High Voltage Push-Pull Outputs, POL, Hi-Z, and Short Circuit Detect

Features

- □ HVCMOS, technology
- □ Operating output voltage of 250V
- Low power level shifting from 5V to 250V
- □ Shift register speed 8MHz @ V_{DD}=5V
- 8 latch data outputs
- Output polarity and blanking
- CMOS compatible inputs
- Output short circuit detect
- Output high-Z control

Applications

- Piezoelectric transducer driver
- Weaving applications
- □ Braille
- Printers
- □ MEMs
- Displays

General Description

The HV513 is a low voltage serial to high voltage parallel converter with 8 high voltage push-pull outputs. This device has been designed to drive small capacitve loads such as piezoelectric transducers. It can also be used in any application requiring multiple high voltage outputs, with medium current source and sink capabilities.

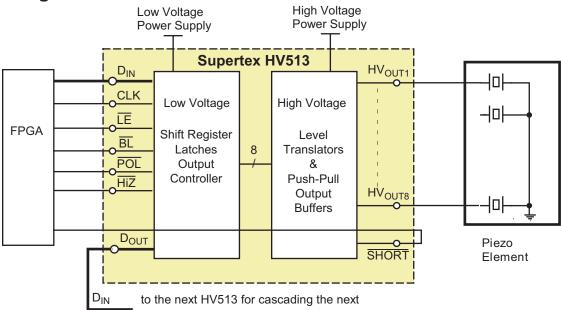
The device consists of an 8-bit shift register, 8 latches, and control logic to perform the polarity select and blanking of the outputs. Data is shifted through the shift register on the low to high transition of the clock. A data output buffer is provided for cascading devices. Operation of the shift register is not affected by the $\overline{\text{LE}}$, $\overline{\text{BL}}$, $\overline{\text{POL}}$, or the $\overline{\text{HI-Z}}$ control inputs. Transfer of data from the shift register to the latch occurs when the $\overline{\text{LE}}$ is high. The data in the latch is stored when $\overline{\text{LE}}$ is low. A high-Z, $\overline{\text{HI-Z}}$, pin is provided to set all the outputs in a high-Z state.

All outputs have short circuit protection that detects if the outputs have reached the required output state. If output does not track the required state, then the SHORT pin will be low. This output will pulse low during the output transistion period under normal operation; see SC Timing Diagram for details.

All outputs will have a break-before-make circuitry to reduce cross-over current during output state changes.

The \overline{POL} , \overline{BL} , \overline{LE} , and $\overline{HI-Z}$ inputs have an internal pull up resistor.

Application Diagram



A122104

DC Electrical Characteristics (Over operating supply voltages unless otherwise noted)

Symbol	Parameter		Min	Тур	Max	Units	Conditions
I _{DD}	V _{DD} supply current				4	mA	$f_{CLK}=8MHz$, $\overline{LE}=LOW$
	Quiescent V _{DD} supply current				0.1	mA	All V _{IN} =V _{DD}
DDQ					2.0		All V _{IN} =0V
I _{PP}	V _{PP} supply current				100	μA	V _{PP} =250V, f _{OUT} =300Hz, no load
I _{PPQ}	Quiescent V _{PP} supply current				100	μA	V _{PP} =240V, outputs static
I _{IH}	High-level logic input current				10	μA	$V_{IH} = V_{DD}$
	I and I am I a				-10		V _{IL} =0V
I _{IL}	Low-level logic input current				-350	μA	V _{IL} =0V, for inputs w/pull-up resistors
\/	Lligh lovel output	H _{VOUT}	140			V	V _{PP} =200V, I _{HVOUT} =-20mA
V _{OH}	High-level output	Data out	V _{DD} -1V			V	I _{DOUT} =-0.1mA
W	Low level output	H _{VOUT}			60	V	V _{DD} =4.5V, I _{HVOUT} =20mA
V _{OL}	Low-level output	Data out			1.0		I _{DOUT} =0.1mA

DC Electrical Characteristics (Over operating supply voltages unless otherwise noted)

Symbol	Parameter	Min	Тур	Max	Units	Conditions
f _{CLK}	Clock frequency	0		8	MHz	
f _{out}	Output switching frequency (SOA limited)		300		Hz	C _L =50nF, V _{PP} =200V
t _w	Clock width high and low	62			ns	
t _{su}	Data setup time before clock rises	15			ns	
t _H	Data hold time after clock rises	30			ns	
t _{wle}	Width of latch enable pulse	80			ns	
t _{DLE}	LE delay time after rising edge of clock	35			ns	
t _{SLE}	LE setup time before rising edge of clock	40			ns	
t _{OR} , t _{OF}	Rise/fall time of HV _{OUT}			1000	μs	C _L =100nF, V _{PP} =200V
t _{d ON/OFF}	Delay time for output to start rise/fall			500	ns	
t _{DHL}	Delay time clock to D _{OUT} high to low			110	ns	C _L =15pF
t _{DLH}	Delay time clock to D _{OUT} low to high			110	ns	C _L =15pF
t _R , t _F	All logic inputs			5	ns	
t _{sd}	Output short circuit detection			500	ns	Short to output fall of \overline{SHORT} , $C_L=15pF$
t _{sc}	Output short circuit clear			3000	ns	Short clear to output rise of SHORT
t _{HI-Z}	Output high-Z state			500	ns	

Absolute Maximum Ratings¹

Supply Voltage, V _{DD}	-0.5V to 6V
Supply Voltage, V _{PP}	$V_{\rm DD}$ to 275V
Logic input levels	-0.5V to V _{DD} +0.5V
Ground current ²	0.3A
High voltage supply current ²	0.25A
Continuous total power dissipation ³	750mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C +150°C

^{1.} All voltages are referenced to GND.

Ordering Information

Device Part Number		Package			
HV513 HV513WG		24-Lead SOW			
HV513	HV513X	Die in Wafer Form			

^{2.} Connection to all power and ground pads is required. Duty cycle is limited by the total power dissipated in the package.

^{3.} For operation above 25°C ambient derate linearly to 85°C at 12mW/°C.

Operating Supply Voltages

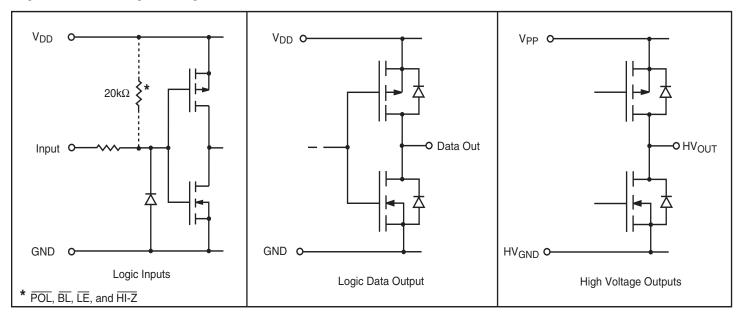
Symbol	Parameter	Min	Тур	Max	Units	Conditions
V _{DD}	Logic supply voltage	4.5	5.0	5.5	V	
V _{PP}	High voltage supply	50		250	V	Note 1
V _{IH}	High-level input voltage	V _{DD} -0.9		V _{DD}	V	
V _{IL}	Low-level input voltage	0		0.9	V	
T _A	Operating free-air temperature	-40		+85	°C	

Notes:

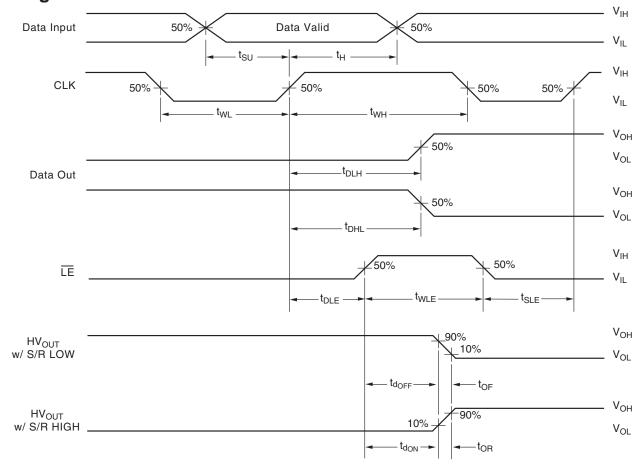
- 1. Below minimum $\boldsymbol{V}_{_{\boldsymbol{PP}}}$ the output may not switch.
- 2. Power-up sequence should be the following:
 - 1. Connect ground.
 - 2. Apply V_{DD} .
 - 3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
 - 4. Apply V_{PP} .

Power-down sequence should be the reverse of the above.

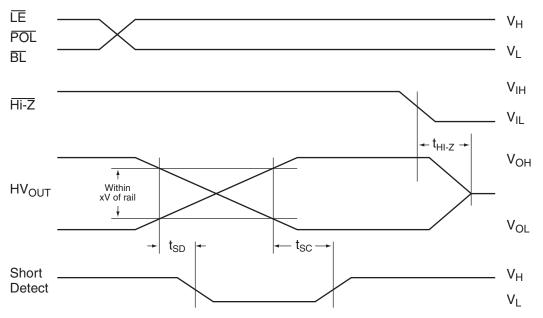
Input and Output Equivalent Circuits



Switching Waveforms



Short Circuit Detect Detail Timing (HV513)



 $\underline{\text{Note}}$: For V_{PP} greater than 150V:

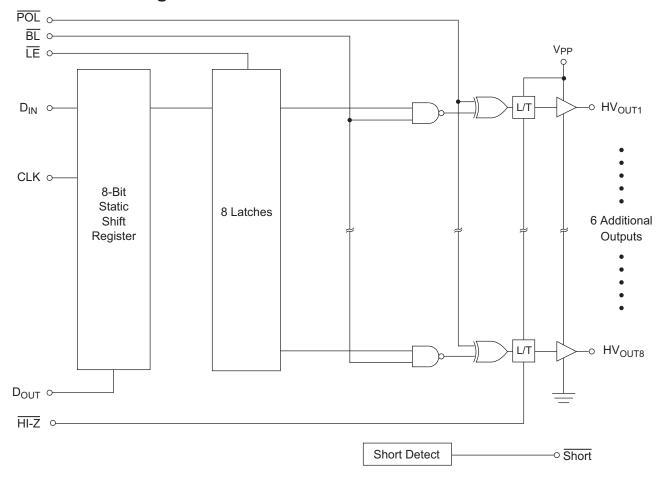
Short detect output will flag short conditions

- HV_{OUT} is higher than 10V when expected low
- HV_{OUT} is lower than V_{PP} 100V when expected high

Short detect output will stay clear

- $\mathrm{HV}_{\mathrm{OUT}}$ is lower than 2V when expected low
- HV_{OUT} is higher than V_{PP} 60V when expected high

Functional Block Diagram



 $\overline{\text{POL}},\,\overline{\text{BL}},\,\overline{\text{LE}},$ and $\overline{\text{HI-Z}}$ have internal 20k Ω pull-up resistors.

Function Table

		Inputs						Output		
Function	Data	CLK	ΙĒ	BL	POL	HI-Z	Shift Reg 1 28	HV Outputs 1 28	Data Out	
All on	Х	Х	Х	L	L	Н	* **	Н НН	*	
All off	Х	Х	Х	L	Н	Н	* **	L LL	*	
Invert mode	Х	Х	L	Н	L	Н	* *	* ** (b)	*	
Load S/R	H or L		L	Н	Н	Н	H or L **	* * *	*	
Store Data in latches	Х	Х	L	Н	Н	Н	* *	* * *	*	
Store Data in lateries	Х	Х	L	Н	L	Н	* *	* ** (b)	*	
Transparent made	L		Н	Н	Н	Н	L **	L **	*	
Transparent mode	Н		Н	Н	Н	Н	H **	H **	*	
Outputs High-Z	Х	Х	Х	Х	Х	L	* **	High impedance outputs	*	
Outputs ON	Х	Х	Х	Х	Х	Н	* * *	* * *	*	

Pin Configuration

Pin	Function
1	N/C
2	$V_{_{\mathrm{DD}}}$
3	D _{out}
4	BL
5	POL
6	CLK
7	Œ
8	SHORT
9	HI-Z
10	D _{IN}
11	LGND
12	N/C

Pin	Function
13	HVGND
14	HVGND
15	HV _{OUT1}
16	HV _{OUT2}
17	HV _{OUT3}
18	HV _{OUT4}
19	HV _{OUT5}
20	HV _{OUT6}
21	HV _{OUT7}
22	HV _{OUT8}
23	V _{PP}
24	V _{PP}

Package Outline

	_	1
1		24
2		23
3		22
4		21
5		20
6		19
7		18
8		17
9		16
10		15
11		14
12		13

24-Lead SOW Package (WG) (Wide Body)

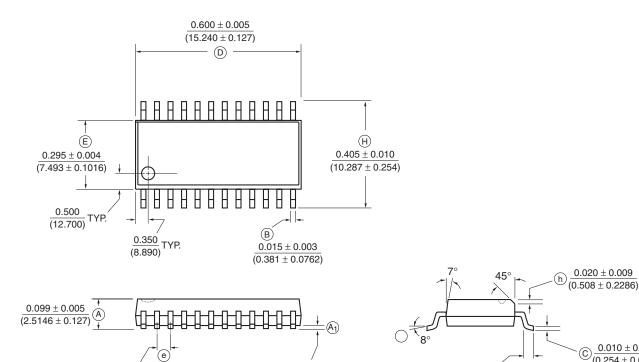
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 0.020 ± 0.009

 0.010 ± 0.002 $\bigcirc \frac{0.010 \pm 0.0}{(0.254 \pm 0.0508)}$



24-LEAD SOW PACKAGE (WG) (WIDE BODY)



 0.008 ± 0.003

 (0.2032 ± 0.0762)

Note: Circle (e.g. (B)) indicates JEDEC Reference.

 $\frac{0.050}{(1.270)}$ TYP.

Dimensions in Inches Measurement Legend = (Dimensions in Millimeters)

 0.035 ± 0.015

 (0.889 ± 0.381)

DSPD-24SOWWG