International IOR Rectifier

PD- 94828

SMPS MOSFET

IRF740APbF

HEXFET® Power MOSFET

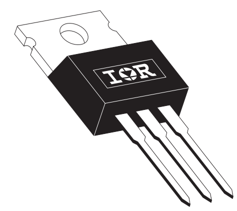
Applications

- Switch Mode Power Supply (SMPS)
- Uninterruptable Power Supply
- High speed power switching
- Lead-Free

V_{DSS}	Rds(on) max	I_D
400V	**0.55Ω**	**10A**

Benefits

- Low Gate Charge Qg results in Simple Drive Requirement
- Improved Gate, Avalanche and dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective Coss specified (See AN 1001)



TO-220AB G D S

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	10	
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	6.3	A
I_{DM}	Pulsed Drain Current ①	40	
P_D @T_C = 25°C	Power Dissipation	125	W
	Linear Derating Factor	1.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	5.9	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torqe, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Typical SMPS Topologies:

- Single transistor Flyback Xfmr. Reset
- Single Transistor Forward Xfmr. Reset
  (Both for US Line Input only)

Notes ① through ⑤ are on page 8

11/10/03

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	400	——	——	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.48	——		V/°C Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	——	0.55	Ω	V_{GS} = 10V, I_D = 6.0A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{DSS}	Drain-to-Source Leakage Current	——	——	25	μA	V_{DS} = 400V, V_{GS} = 0V
		——	——	250		V_{DS} = 320V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 30V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -30V

Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	4.9	——	——	S	V_{DS} = 50V, I_D = 6.0A
Q_g	Total Gate Charge	——	——	36	nC	I_D = 10A
Q_{gs}	Gate-to-Source Charge	——	——	9.9		V_{DS} = 320V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	——	16		V_{GS} = 10V, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	——	10	——	ns	V_{DD} = 200V
t_r	Rise Time	——	35	——		I_D = 10A
$t_{d(off)}$	Turn-Off Delay Time	——	24	——		R_G = 10Ω
t_f	Fall Time	——	22	——		R_D = 19.5Ω,See Fig. 10 ④
C_{iss}	Input Capacitance	——	1030	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	170	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	7.7	——		ƒ = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	——	1490	——		V_{GS} = 0V, V_{DS} = 1.0V, ƒ = 1.0MHz
C_{oss}	Output Capacitance	——	52	——		V_{GS} = 0V, V_{DS} = 320V, ƒ = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	——	61	——		V_{GS} = 0V, V_{DS} = 0V to 320V ⑤

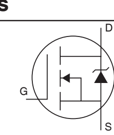
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	——	630	mJ
I_{AR}	Avalanche Current①	——	10	A
E_{AR}	Repetitive Avalanche Energy①	——	12.5	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	1.0	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient	——	62	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	10	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	40		
V_{SD}	Diode Forward Voltage	——	——	2.0	V	T_J = 25°C, I_S = 10A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	240	360	ns	T_J = 25°C, I_F = 10A
Q_{rr}	Reverse RecoveryCharge	——	1.9	2.9	μC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

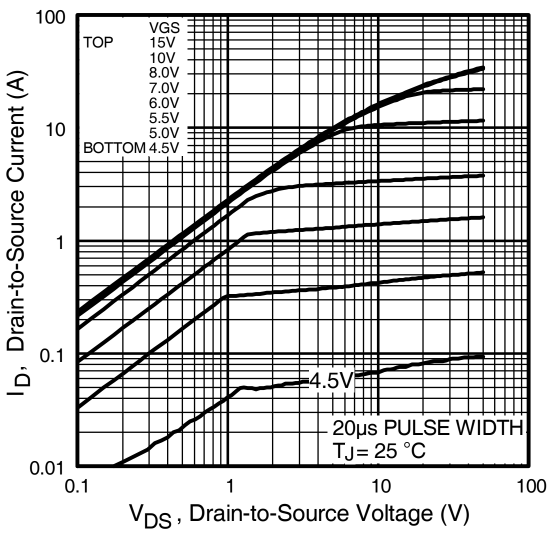


Fig 1. Typical Output Characteristics

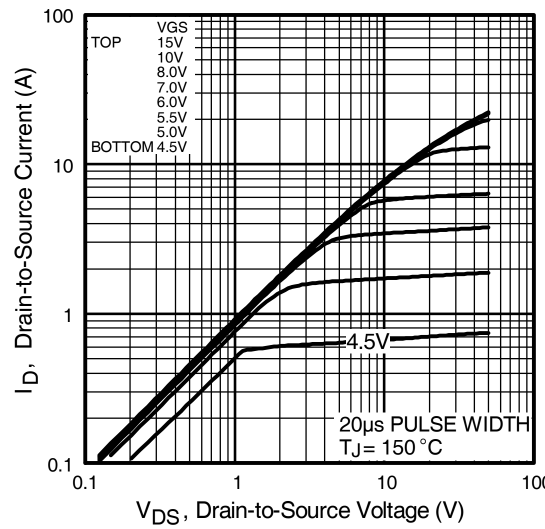


Fig 2. Typical Output Characteristics

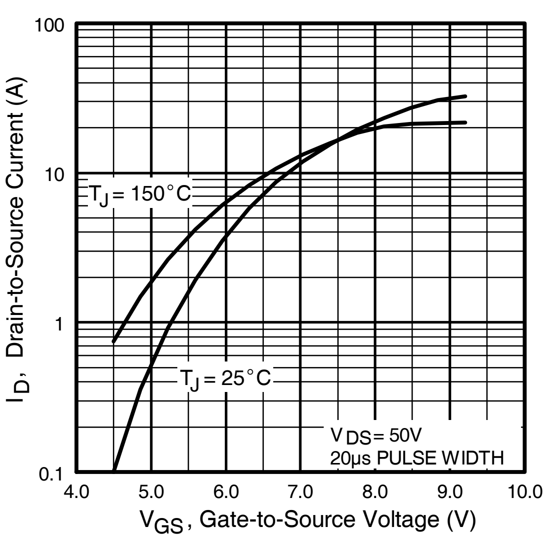


Fig 3. Typical Transfer Characteristics

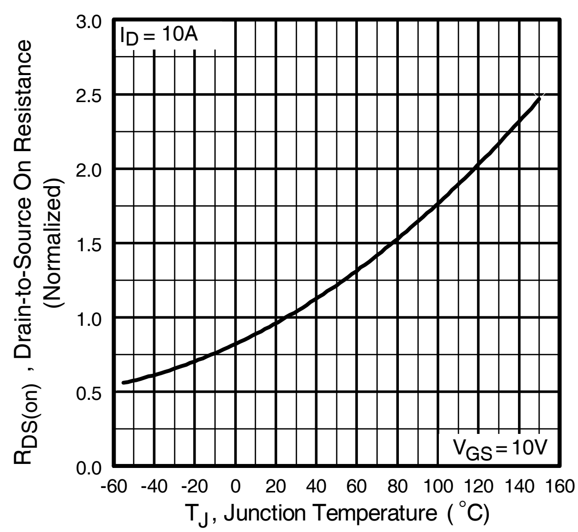


Fig 4. Normalized On-Resistance Vs. Temperature

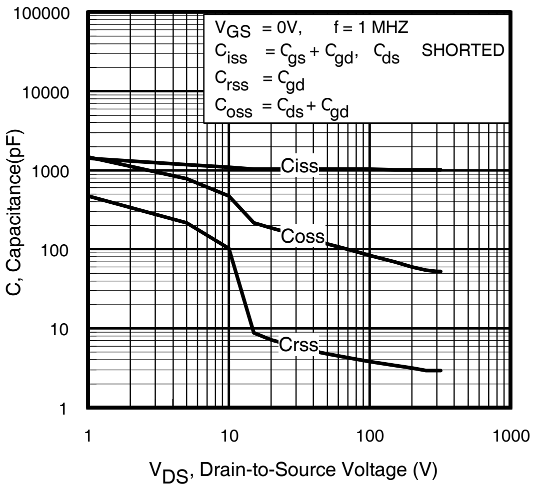


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

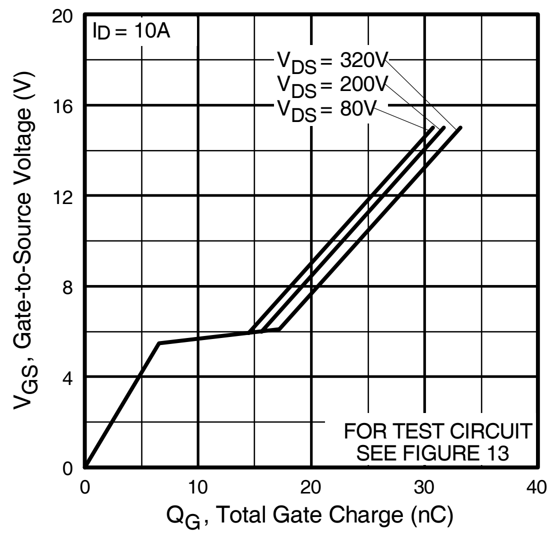


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

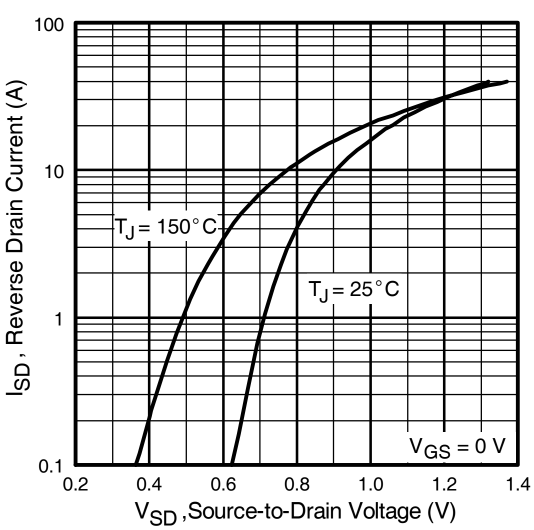


Fig 7. Typical Source-Drain Diode Forward Voltage

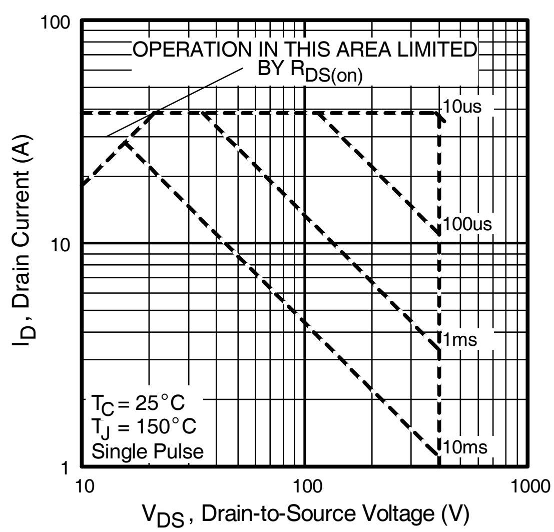


Fig 8. Maximum Safe Operating Area

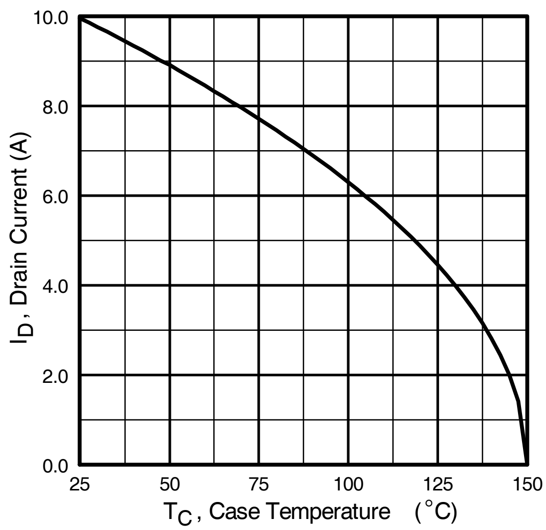


Fig 9. Maximum Drain Current Vs. Case Temperature

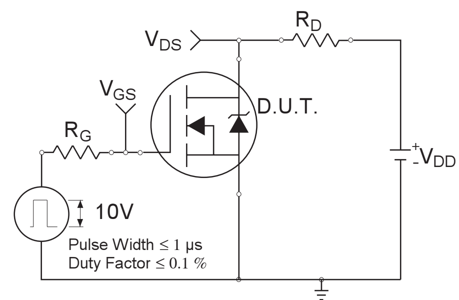


Fig 10a. Switching Time Test Circuit

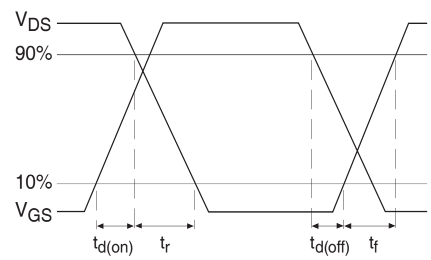


Fig 10b. Switching Time Waveforms

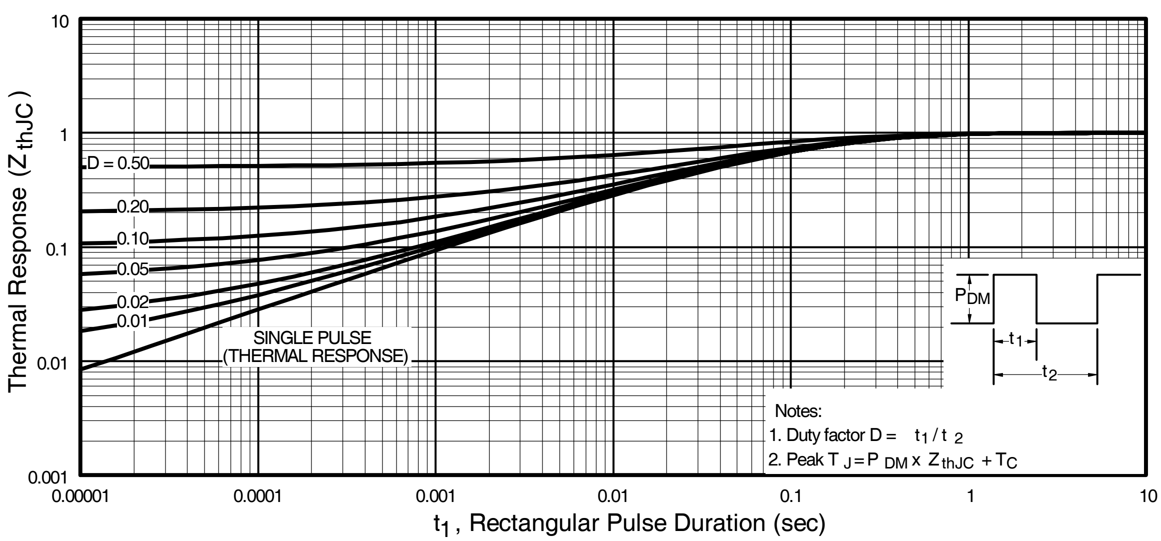


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

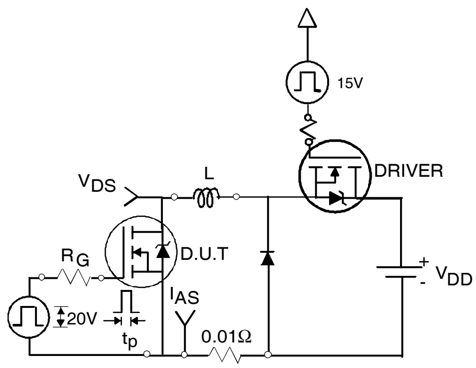


Fig 12a. Unclamped Inductive Test Circuit

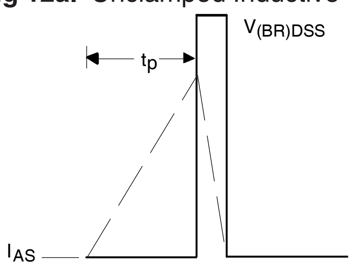


Fig 12b. Unclamped Inductive Waveforms

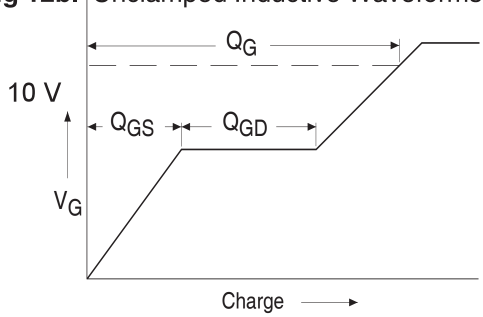


Fig 13a. Basic Gate Charge Waveform

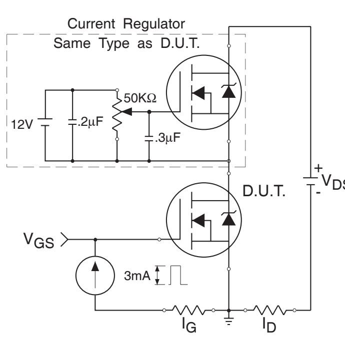


Fig 13b. Gate Charge Test Circuit

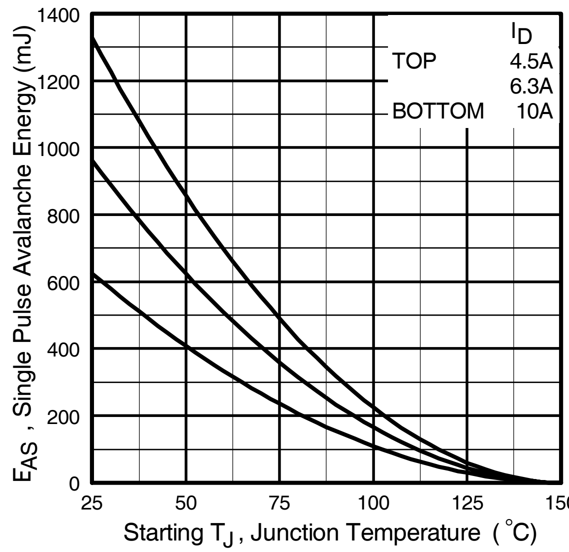


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

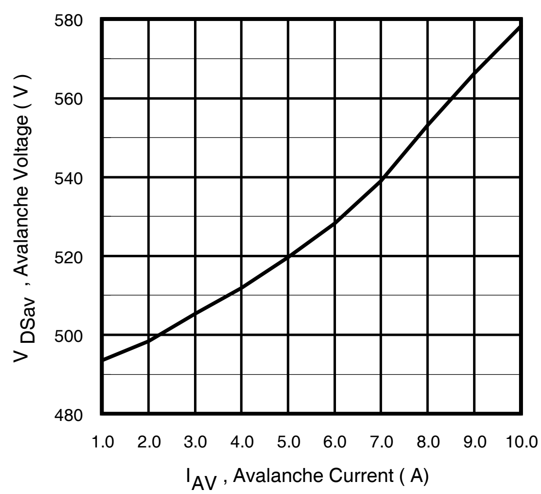
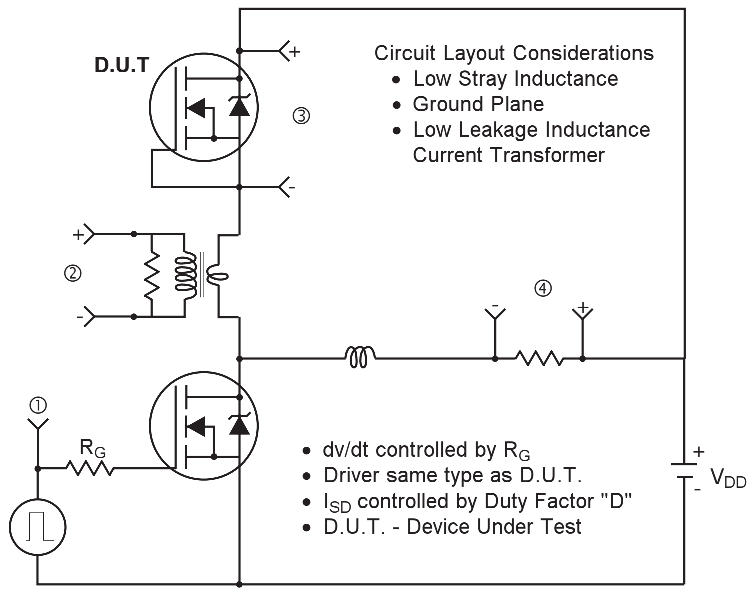
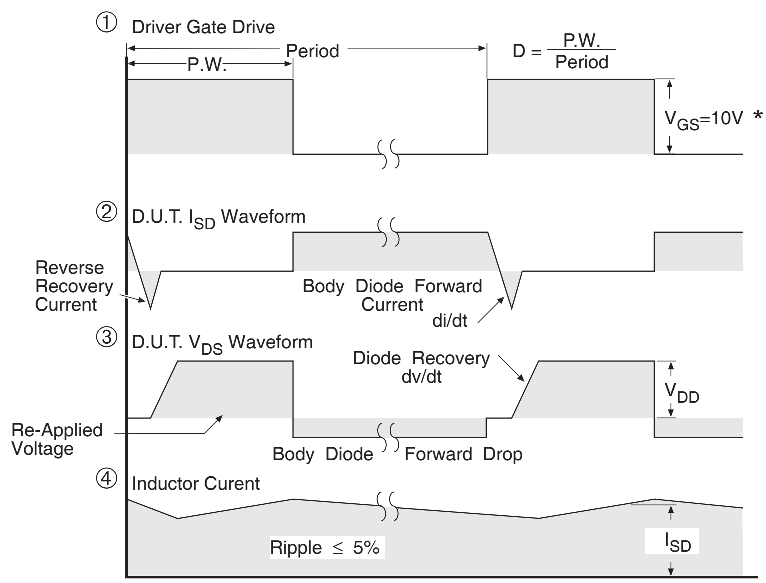


Fig 12d. Typical Drain-to-Source Voltage Vs. Avalanche Current

Peak Diode Recovery dv/dt Test Circuit



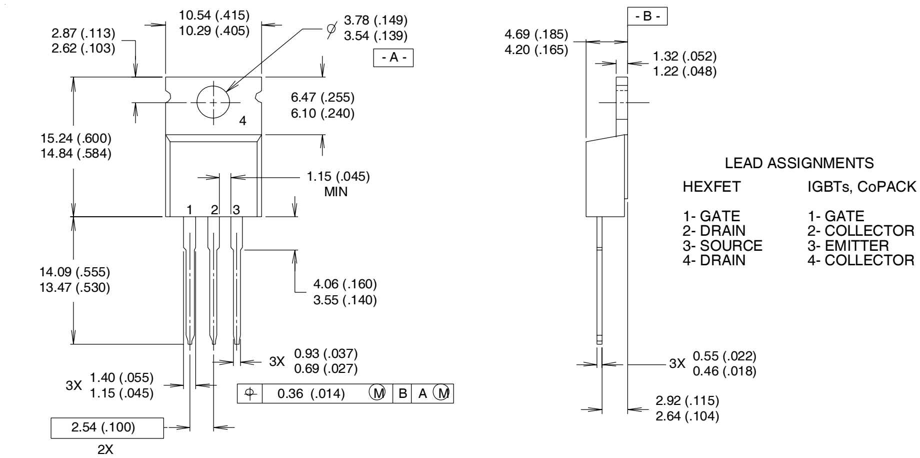


* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFETS

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)

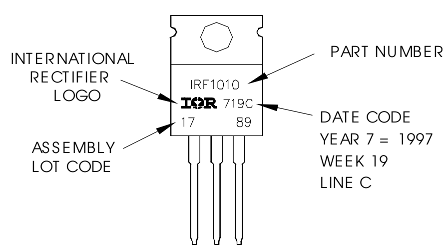


NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH
3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free"



Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting $T_J = 25°C$, L = 12.6mH $R_G = 25\Omega$, $I_{AS} = 10A$. (See Figure 12)

③ $I_{SD} \leq 10A$, $di/dt \leq 330A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150°C$

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

Data and specifications subject to change without notice.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
11/03

Notice

The products described herein were acquired by Vishay Intertechnology, Inc., as part of its acquisition of International Rectifier's Power Control Systems (PCS) business, which closed in April 2007. Specifications of the products displayed herein are pending review by Vishay and are subject to the terms and conditions shown below.

Specifications of the products displayed herein are subject to change without notice. Vishay Intertechnology, Inc., or anyone on its behalf, assumes no responsibility or liability for any errors or inaccuracies.

Information contained herein is intended to provide a product description only. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Vishay's terms and conditions of sale for such products, Vishay assumes no liability whatsoever, and disclaims any express or implied warranty, relating to sale and/or use of Vishay products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright, or other intellectual property right.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Vishay for any damages resulting from such improper use or sale.

International Rectifier®, IR®, the IR logo, HEXFET®, HEXSense®, HEXDIP®, DOL®, INTERO®, and POWIRTRAIN® are registered trademarks of International Rectifier Corporation in the U.S. and other countries. All other product names noted herein may be trademarks of their respective owners.