



Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	250	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.435
Q_g (Max.) (nC)	34	
Q_{gs} (nC)	6.5	
Q_{gd} (nC)	16	
Configuration	Single	

FEATURES

- Advanced Process Technology
- Dynamic dV/dt Rating
- 175 °C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Ease of Paralleling
- Simple Drive Requirements
- Lead (Pb)-free Available



Available
RoHS*
COMPLIANT

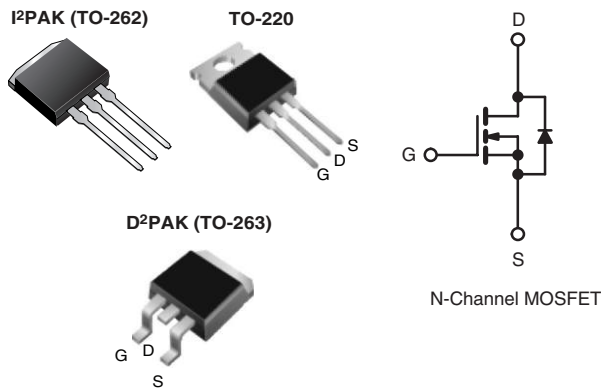
DESCRIPTION

Fifth generation Power MOSFETs from Vishay utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

The D²PAK (TO-263) is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

The through-hole version (IRF634NL/SiHF634NL) is available for low-profile application.



ORDERING INFORMATION					
Package	TO-220	D ² PAK (TO-263)	D ² PAK (TO-263)	D ² PAK (TO-263)	I ² PAK (TO-262)
Lead (Pb)-free	IRF634NPbF	IRF634NSPbF	IRF634NSTRLPbF ^a	IRF634NSTRRPbF ^a	IRF634NLPbF
	SiHF634N-E3	SiHF634NS-E3	SiHF634NSTL-E3 ^a	SiHF634NSTR-E3 ^a	SiHF634NL-E3
SnPb	IRF634N	IRF634NS	IRF634NSTRL ^a	IRF634NSTRR ^a	-
	SiHF634N	SiHF634NS	SiHF634NSTL ^a	SiHF634NSTR ^a	-

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted				
PARAMETER	SYMBOL		LIMIT	UNIT
Drain-Source Voltage	V_{DS}		250	V
Gate-Source Voltage	V_{GS}		± 20	
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25\text{ }^\circ\text{C}$	8.0	A
		$T_C = 100\text{ }^\circ\text{C}$	5.6	
Pulsed Drain Current ^a	I_{DM}		32	
Linear Derating Factor			0.59	W/°C
Single Pulse Avalanche Energy ^b	E_{AS}		110	mJ
Avalanche Current ^a	I_{AR}		4.8	A
Repetitive Avalanche Energy ^a	E_{AR}		8.8	mJ

* Pb containing terminations are not RoHS compliant, exemptions may apply



ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted				
PARAMETER		SYMBOL	LIMIT	UNIT
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	88	W
Maximum Power Dissipation (PCB Mount) ^e	$T_A = 25\text{ }^\circ\text{C}$		3.8	
Peak Diode Recovery dV/dt		dV/dt	7.3	V/ns
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to + 175	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s		300 ^c	
Mounting Torque ^d	6-32 or M3 screw		10	lbf · in
			1.1	N · m

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature.
- b. Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 9.5\text{ mH}$, $R_G = 25\text{ }\Omega$, $I_{AS} = 4.8\text{ A}$, $V_{GS} = 10\text{ V}$.
- c. 1.6 mm from case.
- d. This is only applied to TO-220 package.
- e. This is applied to D²PAK, when mounted 1" square PCB (FR-4 or G-10 material).

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient ^a	R_{thJA}	-	62	$^\circ\text{C/W}$
Maximum Junction-to-Ambient (PCB Mount) ^b	R_{thJA}	-	40	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.7	
Case-to-Sink, Flat, Greased Surface ^a	R_{thCS}	0.50	-	

Notes

- a. This is only applied to TO-220 package.
- b. This is applied to D²PAK, when mounted 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	250	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$	-	0.33	-	$\text{V}/^\circ\text{C}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 250\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	25	μA
		$V_{DS} = 200\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 4.8\text{ A}^b$	-	-	0.435	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}$, $I_D = 4.8\text{ A}^b$	5.4	-	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5	-	620	-	pF
Output Capacitance	C_{oss}		-	84	-	
Reverse Transfer Capacitance	C_{rss}		-	23	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$, $I_D = 4.8\text{ A}$, $V_{DS} = 200\text{ V}$, see fig. 6 and 13 ^b	-	-	34	nC
Gate-Source Charge	Q_{gs}		-	-	6.5	
Gate-Drain Charge	Q_{gd}		-	-	16	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 125\text{ V}$, $I_D = 4.8\text{ A}$, $R_G = 1.3\text{ }\Omega$, see fig. 10 ^b	-	8.4	-	ns
Rise Time	t_r		-	16	-	
Turn-Off Delay Time	$t_{d(off)}$		-	28	-	
Fall Time	t_f		-	15	-	



SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Dynamic							
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact	-	4.5	-	nH	
Internal Source Inductance	L_S		-	7.5	-		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode	-	-	8.0	A	
Pulsed Diode Forward Current ^a	I_{SM}		-	-	32		
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}$, $I_S = 4.8\text{ A}$, $V_{GS} = 0\text{ V}^b$	-	-	1.3	V	
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}$, $I_F = 4.8\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}^b$	-	130	200	ns	
Body Diode Reverse Recovery Charge	Q_{rr}		-	650	980	nC	
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS $25\text{ }^\circ\text{C}$, unless otherwise noted

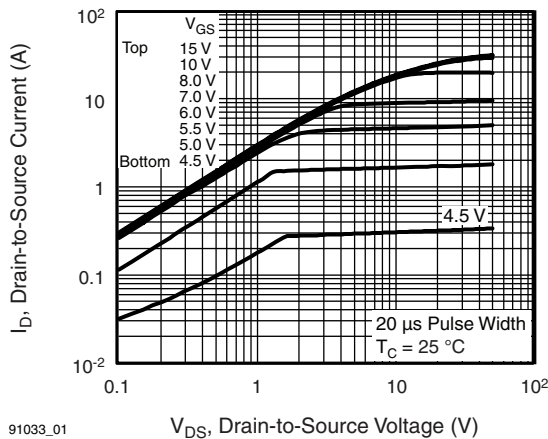


Fig. 1 - Typical Output Characteristics

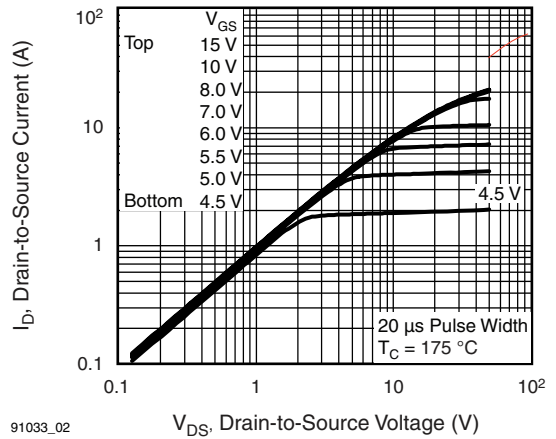


Fig. 2 - Typical Output Characteristics

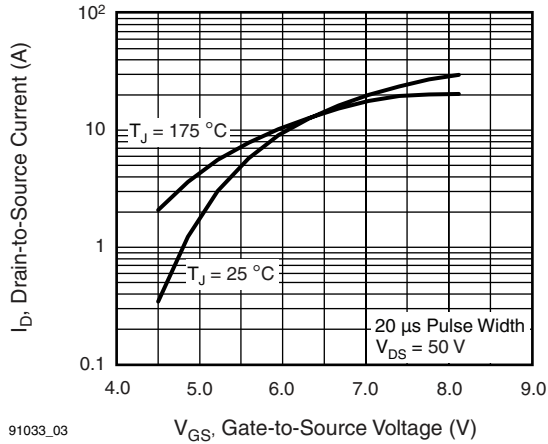


Fig. 3 - Typical Transfer Characteristics

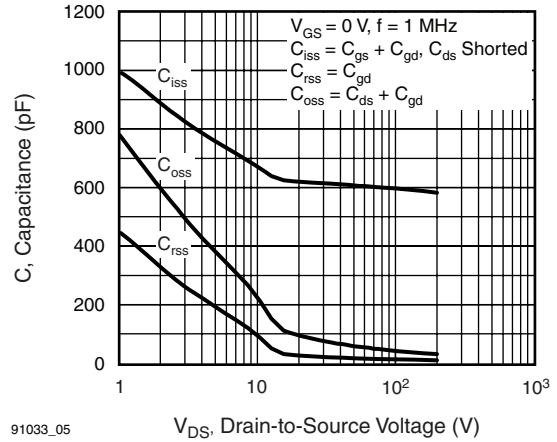


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

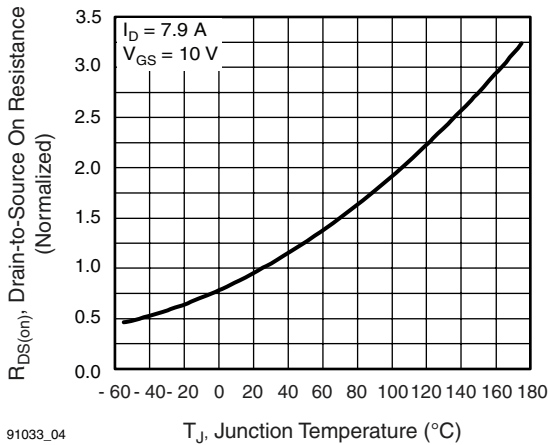


Fig. 4 - Normalized On-Resistance vs. Temperature

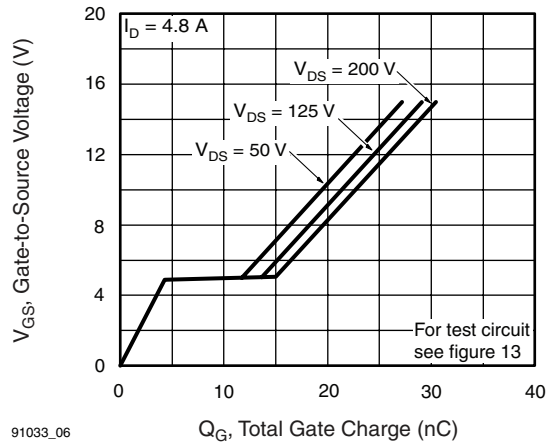
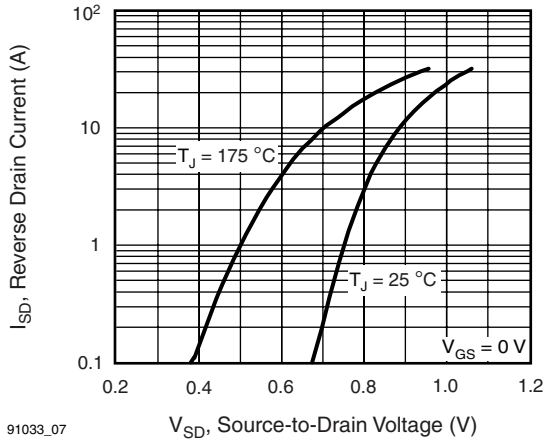
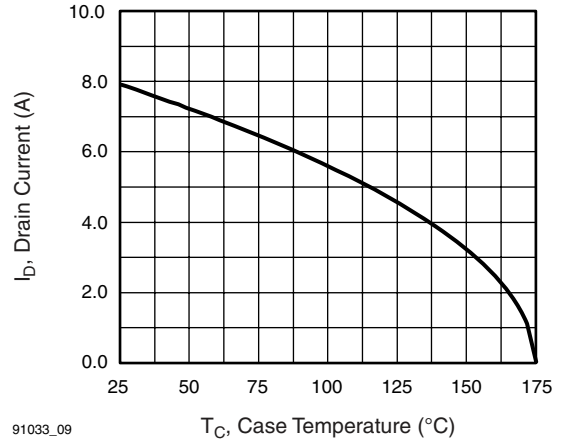


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



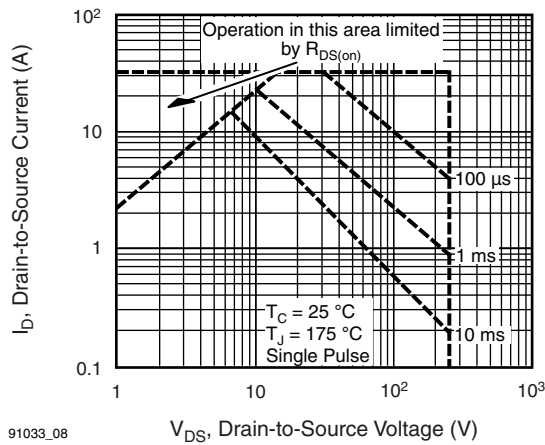
91033_07

Fig. 7 - Typical Source-Drain Diode Forward Voltage



91033_09

Fig. 9 - Maximum Drain Current vs. Case Temperature



91033_08

Fig. 8 - Maximum Safe Operating Area

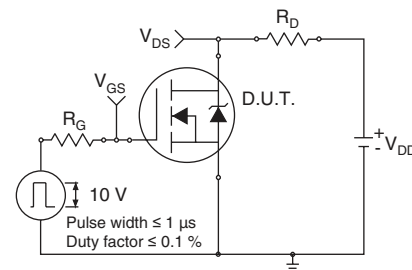


Fig. 10a - Switching Time Test Circuit

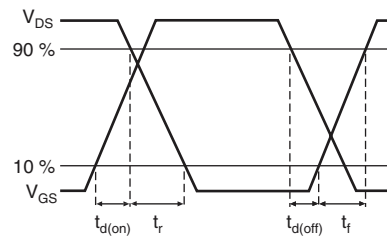


Fig. 10b - Switching Time Waveforms

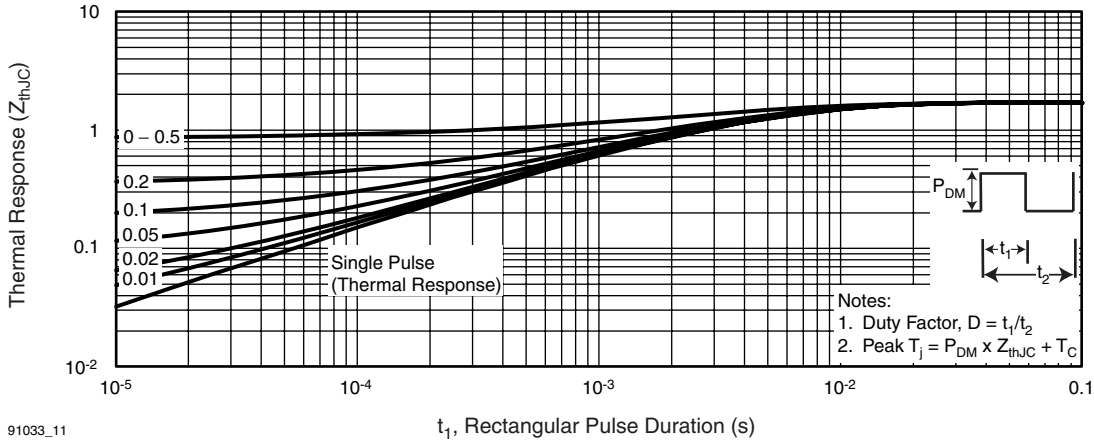


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

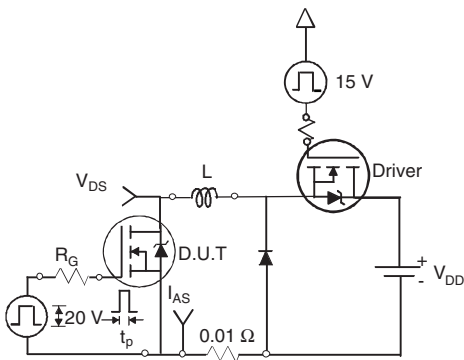


Fig. 12a - Unclamped Inductive Test Circuit

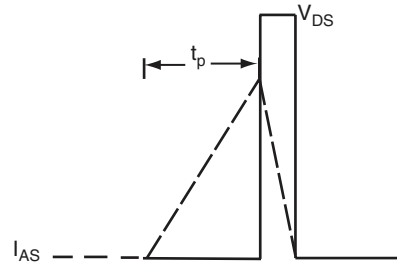


Fig. 12b - Unclamped Inductive Waveforms

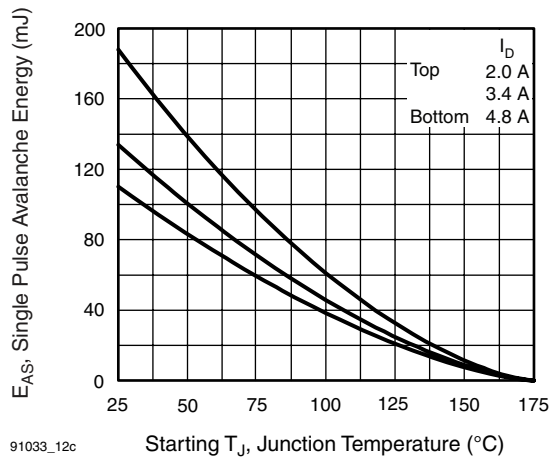


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

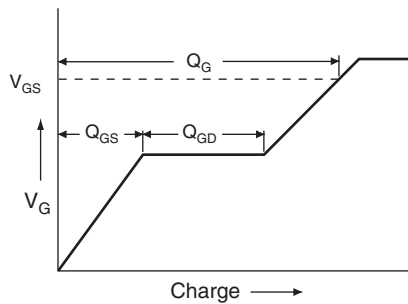


Fig. 13a - Basic Gate Charge Waveform

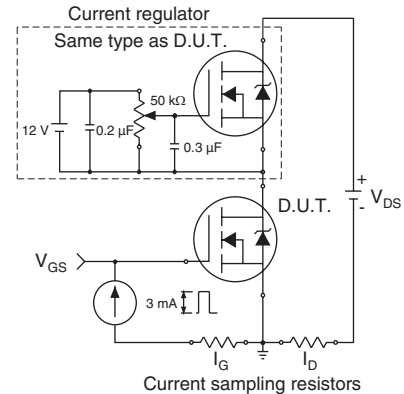
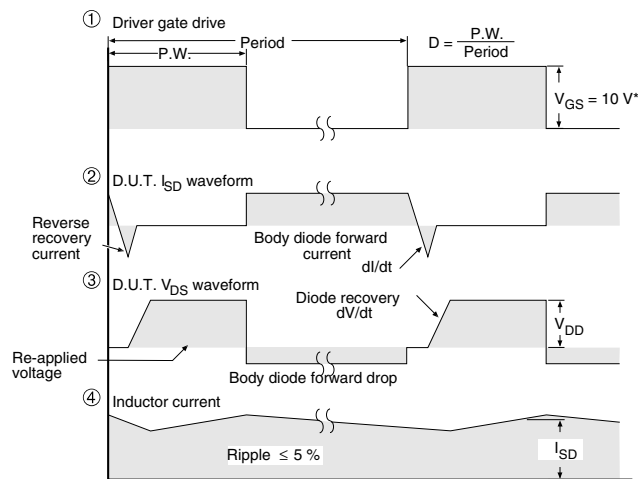
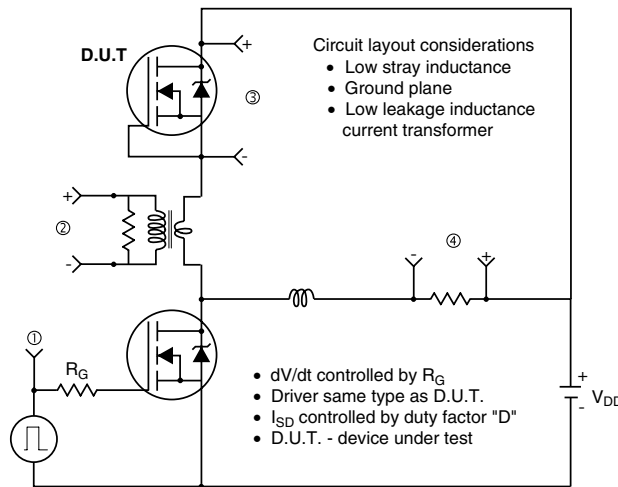


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5V$ for logic level devices

Fig. 14 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?91033>.



Disclaimer

All product specifications and data are subject to change without notice.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained herein or in any other disclosure relating to any product.

Vishay disclaims any and all liability arising out of the use or application of any product described herein or of any information provided herein to the maximum extent permitted by law. The product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein, which apply to these products.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications unless otherwise expressly indicated. Customers using or selling Vishay products not expressly indicated for use in such applications do so entirely at their own risk and agree to fully indemnify Vishay for any damages arising or resulting from such use or sale. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

Product names and markings noted herein may be trademarks of their respective owners.